

# SN54HC14, SN74HC14 HEX SCHMITT-TRIGGER INVERTERS

SCLS085E – DECEMBER 1982 – REVISED NOVEMBER 2004

- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 20- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 11$  ns
- $\pm 4$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max

SN54HC14 . . . J OR W PACKAGE  
SN74HC14 . . . D, DB, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54HC14 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

These Schmitt-trigger devices contain six independent inverters. They perform the Boolean function  $Y = \bar{A}$  in positive logic.

### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube of 25	SN74HC14N	SN74HC14N
		Tube of 50	SN74HC14D	HC14
	SOIC – D	Reel of 2500	SN74HC14DR	
		Reel of 250	SN74HC14DT	
	SOP – NS	Reel of 2000	SN74HC14NSR	HC14
	SSOP – DB	Reel of 2000	SN74HC14DBR	HC14
	TSSOP – PW	TSSOP – PW	Tube of 90	SN74HC14PW
Reel of 2000			SN74HC14PWR	
Reel of 250			SN74HC14PWT	
-55°C to 125°C	CDIP – J	Tube	SNJ54HC14J	SNJ54HC14J
	CFP – W	Tube	SNJ54HC14W	SNJ54HC14W
	LCCC – FK	Tube	SNJ54HC14FK	SNJ54HC14FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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 **TEXAS  
INSTRUMENTS**

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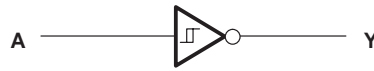
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**FUNCTION TABLE**  
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1)	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
D package	86°C/W
DB package	96°C/W
N package	80°C/W
NS package	76°C/W
PW package	113°C/W
Storage temperature range, $T_{stg}$	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

	SN54HC14			SN74HC14			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage	2	5	6	2	5	6	V
$V_I$ Input voltage	0		$V_{CC}$	0		$V_{CC}$	V
$V_O$ Output voltage	0		$V_{CC}$	0		$V_{CC}$	V
$T_A$ Operating free-air temperature	-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54HC14, SN74HC14 HEX SCHMITT-TRIGGER INVERTERS

SCLS085E – DECEMBER 1982 – REVISED NOVEMBER 2004

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC14		SN74HC14		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>T+</sub>			2 V	0.7	1.2	1.5	0.7	1.5	0.7	1.5	V
			4.5 V	1.55	2.5	3.15	1.55	3.15	1.55	3.15	
			6 V	2.1	3.3	4.2	2.1	4.2	2.1	4.2	
V <sub>T-</sub>			2 V	0.3	0.6	1	0.3	1	0.3	1	V
			4.5 V	0.9	1.6	2.45	0.9	2.45	0.9	2.45	
			6 V	1.2	2	3.2	1.2	3.2	1.2	3.2	
V <sub>T+</sub> - V <sub>T-</sub>			2 V	0.2	0.6	1.2	0.2	1.2	0.2	1.2	V
			4.5 V	0.4	0.9	2.1	0.4	2.1	0.4	2.1	
			6 V	0.5	1.3	2.5	0.5	2.5	0.5	2.5	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	2 V	1.9	1.998		1.9		1.9	V	
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I <sub>OH</sub> = -4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I <sub>OH</sub> = -5.2 mA	6 V	5.48	5.8		5.2		5.34		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I <sub>OL</sub> = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I <sub>OL</sub> = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0		6 V		±0.1	±100		±1000		±1000	nA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0		6 V			2		40		20	μA
C <sub>i</sub>			2 V to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC14		SN74HC14		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	2 V		55	125		190		155	ns
			4.5 V		12	25		38		31	
			6 V		11	21		32		26	
t <sub>t</sub>		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics, T<sub>A</sub> = 25°C

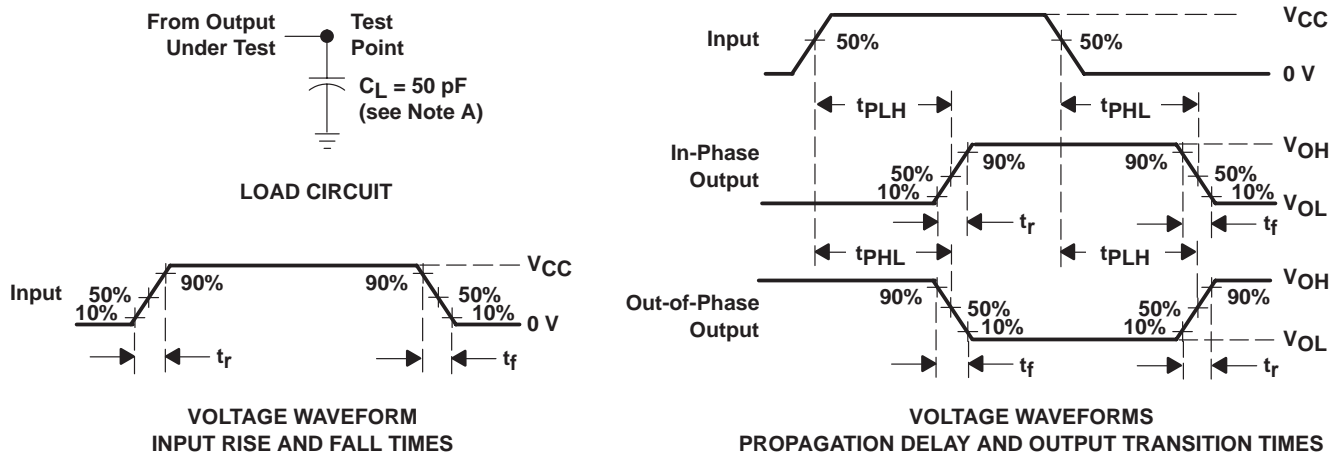
PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance per inverter	No load	20	pF



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SCLS085E – DECEMBER 1982 – REVISED NOVEMBER 2004

## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
  - C. The outputs are measured one at a time, with one input transition per measurement.
  - D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-8409101VCA	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
5962-8409101VDA	ACTIVE	CFP	W	14	1	None	Call TI	Level-NC-NC-NC
84091012A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
8409101CA	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
8409101DA	ACTIVE	CFP	W	14	1	None	Call TI	Level-NC-NC-NC
JM38510/65702BCA	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
JM38510/65702BDA	ACTIVE	CFP	W	14	1	None	Call TI	Level-NC-NC-NC
SN54HC14J	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SN74HC14D	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74HC14DBR	ACTIVE	SSOP	DB	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74HC14DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC14DT	ACTIVE	SOIC	D	14	250	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74HC14N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74HC14N3	OBSOLETE	PDIP	N	14		None	Call TI	Call TI
SN74HC14NS	ACTIVE	SO	NS	14		Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74HC14NSLE	OBSOLETE	SO	NS	14		None	Call TI	Call TI
SN74HC14NSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74HC14PW	ACTIVE	TSSOP	PW	14	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74HC14PWLE	OBSOLETE	TSSOP	PW	14		None	Call TI	Call TI
SN74HC14PWR	ACTIVE	TSSOP	PW	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74HC14PWT	ACTIVE	TSSOP	PW	14	250	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SNJ54HC14FK	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
SNJ54HC14J	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SNJ54HC14W	ACTIVE	CFP	W	14	1	None	Call TI	Level-NC-NC-NC

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



4040180-2/D 07/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB



FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-012 variation AB.

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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