

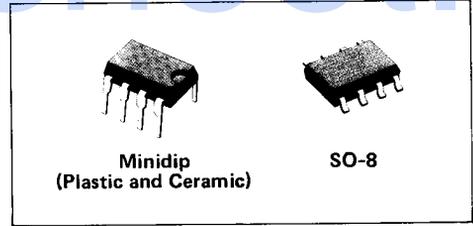
LOW NOISE JFET-INPUT QUAD OPERATIONAL AMPLIFIERS

- LOW-NOISE
- LOW INPUT BIAS AND OFFSET CURRENTS
- HIGH INPUT IMPEDANCE . . . JFET-INPUT STAGE
- LOW POWER CONSUMPTION
- WIDE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- OUTPUT SHORT-CIRCUIT PROTECTION
- INTERNAL FREQUENCY COMPENSATION
- LATCH-UP-FREE OPERATION
- HIGH SLEW-RATE . . . 13V/ μ s TYP.

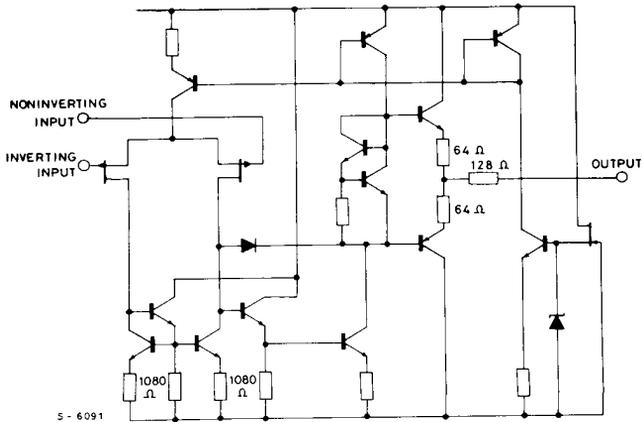
voltage temperature coefficient. Each JFET-input operational amplifier incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit.

Devices with an "I" suffix are characterized for operation from -25°C to 85°C, and those with a "C" suffix are characterized for operation from 0°C to 70°C.

The TL072 JFET-input operational amplifiers are designed to offer low-noise high slew-rate, low input bias and offset current, and low offset



SCHEMATIC DIAGRAM
(one section)

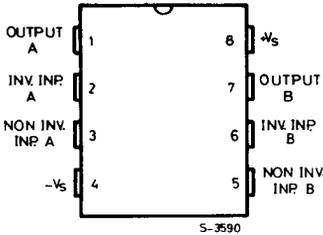


ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 18	V
V_{is}	Differential input voltage	± 30	V
V_i	Input voltage	± 15	V
T_{op}	Operating temperature (TL072I) (TL072C)	-25 to 85 0 to 70	$^{\circ}$ C $^{\circ}$ C
T_j	Junction temperature	150	$^{\circ}$ C
T_{stg}	Storage temperature	-55 to 150	$^{\circ}$ C

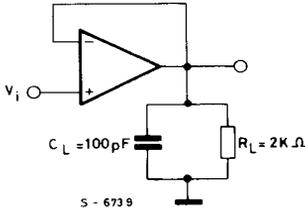
CONNECTION DIAGRAM AND ORDERING NUMBERS

(Top view)

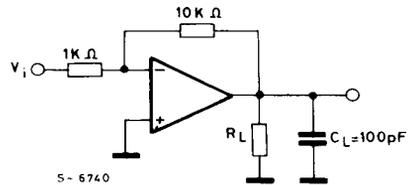


0 to 70 $^{\circ}$ C	-25 + 85 $^{\circ}$ C	Package
TL072CJG TL072ACJG TL072BCJG	TL072IJG — —	Ceramic Minidip
TL072CP TL072ACP TLOBCP	TL072IP — —	Plastic Minidip
TL072CD	TL072ID	SO-8

TEST CIRCUITS



Unity gain amplifier



Gain of 10 inverting amplifier

THERMAL DATA

		Plastic Minidip	Ceramic Minidip	SO-8	
$R_{thj-amb}$	Thermal resistance junction-ambient	max	120 $^{\circ}$ C/W	150 $^{\circ}$ C/W	200 $^{\circ}$ C/W



TL072

ELECTRICAL CHARACTERISTICS ($V_s = 15V$, $T_{amb} = 25^\circ C$, otherwise specified)

Parameter	Test conditions	"I"			"C"			Unit	
		Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{OS} Input offset voltage	$R_s = 50\Omega$	TL072		3	6		3	10	mV
		TL072A					3	6	
		TL072B					2	3	
	$R_s = 50\Omega$ $T_{amb} = \text{full range}$	TL072			9			13	
		TL072A						7.5	
		TL072B						5	
$\frac{\Delta V_{OS}}{\Delta T}$ Input offset voltage drift	$R_s = 500\Omega$ $T_{amb} = \text{full range}$		10			10		$\mu V/^\circ C$	
I_{OS} Input offset current		TL072		5	50		5	50	pA
		TL072A					5	50	
		TL072B					5	50	
	$T_{amb} = \text{full range}$	TL072			10			2	nA
		TL072A						2	
		TL072B						2	
I_b Input bias current		TL072		30	200		30	200	pA
		TL072A					30	200	
		TL072B					30	200	
	$T_{amb} = \text{full range}$	TL072			20			7	nA
		TL072A						7	
		TL072B						7	
V_{CM} Common mode input voltage range		TL072	± 11	± 12		± 10	± 11	V	
		TL072A				± 11	± 12		
		TL072B				± 11	± 12		
V_{OPP} Large signal voltage swing	$T_{amb} = \text{full range}$	$R_L = 10K\Omega$	24	27		24	27	V	
		$R_L > 10K\Omega$	24			24			
		$R_L > 2K\Omega$	20	24		20	24		
G_V Large signal voltage gain	$R_L \geq 2K\Omega$ $V_o = \pm 10V$	TL072	50	200		25	200	V/mV	
		TL072A				50	200		
		TL072B				50	200		
	$R_L \geq 2K\Omega$ $V_o = \pm 10V$ $T_{amb} = \text{full range}$	TL072	25			15			
		TL072A				25			
		TL072B				25			
B Unity gain bandwidth			3			3	MHz		
R_I Input resistance			10^{12}			10^{12}	Ω		
CMR Common mode rejection	$R_s \geq 10K\Omega$	TL072	80	86		70	76	dB	
		TL072A				80	86		
		TL072B							
SVR Supply voltage rejection	$R_s \geq 10K\Omega$	TL072	80	86		70	76	dB	
		TL072A				80	86		
		TL072B				80	86		
I_S Supply current	$R_L = \infty$		2.8	5		2.8	5	mA	

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test conditions	"I"			"C"			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Cs	Channel separation	$G_V = 100$			120		120	dB
SR	Slew-rate at	$V_I = 10V$ $C_L = 100pF$	$R_L = 2K\Omega$		13		13	V/ μs
t _r	Rise time	$V_I = 20mV$	$R_L = 2K\Omega$		0.1		0.1	μs
	Overshoot factor	$C_L = 100pF$			10		10	%
e _N	Total input noise voltage	$R_S = 100\Omega$	$F = 1KHz$		18		18	$\frac{nV}{\sqrt{Hz}}$
			$f = 10KHz \text{ to } 10KHz$		4		4	μV
i _N	Input noise current	$f = 1KHz$			0.01		0.01	$\frac{pA}{\sqrt{Hz}}$
d	Total harmonic distortion	$V_O = 10V_{rms}$ $R_S < 1K\Omega$ $R_L > 2K\Omega$	$f = 1KHz$		0.01		0.01	%

Fig. 1 — Maximum peak to peak output voltage vs. frequency.

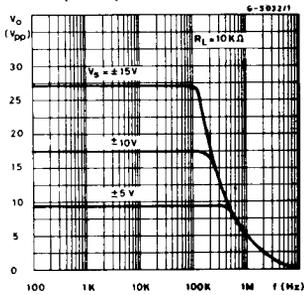


Fig. 2 — Maximum peak to peak output voltage vs. frequency

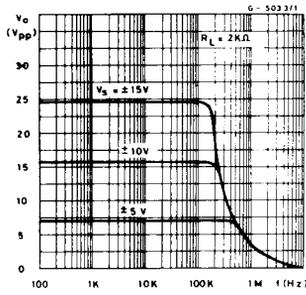


Fig. 3 — Maximum peak to peak output voltage vs. load resistance

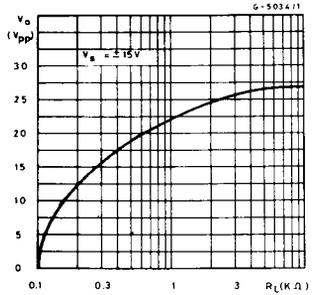


Fig. 4 — Large signal voltage gain and phase shift vs. frequency

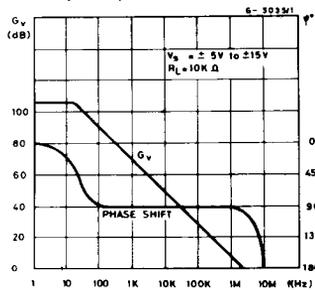


Fig. 5 Supply current vs. supply voltage

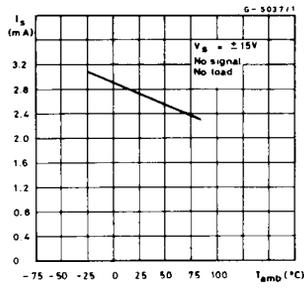


Fig. 6 — Supply current vs. supply voltage

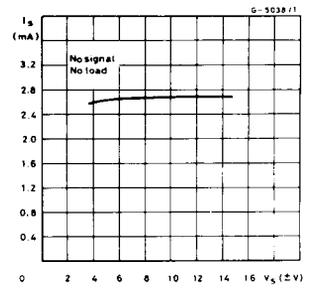




Fig. 7 – Input bias current vs. temperature

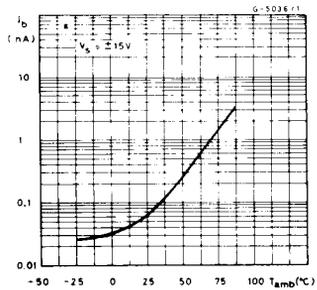


Fig. 8 – Voltage follower large signal pulse response

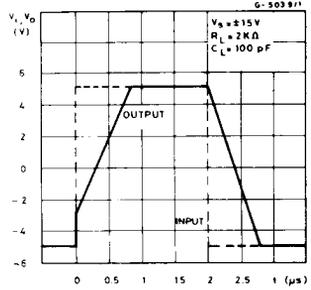


Fig. 9 – Output voltage vs. elapsed time

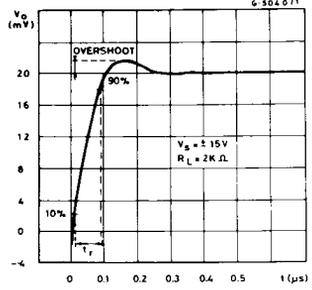


Fig. 10 – Equivalent input noise voltage vs. frequency

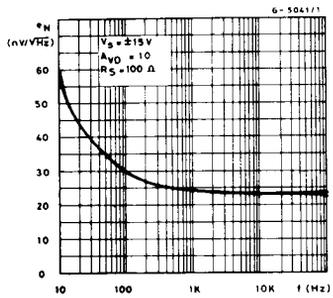


Fig. 11 – Total harmonic distortion vs. frequency

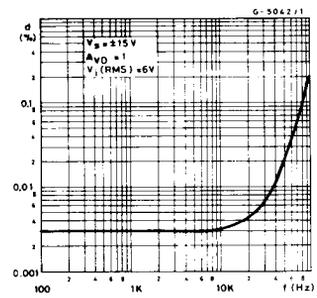
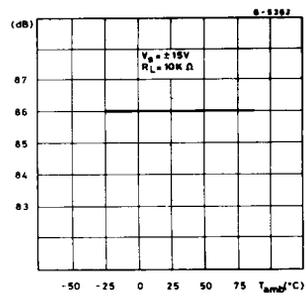
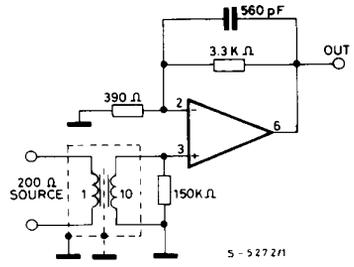


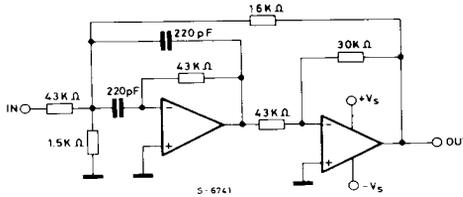
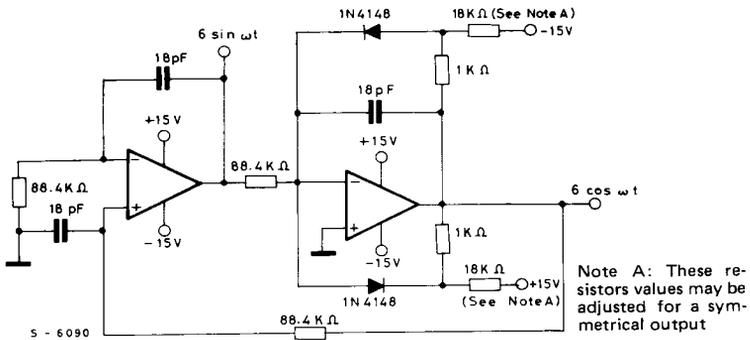
Fig. 12 Common mode rejection vs. temperature



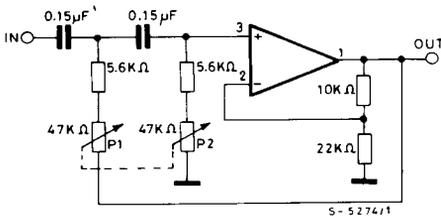
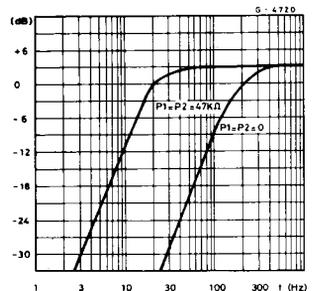
APPLICATION INFORMATION

Fig. 13 – Low-Noise High Slew-Rate mike preamplifier ($G_v = 40$ dB)



APPLICATION INFORMATION (continued)
Fig. 14 – Second order high Q band pass filter ($f_o = 100\text{KHz}$, $Q = 30$, gain = 4)

Fig. 15 – 100KHz quadrature oscillator


Note A: These resistors values may be adjusted for a symmetrical output

Fig. 16 – 20Hz to 200Hz variable High-pass filter ($G_v = 3\text{dB}$)

Fig. 17 – Frequency response of the high-pass filter of fig. 17


APPLICATION INFORMATION (continued)

Fig. 18 — Unity-gain absolute-value circuit

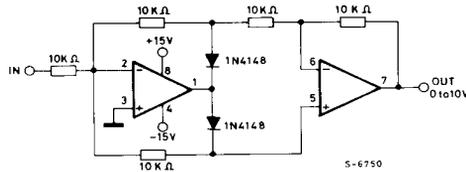


Fig. 19 — Single supply sample and hold

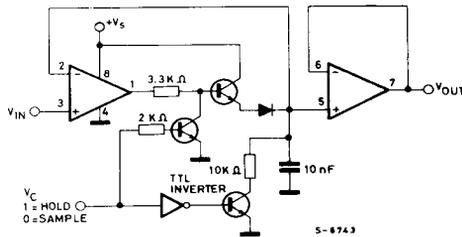
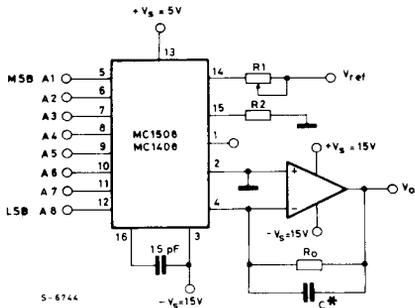


Fig. 20 — Output current to voltage transformation for a DA converter



(*) The value of C may be selected to minimize overshoot and ringing (C ≈ 68 pF).

Settling time to within 1/2 LSB (± 19.5 mV) is approximately 4.0 μs from the time all bits are switched.

$$V_{ref} = 2.0 V_{dc}$$

$$R1 = R2 \approx 1.0 \text{ k}\Omega$$

$$R_0 = 5.0 \text{ k}\Omega$$

Theoretical V_0 :

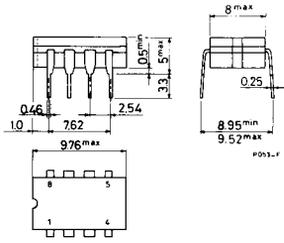
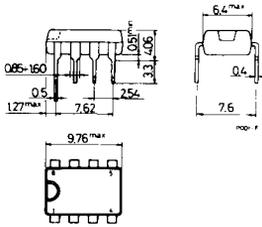
$$V_0 = \frac{V_{ref}}{R1} (R_0) \left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256} \right]$$

$$V_0 = \frac{2V}{1k} (5k) \left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256} \right]$$

$$= 10V \left[\frac{255}{256} \right] = 9.961V$$

Adjust V_{ref} , R1 or R_0 so that V_0 with all digital inputs at high level is equal to 9.961 volts.

MECHANICAL DATA (Dimensions in mm)

Minidip (Ceramic)

Minidip (Plastic)

SO-8 (Micropackage)
