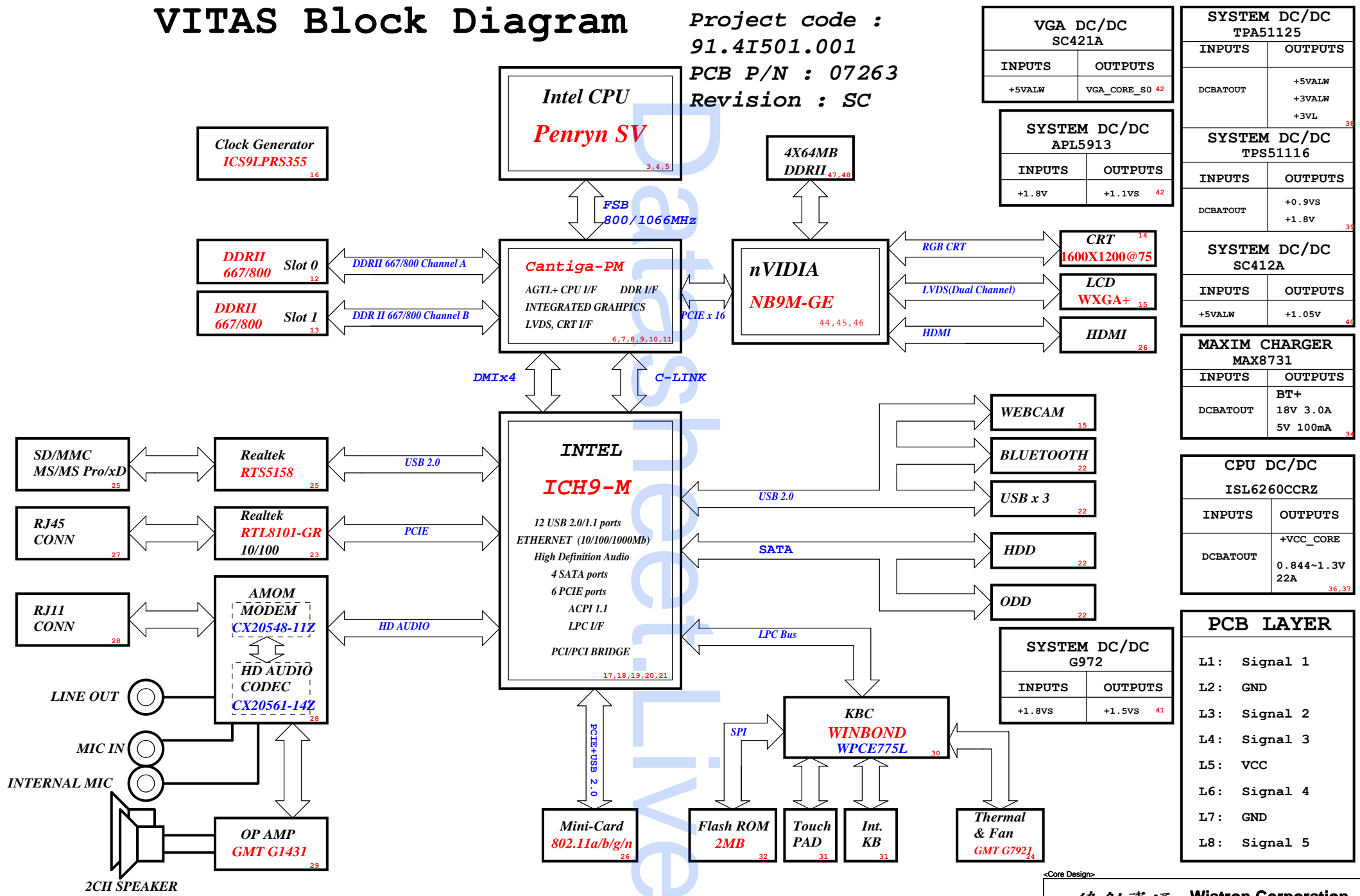


VITAS Block Diagram

Project code :
91.4I501.001
PCB P/N : 07263
Revision : SC



VGA DC/DC SC421A	
INPUTS	OUTPUTS
+5VALW	VGA_CORE_S0 42

SYSTEM DC/DC TPA51125	
INPUTS	OUTPUTS
DCBATOUT	+5VALW +3VALW +3VL 39

SYSTEM DC/DC APL5913	
INPUTS	OUTPUTS
+1.8V	+1.1VS 42

SYSTEM DC/DC TPS51116	
INPUTS	OUTPUTS
DCBATOUT	+0.9VS +1.8V 39

SYSTEM DC/DC SC412A	
INPUTS	OUTPUTS
+5VALW	+1.05V 40

MAXIM CHARGER MAX8731	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA 34

CPU DC/DC ISL6260CCRZ	
INPUTS	OUTPUTS
DCBATOUT	+VCC_CORE 0.844~1.3V 22A 36,37

SYSTEM DC/DC G972	
INPUTS	OUTPUTS
+1.8VS	+1.5VS 41

PCB LAYER	
L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	Signal 3
L5:	VCC
L6:	Signal 4
L7:	GND
L8:	Signal 5

ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1 Rising Edge of PWROK.	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC (Cofig Registers: offset 224h). This signal has weak internal pull-down.
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of PRC.PC (Config Registers: Offset 224h).
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of PRC.PC2 (Config Registers: Offset 224h).
GPIO20	Reserved.	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK.	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/ GPIO55	Top-Block Swap override. Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWB BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC
SPI_MOSI	Integrated TFM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disable. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of CLPWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0:Offset D8).
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap. Rising Edge of PWROK.	Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resistor.

PCIE Routing page 19

LANE1	LAN
LANE2	MiniCard WLAN

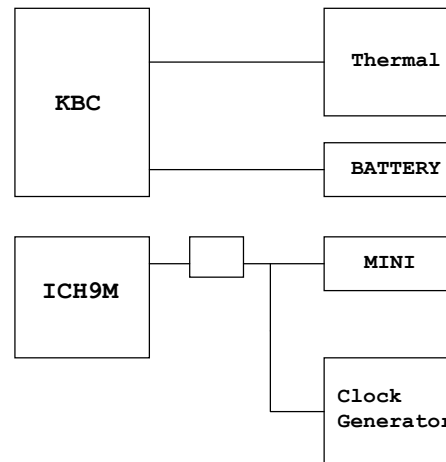
USB Table page 19

USB	
Pair	Device
0	USB3
1	FREE
2	External USB3
3	FREE
4	External USB2
5	FREE
6	WLAN
7	BLUETOOTH
8	CARD_READER
9	FREE
10	CAMERA
11	FREE

ICH9 Integrated pull-up and pull-down Resistors

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller.
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO20	PULL-DOWN 20K
GPIO49	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

SMBus



Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2) 1 = The iTPM Host Interface is disabled (default)
CFG7	Intel Management engine crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (Default)
CFG9	PCIE Graphics Lane	0 = Reserved Lanes, 15->0, 14->1 ect.. 1 = Normal operation (Default): Lane Numbered in Order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1 = Disable (Default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (Default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation (Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode [MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH->ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default) 1 = Digital display Port and PCIE are operating simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1 = LFP Card Present; PCIE disabled

NOTE:

- All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
- iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

<Core Design>

Table of Content	
Size A3	Document Number
VITAS	
Date: Monday, May 05, 2008	Rev SA
Sheet 2	of 48

6 H_A#[35..3] <<>> H_A#[35..3]

U65A 1 OF 4

H_A#3 J4 A3#
 H_A#4 L5 A4#
 H_A#5 L4 A5#
 H_A#6 K5 A6#
 H_A#7 M3 A7#
 H_A#8 N2 A8#
 H_A#9 J1 A9#
 H_A#10 N3 A10#
 H_A#11 P2 A11#
 H_A#12 P2 A12#
 H_A#13 L2 A13#
 H_A#14 P4 A14#
 H_A#15 P1 A15#
 H_A#16 R1 A16#
 M1C
 ADSTB0#

H_REQ#0 K3 REQ0#
 H_REQ#1 H2 REQ1#
 H_REQ#2 K2 REQ2#
 H_REQ#3 J3 REQ3#
 H_REQ#4 L1 REQ4#

H_A#17 Y2 A17#
 H_A#18 U5 A18#
 H_A#19 R3 A19#
 H_A#20 W6 A20#
 H_A#21 U4 A21#
 H_A#22 Y5 A22#
 H_A#23 L1 A23#
 H_A#24 R4 A24#
 H_A#25 T5 A25#
 H_A#26 T3 A26#
 H_A#27 W2 A27#
 H_A#28 W5 A28#
 H_A#29 Y4 A29#
 H_A#30 U2 A30#
 H_A#31 V4 A31#
 H_A#32 W3 A32#
 H_A#33 AA4 A33#
 H_A#34 AB2 A34#
 H_A#35 AA3 A35#
 V1C
 ADSTB1#

6 H_ADSTB#0 <<>>
 6 H_REQ#4[4..0] <<>>

18 H_A20M# <<>>
 18 H_FERR# <<>>
 18 H_IGNNE# <<>>
 18 H_STPCLK# <<>>
 18 H_INTR <<>>
 18 H_NMI <<>>
 18 H_SMI# <<>>

TPAD30 TP65 RSVD_CPU_1 M4
 TPAD30 TP61 RSVD_CPU_2 N5
 TPAD30 TP66 RSVD_CPU_3 T2
 TPAD30 TP64 RSVD_CPU_4 V3
 TPAD30 TP73 RSVD_CPU_5 B2
 TPAD30 TP70 RSVD_CPU_6 C3
 TPAD30 TP69 RSVD_CPU_7 D2
 TPAD30 TP59 RSVD_CPU_8 D22
 TPAD30 TP72 RSVD_CPU_9 D3
 TPAD30 TP60 RSVD_CPU_10 F6
 TPAD30 TP74 RSVD_CPU_11 B1

BGA479-SKT6-GPU6
62.10079.001

ADDR_GROUP_0
 CONTROL

ADDR_GROUP_1
 STANDBY/ITI/DPX

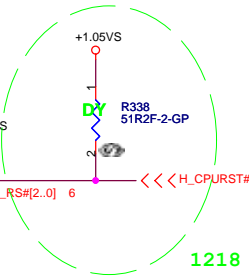
THERMAL
 PROCHOT#
 THRMDA
 THRMDC
 THERMTRIP#

ICH
 HCLK
 BCLK0
 BCLK1

RESERVED

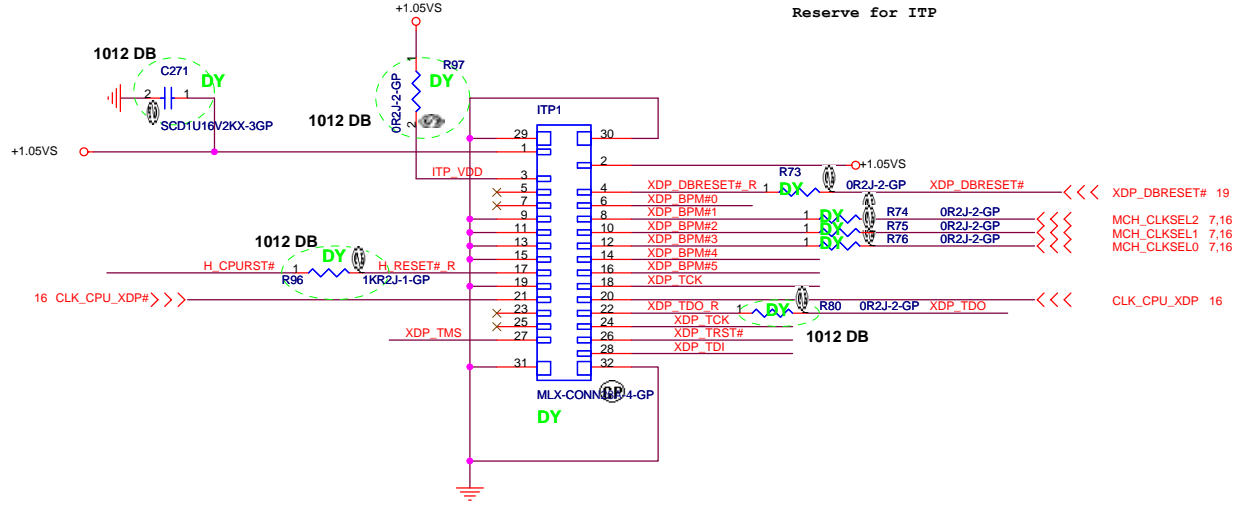
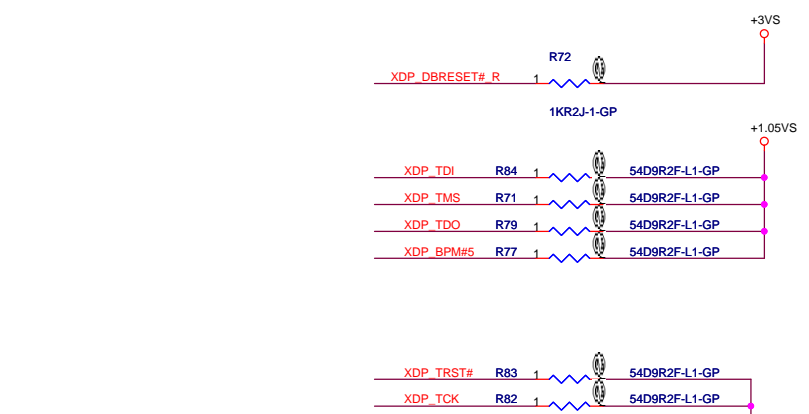
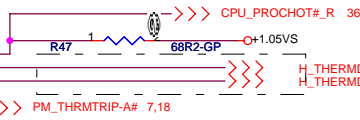
ADS# OH1 <<>> H_ADS# 6
 BNR# OE2 <<>> H_BNR# 6
 BPR# OG5 <<>> H_BPR# 6
 DEFER# OH5 <<>> H_DEFER# 6
 DRDY# FE21 <<>> H_DRDY# 6
 DBSY# OE1 <<>> H_DBSY# 6
 BR0# OE1 <<>> H_BR0# 6
 CPU_IERR# 1 R49 <<>> H_IERR# 18
 INIT# B3 <<>> H_INIT# 18
 LOCK# OH4 <<>> H_LOCK# 6
 RESET# C1 <<>> H_RS#0 6
 RS0# FE4 <<>> H_RS#1 6
 RS1# OG3 <<>> H_RS#2 6
 TRDY# OG2 <<>> H_TRDY# 6
 HIT# OE4 <<>> H_HIT# 6
 HITM# OE4 <<>> H_HITM# 6
 AD4 XDP_BPM#0
 AD3 XDP_BPM#1
 AD1 XDP_BPM#2
 AC4 XDP_BPM#3
 AC2 XDP_BPM#4
 AC1 XDP_BPM#5
 AC5 XDP_TCK
 AA6 XDP_TDI
 AB3 XDP_TDO
 AB5 XDP_TMS
 AB6 XDP_TRST#
 C20 XDP_DBRESET#_R

Reserve for ITP, when install ITP connector, install R338.



H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil

Connect to V Core 4/23 Houston



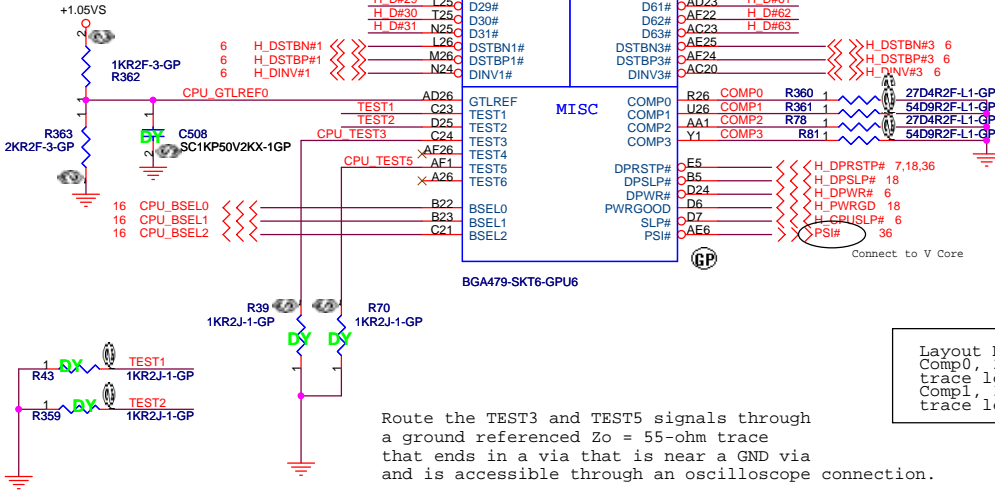
ITP Connector

Reserve for ITP

<Core Design> Place R310 with in 200ps (~1") to CPU

緯創資通 Wistron Corporation
 21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
 Title: CPU (1 of 2)
 Size: Document Number: VITAS
 Date: Monday, May 05, 2008 Sheet 3 of 48 Rev SA

Layout notes
 Z= 55 Ohm 0.5" MAX for GTLREF

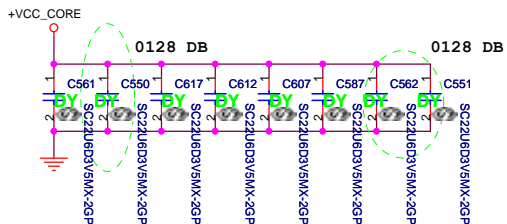


Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

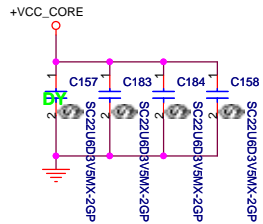
Layout Note:
 Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".
 Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5".

H_DINV#[3..0] <<>> H_DINV#[3..0] 6
 H_DSTBN#[3..0] <<>> H_DSTBN#[3..0] 6
 H_DSTBP#[3..0] <<>> H_DSTBP#[3..0] 6
 H_D#[63..0] <<>> H_D#[63..0] 6

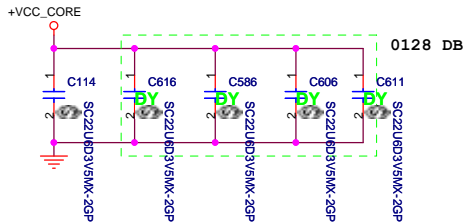
Please these inside socket cavity on L8(North side Secondary)



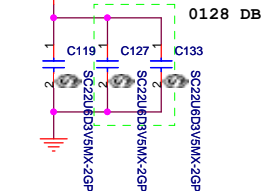
Please these outside socket cavity on L8(North side Secondary)



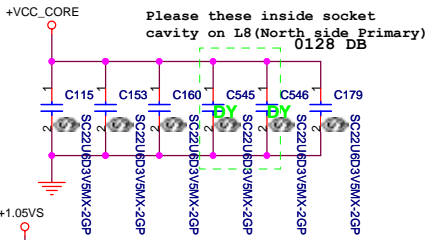
Please these inside socket cavity on L8(South side Secondary)



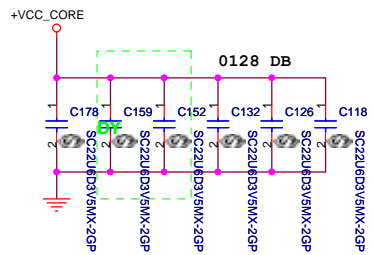
Please these outside socket cavity on L8(South side Secondary)



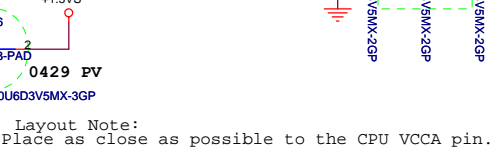
Please these inside socket cavity on L8(North side Primary)



Please these outside socket cavity on L8(South side Primary)



layout note: "1d5V_VCCA_S0" as short as possible

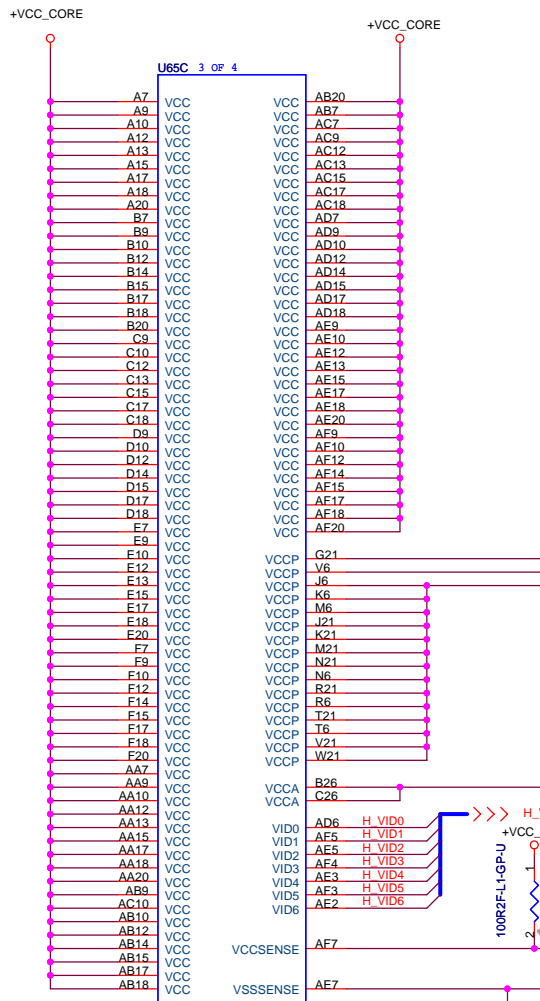
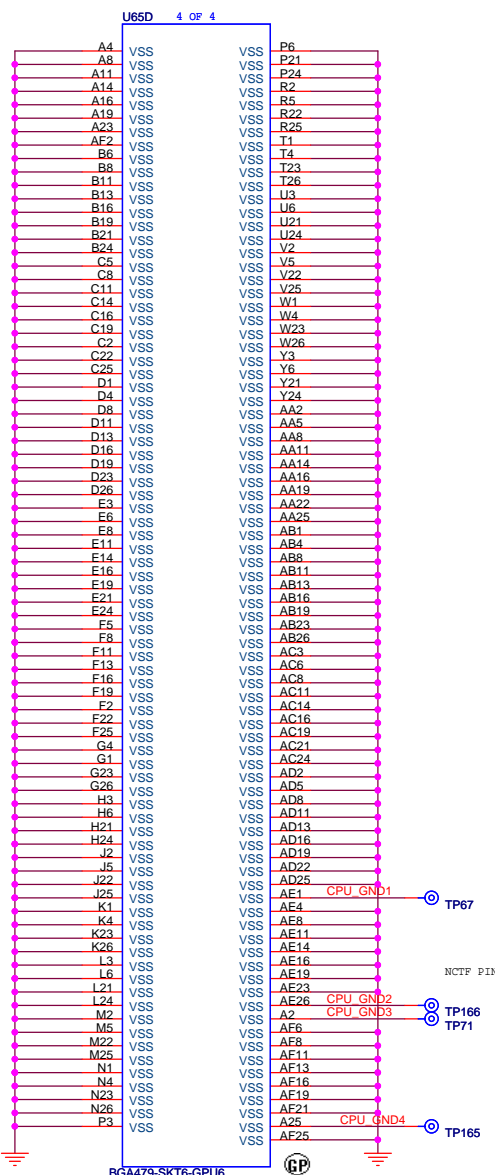
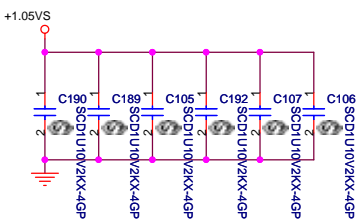


Layout Note: Place as close as possible to the CPU VCCA pin.

Layout Note: VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note: Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

Please these inside socket cavity on L8(North side Secondary)



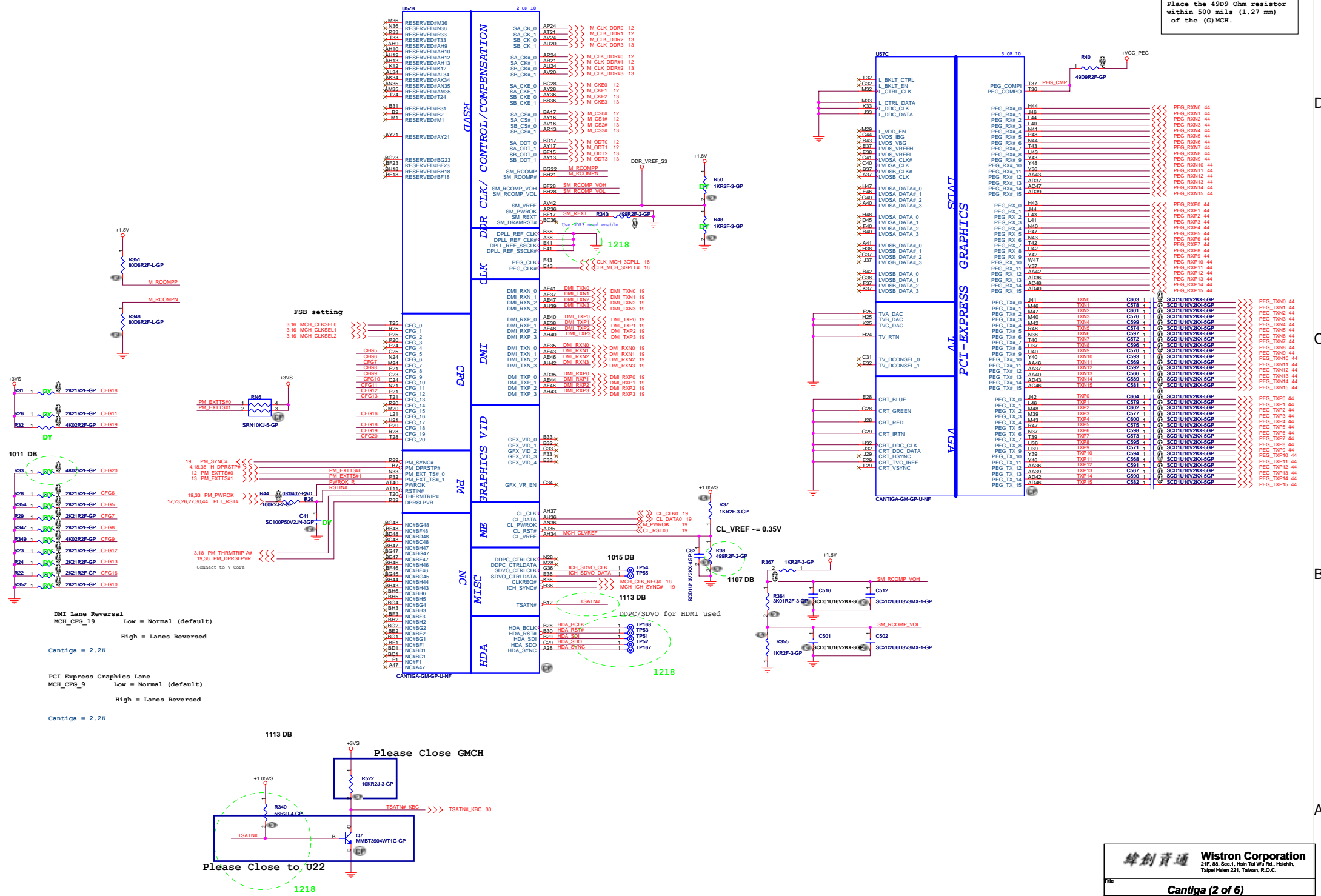
BGA479-SKT6-GPU6

BGA479-SKT6-GPU6

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (3 of 3)
 Size: Document Number: VITAS
 Date: Monday, May 05, 2008 Sheet 5 of 48

Place the 49D9 Ohm resistor within 500 mils (1.27 mm) of the (G)MCH.

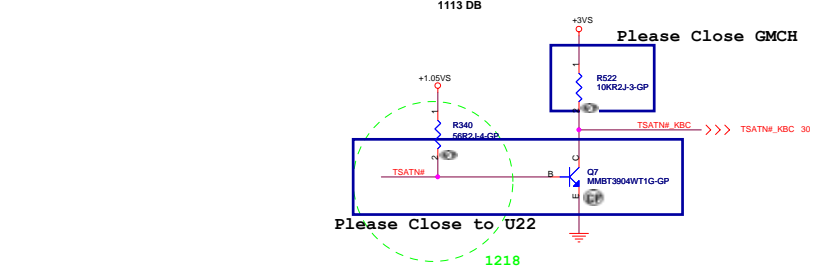


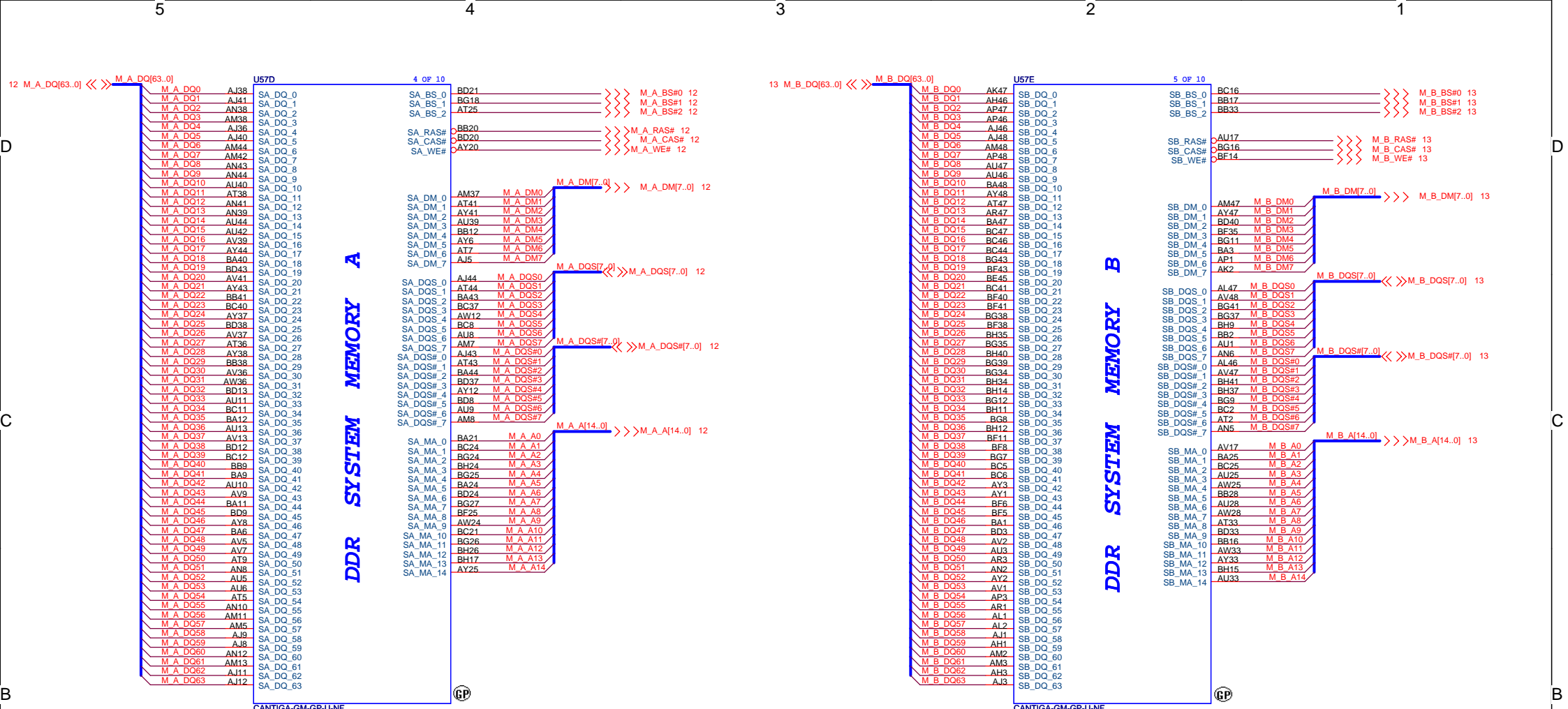
DMI Lane Reversal
MCH_CFG_19 Low = Normal (default)
High = Lanes Reversed

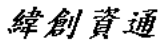
Cantiga = 2.2K

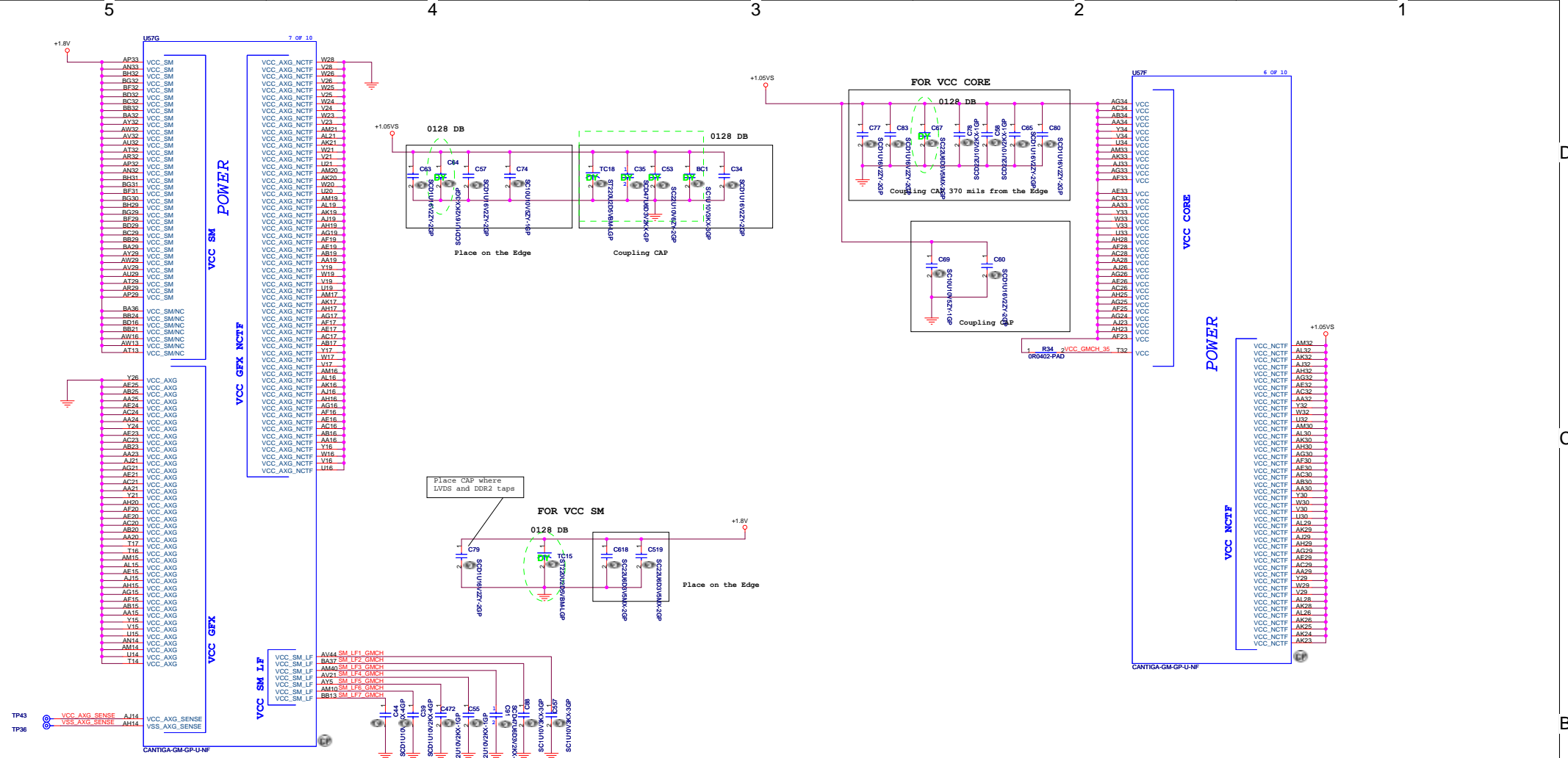
PCI Express Graphics Lane
MCH_CFG_9 Low = Normal (default)
High = Lanes Reversed

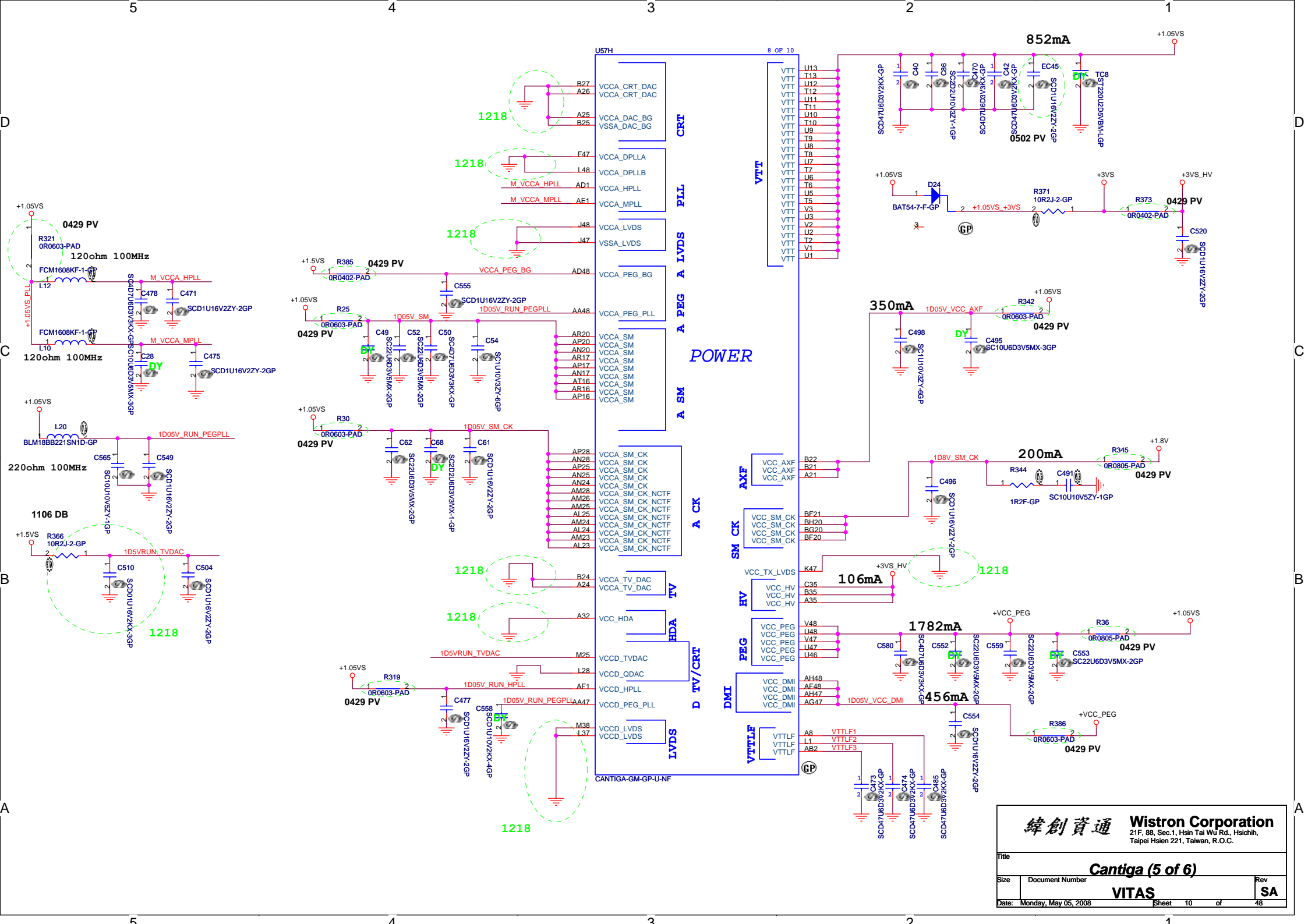
Cantiga = 2.2K





 緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
Cantiga (3 of 6)	
Size	Document Number
VITAS	
Date: Monday, May 05, 2008	Rev SA
Sheet 8 of 48	

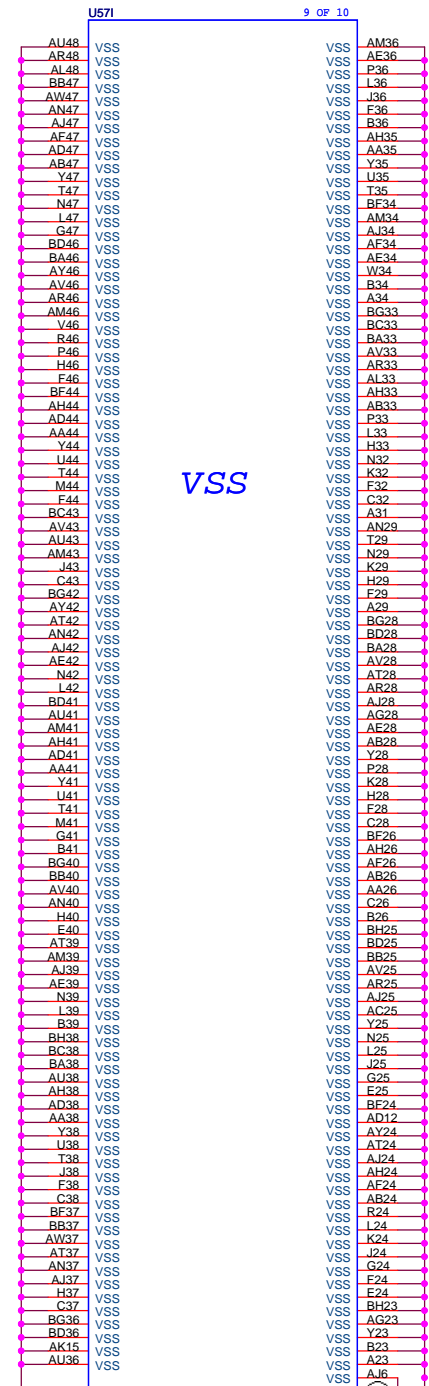




緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

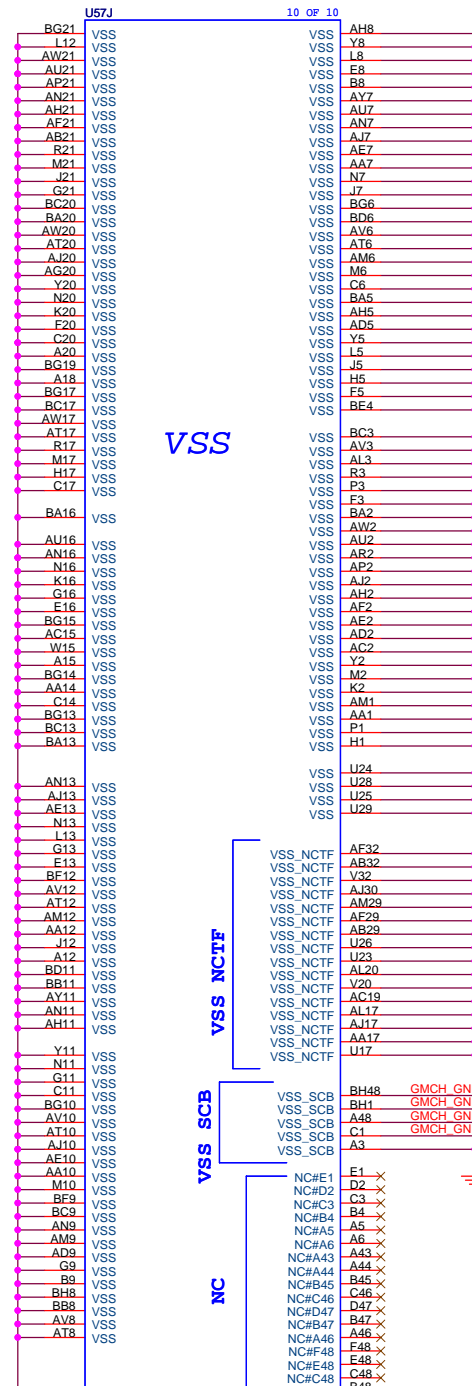
Title: **Cantiga (5 of 6)**

Size: Document Number	Rev: SA
VITAS	
Date: Monday, May 05, 2008	Sheet 10 of 48



CANTIGA-GM-GP-U-NF

Modification AJ6 to reserved Pin

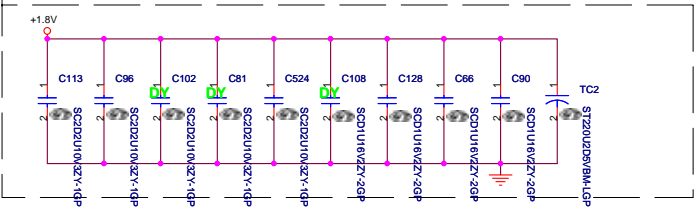


CANTIGA-GM-GP-U-NF

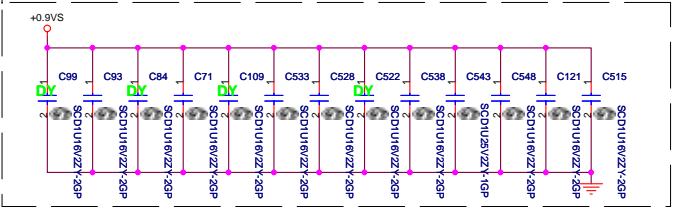
緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
Cantiga (6 of 6)	
Size	Document Number
VITAS	
Date: Monday, May 05, 2008	Rev SA
Sheet 11	of 48

8 M_A_DQS#(7..0) <<>>
 8 M_A_DQ#(63..0) <<>>
 8 M_A_DM7..0 <<>>
 8 M_A_DQS7..0 <<>>
 8 M_A_A[14..0] <<>>

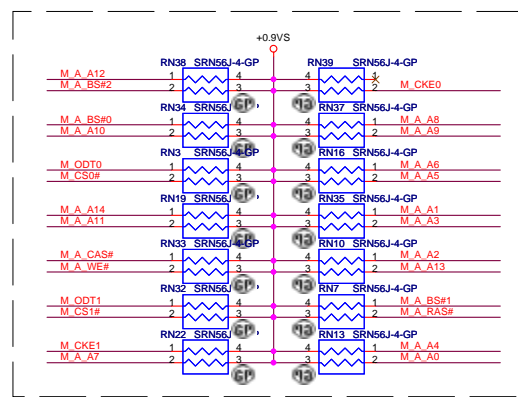
Layout Note:
Place near DM1



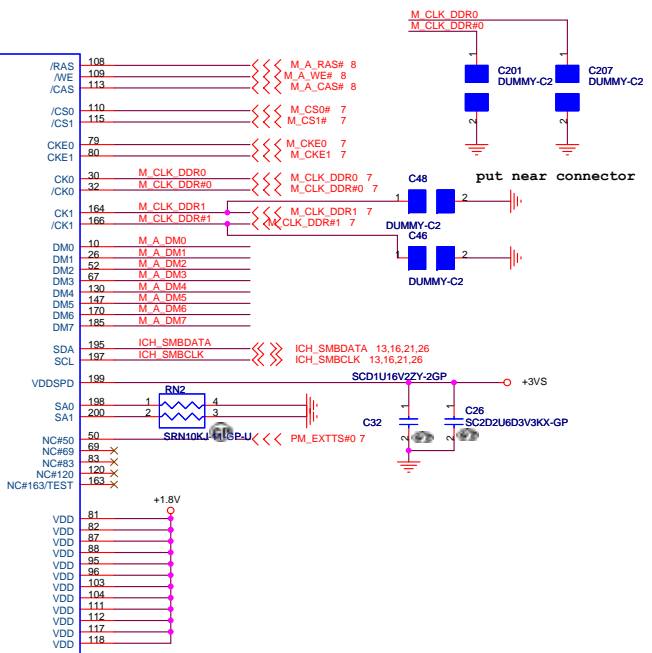
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistors closely DM1, all trace length Max=1.5"



DM2	
M_A A0	102 A0
M_A A1	101 A1
M_A A2	100 A2
M_A A3	99 A3
M_A A4	98 A4
M_A A5	97 A5
M_A A6	94 A6
M_A A7	92 A7
M_A A8	93 A8
M_A A9	91 A9
M_A A10	105 A10/AP
M_A A11	90 A11
M_A A12	89 A12
M_A A13	116 A13
M_A A14	86 A14
M_A A15	84 A15
M_A BS#2	X 84 A16/BA2
M_A BS#0	107 BA0
M_A BS#1	106 BA1
M_A DQ0	5 DQ0
M_A DQ1	7 DQ1
M_A DQ2	17 DQ2
M_A DQ3	19 DQ3
M_A DQ4	4 DQ4
M_A DQ5	6 DQ5
M_A DQ6	14 DQ6
M_A DQ7	16 DQ7
M_A DQ8	23 DQ8
M_A DQ9	25 DQ9
M_A DQ10	35 DQ10
M_A DQ11	37 DQ11
M_A DQ12	20 DQ12
M_A DQ13	22 DQ13
M_A DQ14	36 DQ14
M_A DQ15	38 DQ15
M_A DQ16	43 DQ16
M_A DQ17	45 DQ17
M_A DQ18	55 DQ18
M_A DQ19	57 DQ19
M_A DQ20	44 DQ20
M_A DQ21	46 DQ21
M_A DQ22	56 DQ22
M_A DQ23	58 DQ23
M_A DQ24	61 DQ24
M_A DQ25	63 DQ25
M_A DQ26	73 DQ26
M_A DQ27	75 DQ27
M_A DQ28	62 DQ28
M_A DQ29	64 DQ29
M_A DQ30	74 DQ30
M_A DQ31	76 DQ31
M_A DQ32	123 DQ32
M_A DQ33	125 DQ33
M_A DQ34	135 DQ34
M_A DQ35	137 DQ35
M_A DQ36	124 DQ36
M_A DQ37	134 DQ37
M_A DQ38	126 DQ38
M_A DQ39	136 DQ39
M_A DQ40	141 DQ40
M_A DQ41	143 DQ41
M_A DQ42	151 DQ42
M_A DQ43	153 DQ43
M_A DQ44	140 DQ44
M_A DQ45	142 DQ45
M_A DQ46	152 DQ46
M_A DQ47	154 DQ47
M_A DQ48	157 DQ48
M_A DQ49	159 DQ49
M_A DQ50	173 DQ50
M_A DQ51	175 DQ51
M_A DQ52	158 DQ52
M_A DQ53	160 DQ53
M_A DQ54	174 DQ54
M_A DQ55	176 DQ55
M_A DQ56	179 DQ56
M_A DQ57	181 DQ57
M_A DQ58	189 DQ58
M_A DQ59	191 DQ59
M_A DQ60	180 DQ60
M_A DQ61	182 DQ61
M_A DQ62	192 DQ62
M_A DQ63	194 DQ63
M_A DQS#0	11 /DQ50
M_A DQS#1	29 /DQ51
M_A DQS#2	49 /DQ52
M_A DQS#3	68 /DQ53
M_A DQS#4	123 /DQ54
M_A DQS#5	146 /DQ55
M_A DQS#6	167 /DQ56
M_A DQS#7	188 /DQ57
M_A DQS0	13 DQ50
M_A DQS1	31 DQ51
M_A DQS2	51 DQ52
M_A DQS3	70 DQ53
M_A DQS4	131 DQ54
M_A DQS5	148 DQ55
M_A DQS6	169 DQ56
M_A DQS7	188 DQ57
M_ODT0	114 ODT0
M_ODT1	119 ODT1
VREF	1 VREF
VSS	2 VSS
GND	202 GND



DM2 use 62.10017.E11

<Core Design>

緯創資通 Wistron Corporation
 21F, 80, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

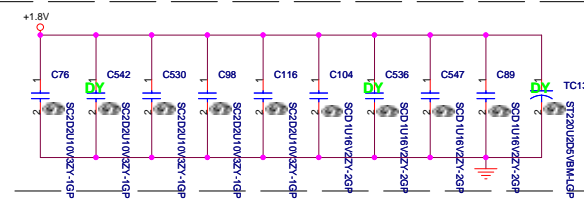
Title: **DDRII-SODIMM SLOT1**

Size Custom Document Number **VITAS** Rev **SA**

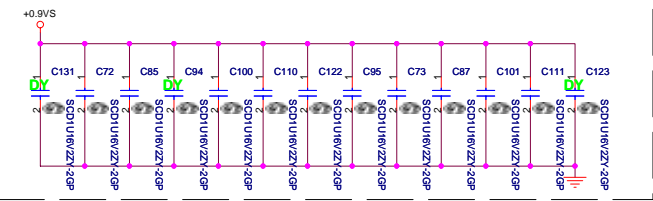
Date: Monday, May 05, 2008 Sheet 12 of 48

8 M_B_DQS[7..0] <<< <<<
 8 M_B_DC[63..0] <<< <<<
 8 M_B_DM[7..0] <<< <<<
 8 M_B_DQS[7..0] <<< <<<
 8 M_B_A[14..0] <<< <<<

Layout Note:
Place near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



M_B_A0	102	A0
M_B_A1	101	A1
M_B_A2	100	A2
M_B_A3	99	A3
M_B_A4	98	A4
M_B_A5	97	A5
M_B_A6	94	A6
M_B_A7	92	A7
M_B_A8	93	A8
M_B_A9	91	A9
M_B_A10	105	A10/AP
M_B_A11	96	A11
M_B_A12	89	A12
M_B_A13	116	A13
M_B_A14	86	A14
M_B_A15	84	A15

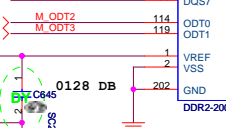
8 M_B_BS#2 >>>
 8 M_B_BS#0 >>>
 8 M_B_BS#1 >>>

M_B_BS#2	107	BA0
M_B_BS#0	107	BA0
M_B_BS#1	106	BA1
M_B_DQ0	5	DQ0
M_B_DQ1	7	DQ1
M_B_DQ2	17	DQ2
M_B_DQ3	14	DQ3
M_B_DQ4	4	DQ4
M_B_DQ5	6	DQ5
M_B_DQ6	14	DQ6
M_B_DQ7	19	DQ7
M_B_DQ8	23	DQ8
M_B_DQ9	25	DQ9
M_B_DQ10	36	DQ10
M_B_DQ11	37	DQ11
M_B_DQ12	20	DQ12
M_B_DQ13	36	DQ13
M_B_DQ14	22	DQ14
M_B_DQ15	38	DQ15
M_B_DQ16	43	DQ16
M_B_DQ17	46	DQ17
M_B_DQ18	55	DQ18
M_B_DQ19	57	DQ19
M_B_DQ20	46	DQ20
M_B_DQ21	94	DQ21
M_B_DQ22	56	DQ22
M_B_DQ23	58	DQ23
M_B_DQ24	61	DQ24
M_B_DQ25	63	DQ25
M_B_DQ26	73	DQ26
M_B_DQ27	75	DQ27
M_B_DQ28	62	DQ28
M_B_DQ29	64	DQ29
M_B_DQ30	74	DQ30
M_B_DQ31	76	DQ31
M_B_DQ32	123	DQ32
M_B_DQ33	125	DQ33
M_B_DQ34	135	DQ34
M_B_DQ35	137	DQ35
M_B_DQ36	124	DQ36
M_B_DQ37	126	DQ37
M_B_DQ38	134	DQ38
M_B_DQ39	136	DQ39
M_B_DQ40	141	DQ40
M_B_DQ41	143	DQ41
M_B_DQ42	151	DQ42
M_B_DQ43	153	DQ43
M_B_DQ44	140	DQ44
M_B_DQ45	142	DQ45
M_B_DQ46	152	DQ46
M_B_DQ47	154	DQ47
M_B_DQ48	157	DQ48
M_B_DQ49	159	DQ49
M_B_DQ50	173	DQ50
M_B_DQ51	175	DQ51
M_B_DQ52	158	DQ52
M_B_DQ53	160	DQ53
M_B_DQ54	174	DQ54
M_B_DQ55	178	DQ55
M_B_DQ56	179	DQ56
M_B_DQ57	181	DQ57
M_B_DQ58	189	DQ58
M_B_DQ59	191	DQ59
M_B_DQ60	180	DQ60
M_B_DQ61	192	DQ61
M_B_DQ62	192	DQ62
M_B_DQ63	194	DQ63

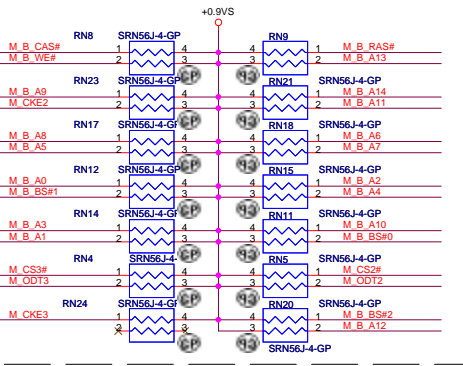
M_B_DQS#0	11	DQS0
M_B_DQS#1	29	DQS1
M_B_DQS#2	48	DQS2
M_B_DQS#3	48	DQS3
M_B_DQS#4	129	DQS4
M_B_DQS#5	146	DQS5
M_B_DQS#6	167	DQS6
M_B_DQS#7	186	DQS7
M_B_DQS0	13	DQS0
M_B_DQS1	31	DQS1
M_B_DQS2	51	DQS2
M_B_DQS3	70	DQS3
M_B_DQS4	131	DQS4
M_B_DQS5	148	DQS5
M_B_DQS6	169	DQS6
M_B_DQS7	189	DQS7
M_B_ODT0	114	ODT0
M_B_ODT1	119	ODT1

M_B_ODT2	7	ODT2
M_B_ODT3	7	ODT3
M_B_DQS#0	11	DQS0
M_B_DQS#1	29	DQS1
M_B_DQS#2	48	DQS2
M_B_DQS#3	48	DQS3
M_B_DQS#4	129	DQS4
M_B_DQS#5	146	DQS5
M_B_DQS#6	167	DQS6
M_B_DQS#7	186	DQS7
M_B_DQS0	13	DQS0
M_B_DQS1	31	DQS1
M_B_DQS2	51	DQS2
M_B_DQS3	70	DQS3
M_B_DQS4	131	DQS4
M_B_DQS5	148	DQS5
M_B_DQS6	169	DQS6
M_B_DQS7	189	DQS7
M_B_ODT0	114	ODT0
M_B_ODT1	119	ODT1

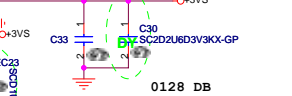
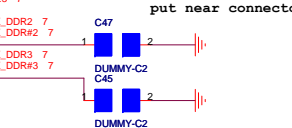
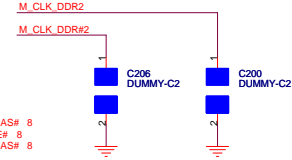
M_B_DQS#0	11	DQS0
M_B_DQS#1	29	DQS1
M_B_DQS#2	48	DQS2
M_B_DQS#3	48	DQS3
M_B_DQS#4	129	DQS4
M_B_DQS#5	146	DQS5
M_B_DQS#6	167	DQS6
M_B_DQS#7	186	DQS7
M_B_DQS0	13	DQS0
M_B_DQS1	31	DQS1
M_B_DQS2	51	DQS2
M_B_DQS3	70	DQS3
M_B_DQS4	131	DQS4
M_B_DQS5	148	DQS5
M_B_DQS6	169	DQS6
M_B_DQS7	189	DQS7
M_B_ODT0	114	ODT0
M_B_ODT1	119	ODT1



DM1 use 62.10017.B51



Layout Note:
Place these resistors closely DM2, all trace length Max=1.5"



<Core Design>

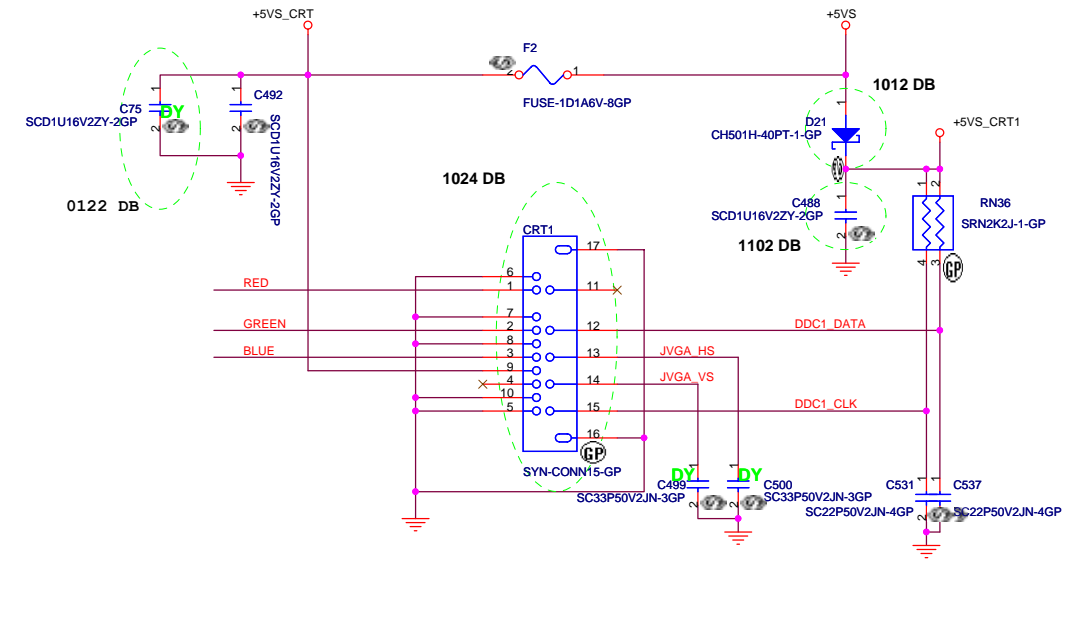
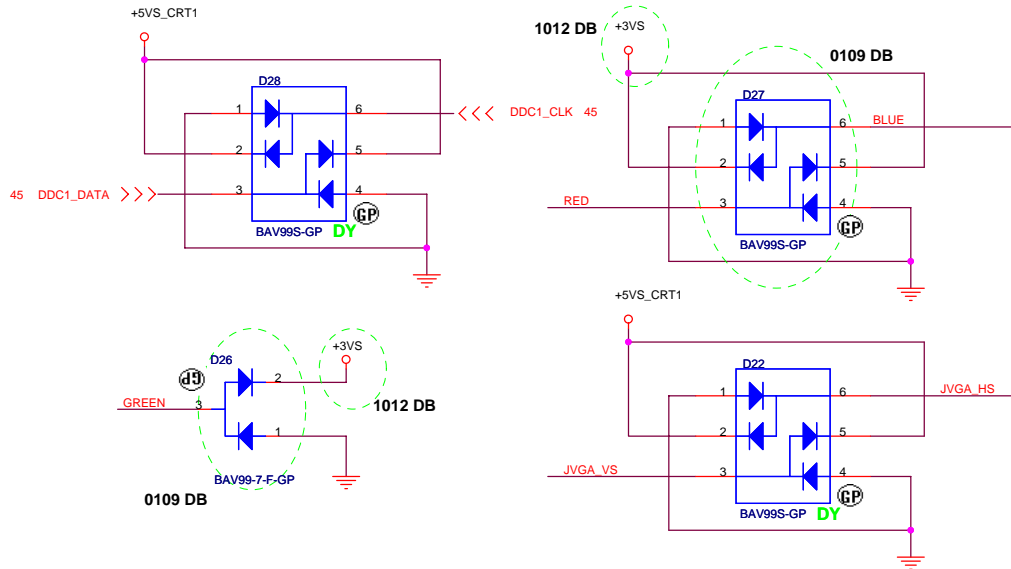
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 321, Taiwan, R.O.C.

Title: **DDR1L-SODIMM SLOT2**

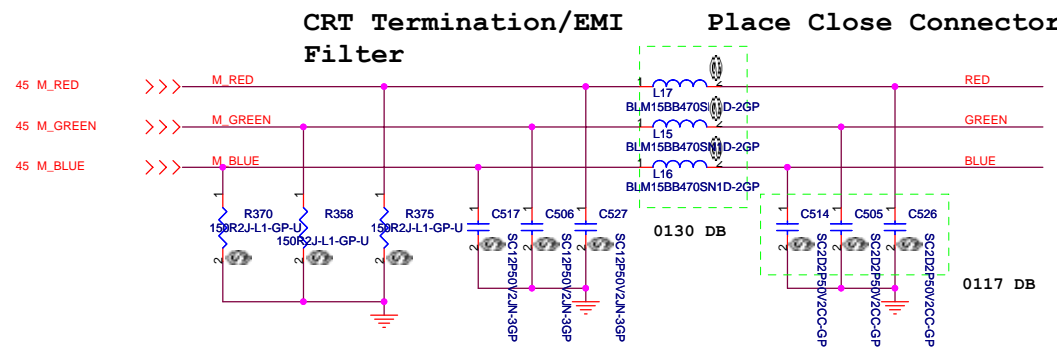
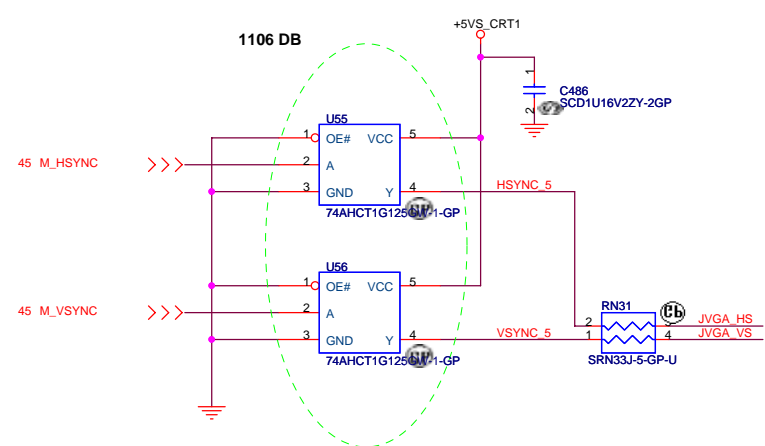
Size: Custom Document Number: VITAS Rev: SA

Date: Monday, May 05, 2008 Sheet 13 of 48

CRT I/F & CONNECTOR



Layout Note:
 * Must be a ground return path between this ground and the ground on the VGA connector.
 Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



<Core Design>

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT Connector**

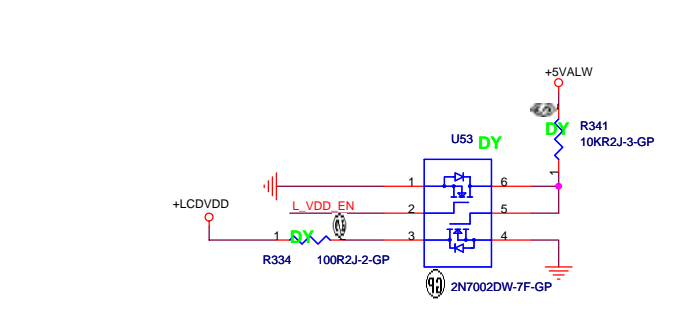
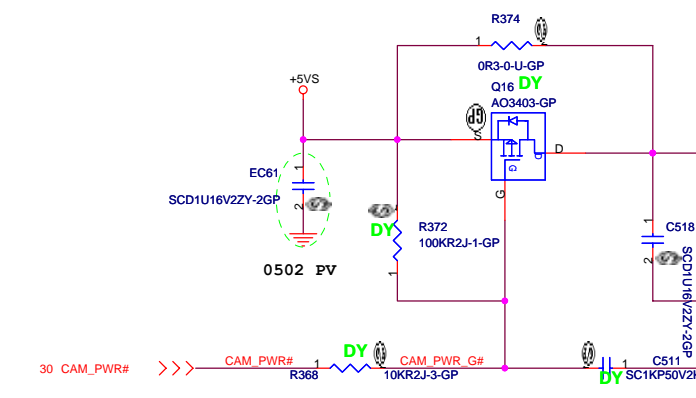
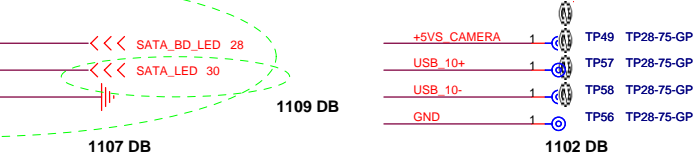
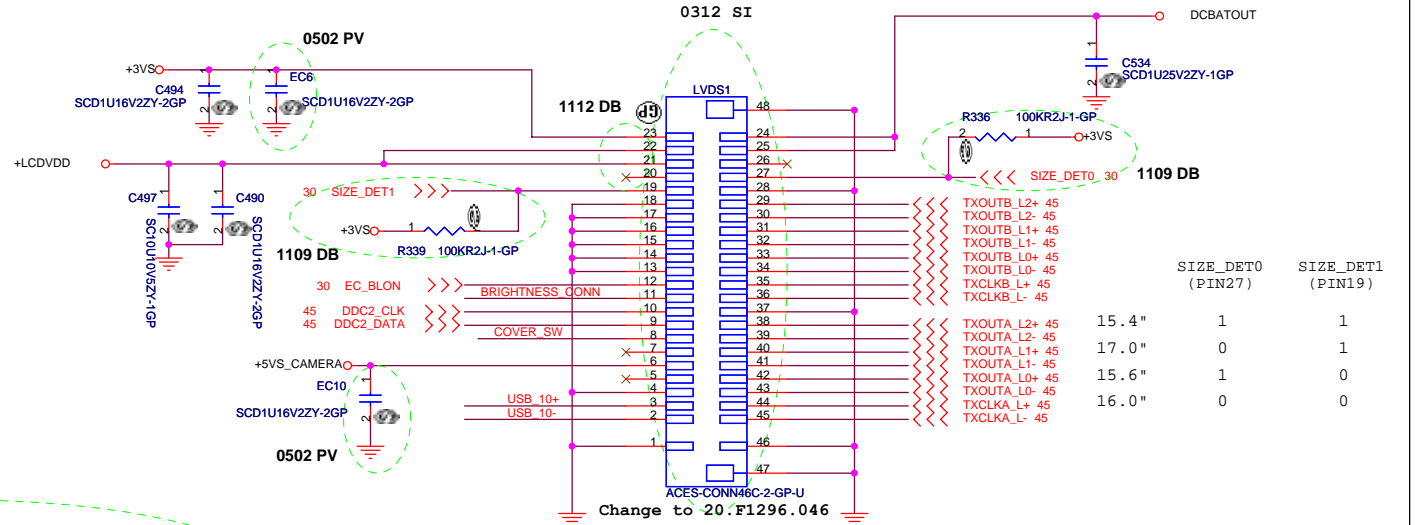
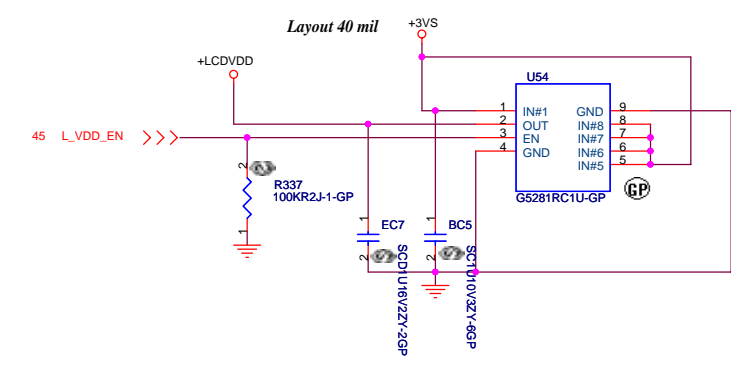
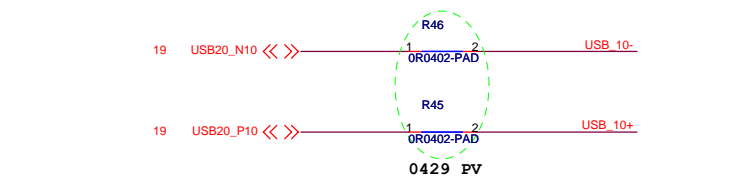
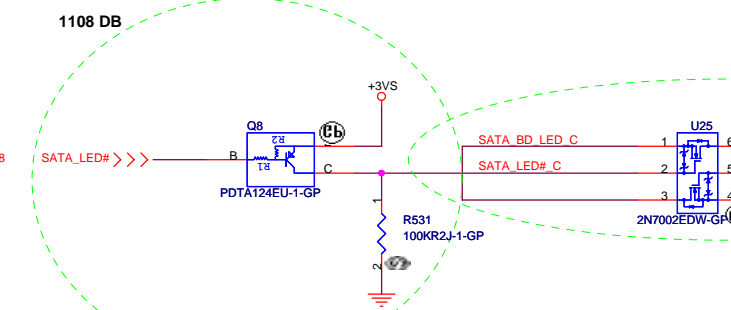
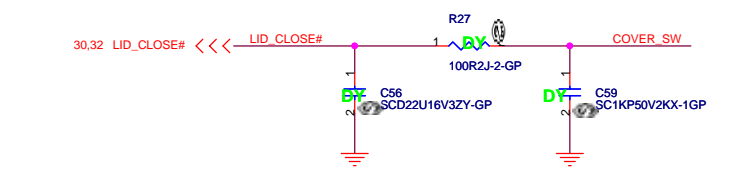
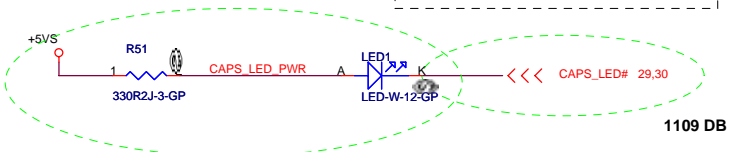
Size: A3 Document Number: **VITAS** Rev: SA

Date: Monday, May 05, 2008 Sheet 14 of 48

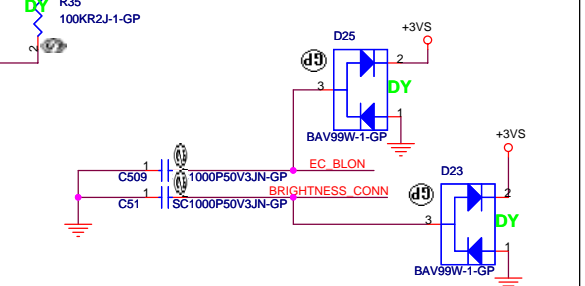
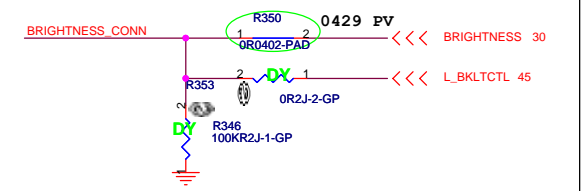
LCD / INVERTER INTERFACE / CAMERA

White LED:

Lite-On 83.00191.D70
Everlight 83.19217.F70



Signal	TXOUTB_L2+ 45	TXOUTB_L2- 45	TXOUTB_L1+ 45	TXOUTB_L1- 45	TXOUTB_L0+ 45	TXOUTB_L0- 45	TXCLKB_L+ 45	TXCLKB_L- 45	SIZE_DET0 (PIN27)	SIZE_DET1 (PIN19)
15.4"	1	1	0	1	15.6"	1	0	16.0"	0	0



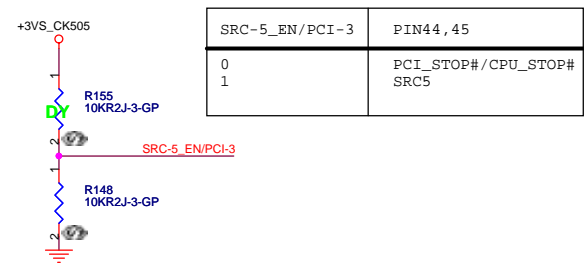
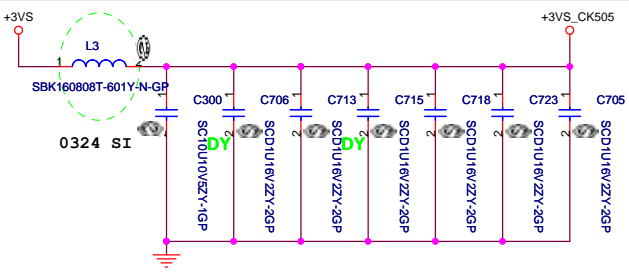
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

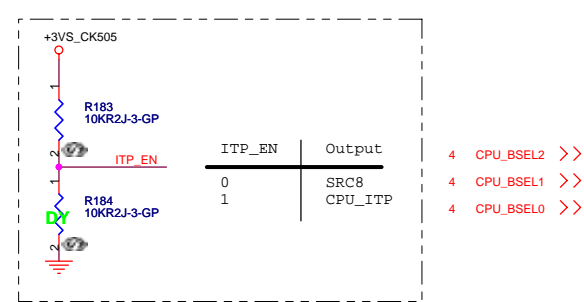
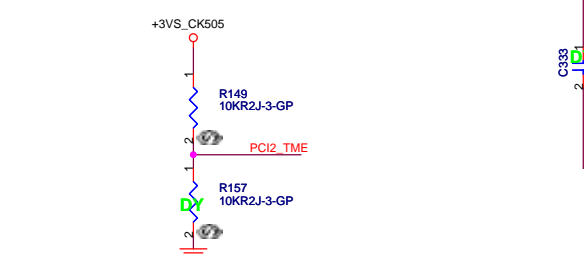
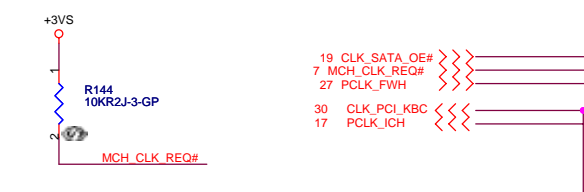
Title: **LCD/Inverter Connector/CAM/LED**

Size A3 | Document Number: **VITAS** | Rev: **SA**

Date: Monday, May 05, 2008 | Sheet 15 of 48

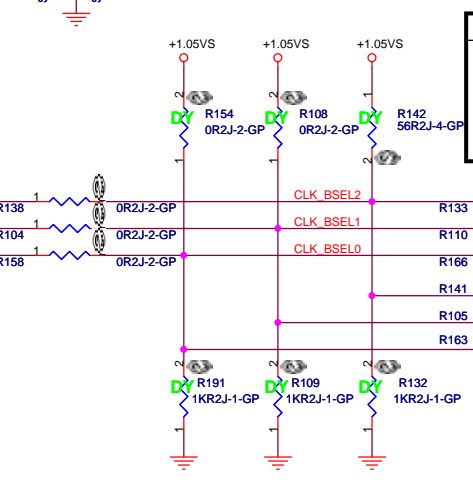
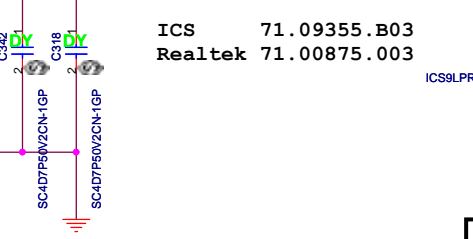
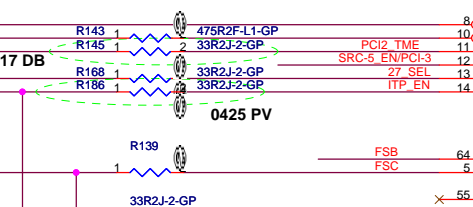
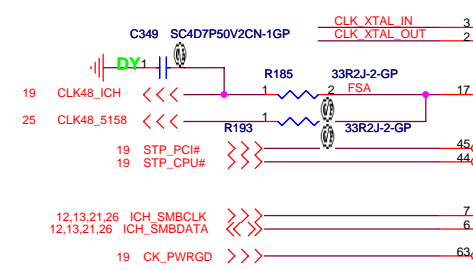
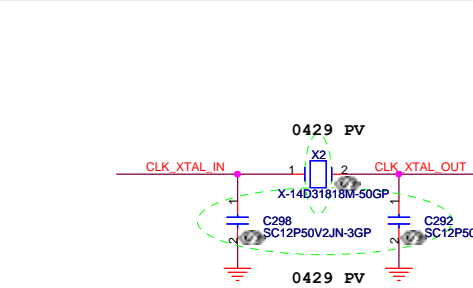


SRC-5_EN/PCI-3	PIN44, 45
0	PCI_STOP#/CPU_STOP#
1	

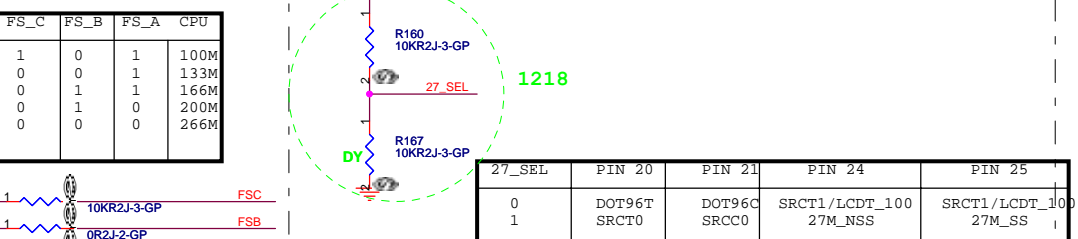
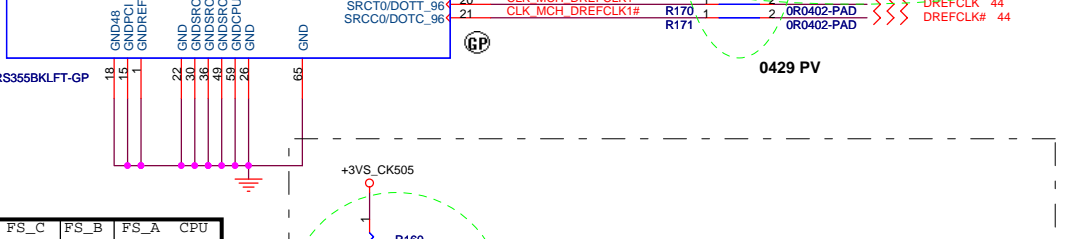
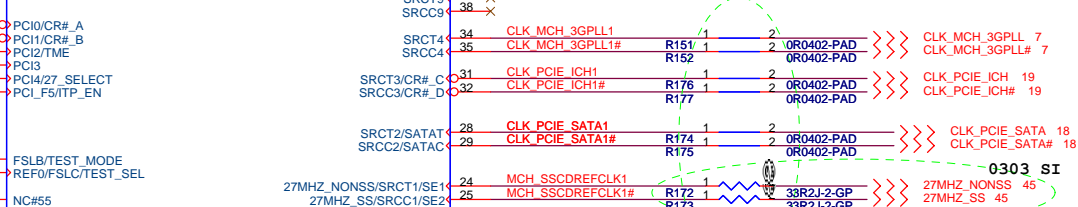
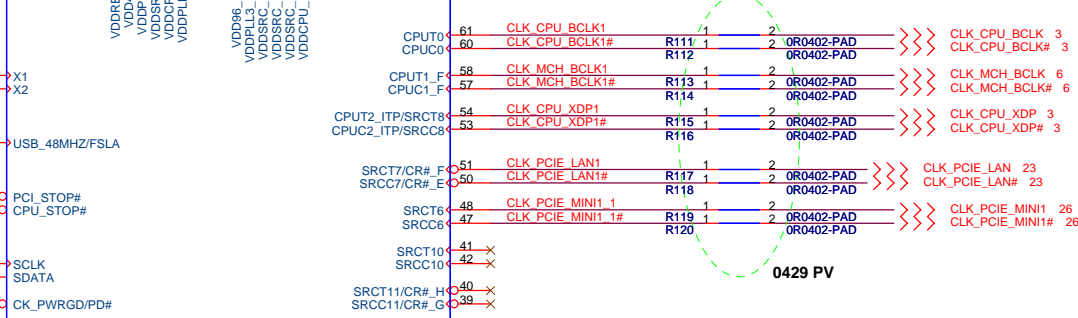
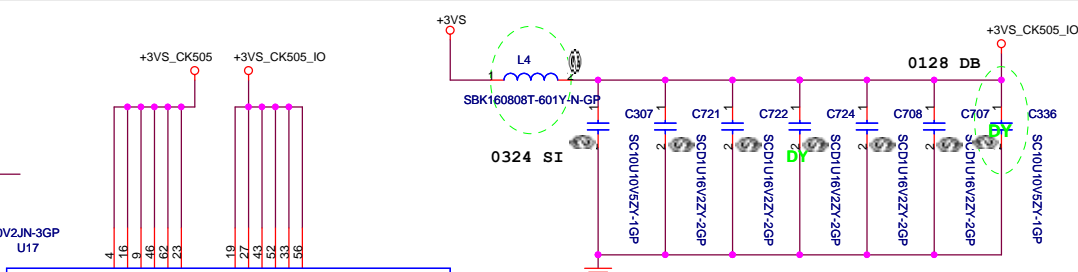


Design Note:

- All of Input pin didn't have internal pull up resistor.
- Clock Request (CR) function are enable by registers.
- CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.



FS_C	FS_B	FS_A	CPU
1	0	1	100M
0	0	1	133M
0	1	1	166M
0	1	0	200M
0	0	0	266M



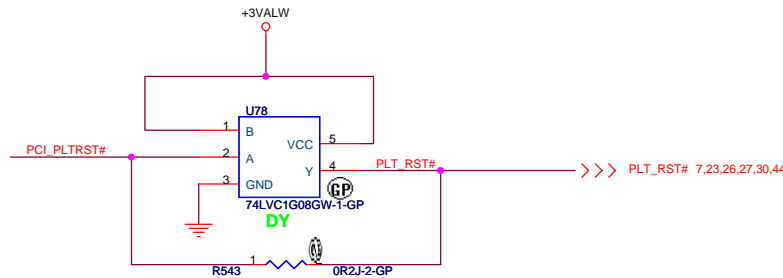
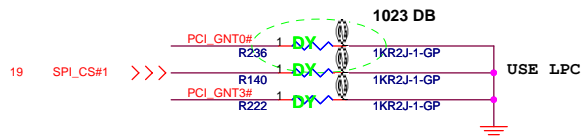
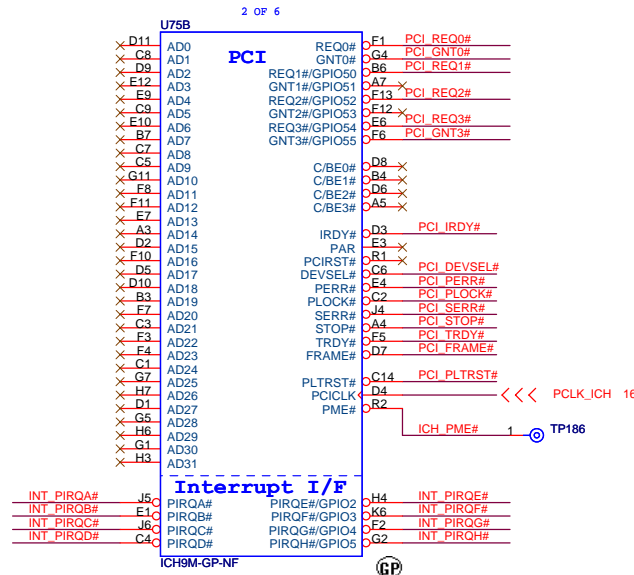
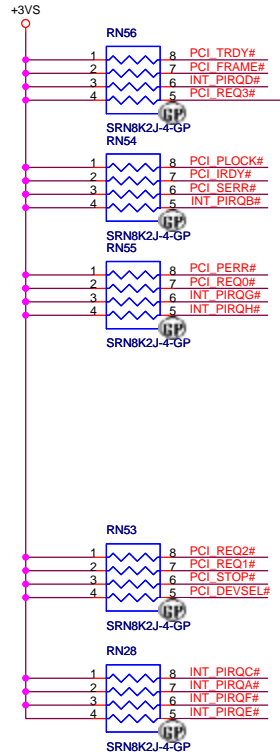
27_SEL	PIN 20	PIN 21	PIN 24	PIN 25
0	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1	SRCT0	SRCC0	27M_NSS	27M_SS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.

Clock Generator ICS9LPRS355

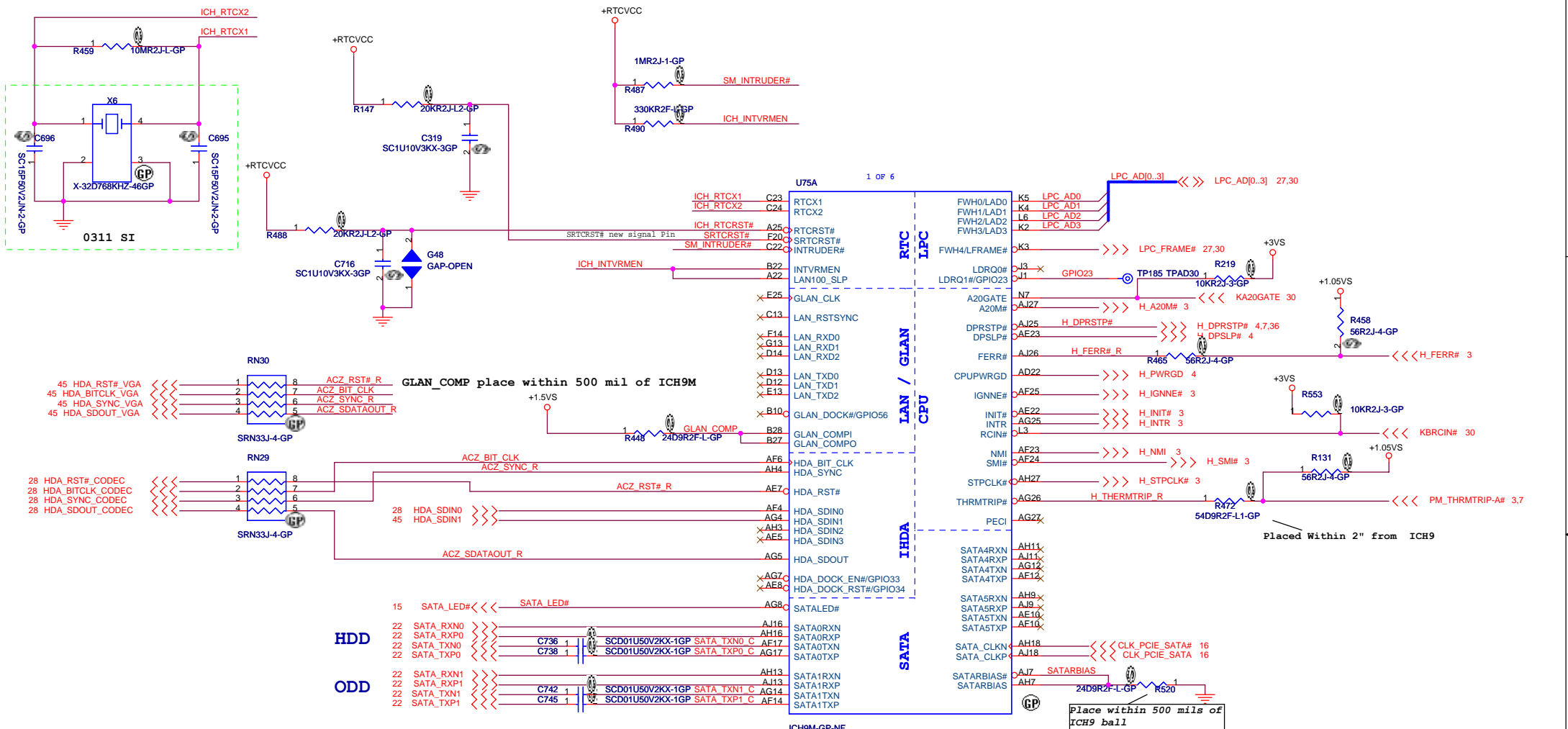
VITAS

Date: Monday, May 05, 2008 Sheet 16 of 48



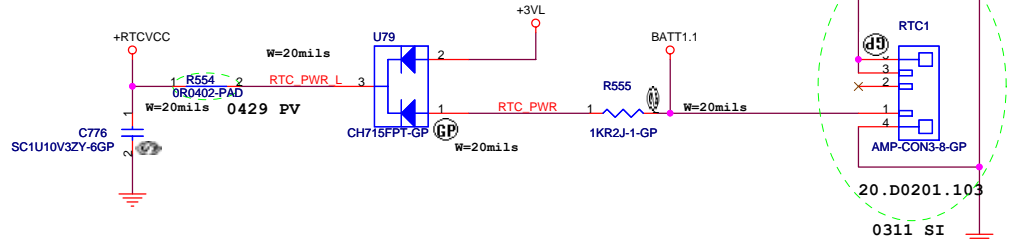
BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC (Default)
A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable high = default	

<Core Design>



GLAN_COMP place within 500 mil of ICH9M

Place within 500 mils of ICH9 ball



integrated VccSus1_05,VccSus1_5,VccCL1_5		
INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

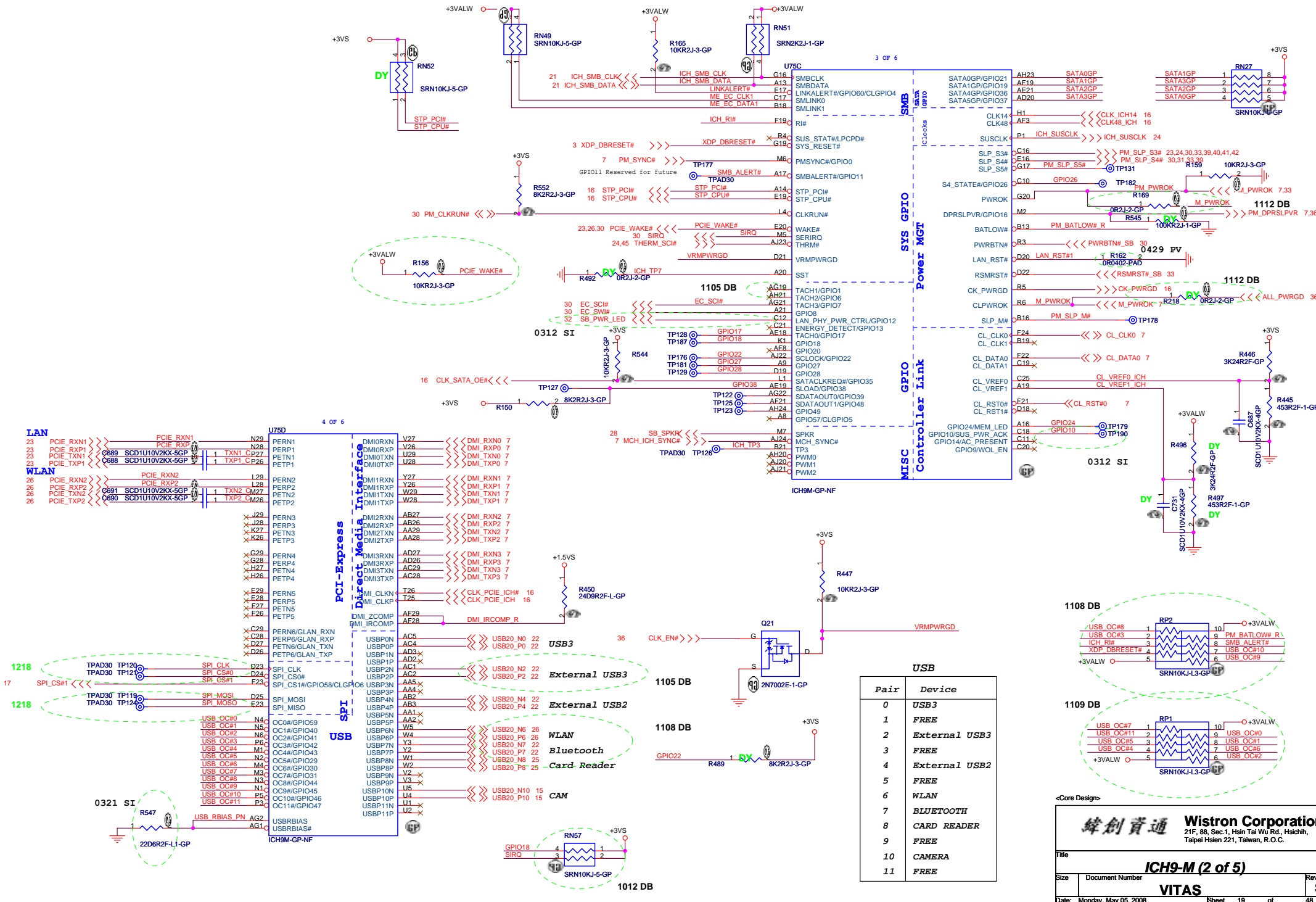
<Core Design>

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH9-M (2 of 5)**

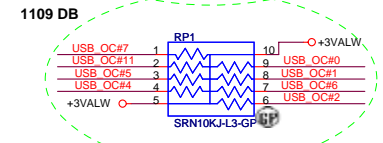
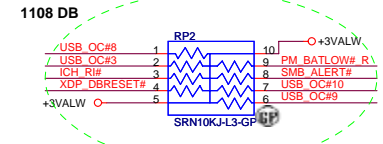
Size: Document Number: **VITAS** Rev: **SA**

Date: Monday, May 05, 2008 Sheet 18 of 48



USB

Pair	Device
0	USB3
1	FREE
2	External USB3
3	FREE
4	External USB2
5	FREE
6	WLAN
7	BLUETOOTH
8	CARD READER
9	FREE
10	CAMERA
11	FREE

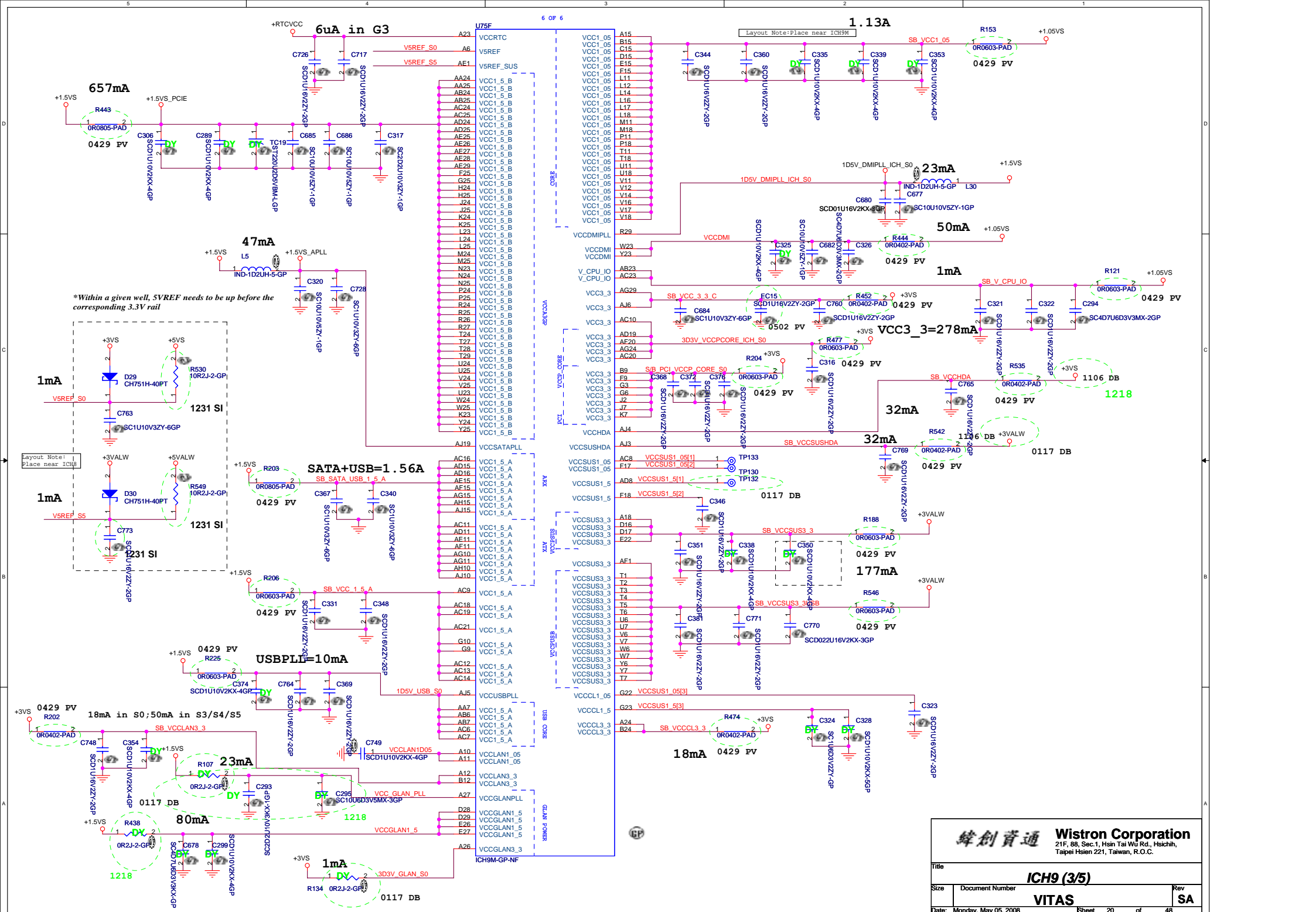


Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

ICH9-M (2 of 5)

VITAS

Date: Monday, May 05, 2008 Sheet 19 of 48

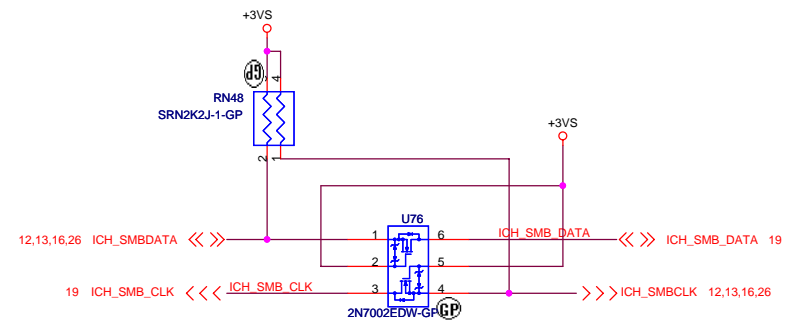


5 OF 6

AA26	VSS	H5
AA27	VSS	J23
AA3	VSS	J26
AA6	VSS	J27
AB1	VSS	AC22
AA23	VSS	K28
AB28	VSS	K29
AB29	VSS	L13
AB4	VSS	L15
AB5	VSS	L2
AC17	VSS	L26
AC26	VSS	L27
AC27	VSS	L5
AC3	VSS	L7
AD1	VSS	M12
AD10	VSS	M13
AD12	VSS	M14
AD13	VSS	M15
AD14	VSS	M16
AD17	VSS	M17
AD18	VSS	M23
AD21	VSS	M28
AD28	VSS	M29
AD29	VSS	N11
AD4	VSS	N12
AD5	VSS	N13
AD6	VSS	N14
AD7	VSS	N15
AD9	VSS	N16
AE12	VSS	N17
AE13	VSS	N18
AE14	VSS	N26
AE16	VSS	N27
AE17	VSS	P12
AE2	VSS	P13
AE20	VSS	P14
AE24	VSS	P15
AE3	VSS	P16
AE4	VSS	P17
AE6	VSS	P2
AE9	VSS	P23
AF13	VSS	P28
AF16	VSS	P29
AF18	VSS	P4
AF22	VSS	P7
AH26	VSS	R11
AE26	VSS	R12
AE27	VSS	R13
AF5	VSS	R14
AF7	VSS	R15
AF9	VSS	R16
AG13	VSS	R17
AG16	VSS	R18
AG18	VSS	R28
AG20	VSS	T12
AG23	VSS	T13
AG3	VSS	T14
AG6	VSS	T16
AG9	VSS	T16
AH12	VSS	T17
AH14	VSS	T23
AH17	VSS	B26
AH19	VSS	U12
AH2	VSS	U13
AH22	VSS	U14
AH25	VSS	U15
AH28	VSS	U16
AH5	VSS	U17
AH8	VSS	AD23
AJ12	VSS	U26
AJ14	VSS	U27
AJ17	VSS	U3
AJ8	VSS	V1
B11	VSS	V13
B14	VSS	V15
B17	VSS	V23
B2	VSS	V28
B20	VSS	V29
B23	VSS	V4
B5	VSS	V5
B8	VSS	W26
C26	VSS	W27
C27	VSS	W3
F11	VSS	Y1
E14	VSS	Y28
F18	VSS	Y29
F2	VSS	Y4
F21	VSS	Y5
F24	VSS	AG28
F5	VSS	AH6
F8	VSS	AF2
F16	VSS	B25
F28	VSS	
F29	VSS	A1 ICH_GND1 TP184
G12	VSS	A2
G14	VSS	A28 ICH_GND2 TP175
G18	VSS	A29
G21	VSS	AH1
G24	VSS	AH29
G26	VSS	AJ1 ICH_GND3 TP183
G27	VSS	AJ2
G8	VSS	AJ28
H2	VSS	AJ29 ICH_GND4 TP174
H23	VSS	B1
H28	VSS	B29
H29	VSS	

ICH9M-GP-NF

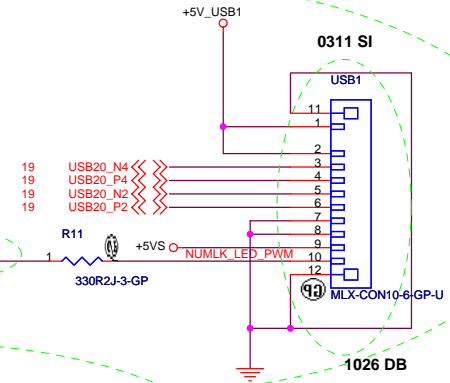
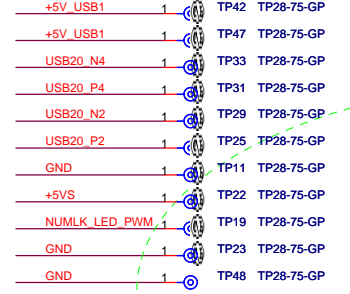
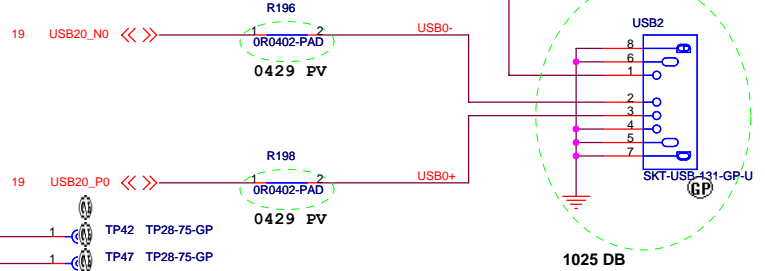
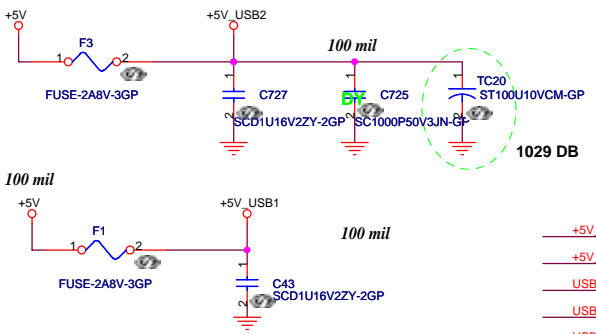
NCTF PIN



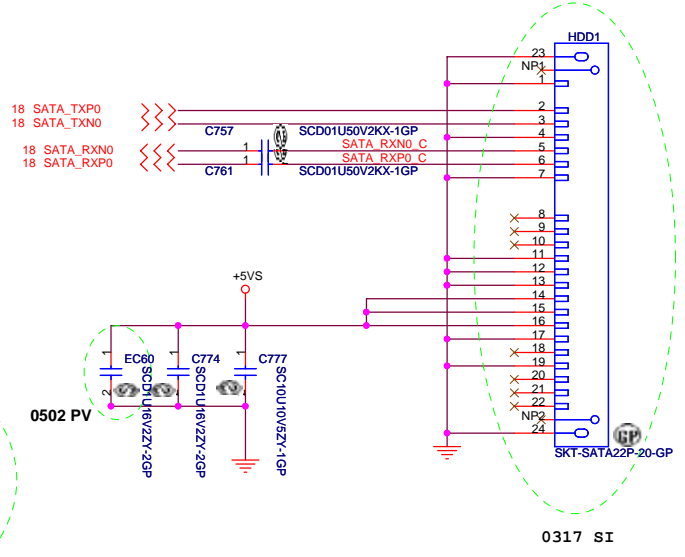
SMBUS

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
ICH9-M (4 of 4)			
Size	Document Number	Rev	SA
VITAS			
Date: Monday, May 05, 2008	Sheet 21	of 48	

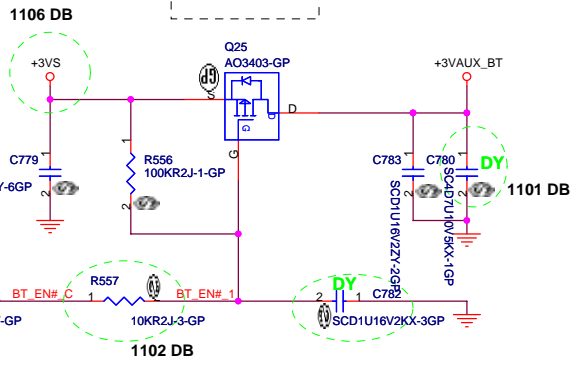
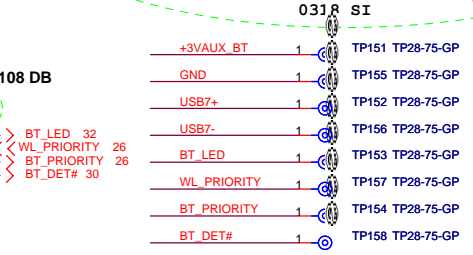
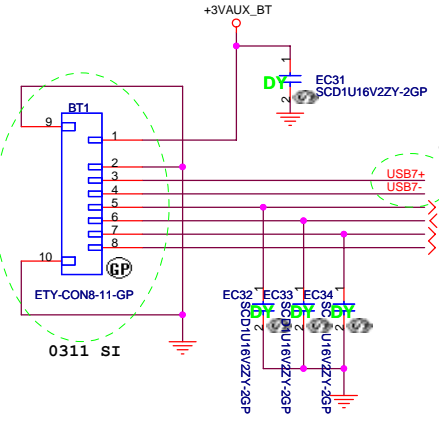
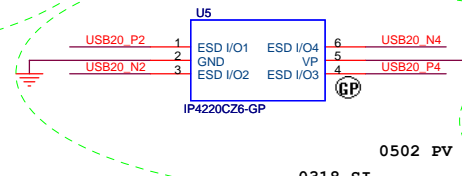
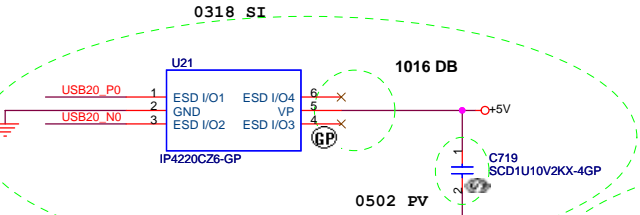
USB PORT



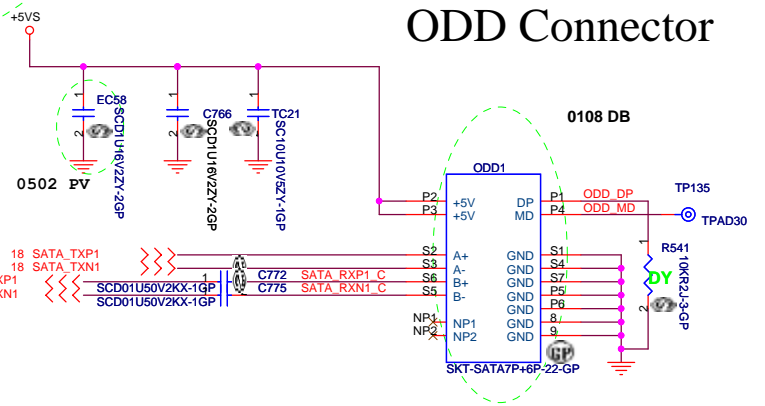
SATA HD Connector



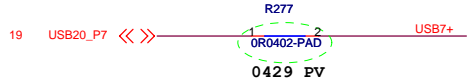
BLUETOOTH



ODD Connector



1108 DB



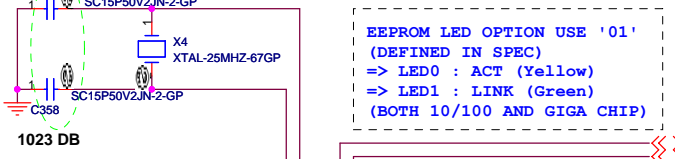
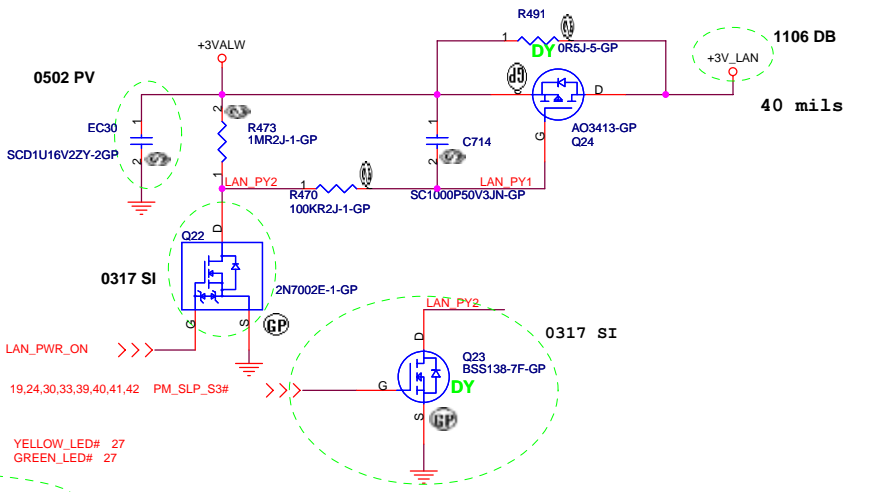
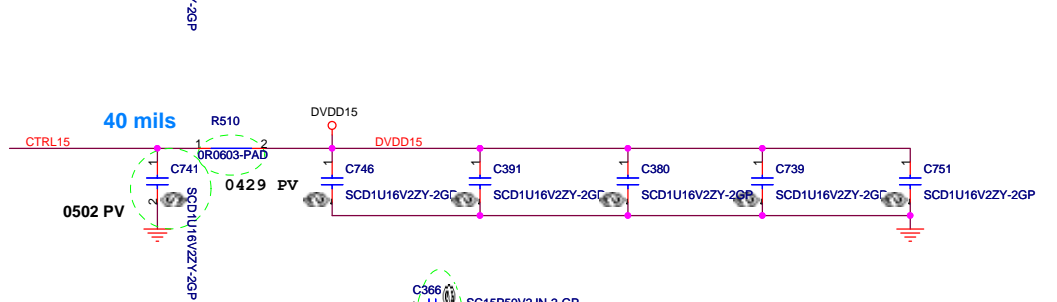
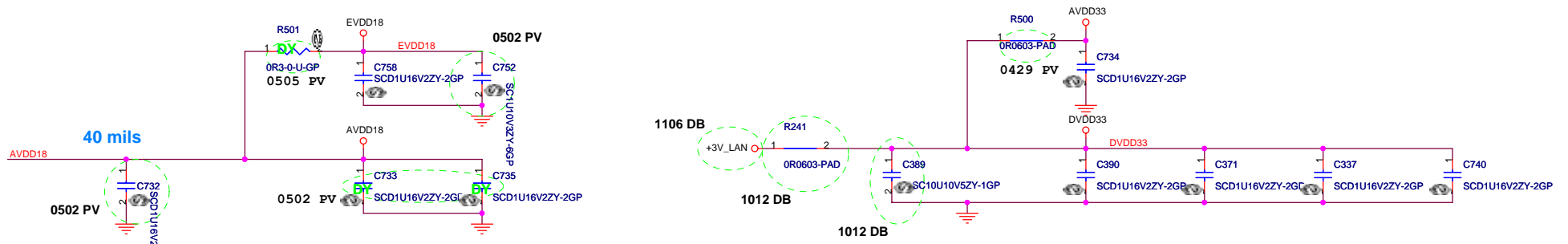
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

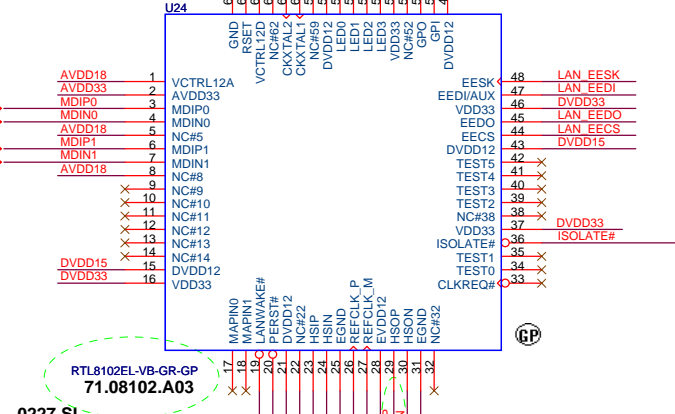
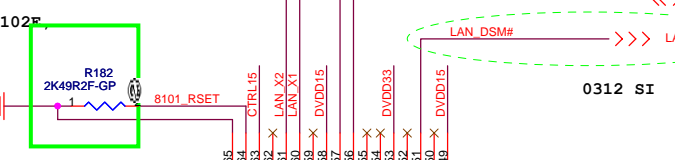
Title: **HDD/CDROM/USB/BT**

Size A3 Document Number: **VITAS** Rev **SA**

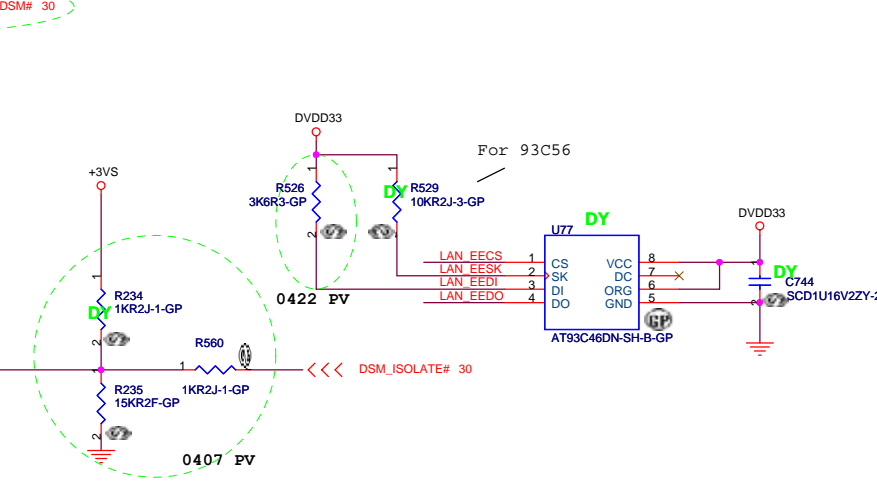
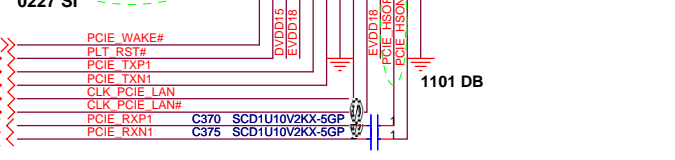
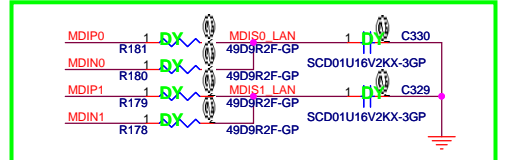
Date: Monday, May 05, 2008 Sheet 22 of 48



R548 should be 2.49K 1% ohm for 8102E
R548 should be 2K 1% for 8101E.



8101E use this circuit, 8102E dummy this circuit



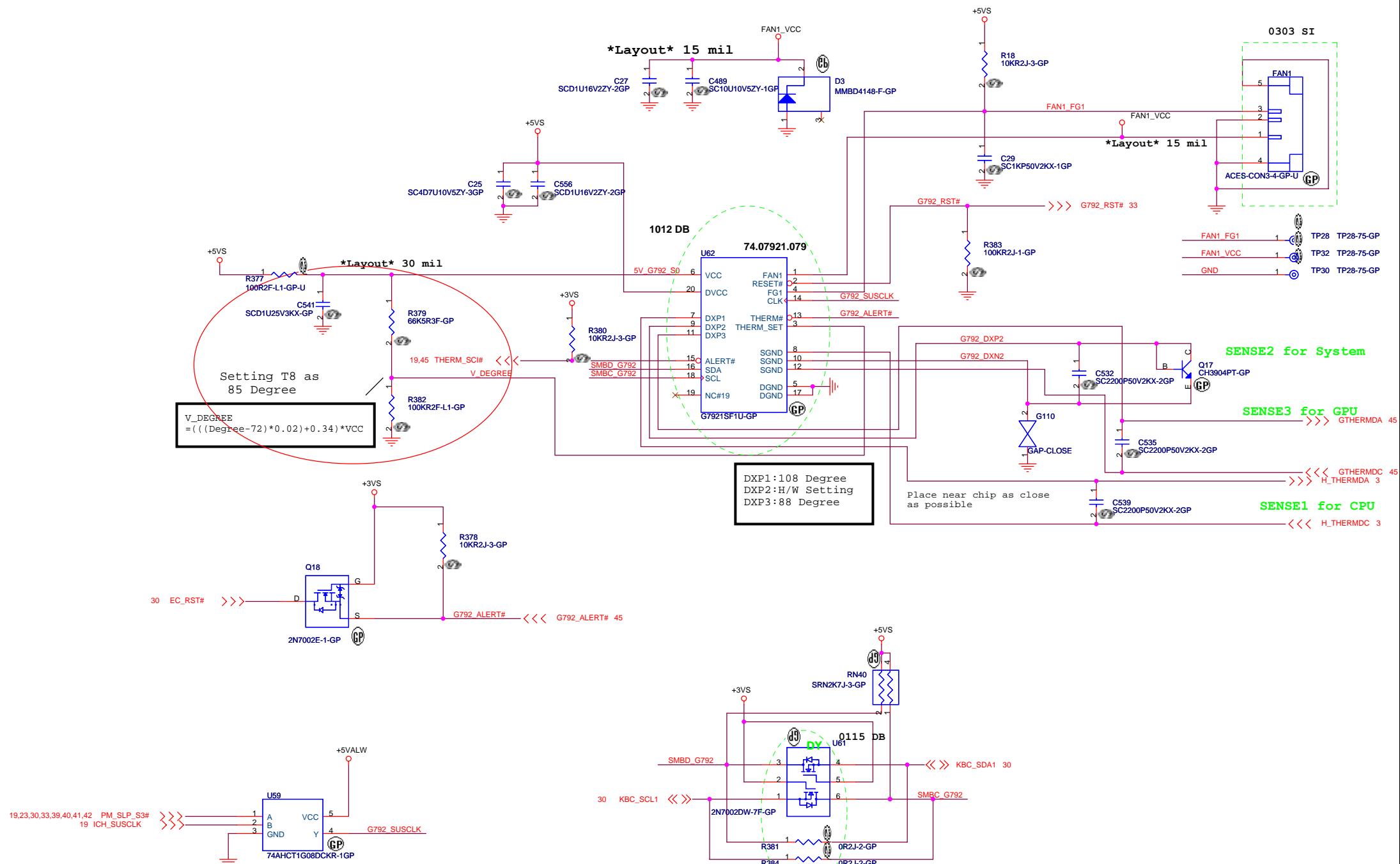
<Core Design>

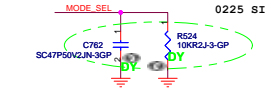
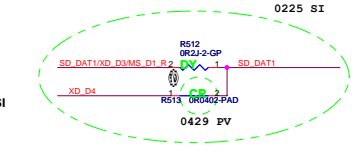
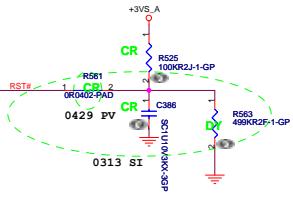
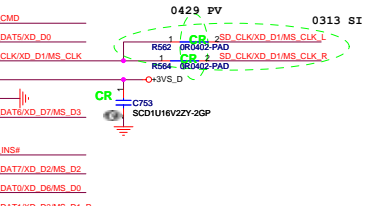
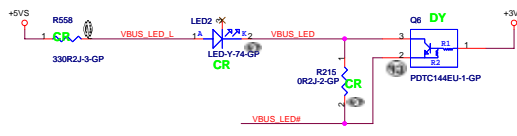
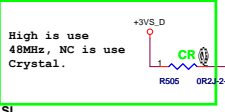
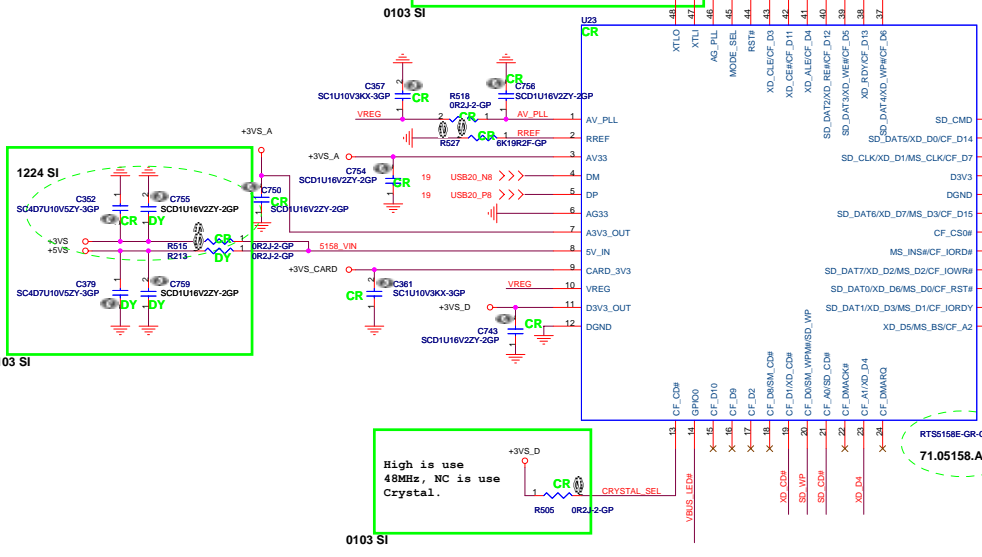
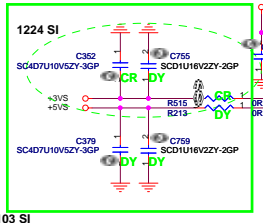
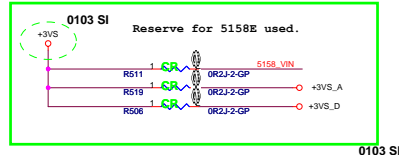
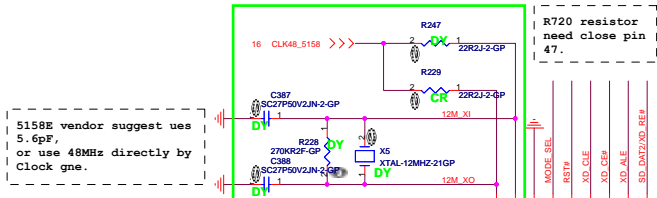
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **RTL8101E**

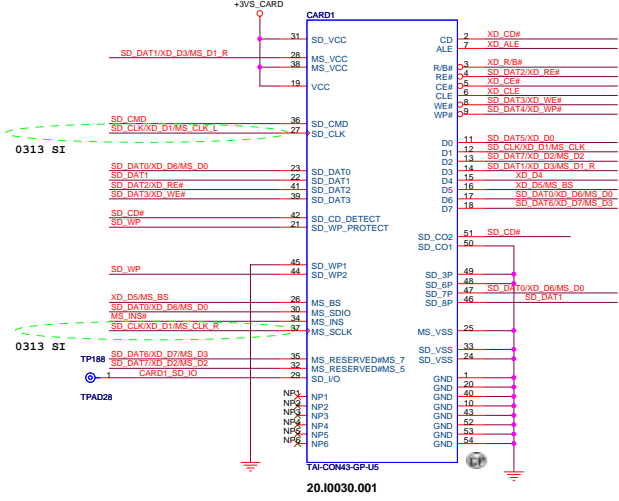
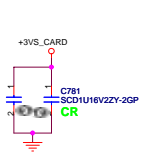
Size: A3 Document Number: **VITAS** Rev: SA

Date: Monday, May 05, 2008 Sheet: 23 of 48





4 IN1 CARD-READER (SD/SD IO/MMC/MMC4.0/MS/MS PRO/XD)

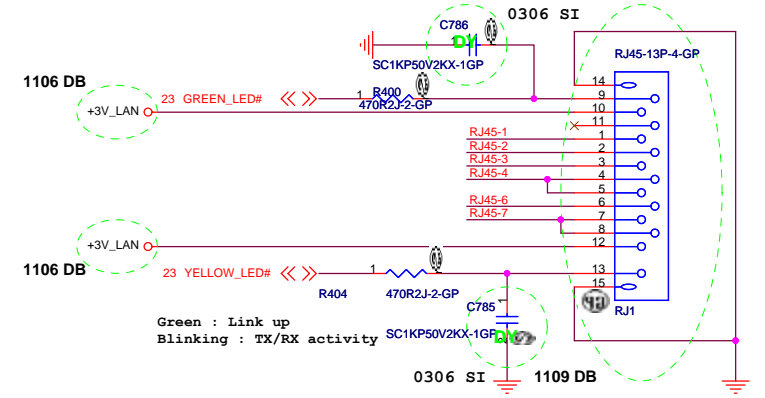
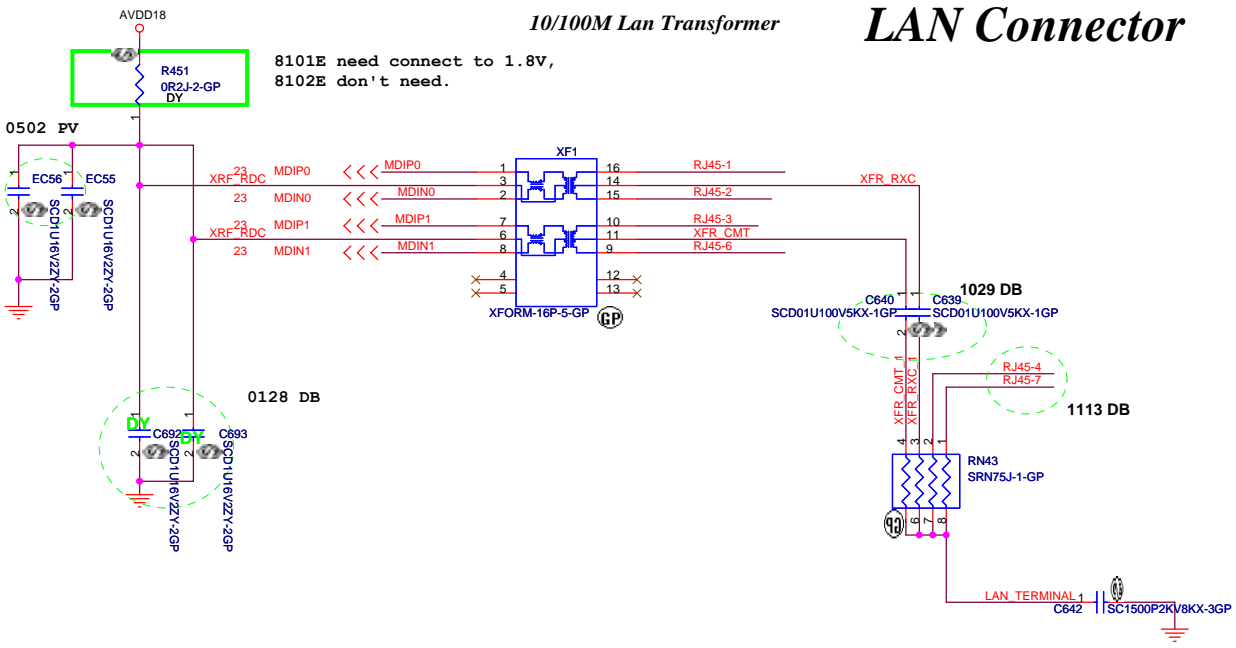


10/100M Lan Transformer

LAN Connector

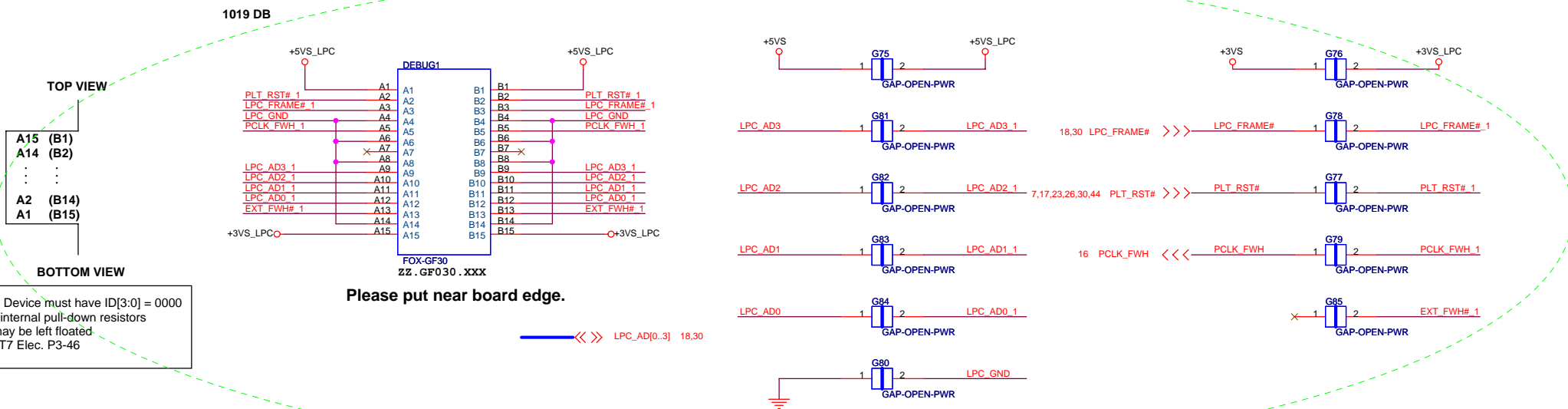
1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

PIN A1 : GREEN
PIN A3 : ORANGE
PIN B2 : YELLOW



Remark:
Add trace width to 20mils for RJ1 pin4, 5 and pin 7, 8.

Golden-Finger for Debug Board



Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

Please put near board edge.

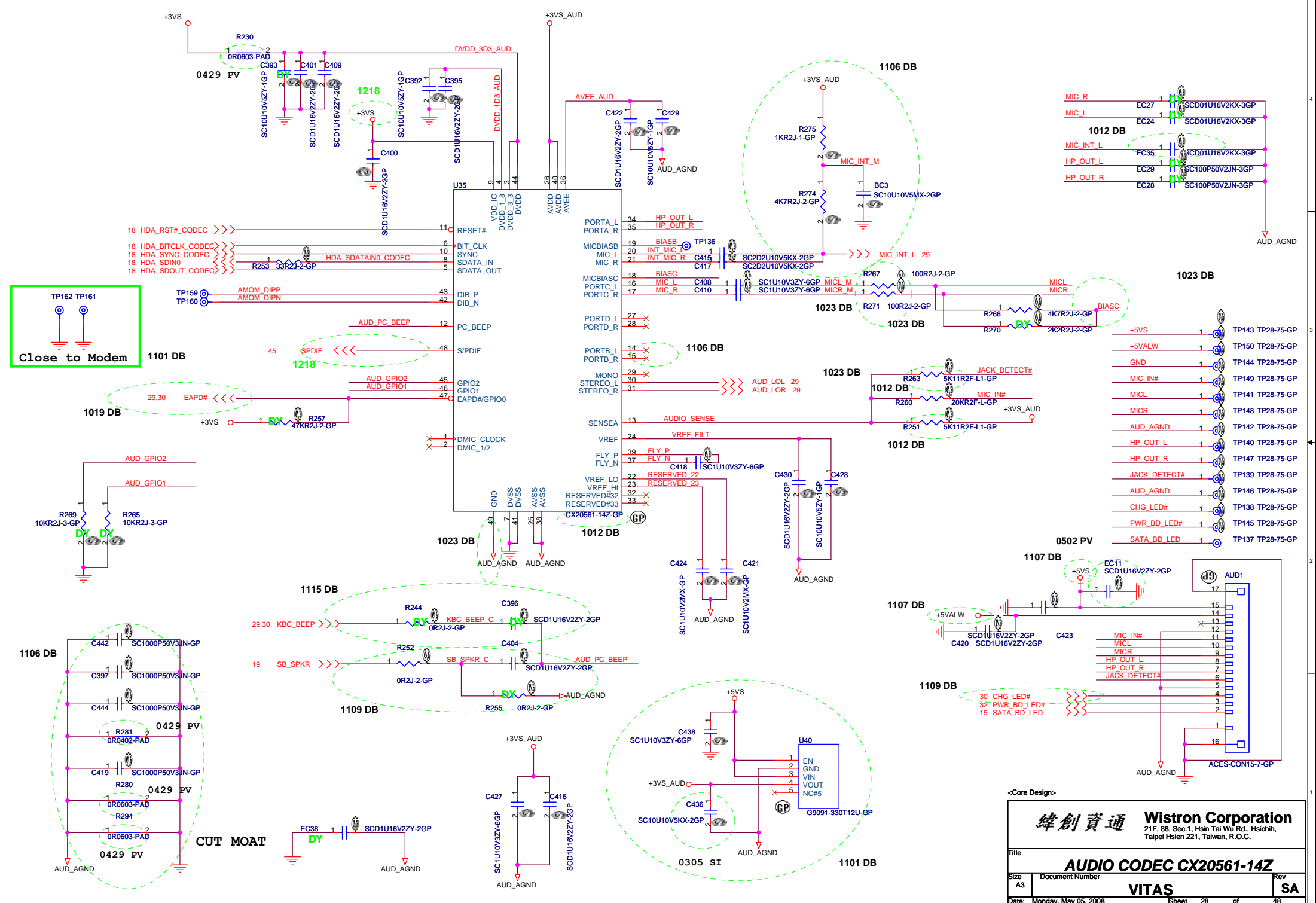
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN CONN/Debug**

Size A3 Document Number: **VITAS** Rev: **SA**

Date: Monday, May 05, 2008 Sheet 27 of 48



TP162 TP161
Close to Modem

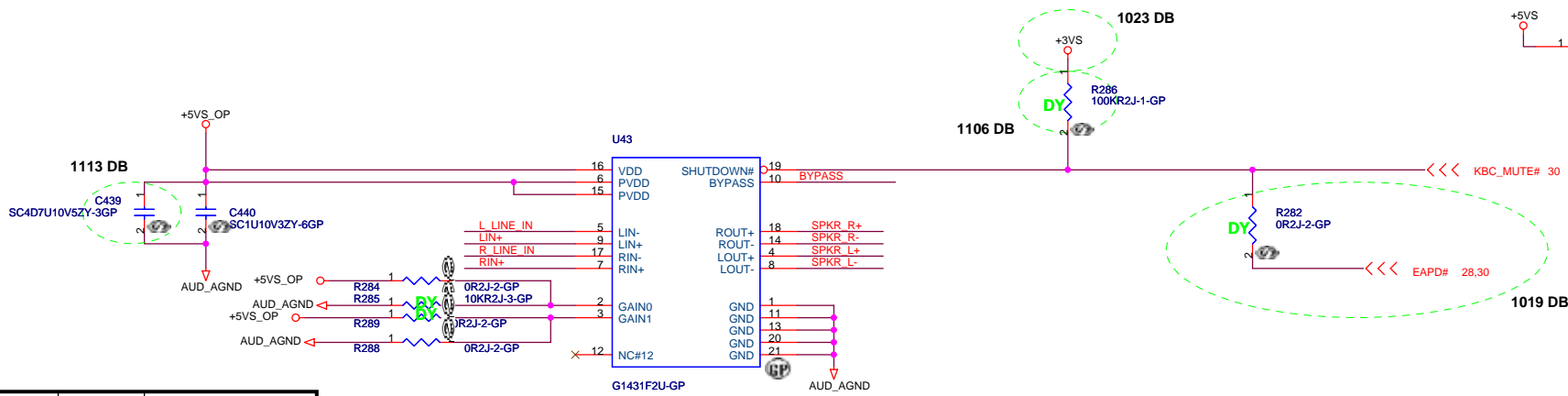
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

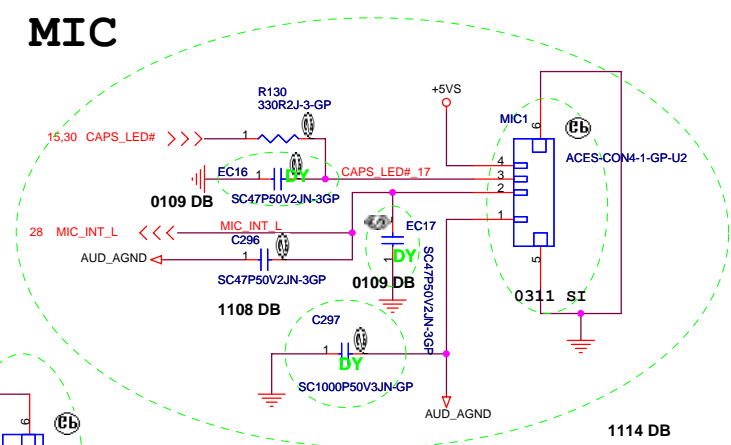
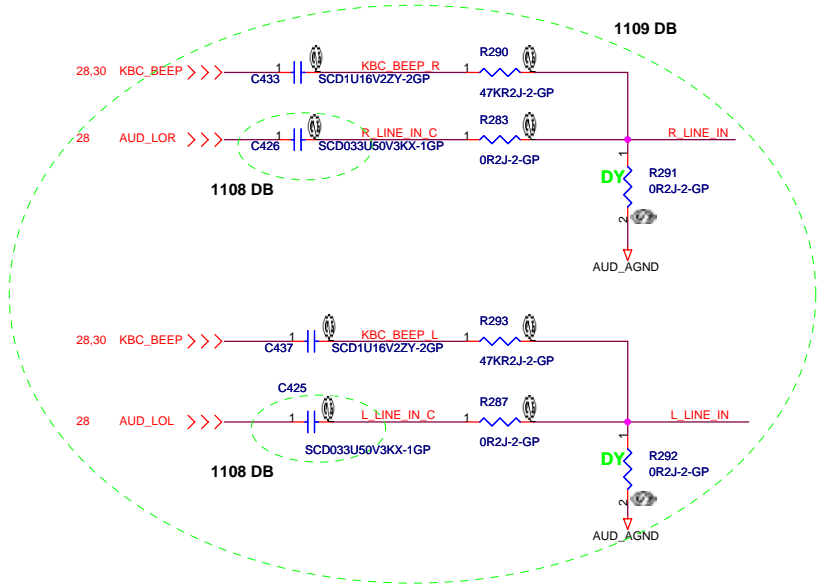
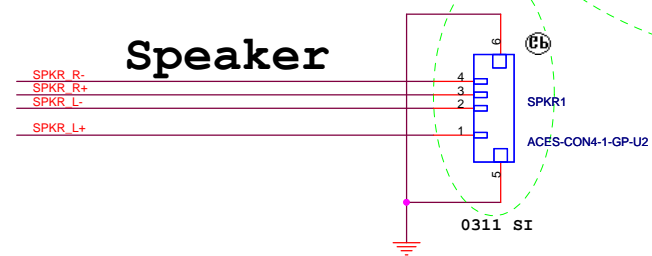
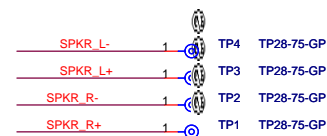
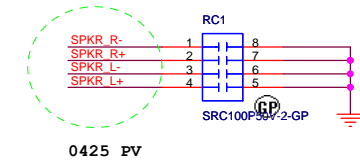
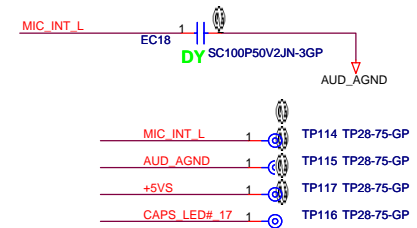
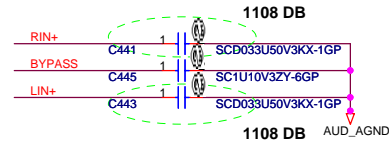
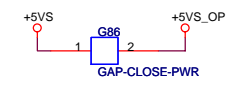
Title: **AUDIO CODEC CX20561-14Z**

Size: A3 Document Number: **VITAS** Rev: SA

Date: Monday, May 05, 2008 Sheet: 28 of 48



GAIN0	GAIN1	Av (dB)
0	0	6
0	1	10
1	0	15.6
1	1	21.6



<Core Design>

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO AMP/SPEAKER**

Size: A3 Document Number: **VITAS** Rev: SA

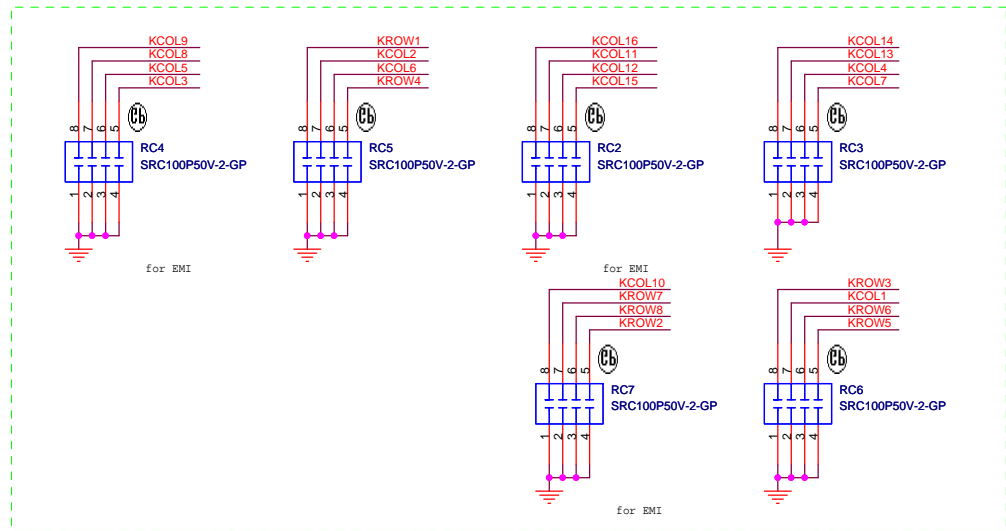
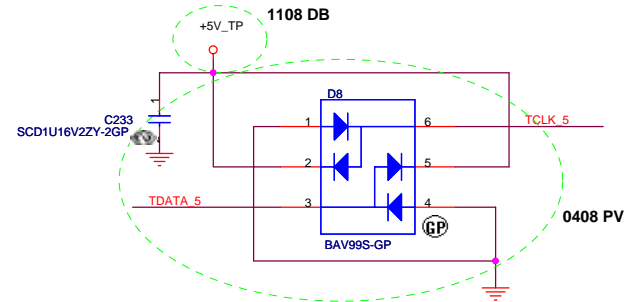
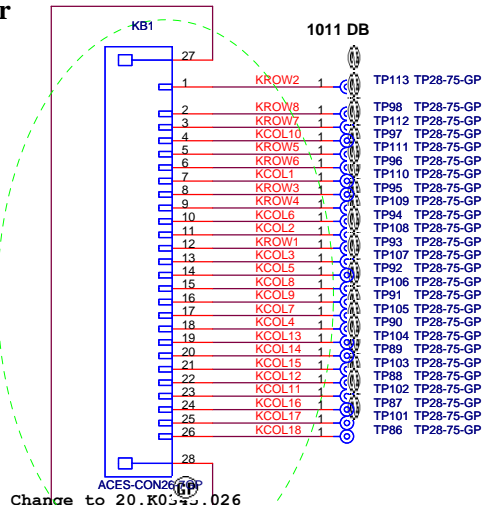
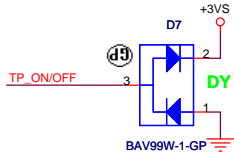
Date: Monday, May 05, 2008 Sheet: 29 of 48

Internal Keyboard Connector

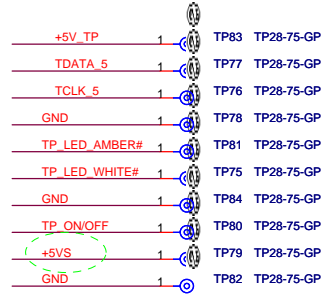
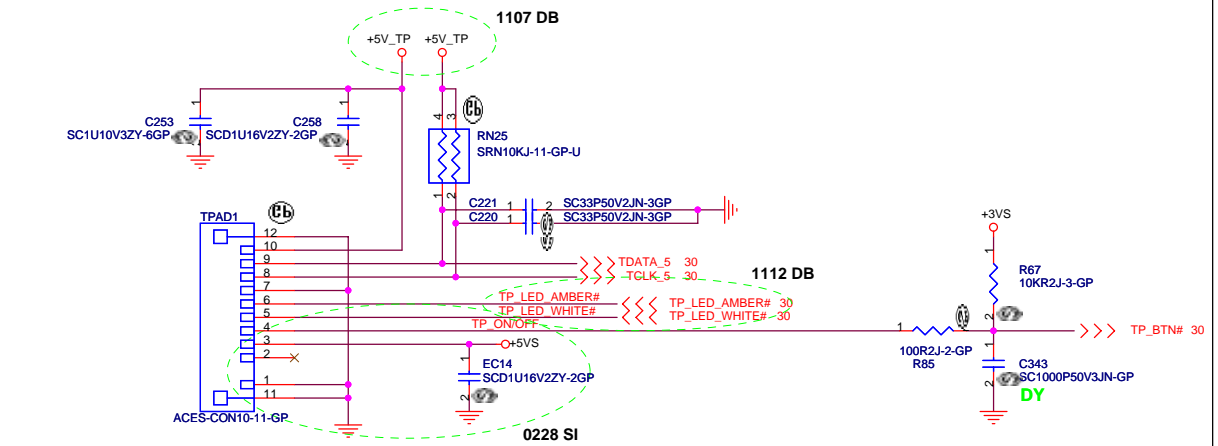
30 KROW[1..8] <<< 
 30 KCOL[1..18] <<< 

Keyboard matrix (from vendor)

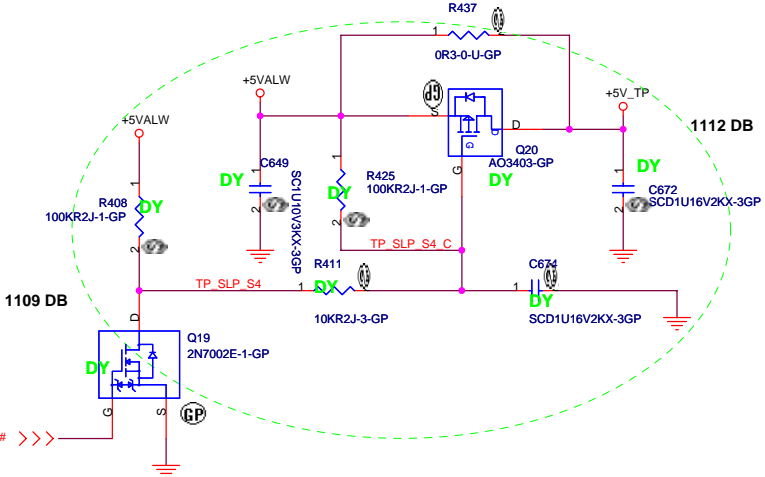
	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1



TouchPad Connector

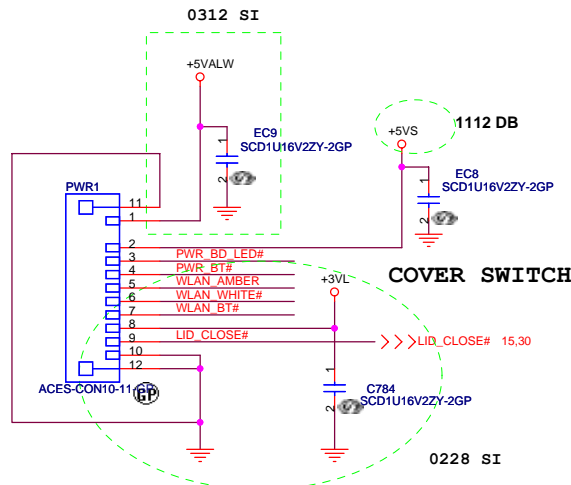
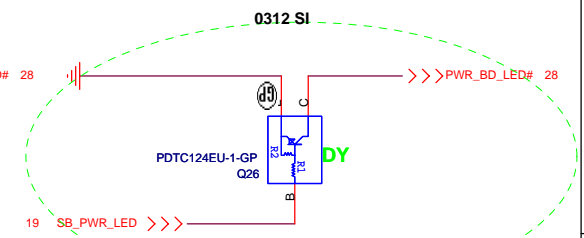
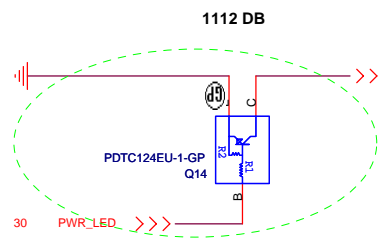
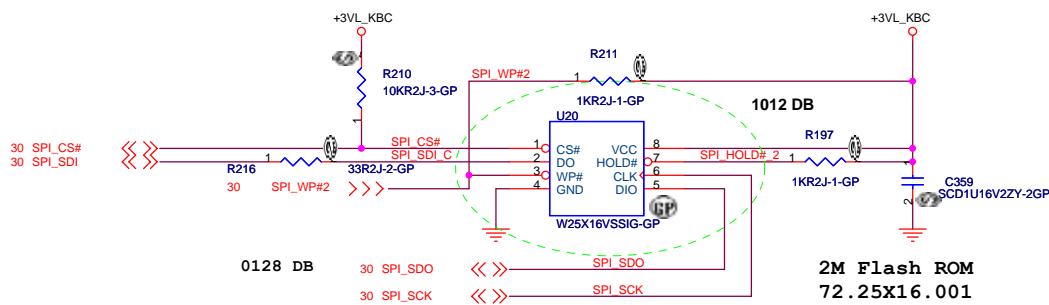


Please populate close TPAD1



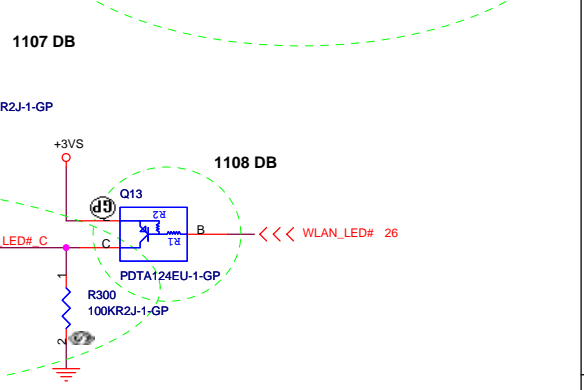
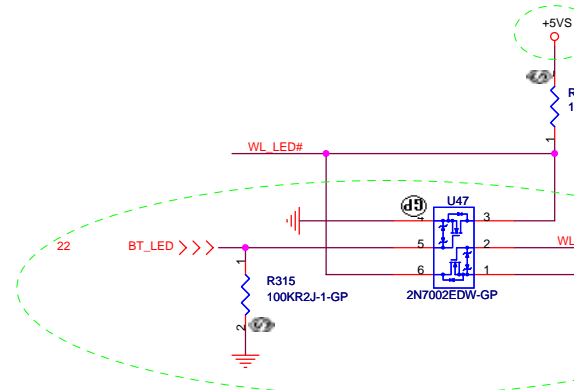
<Core Design>

緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
KeyBoard-CONN	
Title	Rev
Size A3	SA
Document Number	VITAS
Date: Monday, May 05, 2008	Sheet 31 of 48

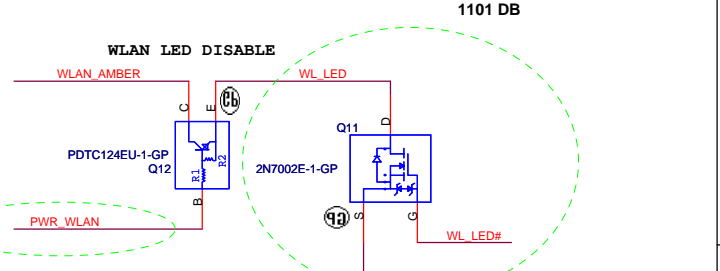
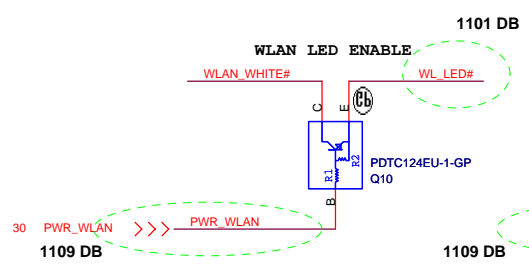
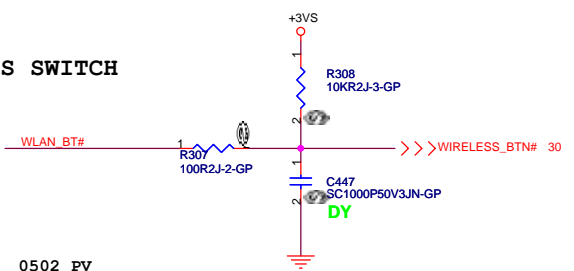


- +5VS 1 TP34 TP28-75-GP
- PWR_BD_LED# 1 TP39 TP28-75-GP
- PWR_BT# 1 TP46 TP28-75-GP
- WLAN_AMBER 1 TP38 TP28-75-GP
- WLAN_WHITE# 1 TP45 TP28-75-GP
- WLAN_BT# 1 TP37 TP28-75-GP
- LID_CLOSE# 1 TP44 TP28-75-GP
- GND 1 TP40 TP28-75-GP
- GND 1 TP41 TP28-75-GP
- +3VL 1 TP189 TP28-75-GP

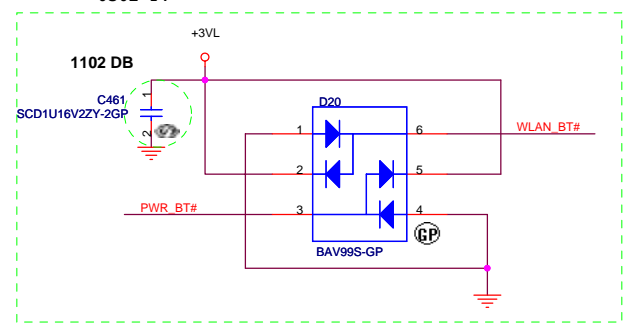
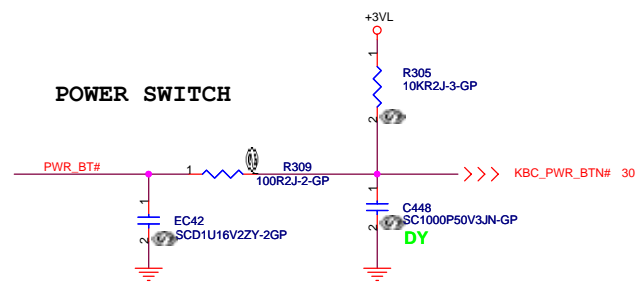
Please populate close PWR1



WIRELESS SWITCH



POWER SWITCH



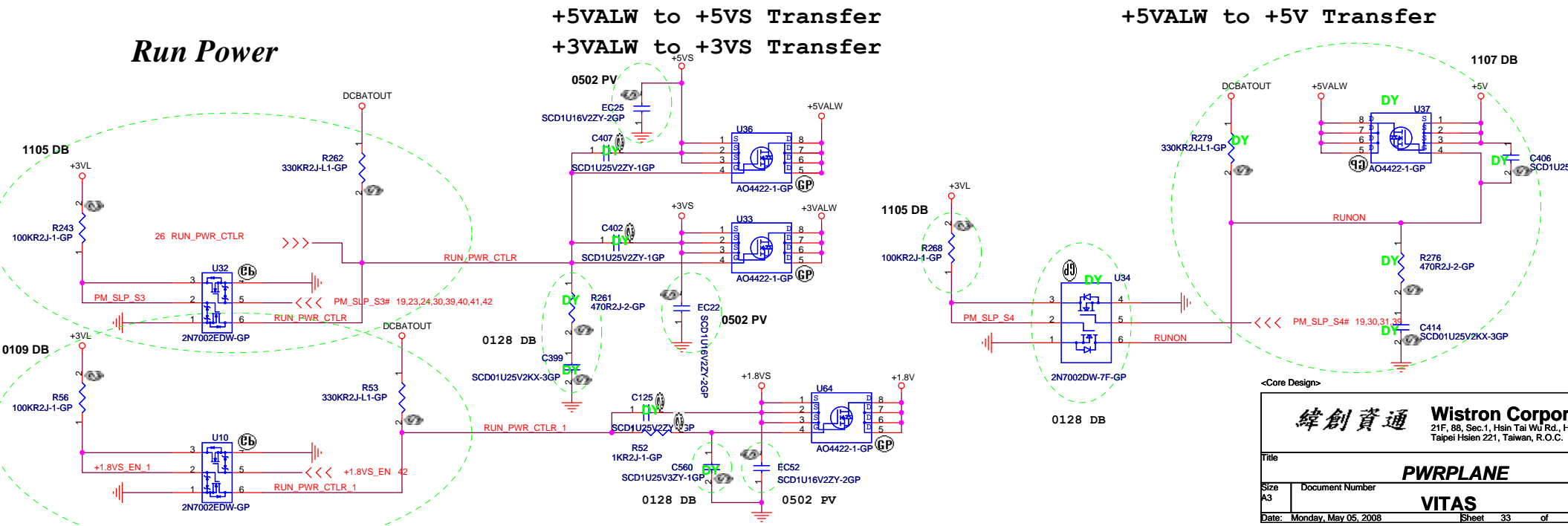
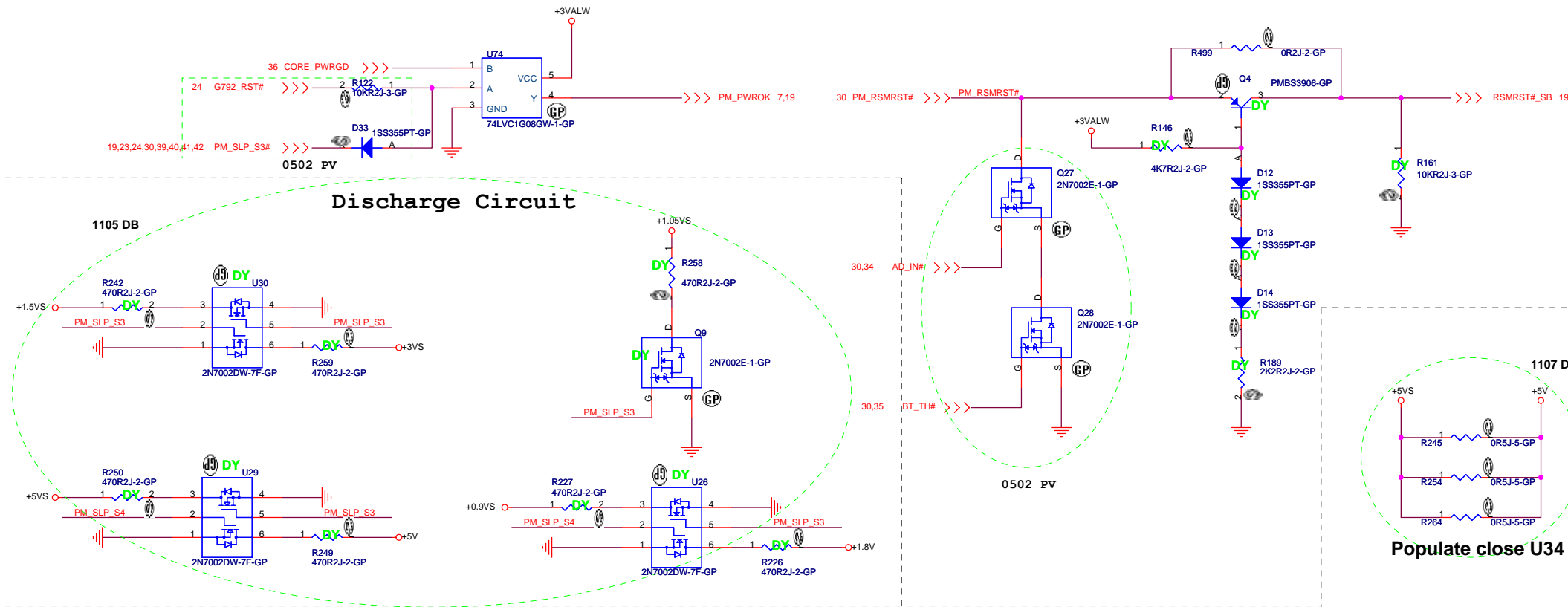
<Core Design>

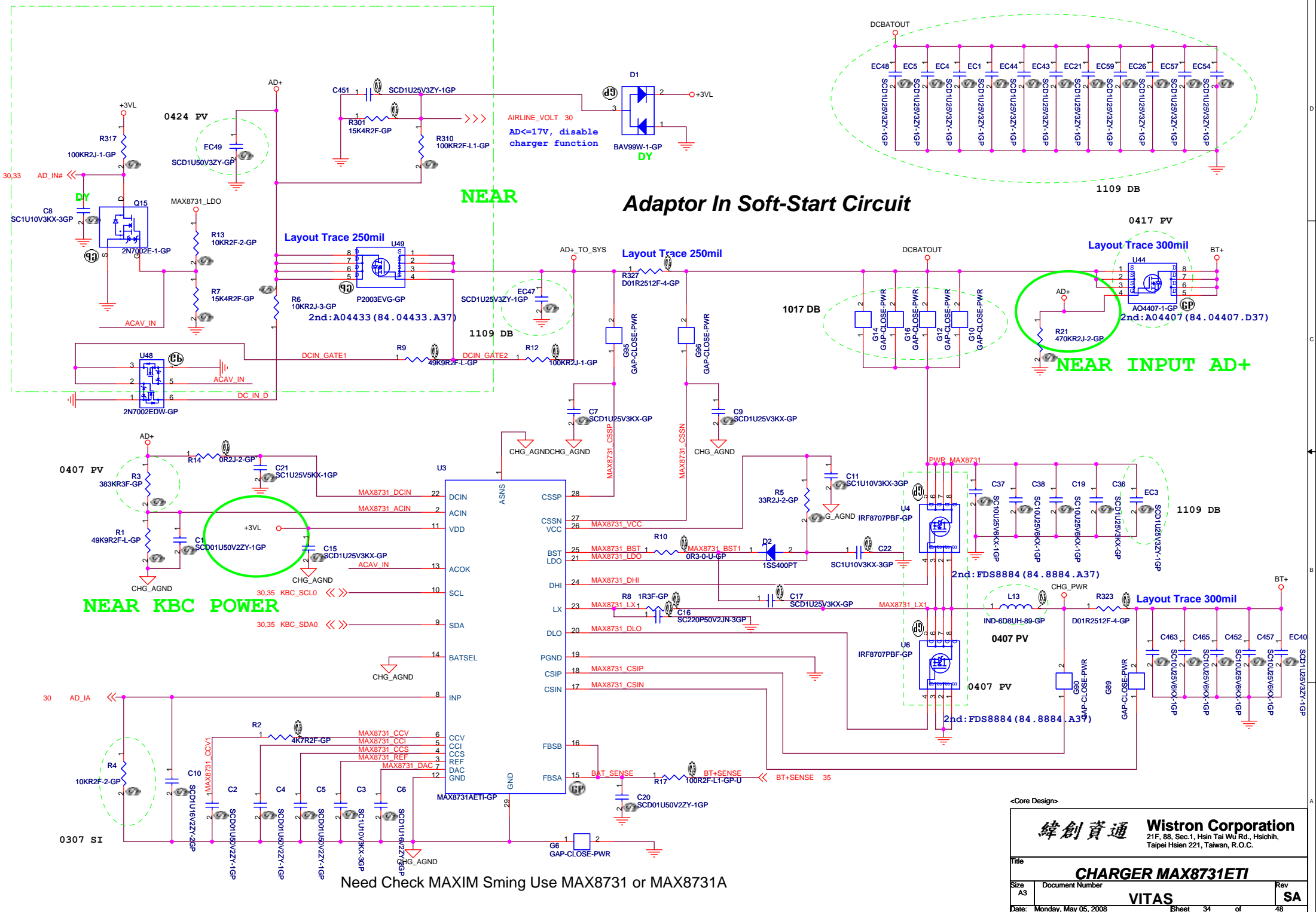
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **FWH and CONN.**

Size: A3 Document Number: **VITAS** Rev: SA

Date: Monday, May 05, 2008 Sheet: 32 of 48





Adaptor In Soft-Start Circuit

NEAR

NEAR KBC POWER

NEAR INPUT AD+

1109 DB

1109 DB

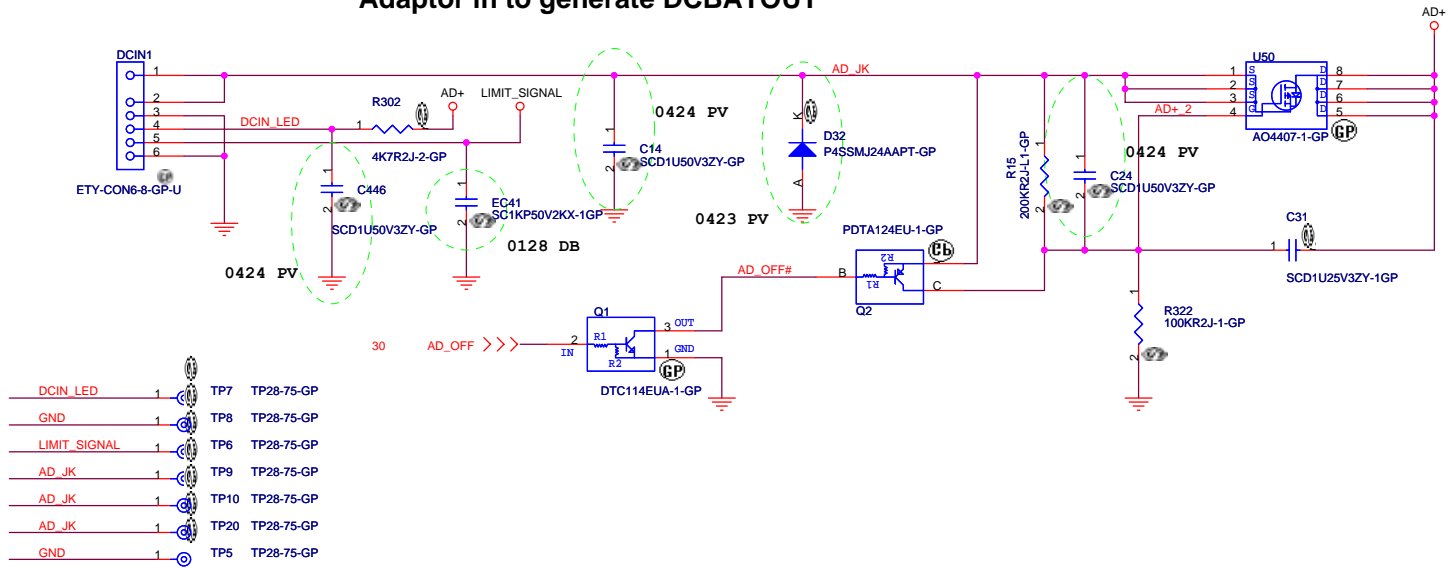
Need Check MAXIM Sming Use MAX8731 or MAX8731A

<Core Design>

緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

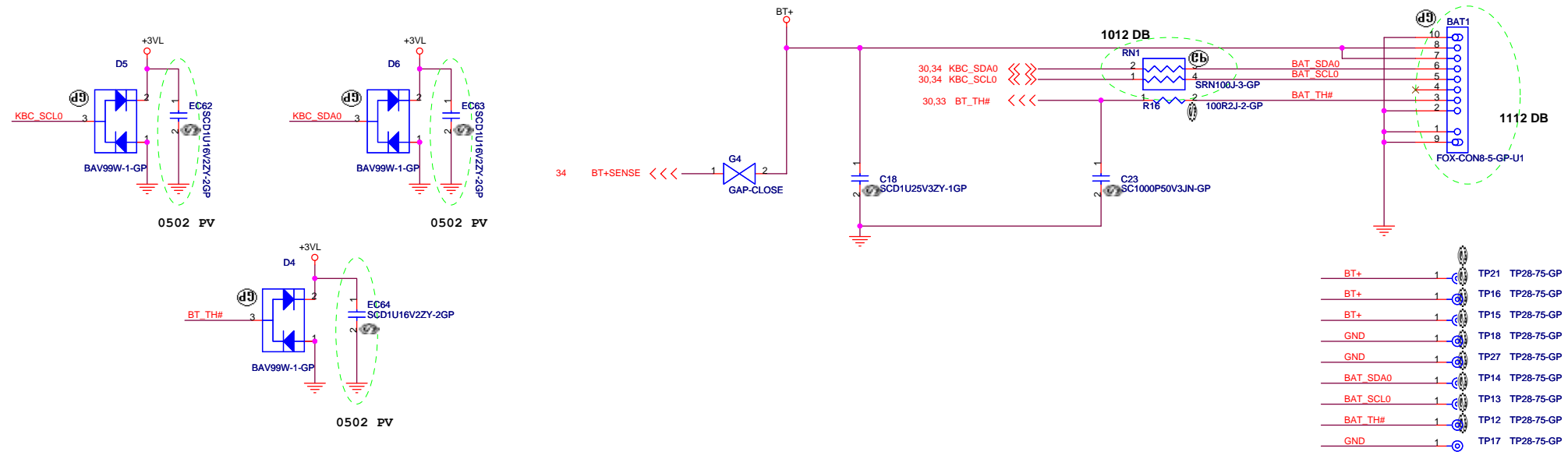
Title		CHARGER MAX8731ETI	
Size A3	Document Number	Rev SA	
Date: Monday, May 05, 2008	Sheet 34	of 48	

Adaptor in to generate DCBATOUT



DCIN_LED	1	TP7	TP28-75-GP
GND	1	TP8	TP28-75-GP
LIMIT_SIGNAL	1	TP6	TP28-75-GP
AD_JK	1	TP9	TP28-75-GP
AD_JK	1	TP10	TP28-75-GP
AD_JK	1	TP20	TP28-75-GP
GND	1	TP5	TP28-75-GP

BATTERY CONNECTOR



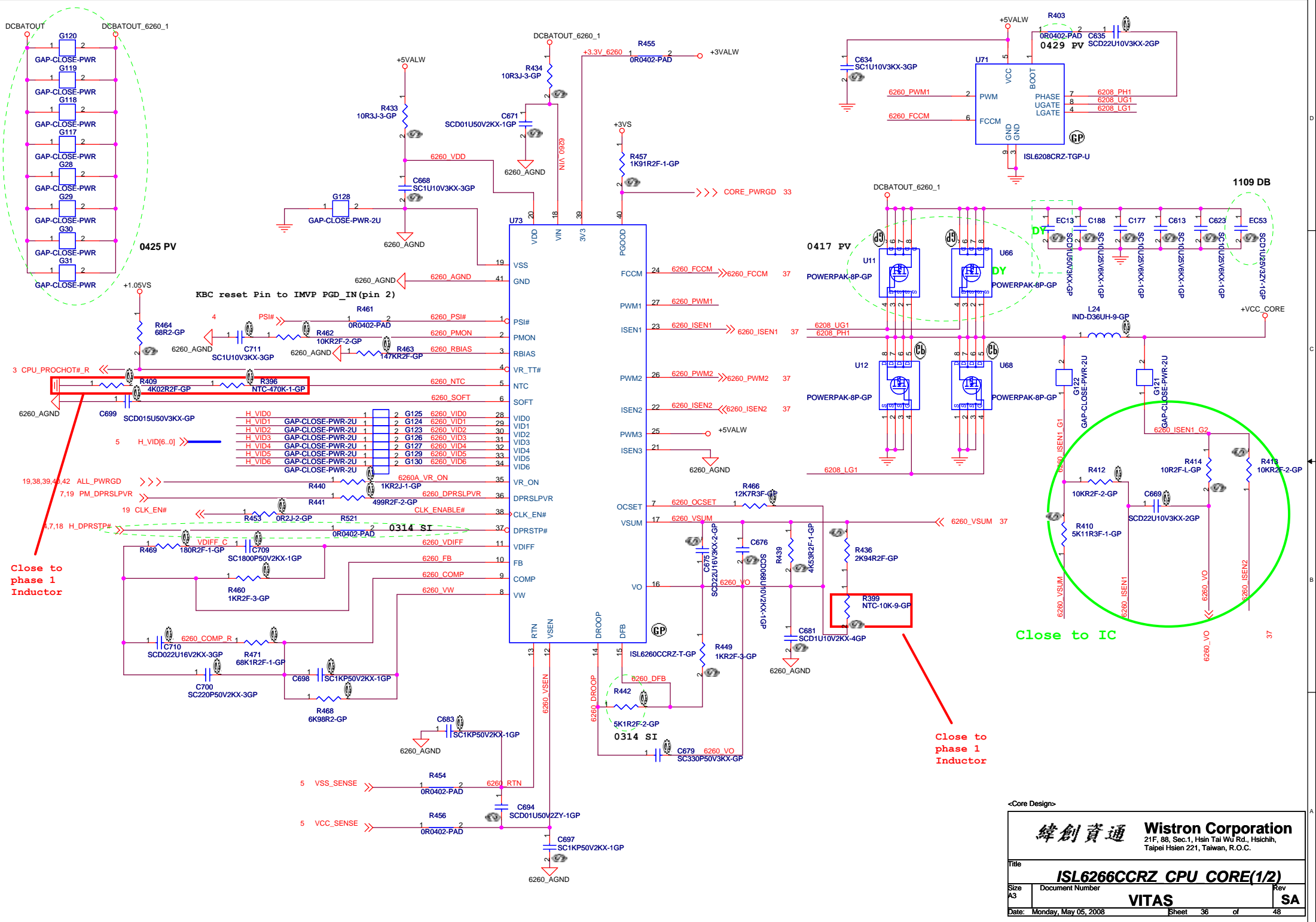
BT+	1	TP21	TP28-75-GP
BT+	1	TP16	TP28-75-GP
BT+	1	TP15	TP28-75-GP
GND	1	TP18	TP28-75-GP
GND	1	TP27	TP28-75-GP
BAT_SDA0	1	TP14	TP28-75-GP
BAT_SCL0	1	TP13	TP28-75-GP
BAT_TH#	1	TP12	TP28-75-GP
GND	1	TP17	TP28-75-GP

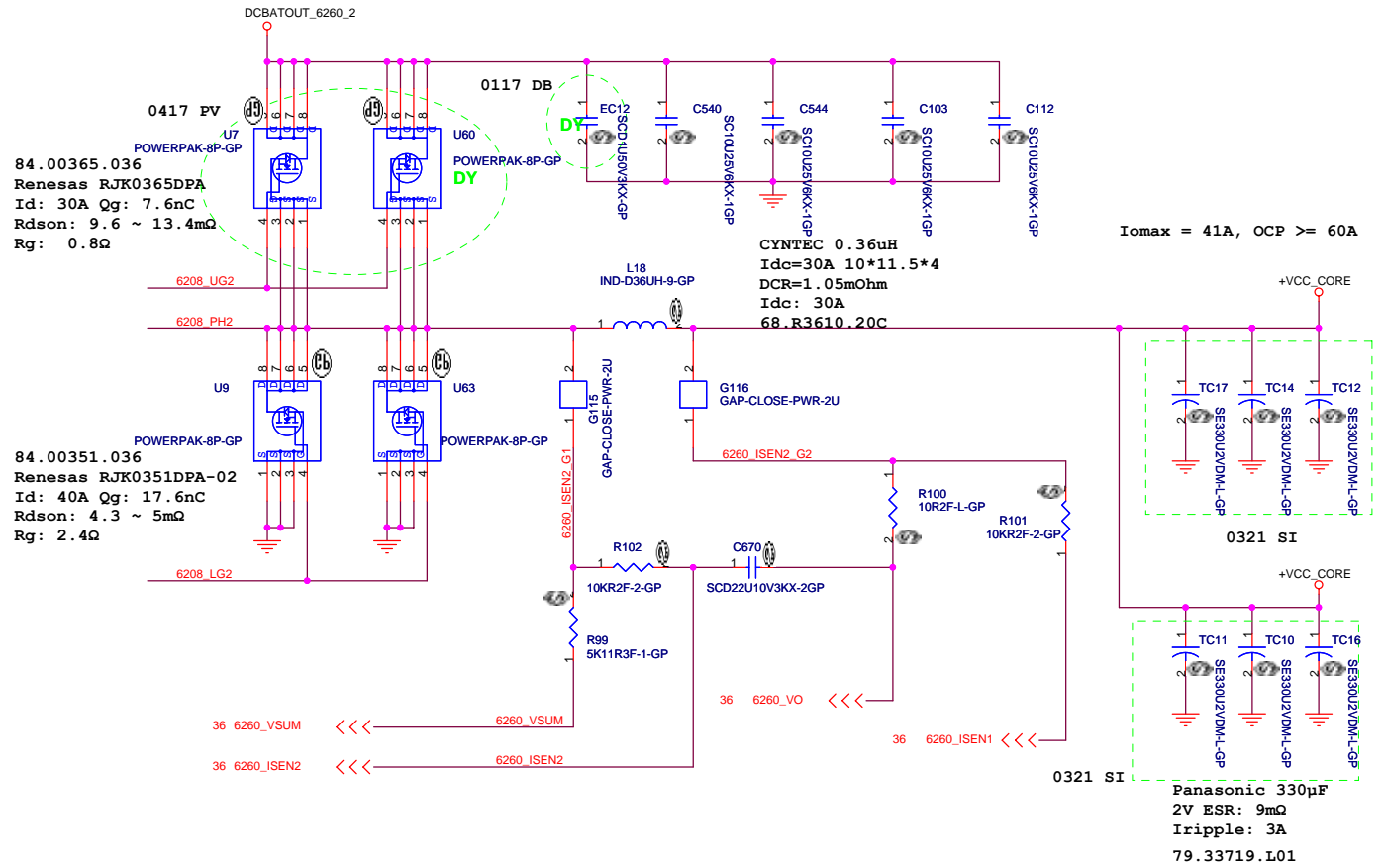
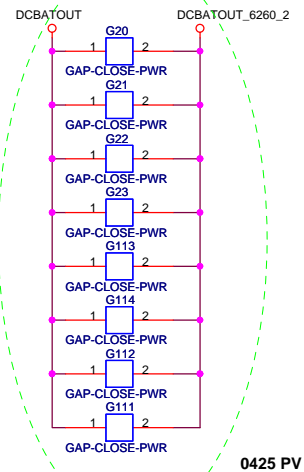
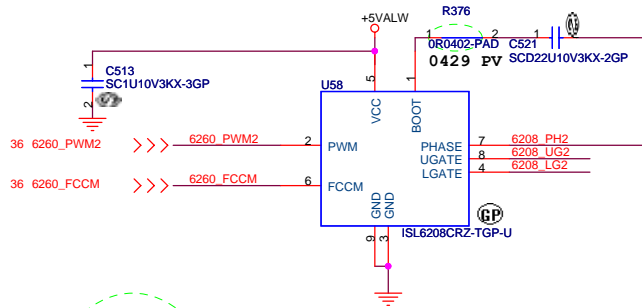
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

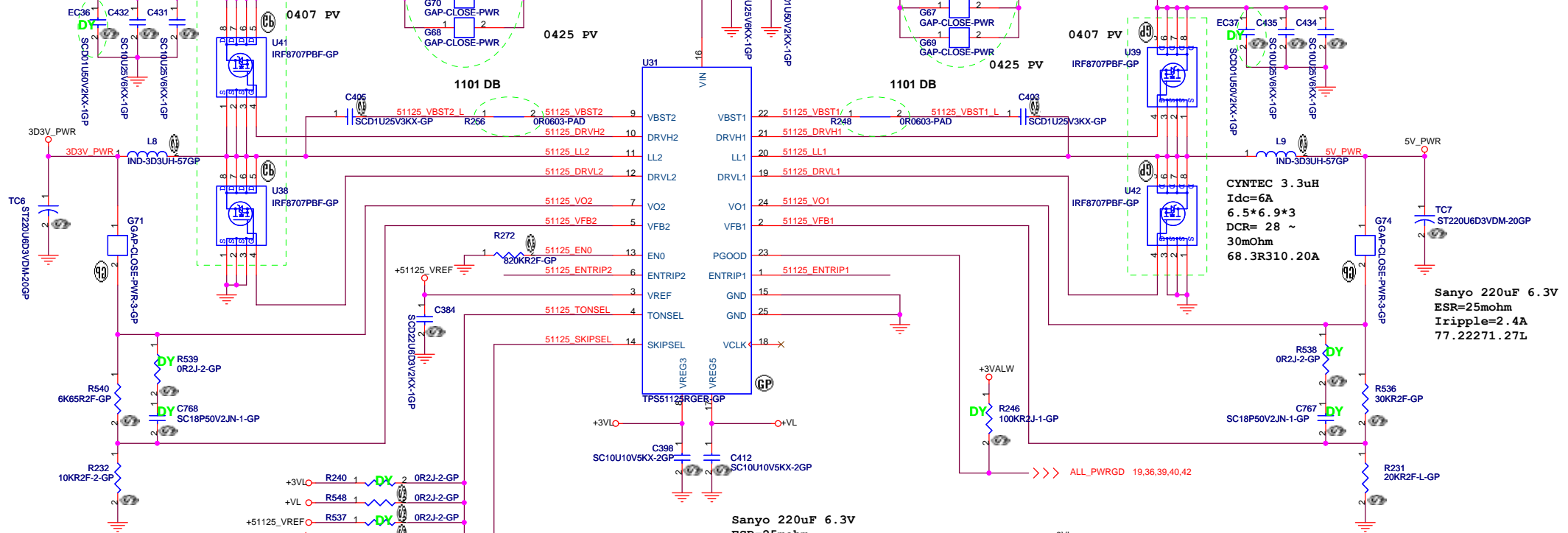
Title: **AD/BATT CONN**

Size: A3	Document Number: VITAS	Rev: SA
Date: Monday, May 05, 2008	Sheet 35 of 48	





SI4800, SO-8
 Id=9A, Qg=8.7~13nC
 Rds(on)=23~30mohm

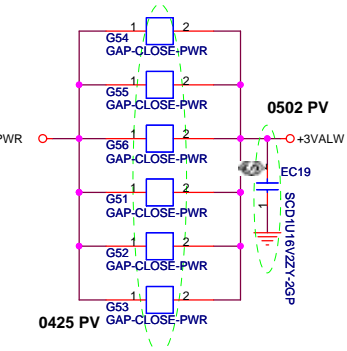


Close to IC TPS51125

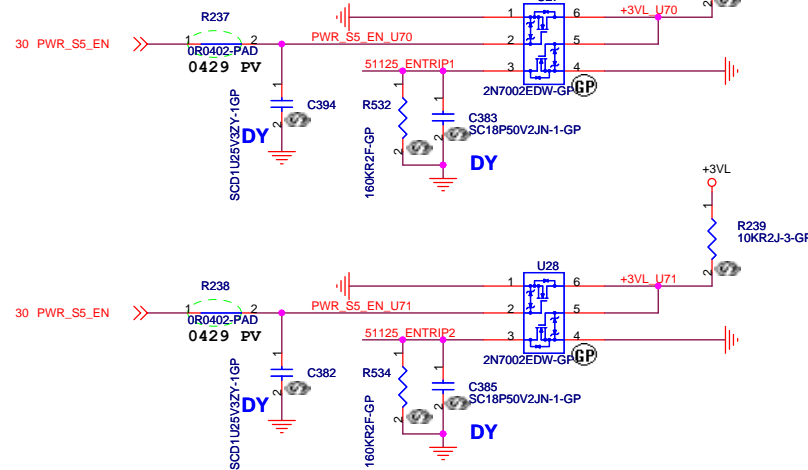
Design Current=1.2A
 OCP>2A

Sanyo 220uF 6.3V
 ESR=25mohm
 Irripple=2.4A
 77.22271.27L

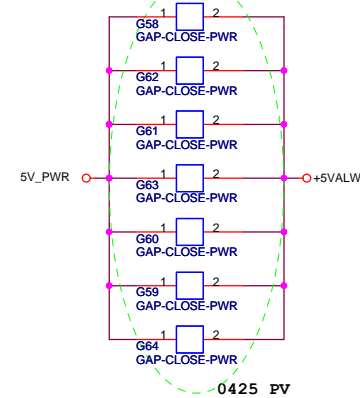
Design Current=4A
 OCP design>6A



0425 PV



0429 PV



0425 PV

	GND	VREF	VREG3	VREG5
SKIPSEL	PWM	AUTOSKIP	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

<Core Design>

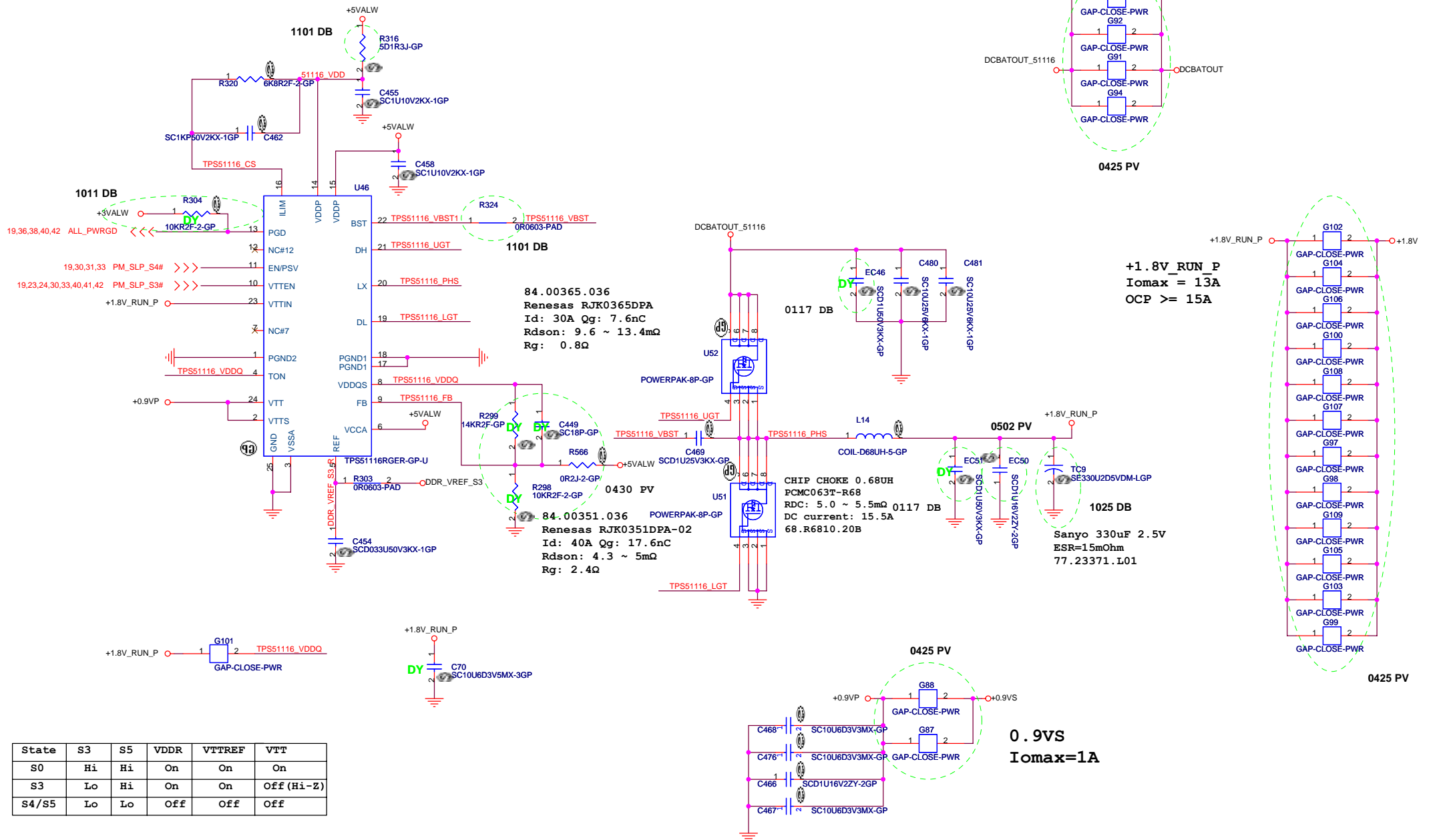
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPA51125 +5VALW +3VALW**

Size A3 Document Number **VITAS** Rev SA

Date: Monday, May 05, 2008 Sheet 38 of 48

TI TPS51116 for 1D8V and 0D9V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

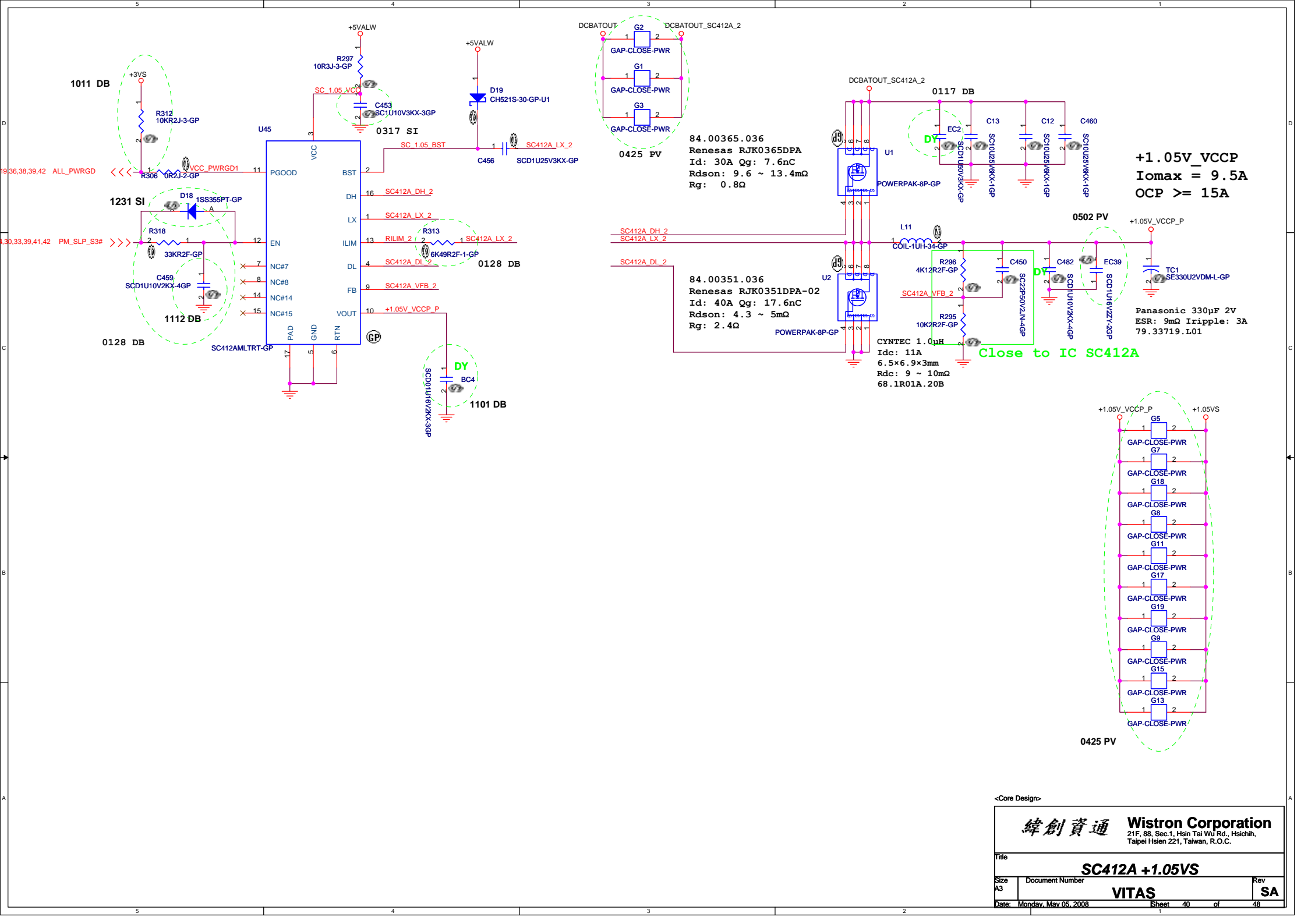
<Core Design>

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51116 1D8V/0D9V**

Size: A3 | Document Number: **VITAS** | Rev: SA

Date: Monday, May 05, 2008 | Sheet: 39 of 48



+1.05V_VCCP
I_{omax} = 9.5A
OCP >= 15A

84.00365.036
 Renesas RJK0365DPA
 Id: 30A Qg: 7.6nC
 Rdson: 9.6 ~ 13.4mΩ
 Rg: 0.8Ω

84.00351.036
 Renesas RJK0351DPA-02
 Id: 40A Qg: 17.6nC
 Rdson: 4.3 ~ 5mΩ
 Rg: 2.4Ω

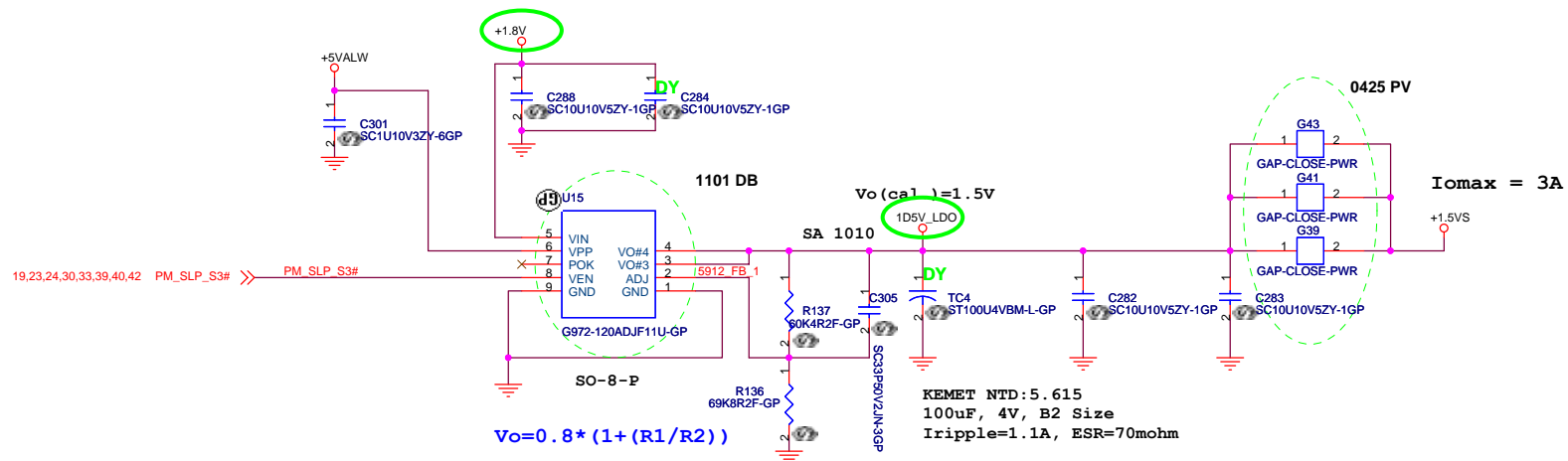
CYNTec 1.0μH
 Idc: 11A
 6.5×6.9×3mm
 Rdc: 9 ~ 10mΩ
 68.1R01A.20B

Close to IC SC412A


Panasonic 330pF 2V
 ESR: 9mΩ Ripple: 3A
 79.33719.L01

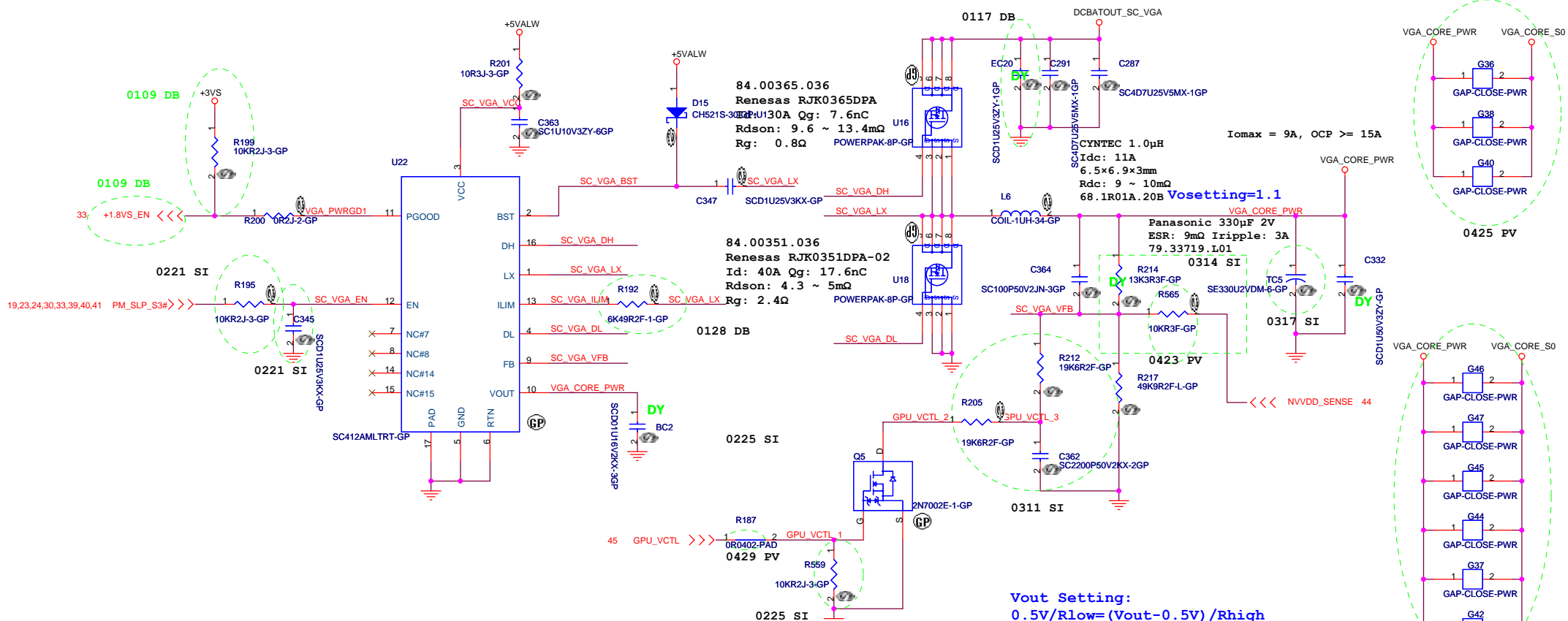
<Core Design>

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
SC412A +1.05VS	
Title	
Size A3	Document Number
Date: Monday, May 05, 2008	Sheet 40 of 48
VITAS	
SA	



<Core Design>

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
GMT 1D5V LDO		
Size A3	Document Number VITAS	Rev SA
Date: Monday, May 05, 2008		Sheet 41 of 48



84.00365.036
 Renesas RJK0365DPA
 Id: 130A Qg: 7.6nC
 Rds(on): 9.6 ~ 13.4mΩ
 Rg: 0.8Ω
 POWERPAK-8P-GP

84.00351.036
 Renesas RJK0351DPA-02
 Id: 40A Qg: 17.6nC
 Rds(on): 4.3 ~ 5mΩ
 Rg: 2.4Ω
 POWERPAK-8P-GP

Iomax = 9A, OCP >= 15A

Vosetting=1.1

Vout Setting:
 0.5V/Rlow=(Vout-0.5V)/Rhigh
 Low (0V) =>Vo=0.9V
 High (3.3V) =>Vo=1.09V

VID=0 0.95V
 VID=1 1.1V

1D1V_S0
 Iomax = 2.4A

Vout=0.8V*(1+R601/R596)

KEMET NTD:5.615
 100uF, 4V, B2 Size
 Irripple=1.1A, ESR=70mohm

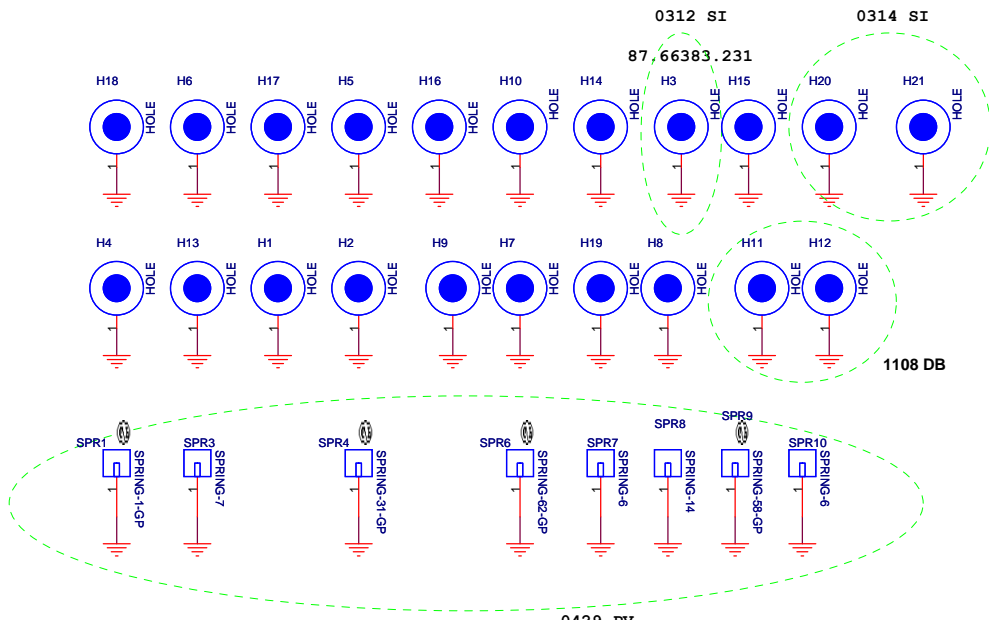
<Core Design>

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

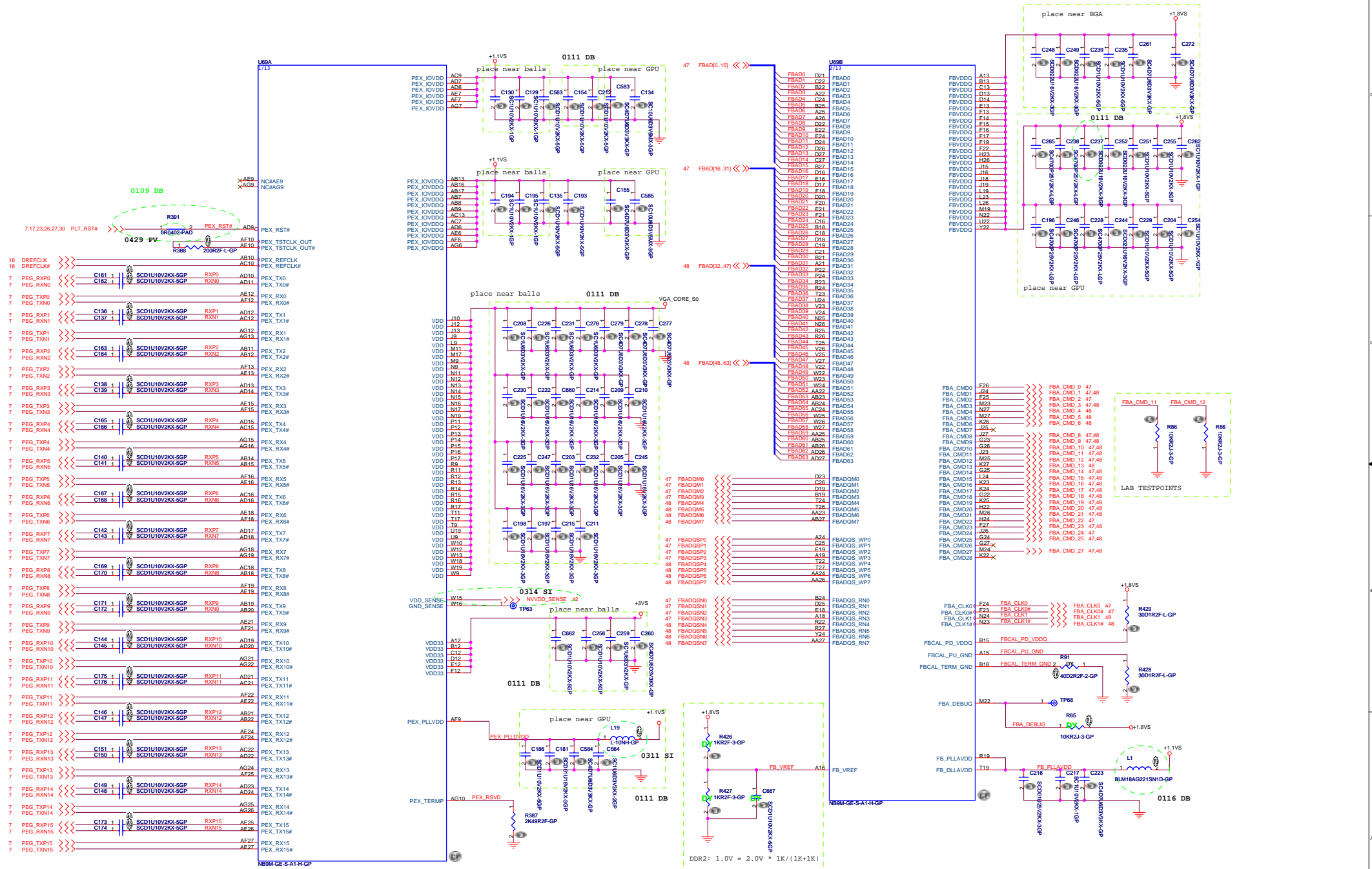
Title: **VGA CORE 1V**

Size A3 Document Number: **VITAS** Rev: **SA**

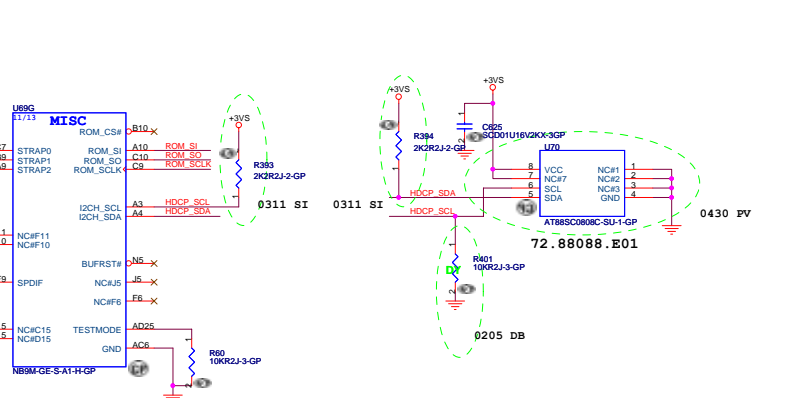
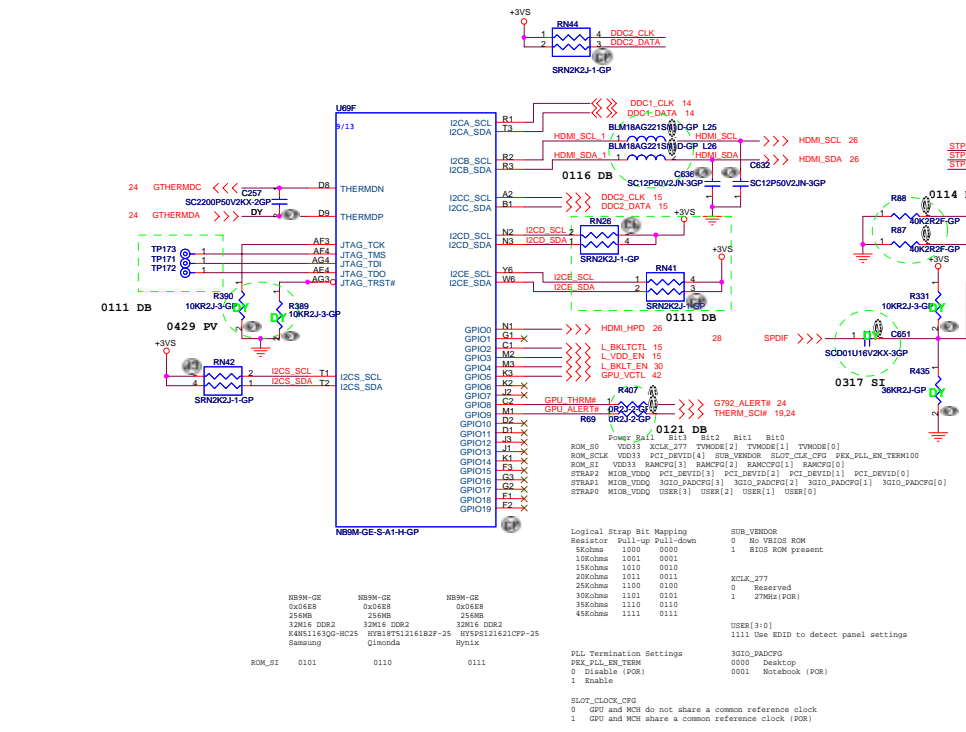
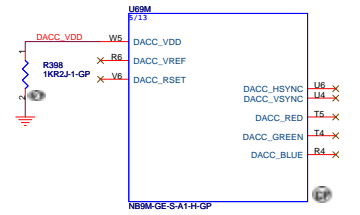
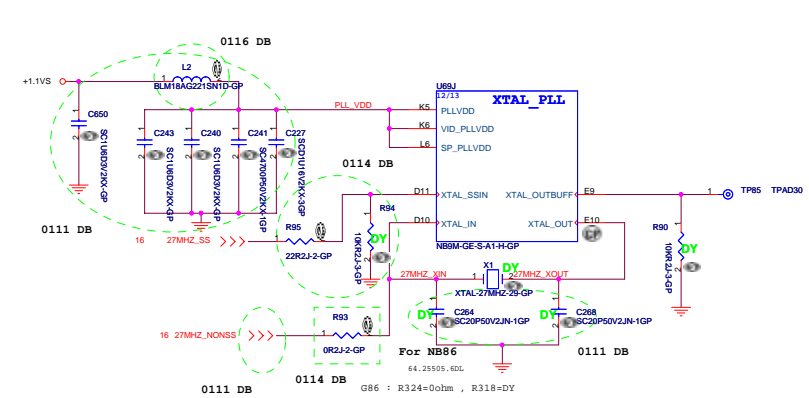
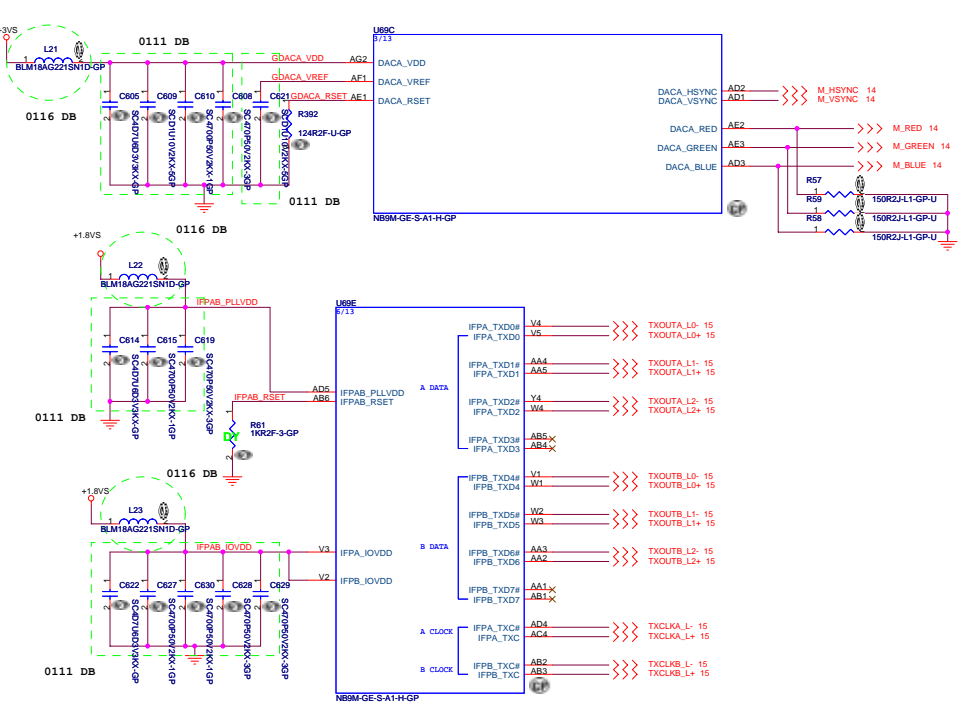
Date: Monday, May 05, 2008 Sheet 42 of 47



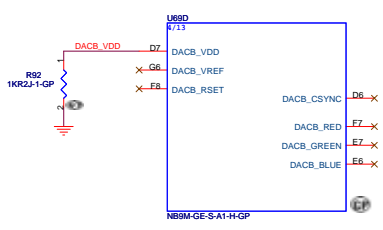
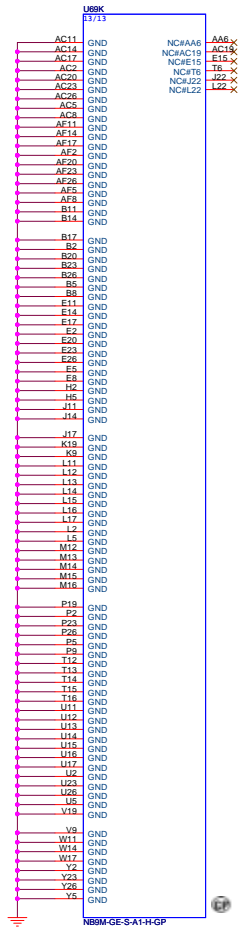
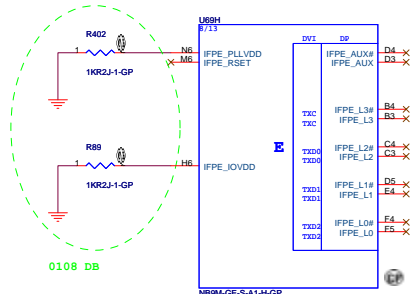
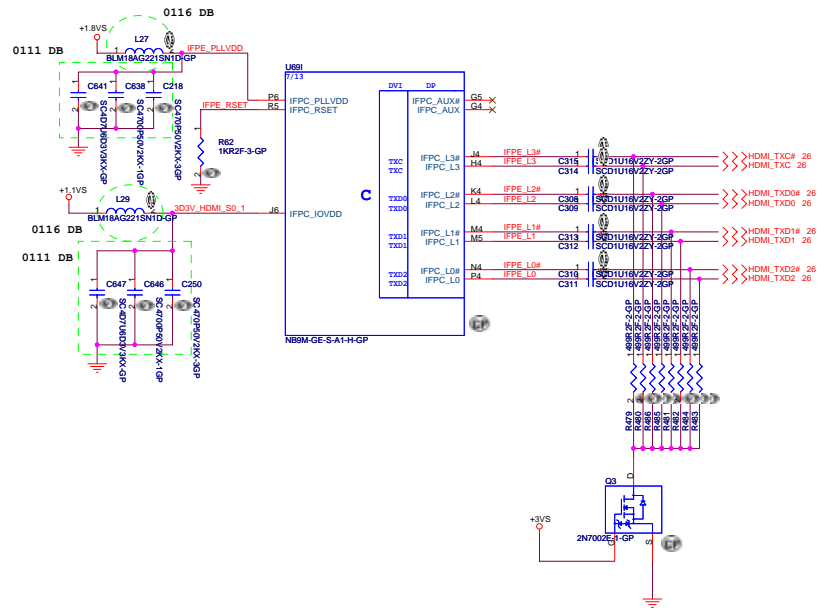
SPR1	34.40V16.001
SPR3	34.49U26.001
SPR4	34.49U24.001
SPR6	34.39S07.003
SPR7	34.13B01.001
SPR8	34.41V01.001
SPR9	34.4B312.002
SPR10	34.13B01.001

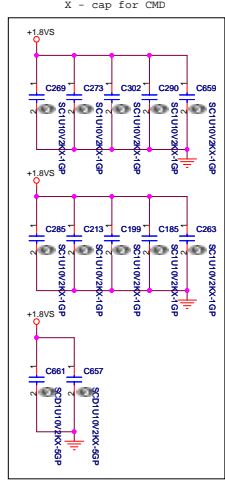
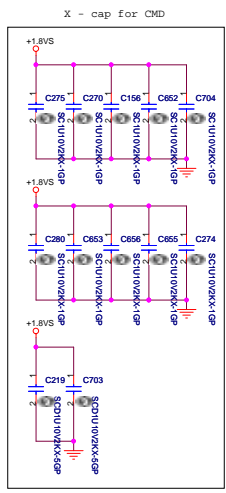
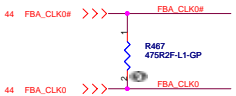
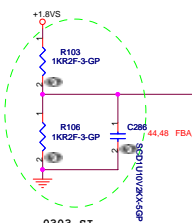
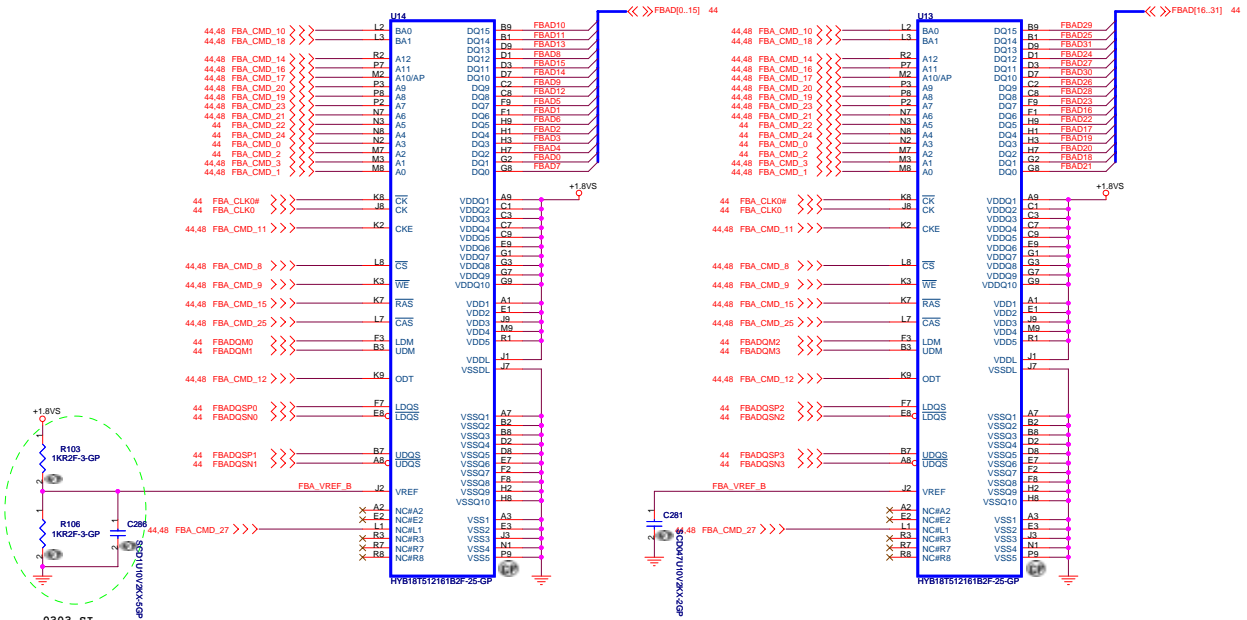


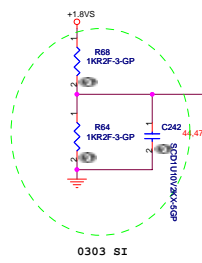
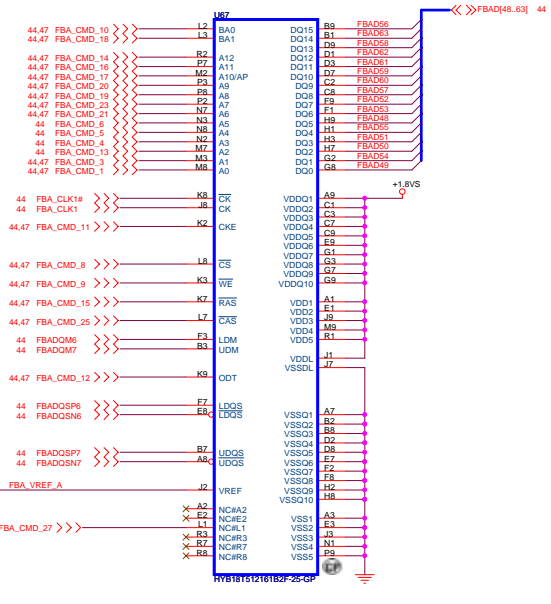
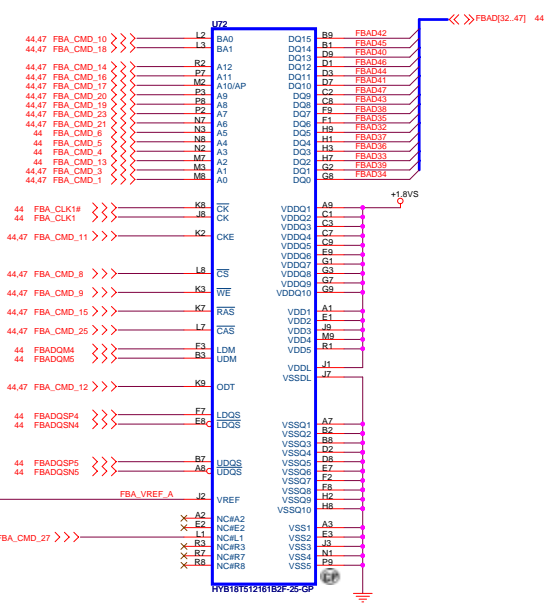
0314 SI



Power	S1	S2	S3	S4	Bit1	Bit0
ROM_SO	VD03	XCL#_277	TVMODE[2]	TVMODE[1]	TVMODE[0]	
ROM_SCLK	VD03	PCI_DEV[0]	SUR_VEN[0]	SLIC_CLK_CPG	PHI_PLL_EN_TERM10	
ROM_SI	VD03	RAMC[0]	RAMC[1]	RAMC[2]	RAMC[3]	
STRAP2	MIOB_VDDO	PCI_DEV[2]	PCI_DEV[1]	PCI_DEV[0]		
STRAP1	MIOB_VDDO	SGO_PADCP[1]	SGO_PADCP[2]	SGO_PADCP[3]	SGO_PADCP[0]	
STRAP0	MIOB_VDDO	USER[1]	USER[2]	USER[3]	USER[0]	

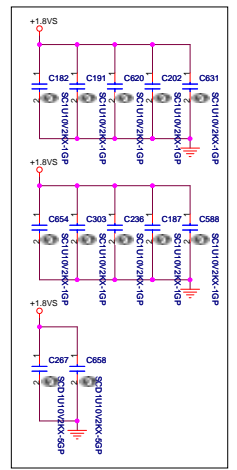
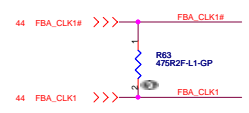






0303 SI

X - cap for CMD



X - cap for CMD

