MC100LVELT22

3.3V Dual LVTTL/LVCMOS to Differential LVPECL Translator

The MC100LVELT22 is a dual LVTTL/LVCMOS to differential LVPECL translator. Because LVPECL (Low Voltage Positive ECL) levels are used, only +3.3 V and ground are required. The small outline 8-lead package and the low skew, dual gate design of the LVELT22 makes it ideal for applications which require the translation of a clock and a data signal.

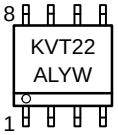
- 350 ps Typical Propagation Delay
- <100 ps Output−to−Output Skew
- Flow Through Pinouts
- The 100 Series Contains Temperature Compensation
- LVPECL Operating Range: V_{CC} = 3.0 V to 3.8 V with GND = 0 V
- When Unused TTL Input is left Open, Q Output will Default High

ON Semiconductor®

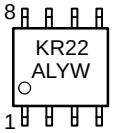
http://onsemi.com

MARKING DIAGRAMS*

SO−8
D SUFFIX
CASE 751



TSSOP−8
DT SUFFIX
CASE 948R



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional marking information, see Application Note AND8002/D.

ORDERING INFORMATION

Device	Package	Shipping**
MC100LVELT22D	SO−8	98 Units/Rail
MC100LVELT22DR2	SO−8	2500 Units/Reel
MC100LVELT22DT	TSSOP−8	98 Units/Rail
MC100LVELT22DTR2	TSSOP−8	2500 Units/Reel

**For additional tape and reel information, see Brochure BRD8011/D.

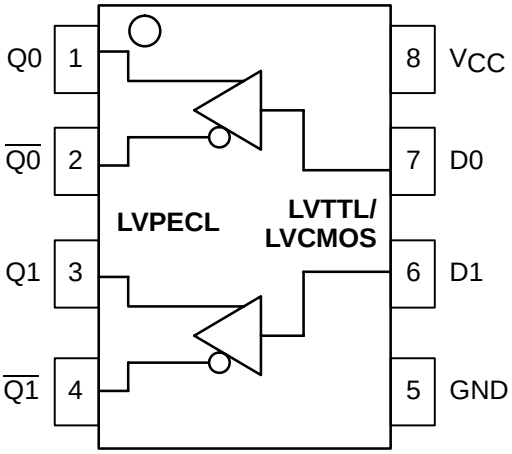


Figure 1. 8−Lead Pinout (Top View)
and Logic Diagram

PIN DESCRIPTION

PIN	FUNCTION
Qn, $\overline{Qn}$	LVPECL Differential Outputs
D0, D1	LVTTL/LVCMOS Inputs
V_{CC}	Positive Supply
GND	Ground

ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor		N/A
Internal Input Pullup Resistor		N/A
ESD Protection	Human Body Model Machine Model	> 4 kV > 200 V
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 6)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		164
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

6. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS (Note 7)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	Positive Power Supply	GND = 0 V		7	V
V_I	Input Voltage	GND = 0 V	$V_I \leq V_{CC}$	7	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 LFPM 500 LFPM	SO−8 SO−8	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	std bd	SO−8	41 to 44 ± 5%	°C/W
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 LFPM 500 LFPM	TSSOP−8 TSSOP−8	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	std bd	TSSOP−8	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

7. Maximum Ratings are those values beyond which device damage may occur.

LVPECL DC CHARACTERISTICS V_{CC} = 3.3 V; GND = 0.0 V (Note 8)

		−40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{CC}	Power Supply Current			28			28			29	mA
V_{OH}	Output HIGH Voltage (Note 9)	2275		2420	2275		2420	2275		2420	mV
V_{OL}	Output LOW Voltage (Note 9)	1490		1680	1490		1680	1490		1680	mV

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

8. Output parameters vary 1:1 with V_{CC}. V_{CC} can vary ±0.15 V.
9. Outputs are terminated through a 50 ohm resistor to V_{CC}−2 volts.

LVTTL/LVCMOS INPUT DC CHARACTERISTICS V_{CC} = 3.3 V; T_A = −40°C to 85°C (Note 10)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current			20	μA	V_{IN} = 2.7 V
I_{IHH}	Input HIGH Current			100	μA	$V_{IN} = V_{CC}$
I_{IL}	Input LOW Current			−0.2	mA	V_{IN} = 0.5 V
V_{IK}				−1.2	V	I_{IN} = −18 mA
V_{IH}	Input HIGH Voltage	2.0			V	
V_{IL}	Input LOW Voltage			0.8	V	

10. V_{CC} can vary ±0.15 V.

AC CHARACTERISTICS V_{CC} = 3.3 V; GND = 0.0 V (Note 11)

		−40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Toggle Frequency					350					MHz
t_{PLH}	Propagation Delay (Note 12)	200	350	600	200	350	600	200	350	600	ps
t_{skew}	Skew Output−to−Output Part−to−Part		30	100 400		30	100 400		30	100 400	ps
tJITTER	Random Clock Jitter (RMS)					1.6					ps
t_r/t_f	Output Rise/Fall Time (20−80%)	200		550	200		500	200		500	ps

11. V_{CC} can vary ±0.15 V.
12. Specifications for standard TTL input signal.

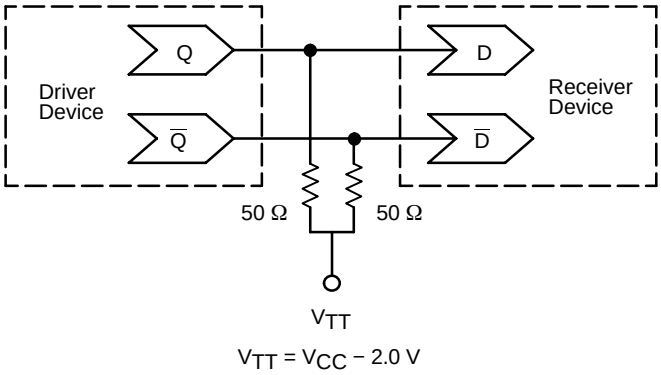


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 − Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	−	ECLinPS Circuit Performance at Non−Standard V_{IH} Levels
AN1405	−	ECL Clock Distribution Techniques
AN1406	−	Designing with PECL (ECL at +5.0 V)
AN1503	−	ECLinPS I/O SPICE Modeling Kit
AN1504	−	Metastability and the ECLinPS Family
AN1560	−	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	−	Interfacing Between LVDS and ECL
AN1596	−	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	−	Using Wire−OR Ties in ECLinPS Designs
AN1672	−	The ECL Translator Guide
AND8001	−	Odd Number Counters Design
AND8002	−	Marking and Date Codes
AND8020	−	Termination of ECL Logic Devices
AND8090	−	AC Characteristics of ECL Devices

MC100LVELT22: 3.3V Dual LVTTL/LVCMOS to Differential LVPECL Translator

Datasheet ( ) | Application Notes | Models | Product Change Notifications | Reliablility Data | Eval Board: Manual

Parametric Table

Orderable Part	Input	Output	V_{CC} Typ (V)	Channels	f_{Max} Typ (MHz)	t_{pd} Typ (ns)	t_R & t_F Max (ps)	Package
MC100LVELT22D	LVTTL/LVCMOS	LVPECL	3.3	2	2000+	0.35	500	SOIC 8
MC100LVELT22DR2	LVTTL/LVCMOS	LVPECL	3.3	2	2000+	0.35	500	SOIC 8

View all Low-Voltage ECLinPS Lite™
View all Translators

Orderable Devices

Product	Status	Package			MSL*	Container		Budgetary Price	Action
		Type	Pins	Case Outline		Type	Qty.		
MC100LVELT22DTG	Active	TSSOP 3.0x3.0x0.95 mm	8	948R-02	3	Rail	100	$2.53	
MC100LVELT22DR2	Active	SOIC Narrow	8	751-07	1	Tape and Reel	2500	$2.53	Order Samples Availability/Buy
MC100LVELT22D	Active	SOIC Narrow	8	751-07	1	Rail	98	$2.53	Order Samples Availability/Buy
MC100LVELT22DTRG	Active	TSSOP 3.0x3.0x0.95 mm	8	948R-02	3	Tape and Reel	2500	$2.53	

Symbol denotes 2nd Level Interconnect lead (Pb) free content. 2nd Level Interconnect refers to leads, balls or other electrical contact mechanisms of a part

Moisture Sensitivity level (MSL) for surface mount devices (lead free measured at 260°C reflow, non lead free at 235°C reflow)

Evaluation / Demonstration Boards

Evaluation Board	Parts used	Status	Budgetary Price/Unit	Action
ECLSOIC8EVB	MC100EL01 MC100EL04 MC100EL05 MC100EL07 MC100EL11 MC100EL12 MC100EL16 MC100EL31 MC100EL32 MC100EL33 MC100EL35 MC100EL51 MC100EL52 MC100EL58 MC100ELT20 MC100ELT21 MC100ELT22 MC100ELT23 MC100ELT28 MC100EP01 MC100EP05 MC100EP08 MC100EP11 MC100EP16 MC100EP16F MC100EP16T MC100EP16VA MC100EP16VB MC100EP16VC MC100EP16VS MC100EP16VT MC100EP31 MC100EP32 MC100EP33 MC100EP35 MC100EP51 MC100EP52 MC100EP58 MC100EPT20 MC100EPT21 MC100EPT22 MC100EPT23 MC100EPT26 MC100LVEL05 MC100LVEL11 MC100LVEL12 MC100LVEL16	Active	$49.33	Contact local sales office

	MC100LVEL31 MC100LVEL32 MC100LVEL33 MC100LVEL51 MC100LVEL58 MC100LVELT22 MC100LVELT23 MC100LVEP11 MC100LVEP16 MC10EL01 MC10EL04 MC10EL05 MC10EL07 MC10EL11 MC10EL12 MC10EL16 MC10EL31 MC10EL32 MC10EL33 MC10EL35 MC10EL51 MC10EL52 MC10EL58 MC10EL89 MC10ELT20 MC10ELT21 MC10ELT22 MC10ELT28 MC10EP01 MC10EP05 MC10EP08 MC10EP11 MC10EP16 MC10EP16T MC10EP16VA MC10EP31 MC10EP32 MC10EP33 MC10EP35 MC10EP51 MC10EP52 MC10EP58 MC10EPT20 MC10LVEP11 MC10LVEP16 NB6L11 NB6L16			

Features

- 350ps Typical Propagation Delay
- <100ps Output-to-Output Skew
- ESD Protection: >4 KV HBM, >200 V MM
- Flow Through Pinouts
- The 100 Series Contains Temperature Compensation
- LVPECL Operating Range: V_{CC}= 3.0 V to 3.8 V with GND= 0 V
- When Unused TTL Input is left Open, Q Output will Default High
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL-94 code V-0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 164 devices

The MC100LVELT22 is a dual LVTTL/LVCMOS to differential LVPECL translator. Because LVPECL (Low Voltage Positive ECL) levels are used, only +3.3V and ground are required. The small outline 8-lead SOIC package and the low skew, dual gate design of the LVELT22 makes it ideal for applications which require the translation of a clock and a data signal.

Data Sheet

Type	Document Title	Document ID/Size	Rev
Data Sheet	3.3V Dual LVTTL/LVCMOS to Differential LVPECL Translator	MC100LVELT22/D - 54.0 KB	1

Application Notes

Type	Document Title	Document ID/Size	Rev
Application Notes	Designing with PECL (ECL at +5.0V)	AN1406/D - 105.0 KB	2
Application Notes	The ECL Translator Guide	AN1672/D - 51.0 KB	9
Application Notes	Interfacing with ECLinPS	AND8066/D - 58.0 KB	2
Application Notes	Odd Number Divide By Counters with 50% Outputs and Synchronous Clocks	AND8001/D - 90.0 KB	0
Application Notes	AC Characteristics of ECL Devices	AND8090/D - 896.0 KB	1
Application Notes	Termination of ECL Logic Devices	AND8020/D - 157.0 KB	5
Application Notes	ECLinPS, ECLinPS Lite, ECLinPS Plus, ECLinPS MAX, and GigaComm Marking and Ordering Information Guide	AND8002/D - 137.0 KB	5

Application Notes	ECL Clock Distribution Techniques	AN1405/D - 54.0 KB	1

Models

Type	Document Title	Document ID/Size	Rev
Models	Low Voltage ECLinPS SPICE Modeling Kit	AN1560/D - 88.0 KB	5
Models	IBIS Model for MC100LVELT22D	MC100LVELT22D.IBS - 8.0 KB	3
Models	ECLinPS Lite MC100LVELT22 SPICE Model Kit	AND8010/D - 23.0 KB	1

Eval Board: Manual

Type	Document Title	Document ID/Size	Rev
Eval Board: Manual	Evaluation Board Manual for High Frequency SOIC 8 lead	ECLSOIC8EVB - 201.0 KB	1

Catalog

High Performance Logic > Low-Voltage ECLinPS Lite™
High Performance Logic > Translators