

Advance Information
Power Field Effect Transistor
N-Channel Enhancement Mode Silicon Gate TMOS

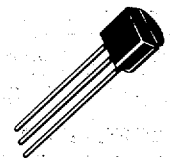
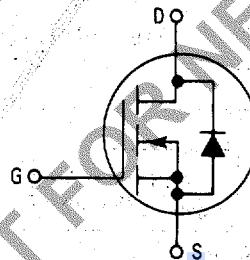
2N7000



**N-CHANNEL
 TMOS POWER FET**
 $r_{DS(on)} = 5 \text{ OHMS}$
60 VOLTS

... are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Logic Level Switch
- CMOS Logic Interface
- Bipolar Darlington Replacement
- Lamp Relay Driver or Buffer
- Analog Signal Switching



**CASE 29-02
 (TO-226AA)**

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	Vdc
Drain-Gate Voltage ($R_{GS} = 1 \text{ m}\Omega$)	V_{DGR}	60	Vdc
Gate-Source Voltage	V_{GS}	± 40	Vdc
Drain Current Continuous	I_D	200	mAdc
Pulsed	I_{DM}	500	
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	400 3.2	mW mW/ $^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Ambient	$R_{\theta JA}$	312,5	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes, 1/16" from case for 10 seconds	T_L	300	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Drain-Source Breakdown Voltage ($V_{GS} = 0, I_D = 10 \mu\text{A}$)	$V_{(BR)DSS}$	60	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 48 \text{ V}, V_{GS} = 0$) ($V_{DS} = 48 \text{ V}, V_{GS} = 0, T_J = 125^\circ\text{C}$)	I_{DSS}	—	1 1	μAdc mA
Gate-Body Leakage Current, Forward ($V_{GSF} = 15 \text{ Vdc}, V_{DS} = 0$)	I_{GSSF}	—	10	nAdc

(continued)

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ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
ON CHARACTERISTICS*				
Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 1 \text{ mA}$)	$V_{GS(th)}$	0.8	3	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10 \text{ Vdc}, I_D = 0.5 \text{ Adc}$) ($V_{GS} = 10 \text{ Vdc}, I_D = 0.5 \text{ V}, T_C = 125^\circ\text{C}$)	$r_{DS(on)}$	—	5 9	Ohm
Drain-Source On-Voltage ($V_{GS} = 10 \text{ V}, I_D = 0.5 \text{ Adc}$) ($V_{GS} = 4.5 \text{ V}, I_D = 75 \text{ mA}$)	$V_{DS(on)}$	—	2.5 0.4	Vdc
On-State Drain Current ($V_{GS} = 4.5 \text{ V}, V_{DS} = 10 \text{ V}$)	$I_{d(on)}$	75	—	mA
Forward Transconductance ($V_{DS} = 10 \text{ V}, I_D = 200 \text{ mA}$)	g_{fs}	100	—	μmhos

DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz})$	C_{iss}	—	60	pF
Output Capacitance		C_{oss}	—	25	
Reverse Transfer Capacitance		C_{rss}	—	5	

SWITCHING CHARACTERISTICS*

Turn-On Delay Time	$(V_{DD} = 15 \text{ V}, I_D = 600 \text{ mA}, R_{gen} = 25 \text{ ohms}, R_L = 25 \text{ ohms})$	t_{on}	—	10	ns
Turn-Off Delay Time		t_{off}	—	10	

*Pulse Test Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.

OUTLINE DIMENSIONS

NOTES:

1. CONTOUR OF PACKAGE BEYOND ZONE "P" IS UNCONTROLLED.
2. DIM "F" APPLIES BETWEEN "H" AND "L". DIM "D" & "S" APPLIES BETWEEN "L" & 12.70 mm (0.5") FROM SEATING PLANE. LEAD DIM IS UNCONTROLLED IN "H" & BEYOND 12.70 mm (0.5") FROM SEATING PLANE.

STYLE 7:
 PIN 1. SOURCE
 PIN 2. DRAIN
 PIN 3. GATE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	—	2.54	—	0.100
J	2.41	2.67	0.095	0.105
K	12.70	—	0.500	—
L	6.35	—	0.250	—
N	2.03	2.67	0.080	0.105
P	2.92	—	0.115	—
R	3.43	—	0.135	—
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply

CASE 29-02 (TO-226AA)

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