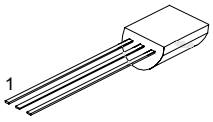
UTC BC327/328 PNP EPITAXIAL SILICON TRANSISTOR

SWITCHING AND AMPLIFIER APPLICATIONS

FEATURES

*Suitable for AF-Driver stages and low power output stages
*Complement to BC337/338



TO-92

1: COLLECTOR 2: BASE 3: EMITTER

ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATING	UNIT
Collector-emitter voltage	V_{CES}		
: BC327		-50	V
: BC328		-30	V
Collector-emitter voltage	V_{CEO}		
: BC327		-45	V
: BC328		-25	V
Emitter-base voltage	V_{EBO}	-5	V
Collector current (DC)	Ic	-800	mA
Collector dissipation	Pc	625	mW
Junction Temperature	T_j	150	°C
Storage Temperature	T_{STG}	-55 ~ +150	°C

ELECTRICAL CHARACTERISTICS (Ta=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Collector-emitter breakdown voltage	BV_{CEO}	I_C=-10mA, I_B=0				
: BC327			-45			V
: BC328			-25			V
Collector-emitter breakdown voltage	BV_{CES}	I_C=-0.1mA, V_{BE}=0				
: BC327			-50			V
: BC328			-30			V
Emitter-base breakdown voltage	BV_{EBO}	I_E=-10mA, I_C=0	-5			V
Collector Cut-off Current	I_{CES}					
: BC327		V_{CE}=-45V, I_B=0		-2	-100	nA
: BC328		V_{CE}=-25V, I_B=0		-2	-100	nA
DC current gain	h_{FE1}	V_{CE}=-1V, I_C=-100mA	100		630	
	h_{FE2}	V_{CE}=-1V, I_C=-300mA	40			
Collector-emitter saturation voltage	V_{CE}(sat)	I_C=-500mA, I_B=-50mA			-0.7	V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Base-emitter on voltage	V_{BE}(on)	V_{CE}=-1V, Ic=-300mA			-1.2	V
Current gain bandwidth product	f_T	V_{CE}=-5V, Ic=-10mA, f=20MHz		100		MHz
Output Capacitance	Cob	V_{CB}=-10V, I_E=0, f=1MHz		12		pF

CLASSIFICATION OF h_{FE}

RANK	16	25	40
h_{FE1}	100-250	160-400	250-630
h_{FE2}	60~	100~	170~

TYPICAL CHARACTERISTICS

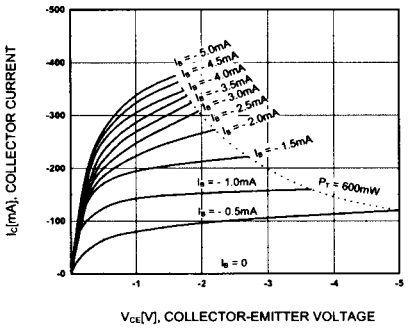


Figure 1. Static Characteristic

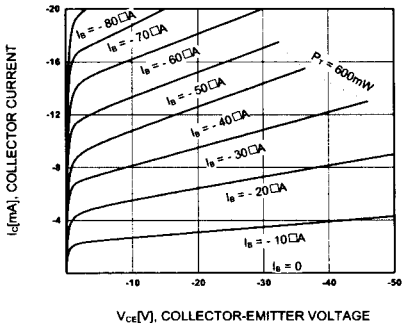


Figure 2. Static Characteristic

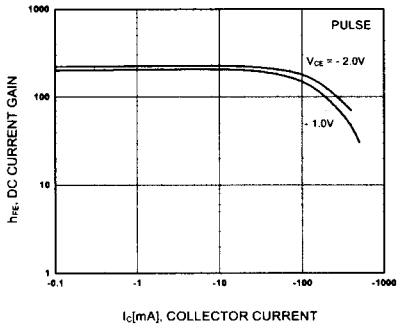


Figure 3. DC current Gain

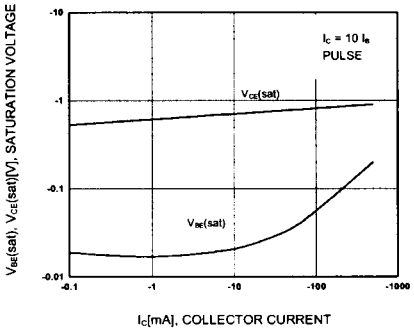


Figure 4. Base-Emitter Saturation Voltage Collector-Emitter Saturation Voltage

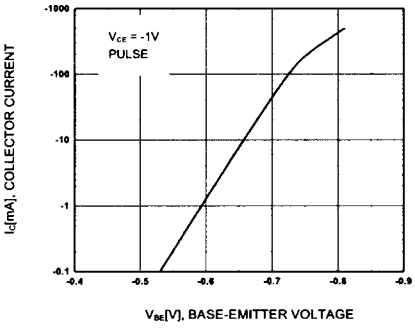


Figure 5. Base-Emitter On Voltage

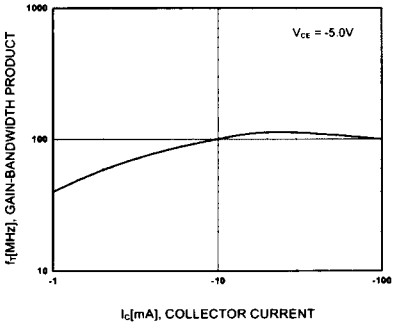


Figure 6. Gain Bandwidth Product

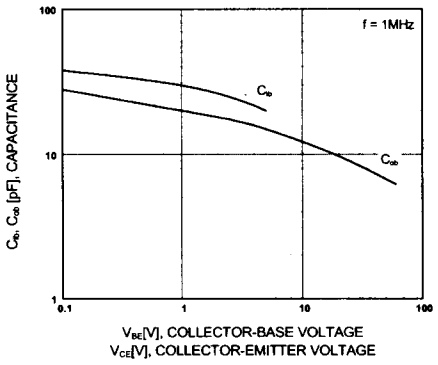


Figure 7. Input and Output Capacitance vs. Reverse Voltage

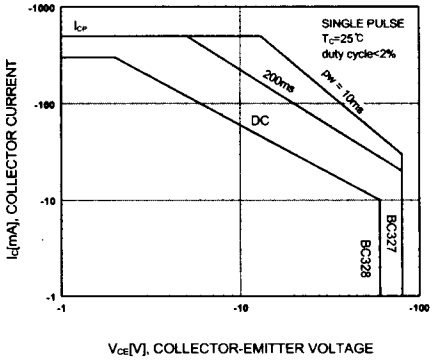


Figure 8. Safe Operating Area

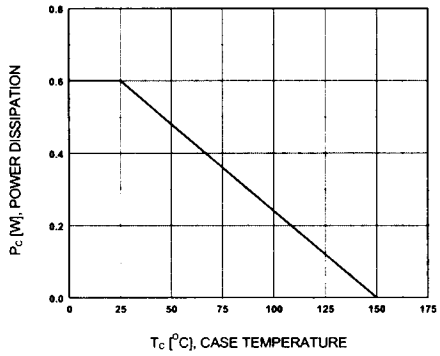


Figure 9. Power Derating