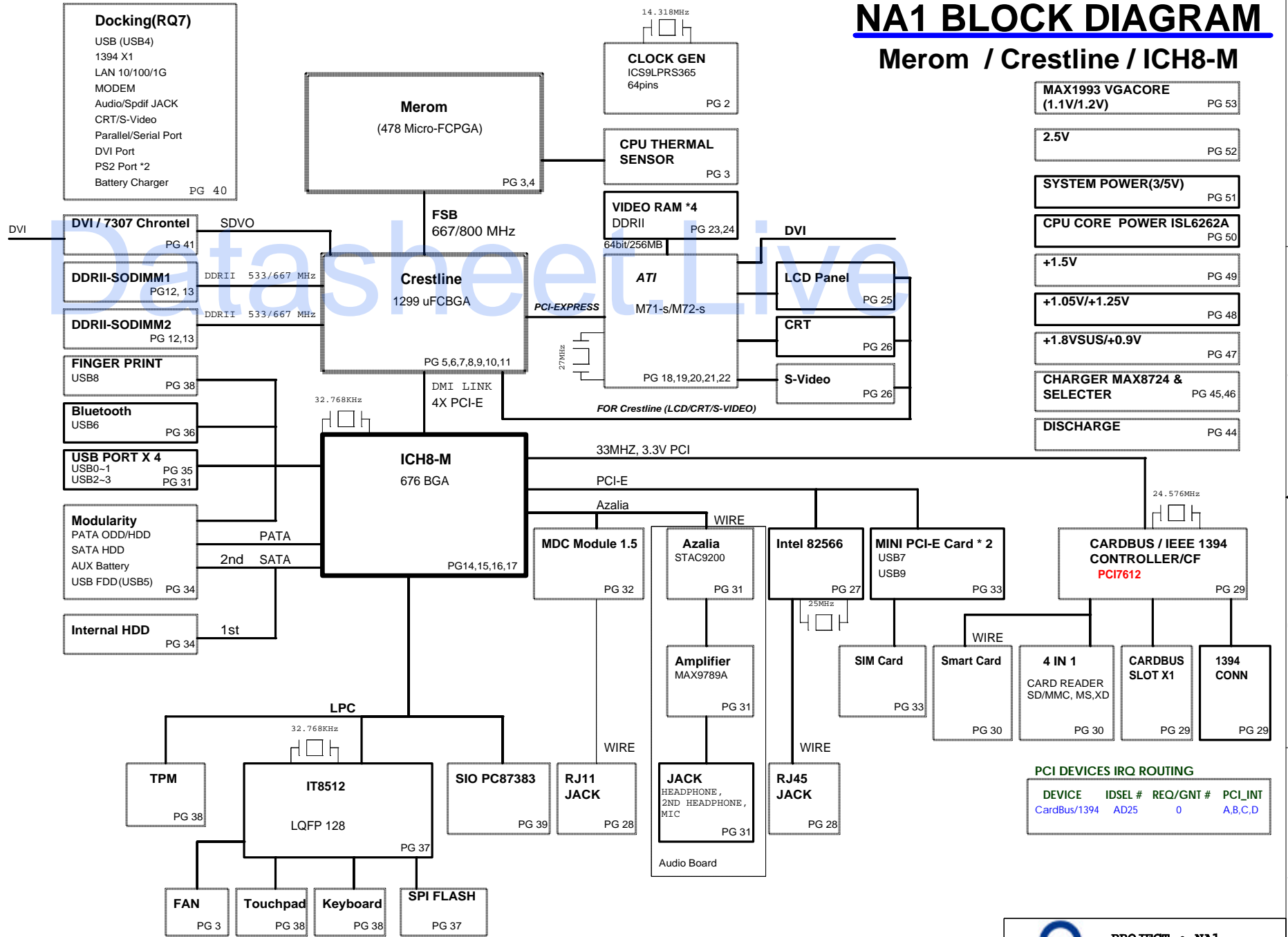
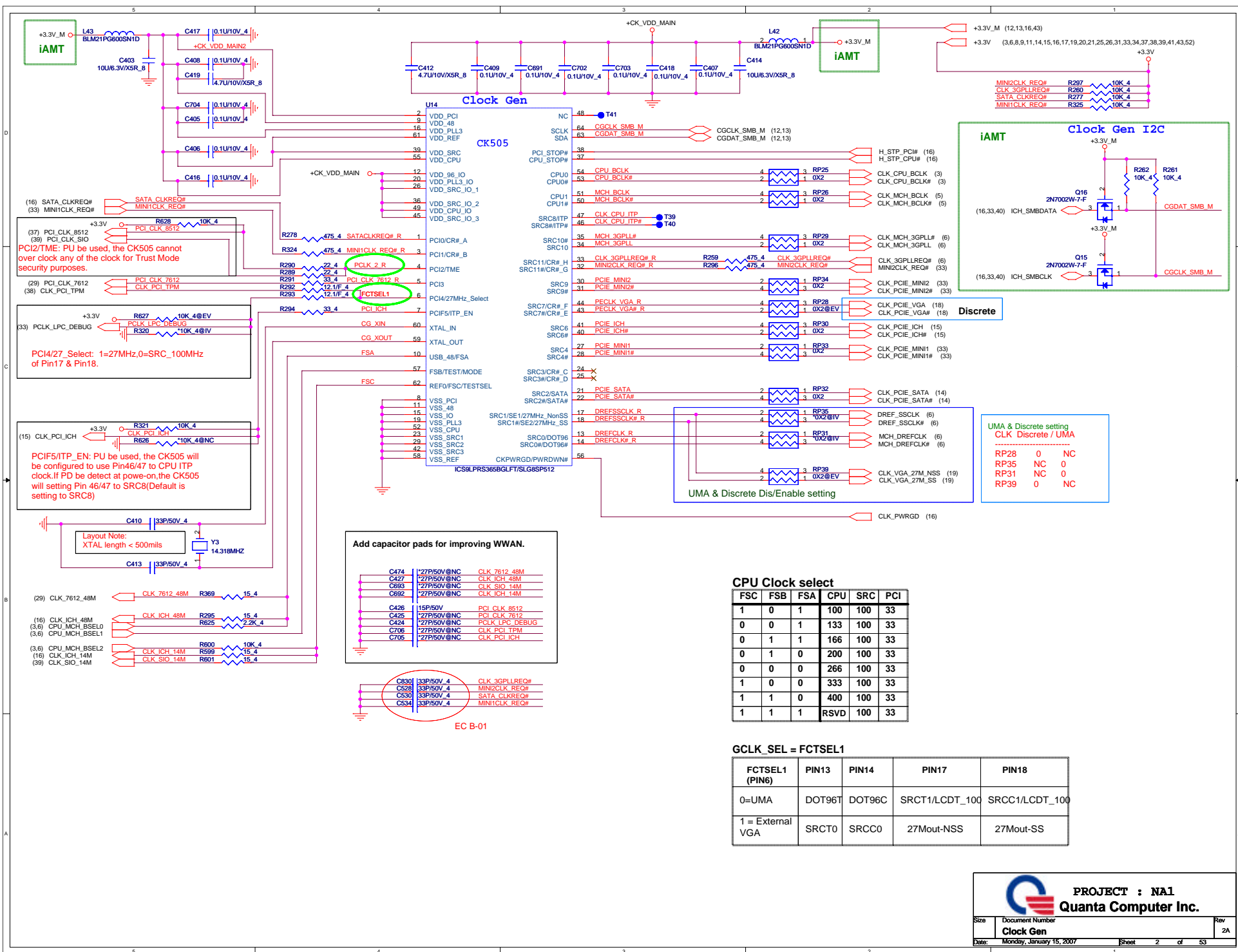


NA1 BLOCK DIAGRAM

Merom / Crestline / ICH8-M





(16) SATA_CLKREQ#
(33) MINI2CLK_REQ#

(37) PCI_CLK_8512
(39) PCI_CLK_SIO

PCI2/TME: PU be used, the CK505 cannot over clock any of the clock for Trust Mode security purposes.

(29) PCI_CLK_7612
(38) CLK_PCI_TPM

(33) PCLK_LPC_DEBUG

PCI4/27_Select: 1=27MHz,0=SRC_100MHz of Pin17 & Pin18.

(15) CLK_PCI_ICH

PCIIFS/ITP_EN: PU be used, the CK505 will be configured to use Pin46/47 to CPU ITP clock. If PD be detect at power-on, the CK505 will setting Pin 46/47 to SRC8(Default is setting to SRC8)

Layout Note:
XTAL length < 500mils

Y3
14.318MHZ

(29) CLK_7612_48M
(16) CLK_ICH_48M
(3,6) CPU_MCH_BSEL0
(3,6) CPU_MCH_BSEL1
(3,6) CPU_MCH_BSEL2
(16) CLK_ICH_14M
(39) CLK_SIO_14M

Add capacitor pads for improving WWAN.

C474	1*27P/50V@NC	CLK_7612_48M
C427	2*27P/50V@NC	CLK_ICH_48M
C693	2*27P/50V@NC	CLK_SIO_14M
C692	2*27P/50V@NC	CLK_ICH_14M
C426	15P/50V	PCI_CLK_8512
C425	2*27P/50V@NC	PCI_CLK_7612
C424	2*27P/50V@NC	PCLK_LPC_DEBUG
C706	2*27P/50V@NC	CLK_PCI_TPM
C705	2*27P/50V@NC	CLK_PCI_ICH

C530	33P/50V_4	CLK_3GPLLREQ#
C528	33P/50V_4	MINI2CLK_REQ#
C530	33P/50V_4	SATA_CLKREQ#
C534	33P/50V_4	MINI1CLK_REQ#

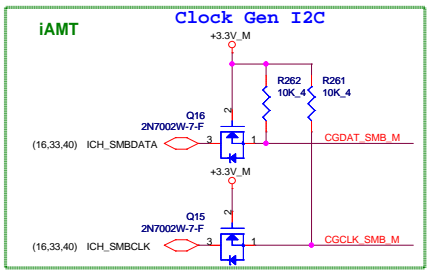
EC B-01

CPU Clock select

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

GCLK_SEL = FCTSEL1

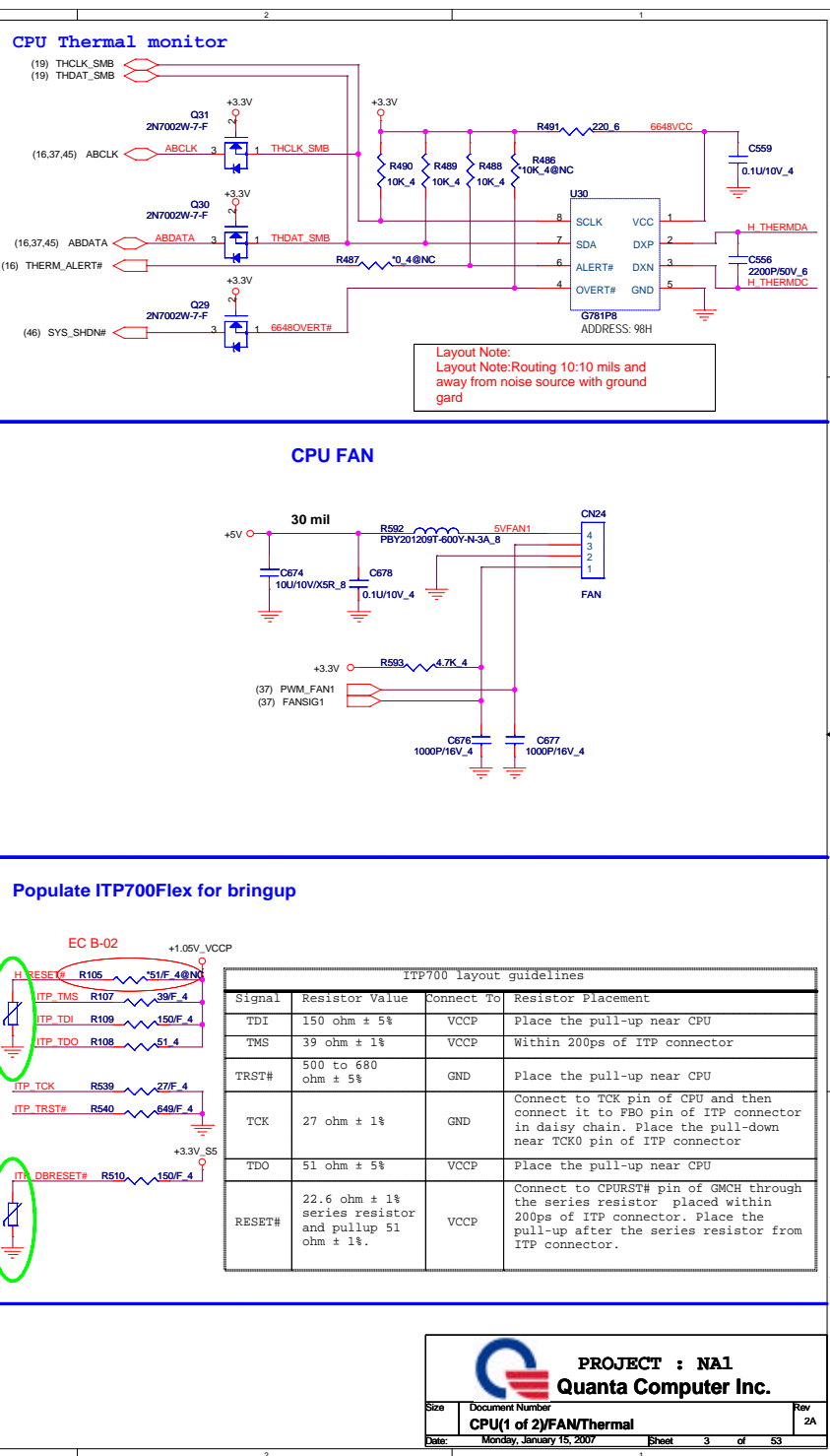
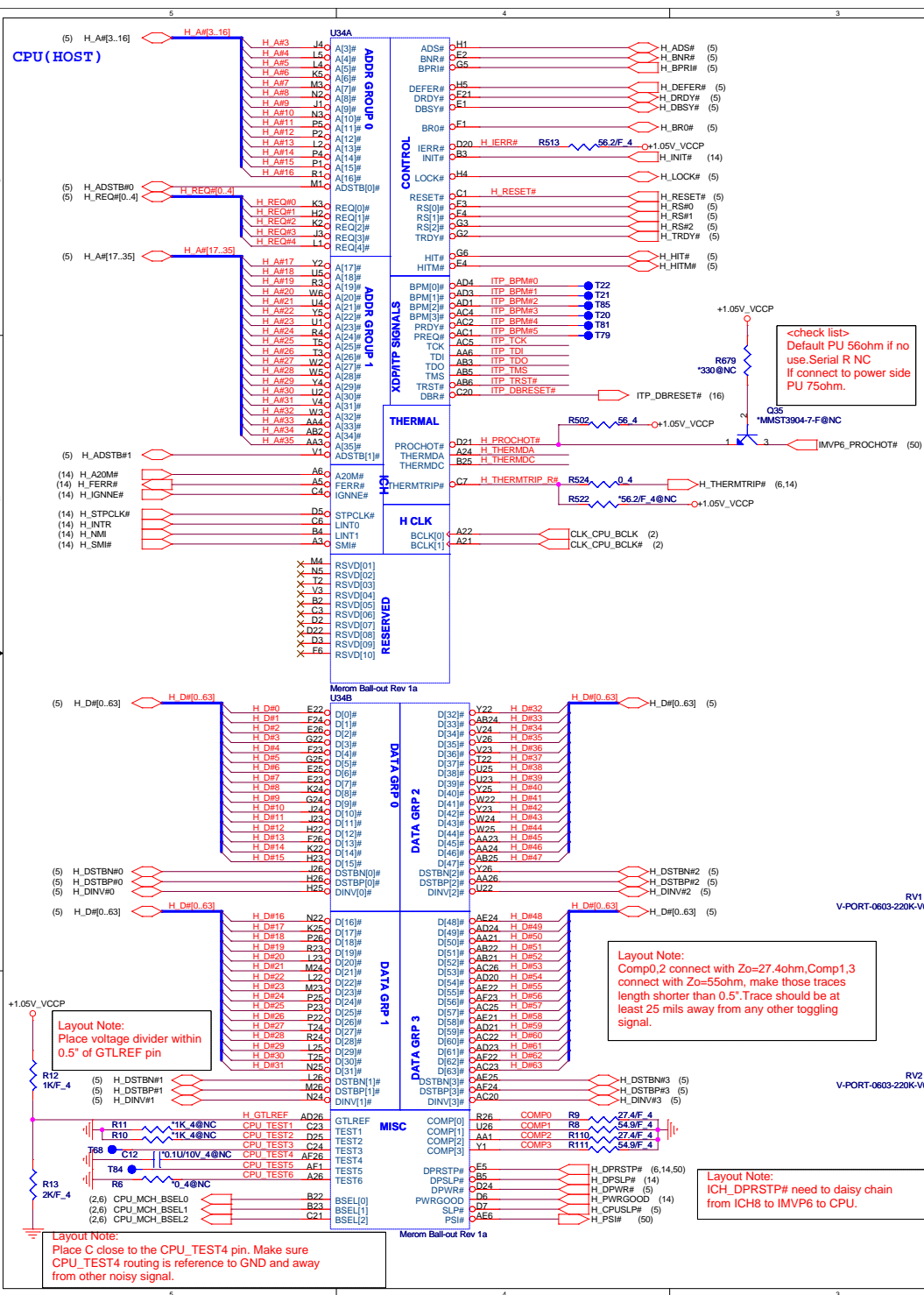
FCTSEL1 (PIN6)	PIN13	PIN14	PIN17	PIN18
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCC1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS



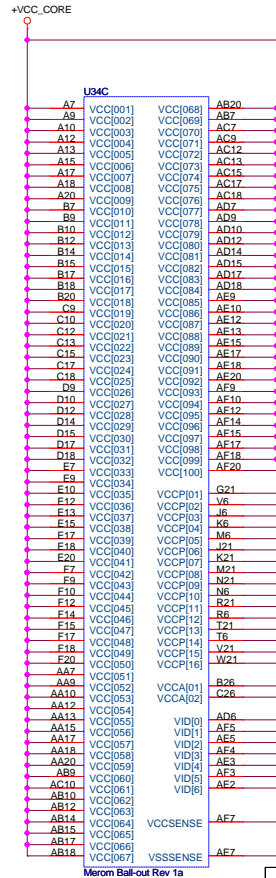
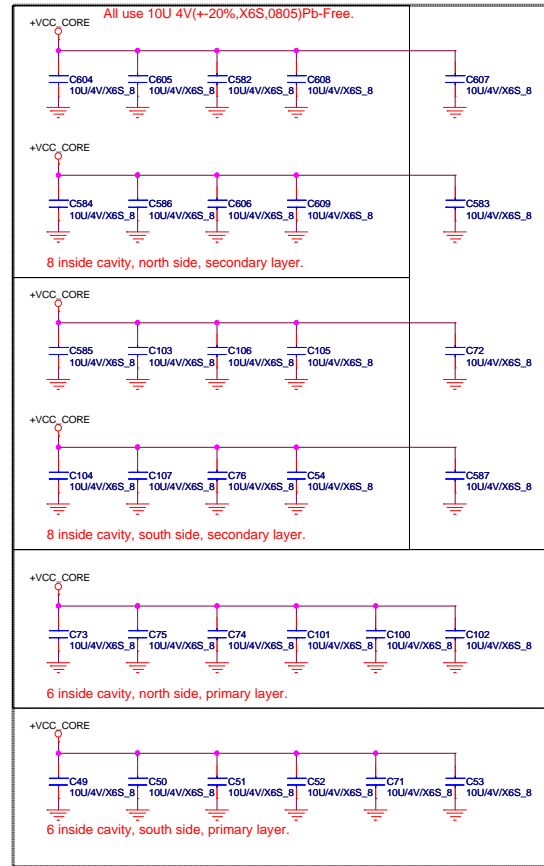
Discrete

UMA & Discrete setting
CLK Discrete / UMA

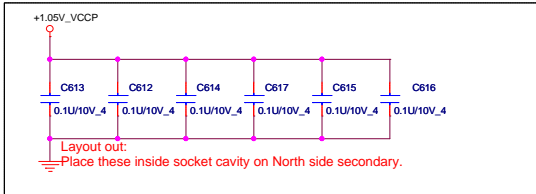
RP28	0	NC
RP35	NC	0
RP31	NC	0
RP39	0	NC



CPU(Power)



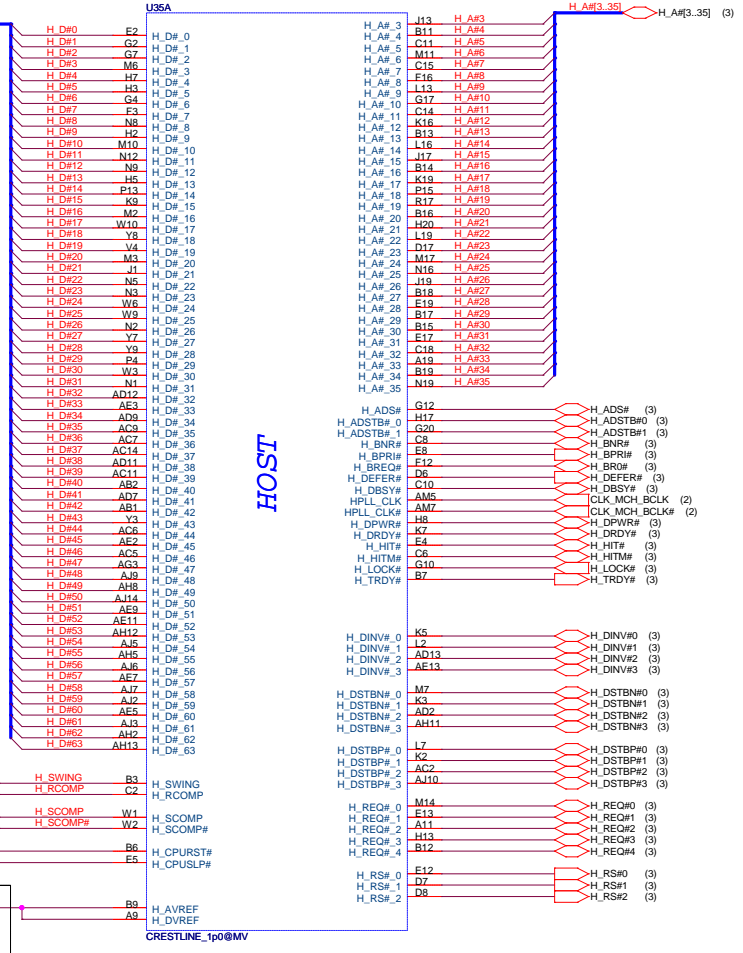
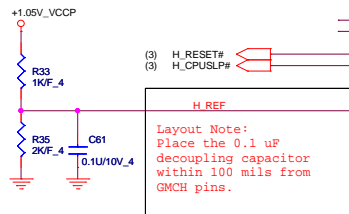
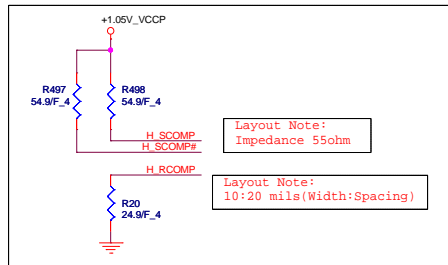
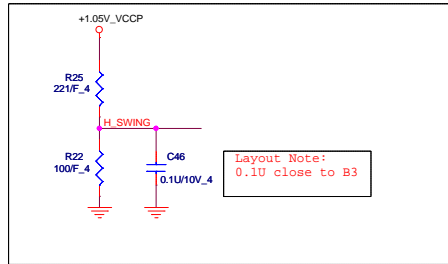
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 Ivcc Max 52A
 Ivccp Max 6A(VCCP supply before Vcc stable)
 Max 2A(VCCP supply after Vcc stable)
 Ivcca Max 130mA

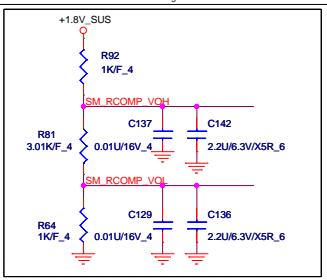


Layout Note:
 Route VCCSENSE and VSSSENSE traces at 27.4ohms and length matched to within 25 mil. Place PU and PD within 2 inch of CPU.

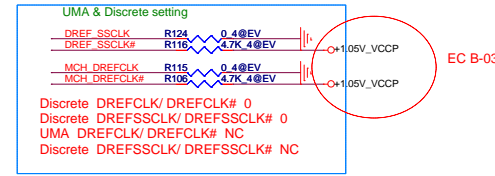
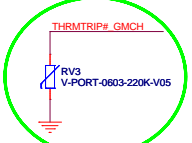
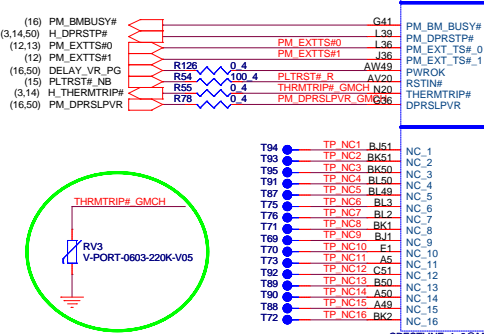
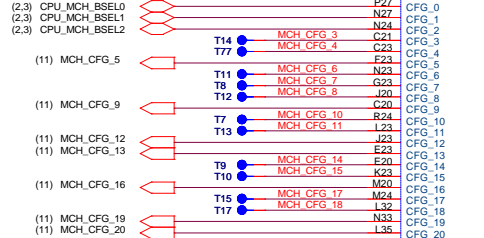
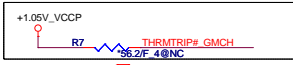
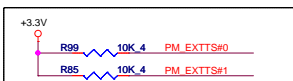
U94D		
A4	VSS[001]	VSS[082]
A8	VSS[002]	VSS[083]
A11	VSS[003]	VSS[084]
A14	VSS[004]	VSS[085]
A16	VSS[005]	VSS[086]
A19	VSS[006]	VSS[087]
A23	VSS[007]	VSS[088]
AE2	VSS[008]	VSS[089]
B6	VSS[009]	VSS[090]
B8	VSS[010]	VSS[091]
B11	VSS[011]	VSS[092]
B13	VSS[012]	VSS[093]
B16	VSS[013]	VSS[094]
B19	VSS[014]	VSS[095]
B21	VSS[015]	VSS[096]
B24	VSS[016]	VSS[097]
C5	VSS[017]	VSS[098]
C8	VSS[018]	VSS[099]
C11	VSS[019]	VSS[100]
C14	VSS[020]	VSS[101]
C16	VSS[021]	VSS[102]
C19	VSS[022]	VSS[103]
C2	VSS[023]	VSS[104]
C22	VSS[024]	VSS[105]
C25	VSS[025]	VSS[106]
D1	VSS[026]	VSS[107]
D4	VSS[027]	VSS[108]
D8	VSS[028]	VSS[109]
D11	VSS[029]	VSS[110]
D13	VSS[030]	VSS[111]
D16	VSS[031]	VSS[112]
D19	VSS[032]	VSS[113]
D23	VSS[033]	VSS[114]
D26	VSS[034]	VSS[115]
E3	VSS[035]	VSS[116]
E6	VSS[036]	VSS[117]
E8	VSS[037]	VSS[118]
E11	VSS[038]	VSS[119]
E14	VSS[039]	VSS[120]
E16	VSS[040]	VSS[121]
E19	VSS[041]	VSS[122]
E21	VSS[042]	VSS[123]
E24	VSS[043]	VSS[124]
F5	VSS[044]	VSS[125]
F8	VSS[045]	VSS[126]
F11	VSS[046]	VSS[127]
F13	VSS[047]	VSS[128]
F16	VSS[048]	VSS[129]
F19	VSS[049]	VSS[130]
F22	VSS[050]	VSS[131]
F25	VSS[051]	VSS[132]
G4	VSS[052]	VSS[133]
G1	VSS[053]	VSS[134]
G23	VSS[054]	VSS[135]
G26	VSS[055]	VSS[136]
H3	VSS[056]	VSS[137]
H6	VSS[057]	VSS[138]
H24	VSS[058]	VSS[139]
H21	VSS[059]	VSS[140]
J2	VSS[060]	VSS[141]
J5	VSS[061]	VSS[142]
J22	VSS[062]	VSS[143]
J25	VSS[063]	VSS[144]
K1	VSS[064]	VSS[145]
K4	VSS[065]	VSS[146]
K23	VSS[066]	VSS[147]
K26	VSS[067]	VSS[148]
L3	VSS[068]	VSS[149]
L16	VSS[069]	VSS[150]
L21	VSS[070]	VSS[151]
L24	VSS[071]	VSS[152]
M2	VSS[072]	VSS[153]
M5	VSS[073]	VSS[154]
M22	VSS[074]	VSS[155]
M25	VSS[075]	VSS[156]
N1	VSS[076]	VSS[157]
N4	VSS[077]	VSS[158]
N23	VSS[078]	VSS[159]
N26	VSS[079]	VSS[160]
P3	VSS[080]	VSS[161]
	VSS[081]	VSS[162]
	VSS[082]	VSS[163]

Merom Ball-out Rev 1a

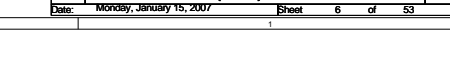
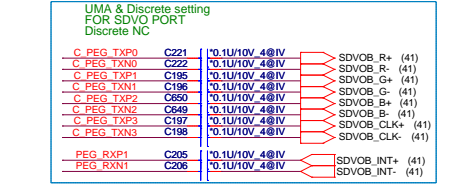
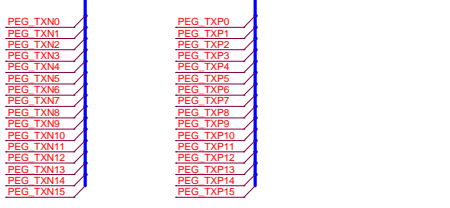
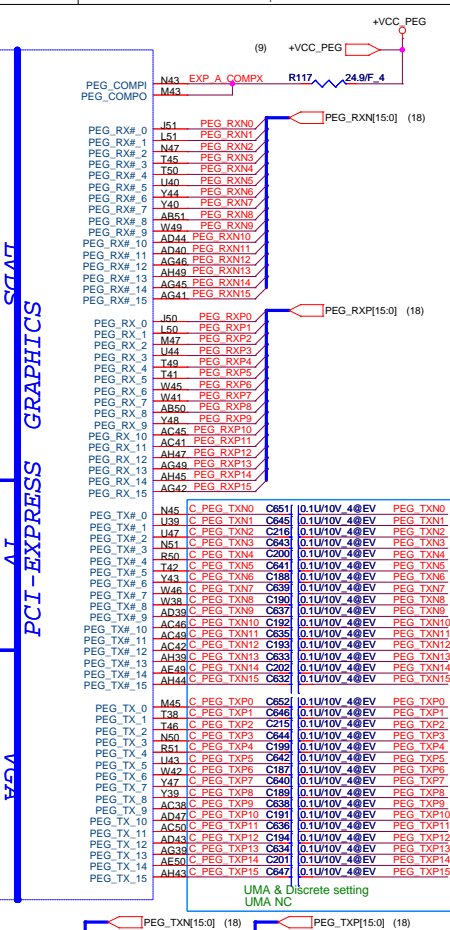
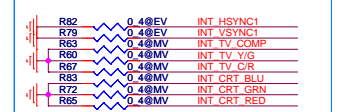
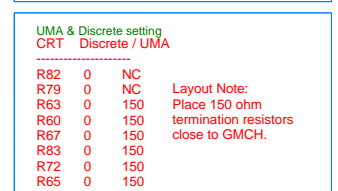
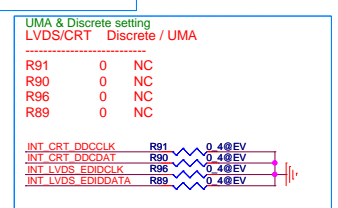
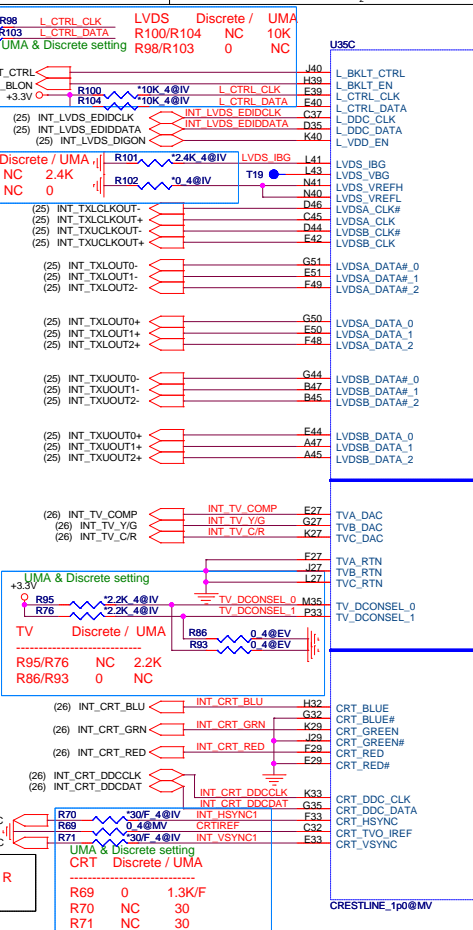
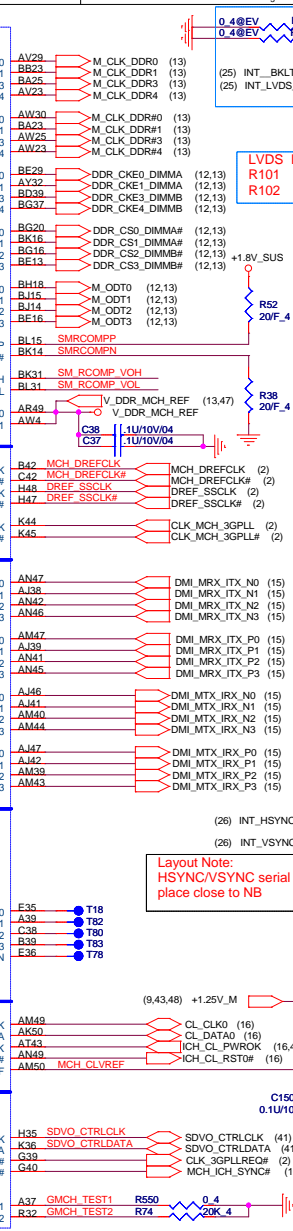
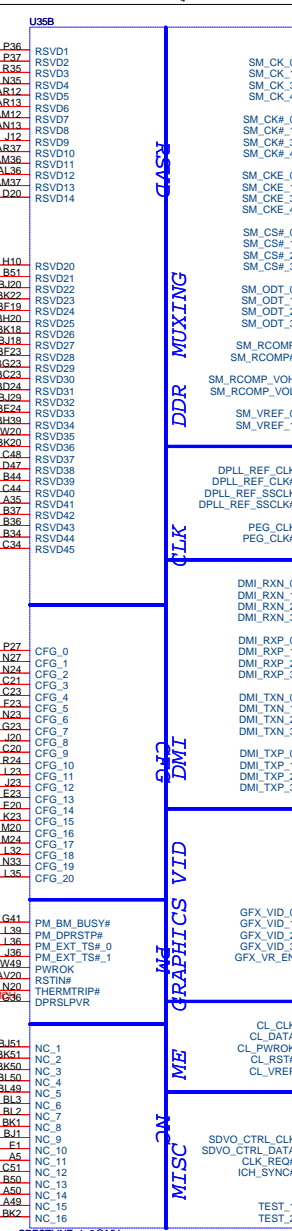




Santa Rosa Platform MOW Ww15
 For 4Gb DRAM support,
 change Pin-BJ29 to DDR_A_Ma14,
 change Pin-BE24 to DDR_B_Ma14.

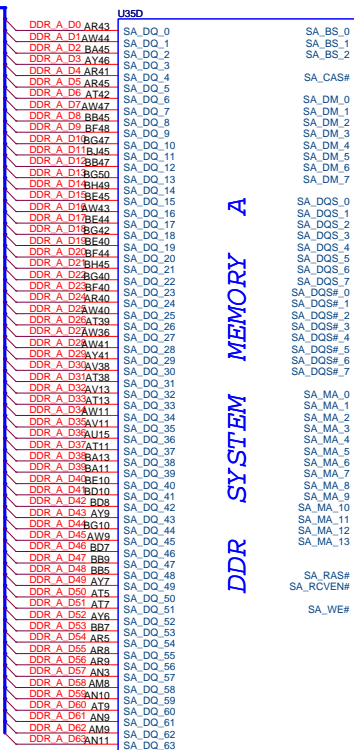


External VGA with @EV part,
 Internal VGA with @IV part.



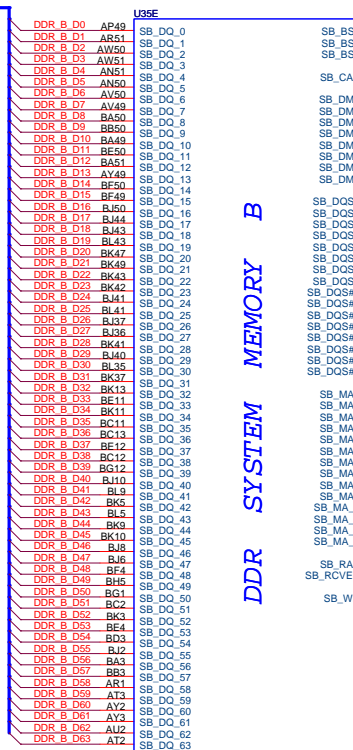
PROJECT : NAI
 Quanta Computer Inc.

(13) DDR_A_D[0..63]



CRESTLINE_1p0@MV

(13) DDR_B_D[0..63]



CRESTLINE_1p0@MV

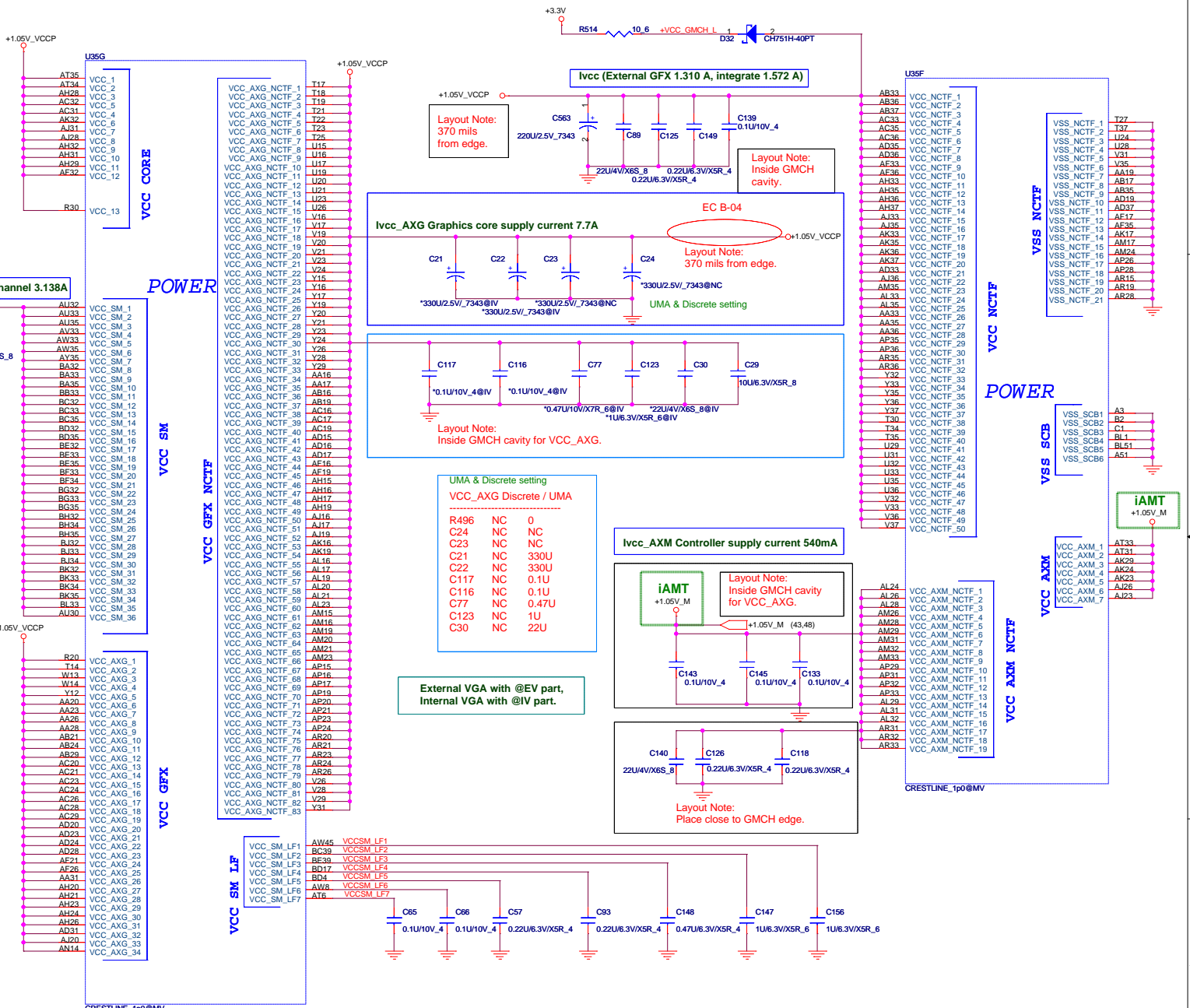
PROJECT : NAI
 Quanta Computer Inc.

Document Number
 GMCH DDR/Strap(3 of 6)

Date: Monday, January 15, 2007 Sheet 7 of 53

Rev 1A

GMCH 1.05V	current(A)	Remark
VCC_Core	1.573	(1.3A for external GFX)
VCC_AXG	7.7	for integrated GFX
VCC_AXD	0.2	
VTT	0.85	FSB VCCP
VCC_PEG	1.2	for PCIEG
VCC_AXM	0.54	for IAMT function
VCCR_RX_DMI1	0.25	DMI
SUM	12.313	



VCCSM supply current 1 channel 1.615A 2 channel 3.138A

Layout Note: Place C2630 where LVDS and DDR2 taps.

Ivcc (External GFX 1.310 A, integrate 1.572 A)

Layout Note: 370 mils from edge.

Layout Note: Inside GMCH cavity.

Ivcc_AXG Graphics core supply current 7.7A

UMA & Discrete setting

Layout Note: 370 mils from edge.

UMA & Discrete setting

Layout Note: Inside GMCH cavity for VCC_AXG.

UMA & Discrete setting

VCC_AXG Discrete / UMA

R496	NC	0
C24	NC	NC
C23	NC	NC
C21	NC	330U
C22	NC	330U
C117	NC	0.1U
C116	NC	0.1U
C77	NC	0.47U
C123	NC	1U
C30	NC	22U

Ivcc_AXM Controller supply current 540mA

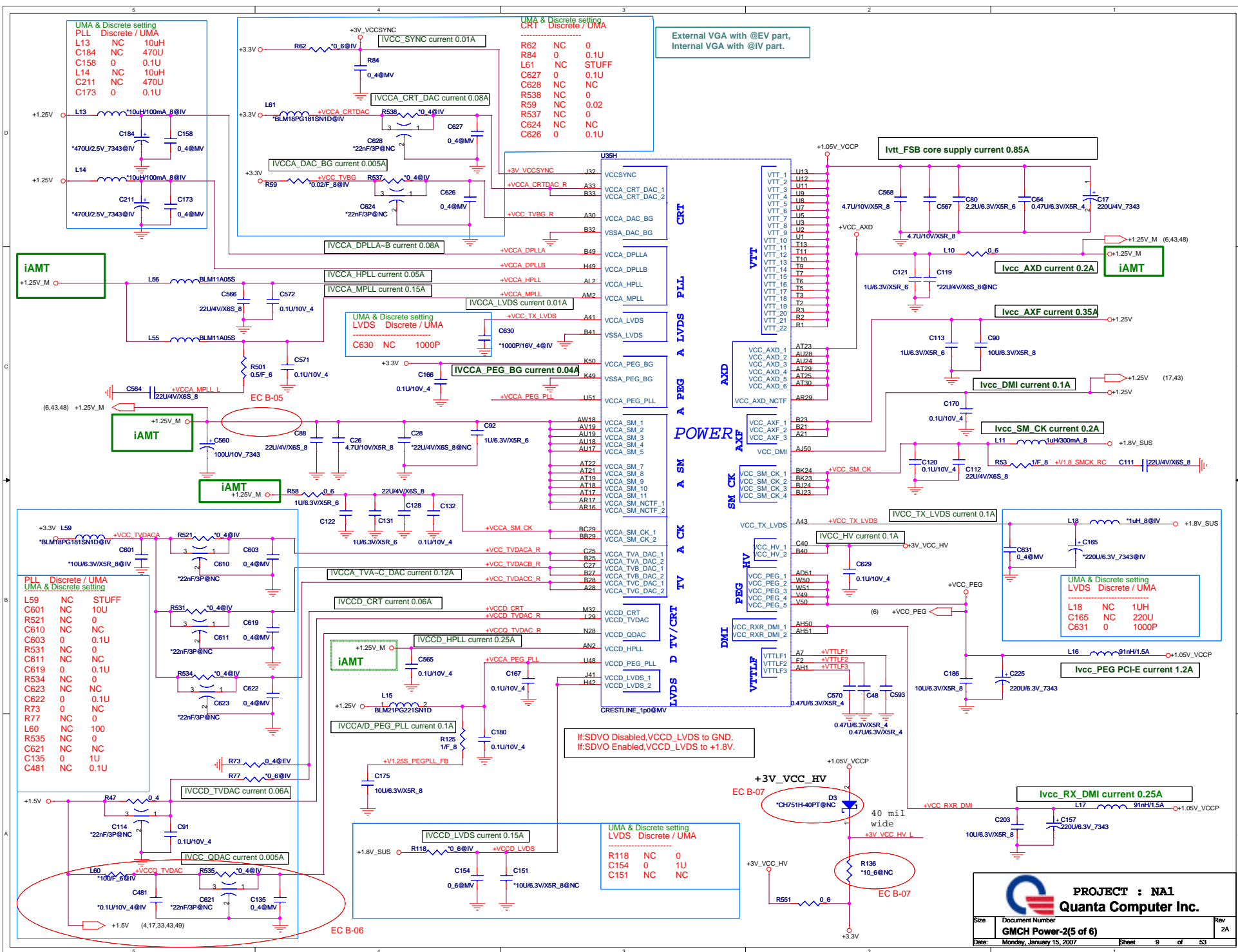
iAMT +1.05V_M

Layout Note: Inside GMCH cavity for VCC_AXG.

Layout Note: Place close to GMCH edge.

External VGA with @EV part, Internal VGA with @IV part.

CRESTLINE_1p0@MV



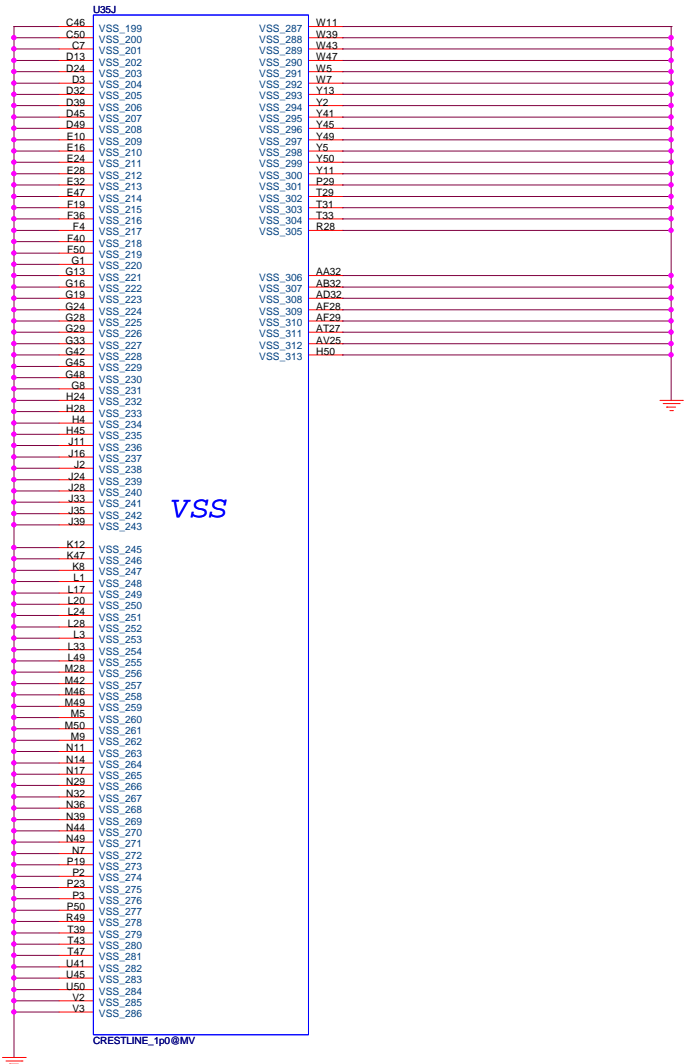
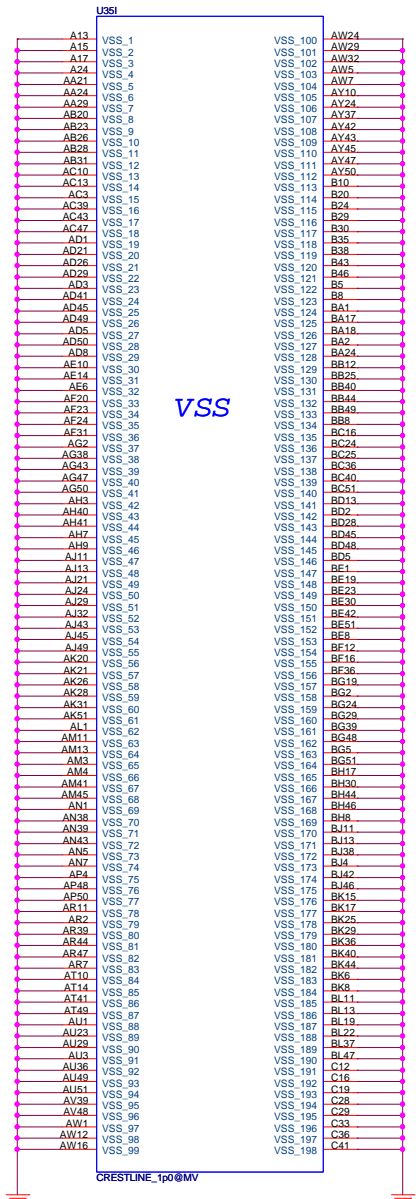
POWER

If:SDVO Disabled,VCCD_LVDS to GND.
If:SDVO Enabled,VCCD_LVDS to +1.8V.

PROJECT : NA1
Quanta Computer Inc.

Size: _____ Document Number: **GMCH Power-2(5 of 6)** Rev: **2A**
Date: **Monday, January 15, 2007** Sheet: **9** of **53**

NB (Power - 3)



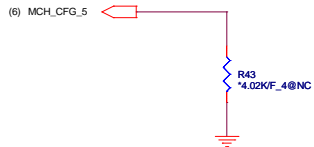
Strap table

All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal
 CFG[17:3] Have internal Pull-up
 CFG[18:19] Have internal Pull-down
 Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

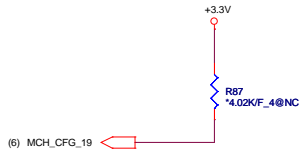
DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMX4(Default)
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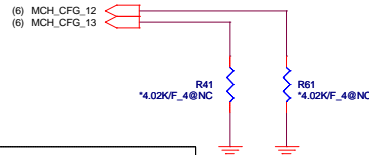
DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane
------------	--



XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)



PCI Express Graphics

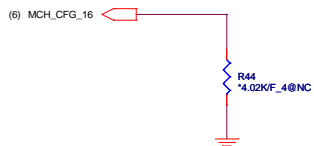
MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)
-----------	--



SDVO Present
Strap define at External DVI control page

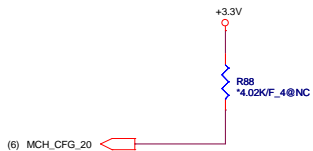
FSB Dynamic ODT

MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)
------------	---



SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO and PCIE X1 are operating simultaneously via the PEG port
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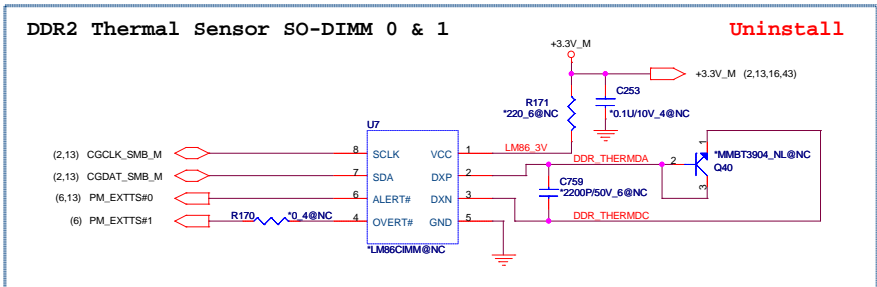
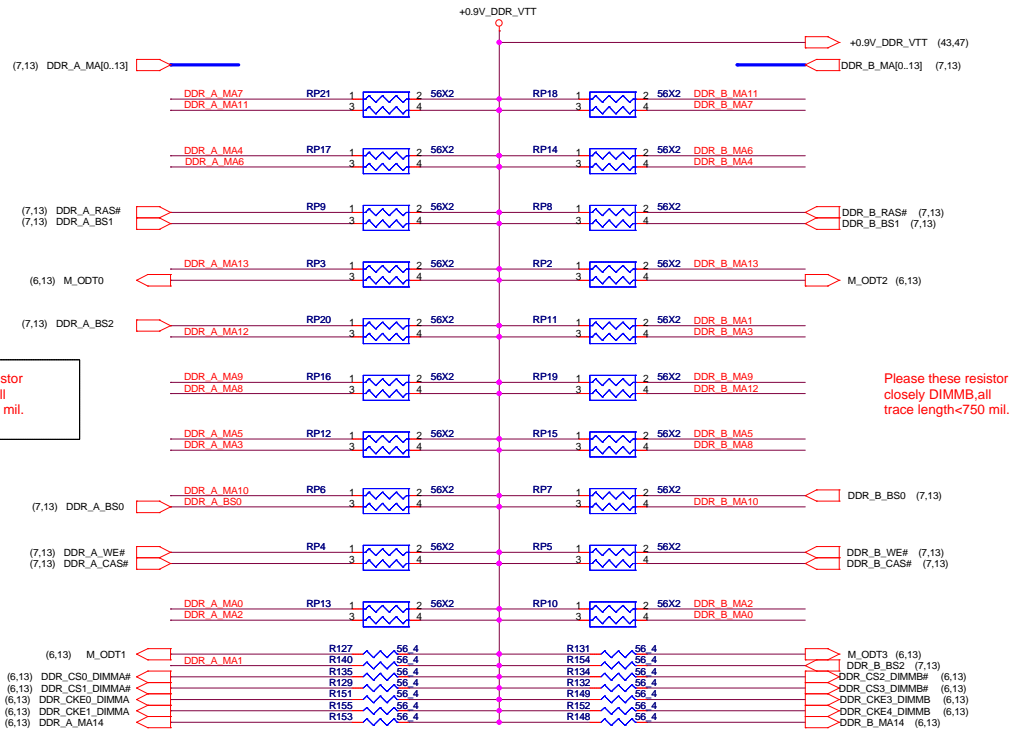
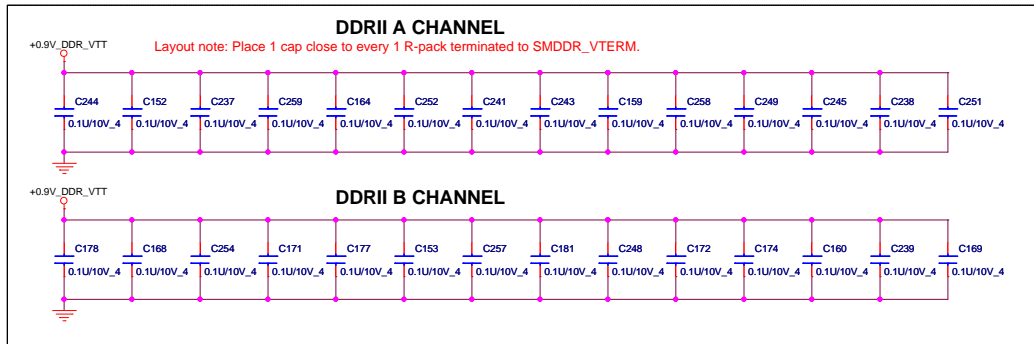


Layout Note:
Location of all MCH_CFG strap resistors needs to be close to minimize stub.

PROJECT : NAI
Quanta Computer Inc.

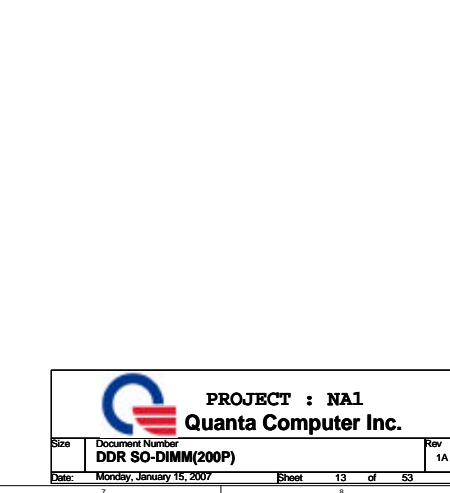
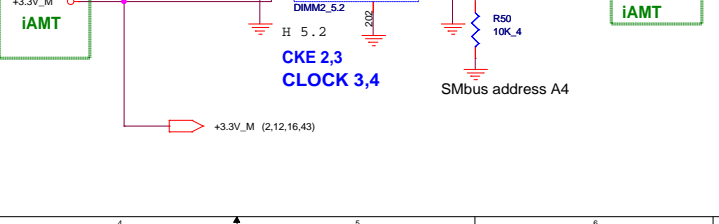
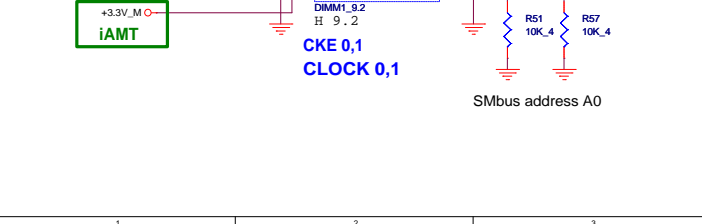
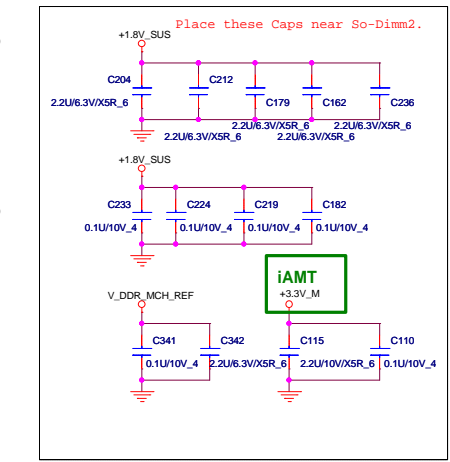
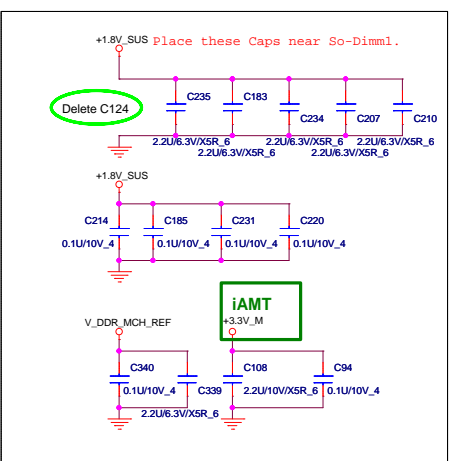
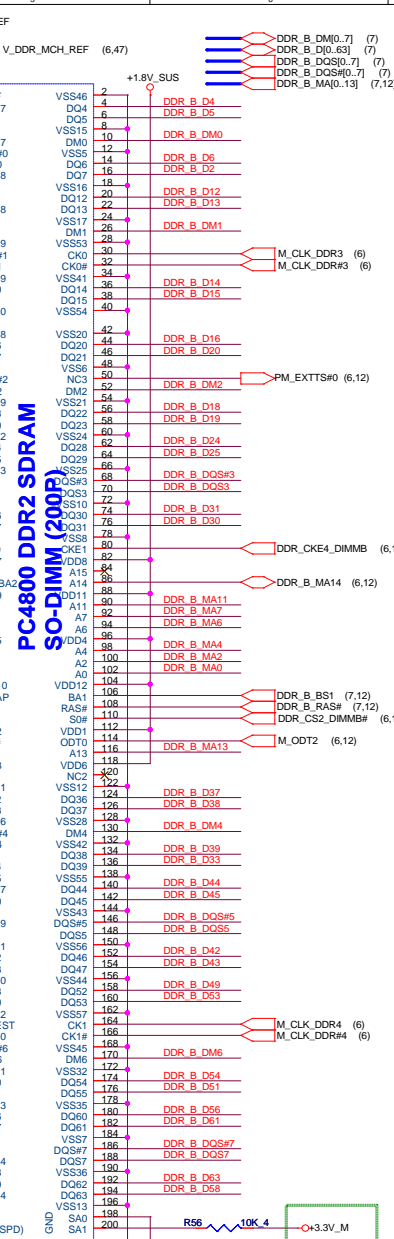
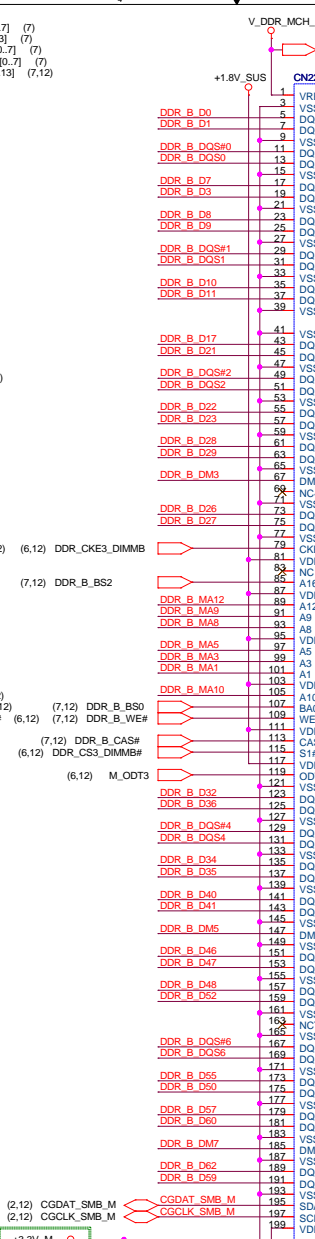
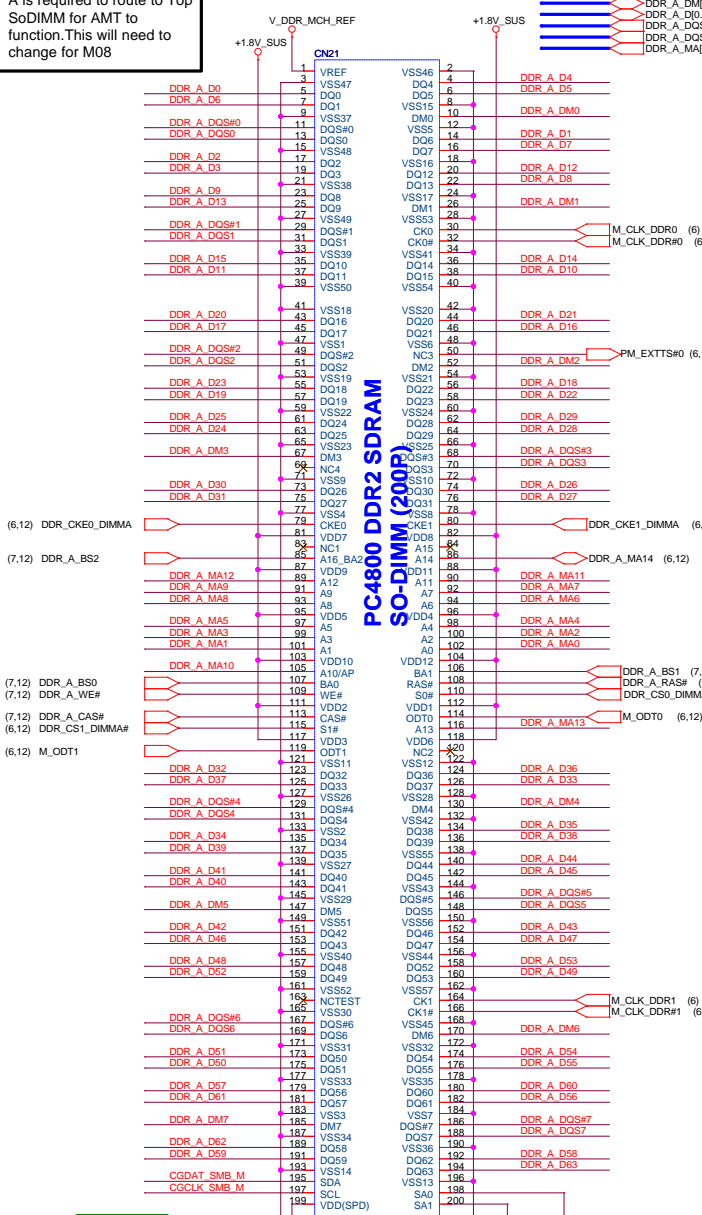
Size	Document Number	Rev
	GMCH Strap Table	1A
Date:	Monday, January 15, 2007	Sheet 11 of 53

DDR2 Dual channel A/B PU

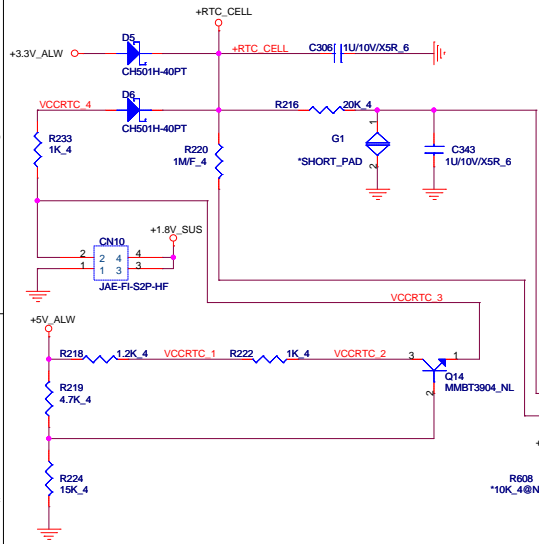


A is required to route to Top SoDIMM for AMT to function. This will need to change for M08

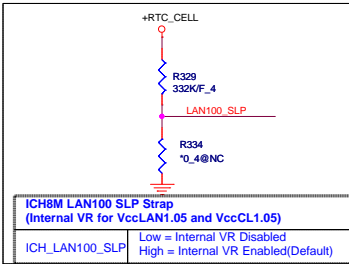
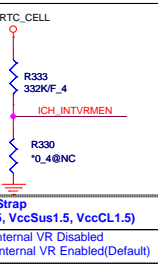
DDR2 Dual channel A/B CONN



RTC

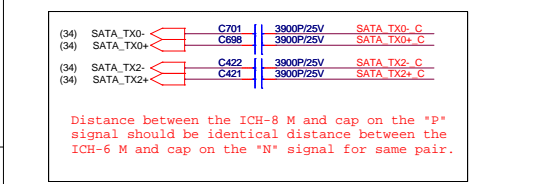
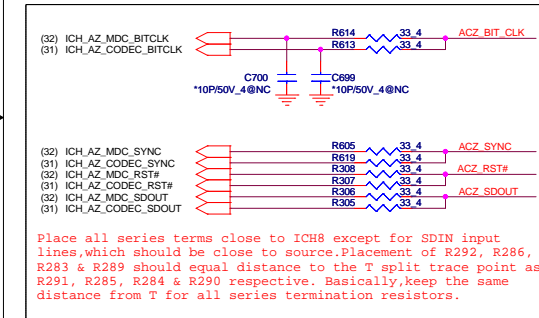


SB Strap

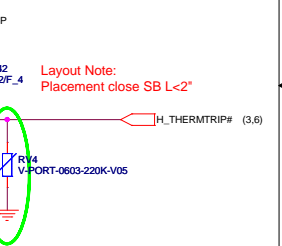
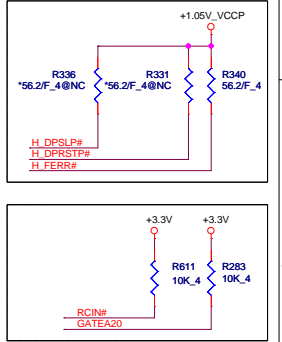
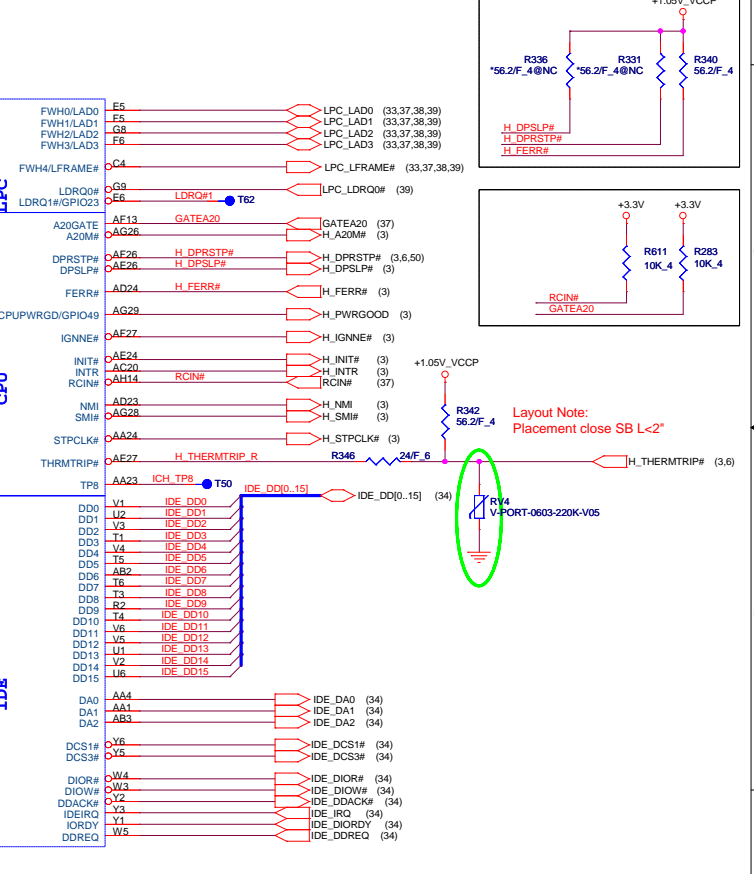
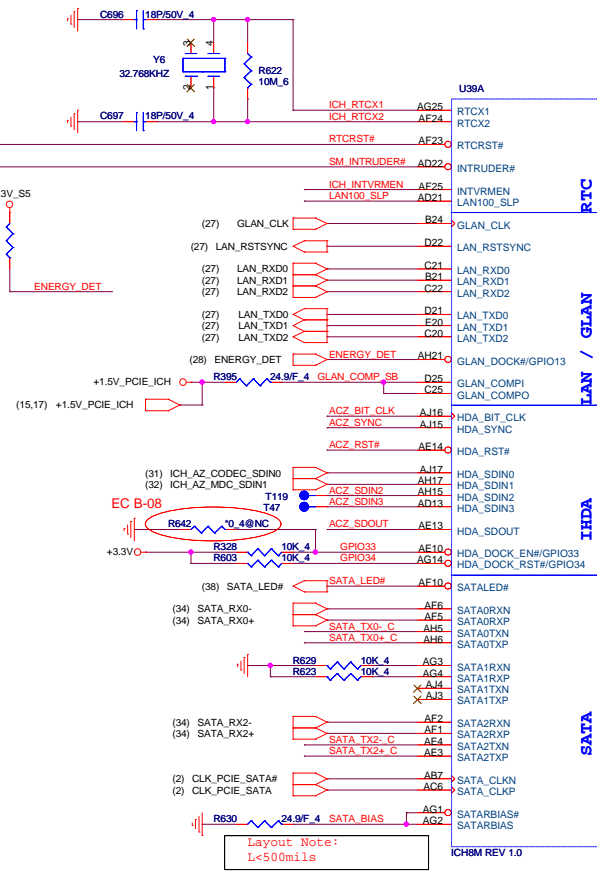


ICH8M Internal VR Enable Strap
(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)
Low = Internal VR Disabled
High = Internal VR Enabled(Default)

ICH8M LAN100 SLP Strap
(Internal VR for VccLAN1.05 and VccCL1.05)
Low = Internal VR Disabled
High = Internal VR Enabled(Default)

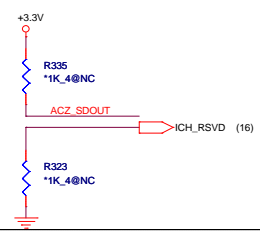


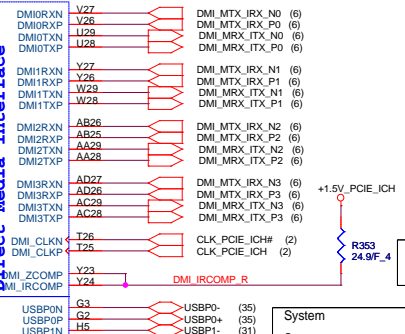
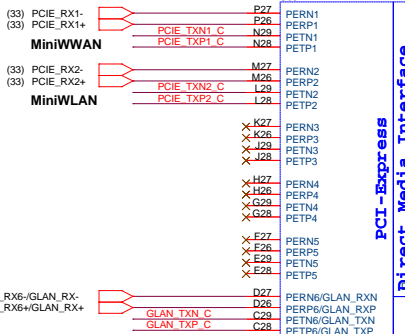
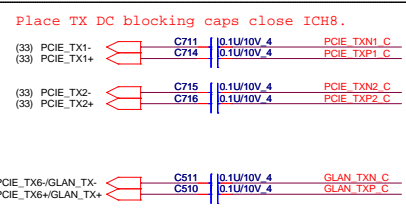
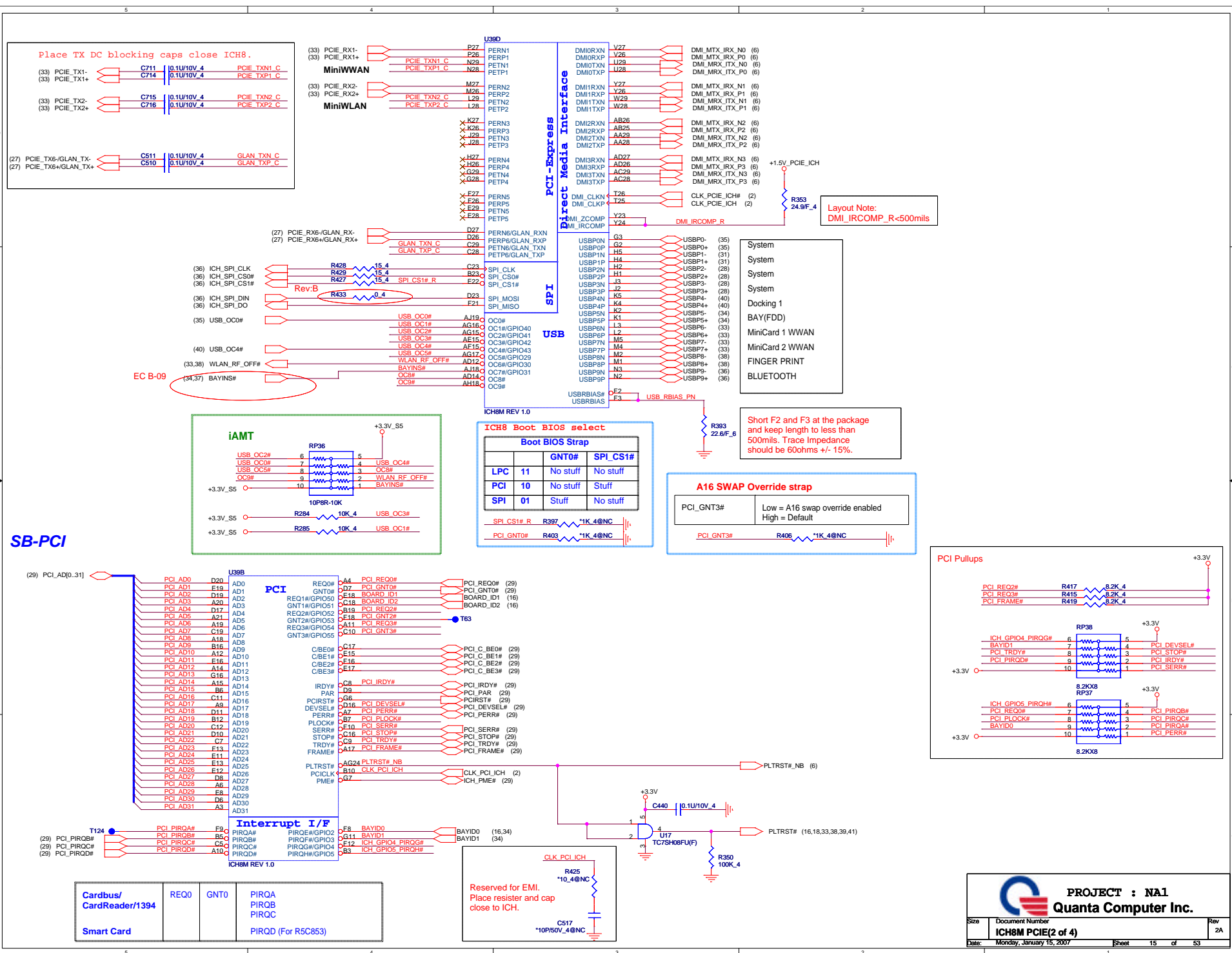
Distance between the ICH-8 M and cap on the "P" signal should be identical distance between the ICH-6 M and cap on the "N" signal for same pair.



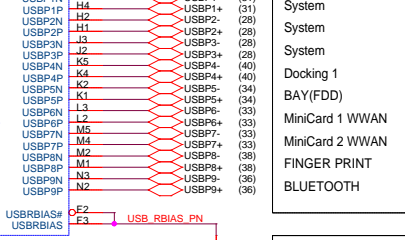
XOR Chain Entrance Strap

ICH_RSVD0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIE port config bit 1

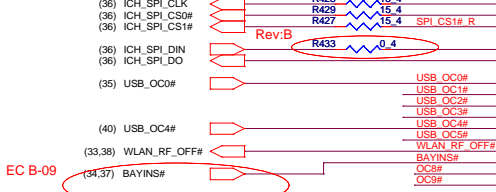




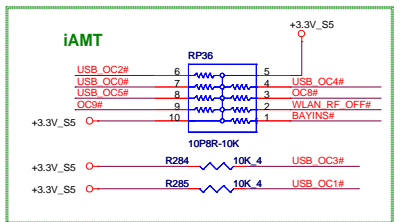
Layout Note:
DMI_IRCOMP_R < 500mils



- System
- System
- System
- System
- Docking 1
- BAY(FDD)
- MiniCard 1 WWAN
- MiniCard 2 WWAN
- FINGER PRINT
- BLUETOOTH



EC B-09 (34,37) BAYINS#



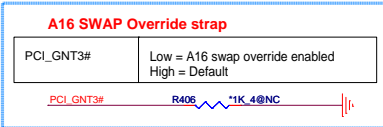
ICH8M REV 1.0

Boot BIOS select

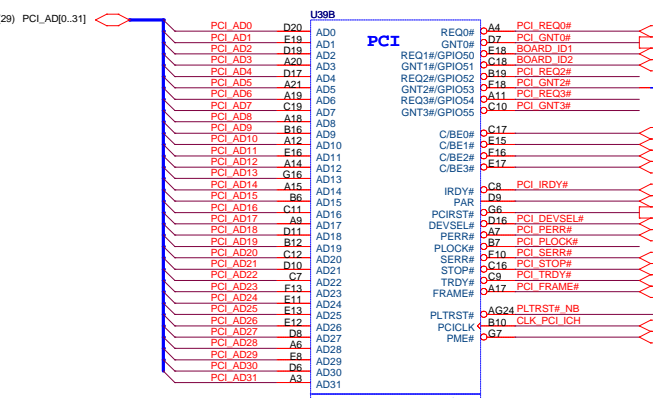
	GNT0#	SPI_CS1#
LPC	11	No stuff
PCI	10	No stuff
SPI	01	Stuff

SPI_CS1#_R R397 *1K 4@NC
 PCI_GNT0# R403 *1K 4@NC

Short F2 and F3 at the package and keep length to less than 500mils. Trace Impedance should be 60ohms +/- 15%.

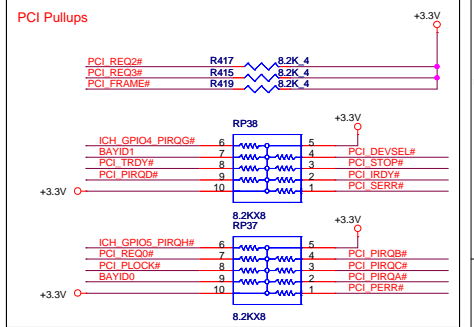


SB-PCI



Cardbus/ CardReader/1394	REQ0	GNT0	PIRQA PIROB PIROD
Smart Card			PIROD (For R5C853)

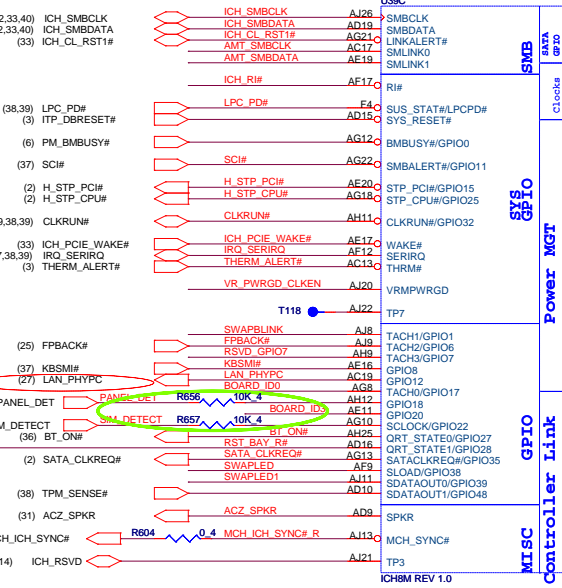
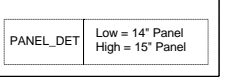
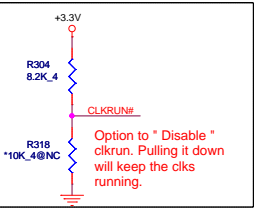
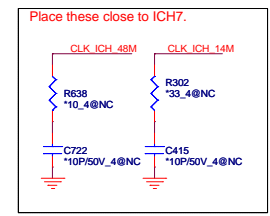
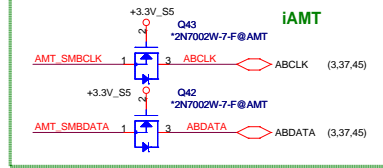
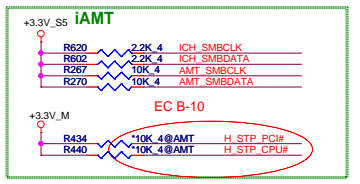
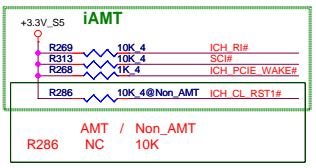
Reserved for EMI. Place resistor and cap close to ICH.



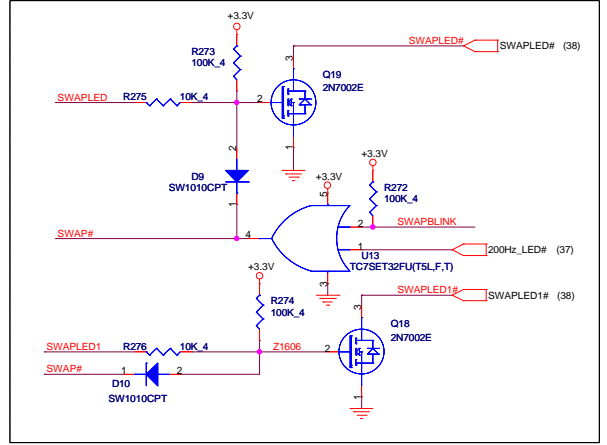
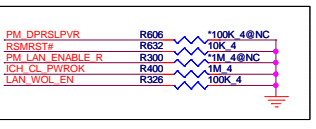
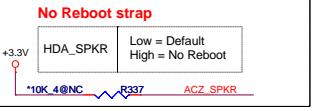
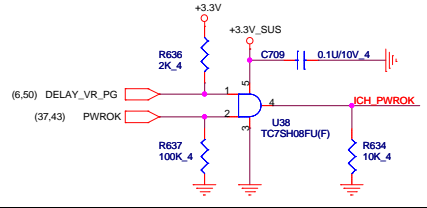
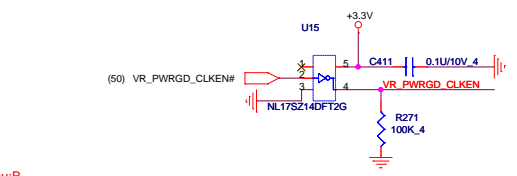
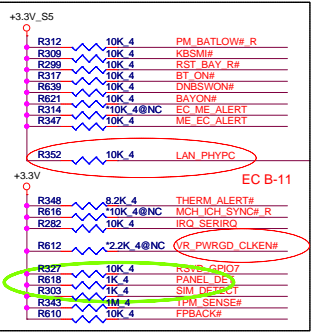
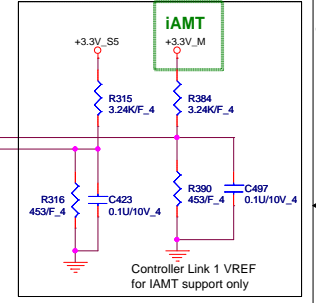
PROJECT : NA1
Quanta Computer Inc.

Size Document Number
ICH8M PCIE(2 of 4)

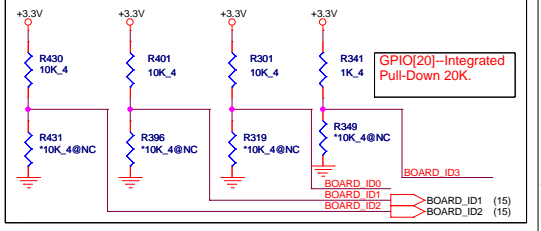
Date: Monday, January 15, 2007 Sheet 15 of 53 Rev 2A

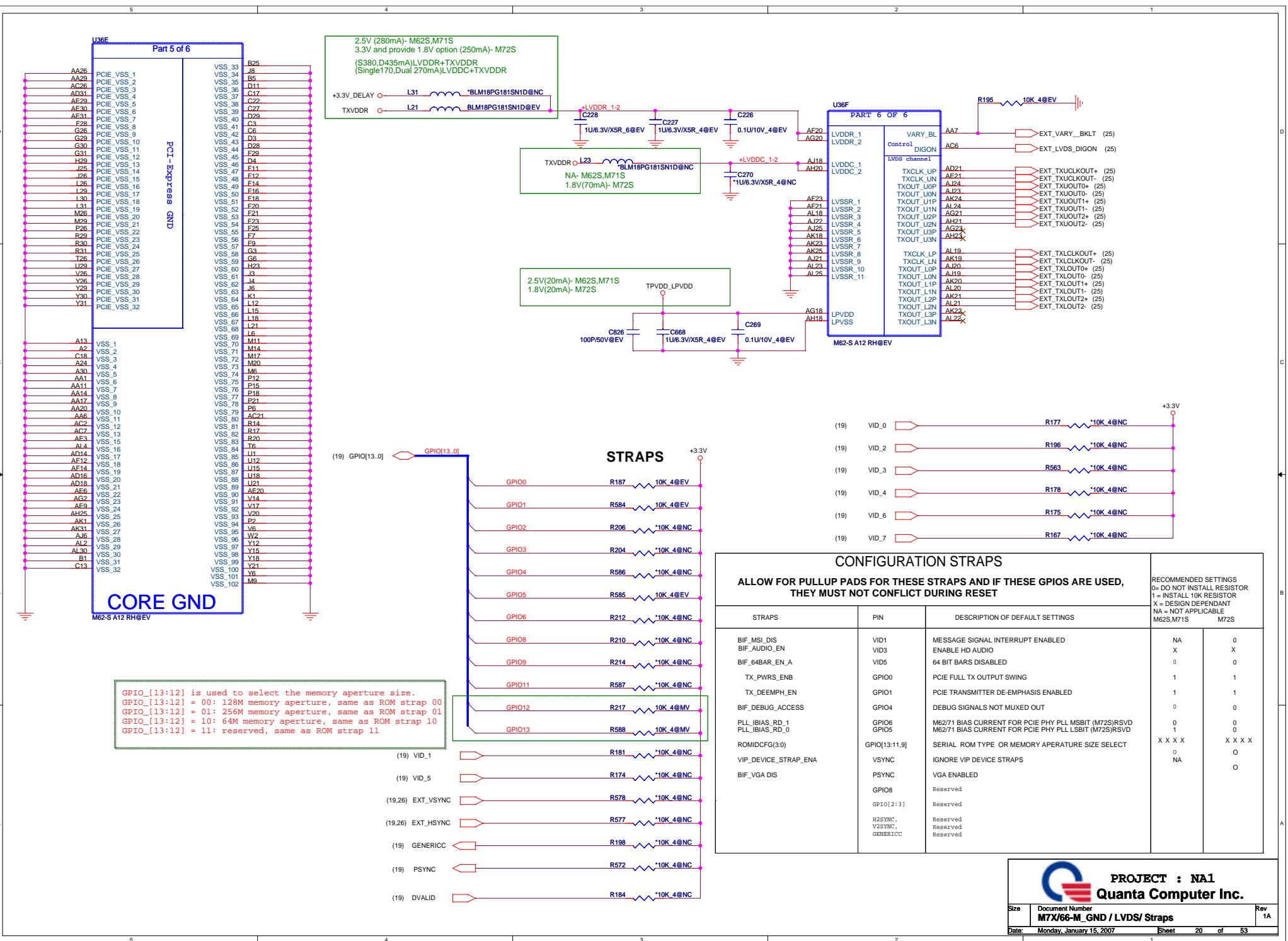


If no use internal LAN MAC connect LAN_RST# to PLTRST#
Use internal LAN MAC connect LAN_RST# to RSMRST# should go high no sooner than 10 ms after both VccLAN3_3 and VccLAN1_5 have reached their nominal voltages.



Board ID	ID3	ID2	ID1	ID0
Default	1	1	1	1
RSV	0	0	0	1
RSV	0	0	1	0
RSV	0	0	1	1
RSV	0	1	0	0





U36E Part 5 of 6

2.5V (280mA)- M62S,M71S
 3.3V and provide 1.8V option (250mA)- M72S
 (S380,D435mA)LVDDR+TXVDDR
 (Single170,Dual 270mA)LVDDC+TXVDDR

2.5V(20mA)- M62S,M71S
 1.8V(20mA)- M72S

U36F PART 6 OF 6

CORE GND
 M62-S A12 RH@EV

STRAPS

GPIO_[13:12] is used to select the memory aperture size.
 GPIO_[13:12] = 00: 128M memory aperture, same as ROM strap 00
 GPIO_[13:12] = 01: 256M memory aperture, same as ROM strap 01
 GPIO_[13:12] = 10: 64M memory aperture, same as ROM strap 10
 GPIO_[13:12] = 11: reserved, same as ROM strap 11

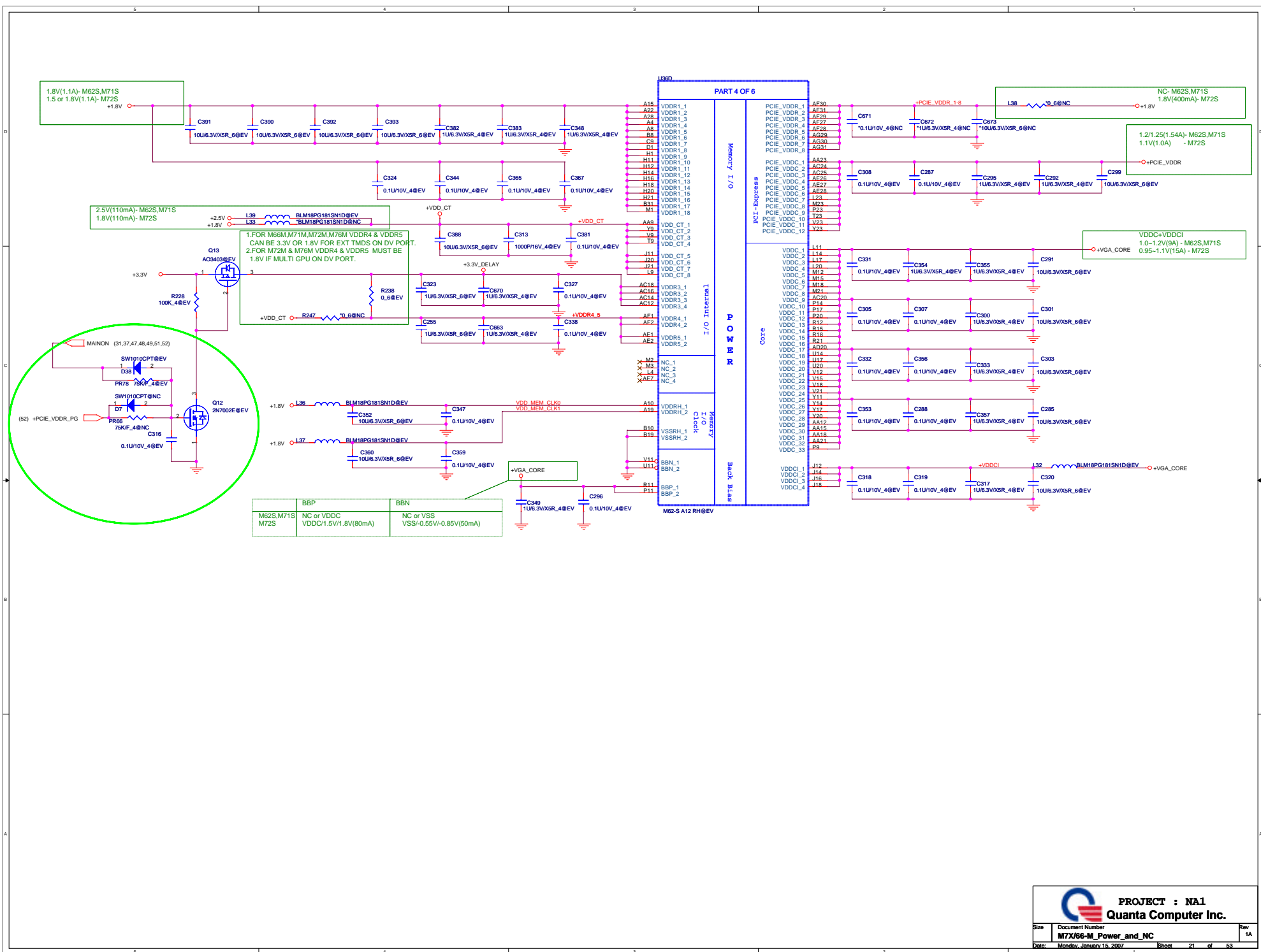
CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS	
			M62S,M71S	M72S
BIF_MSI_DIS	VID1	MESSAGE SIGNAL INTERRUPT ENABLED	NA	0
BIF_AUDIO_EN	VID3	ENABLE HD AUDIO	X	X
BIF_64BAR_EN_A	VID5	64 BIT BARS DISABLED	0	0
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	1	1
TX_DEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1	1
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS NOT MUXED OUT	0	0
PLL_IBIAS_RD_1 PLL_IBIAS_RD_0	GPIO6 GPIO5	M62/71 BIAS CURRENT FOR PCIe PHY PLL MSBIT (M72S)RSVD M62/71 BIAS CURRENT FOR PCIe PHY PLL LSBIT (M72S)RSVD	0 1	0 0
ROMIDCFG(3:0)	GPIO[13:11:9]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X X	X X X X
VIP_DEVICE_STRAP_ENA	VSUNC	IGNORE VIP DEVICE STRAPS	o NA	o
BIF_VGA_DIS	PSUNC	VGA ENABLED		o
	GPIO8	Reserved		
	GPIO[2:3]	Reserved		
	H2SYNC, V25ENC, GENERICCC	Reserved Reserved Reserved		


PROJECT : NA1
Quanta Computer Inc.

Size	Document Number	Rev
	M7X/66-M_GND / LVDS/ Straps	1A
Date:	Monday, January 15, 2007	Sheet 20 of 53



1.FOR M66M,M71M,M72M,M76M VDDR4 & VDDR5 CAN BE 3.3V OR 1.8V FOR EXT TMD5 ON DV PORT.
 2.FOR M72M & M76M VDDR4 & VDDR5 MUST BE 1.8V IF MULTI GPU ON DV PORT.

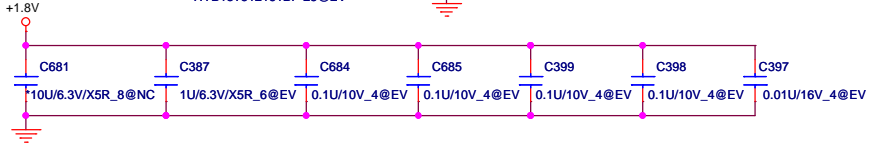
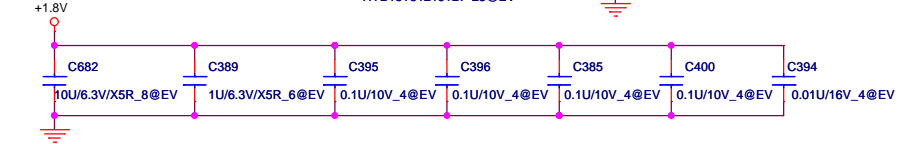
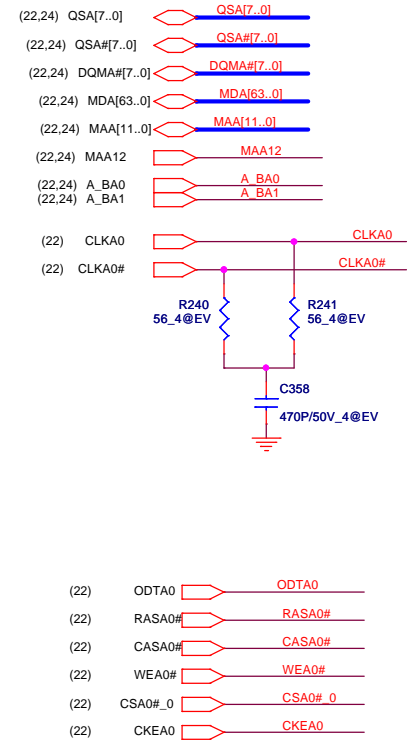
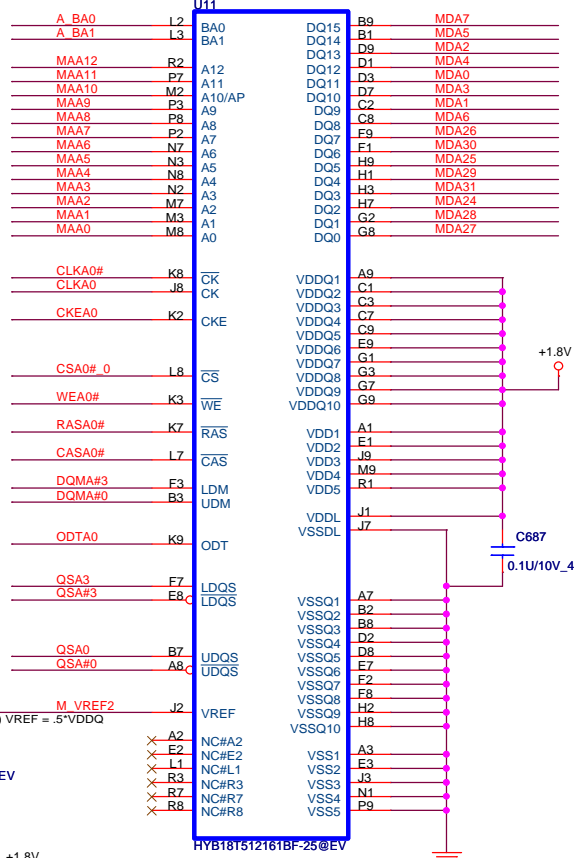
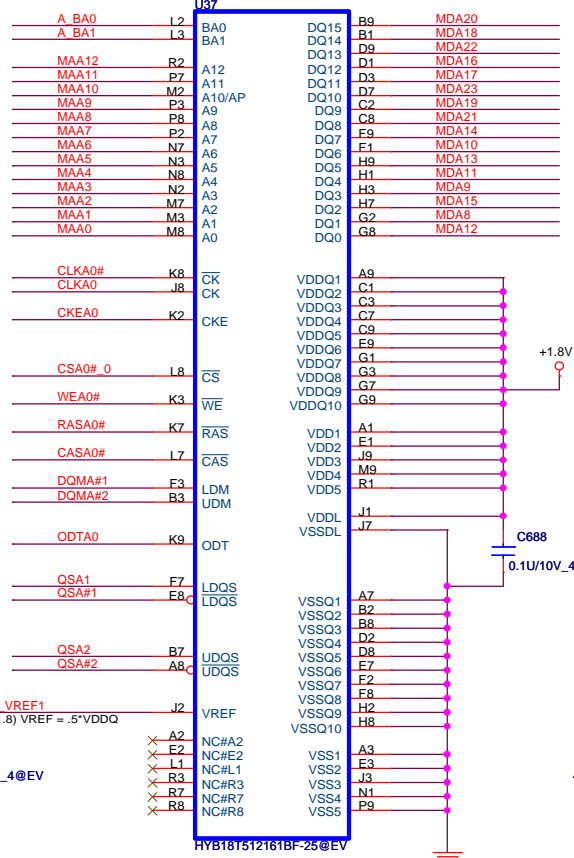
	BBP	BBN
M62S.M71S	NC or VDDC	NC or VSS
M72S	VDDC/1.5V/1.8V(80mA)	VSS/-0.55V/-0.85V(50mA)



PROJECT : NA1
Quanta Computer Inc.

Size	Document Number	Rev
M7X86-M Power_and_NC	M7X86-M Power_and_NC	1A
Date	Monday, January 15, 2007	Sheet 21 of 53

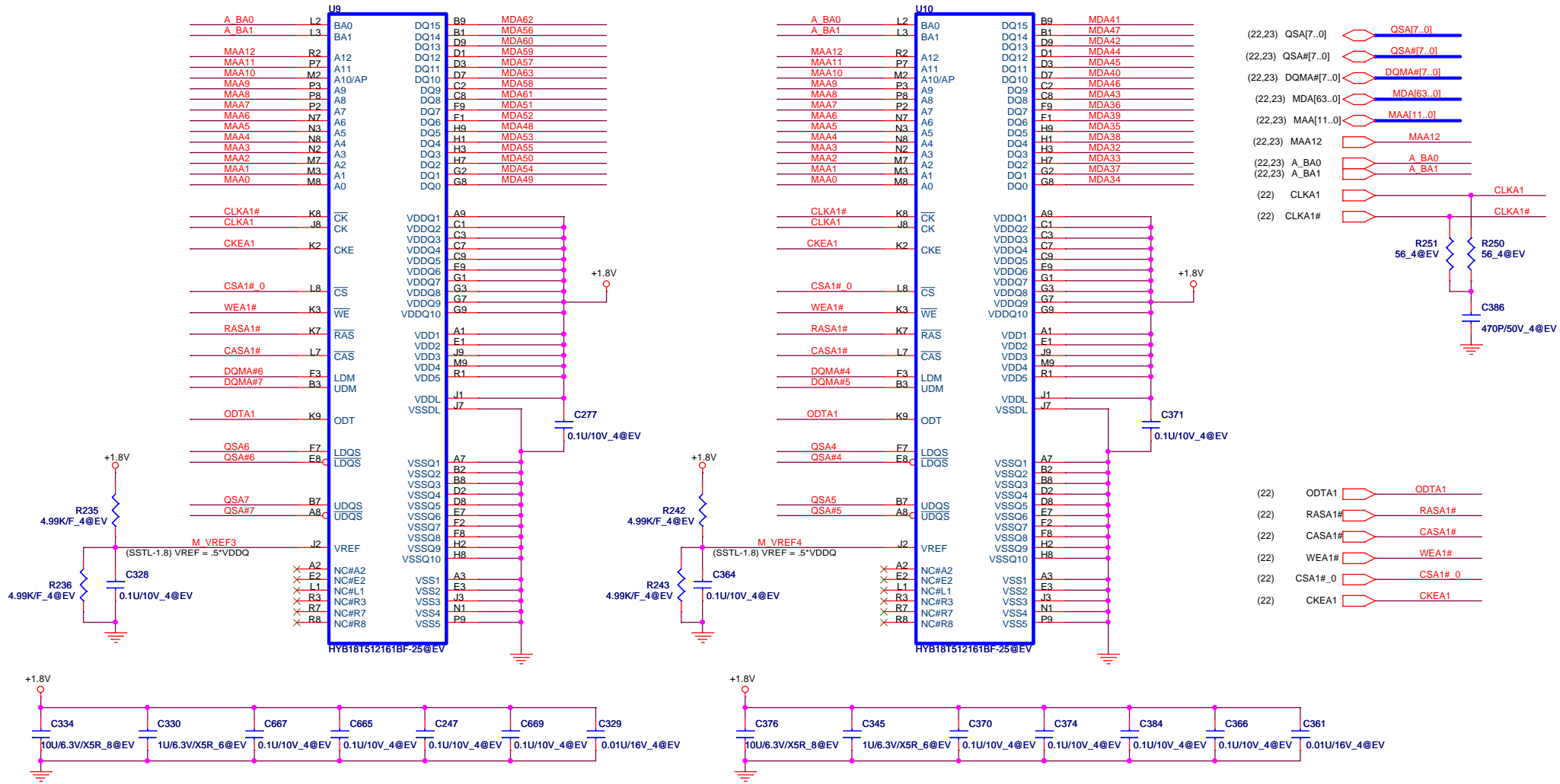
DDR2 BGA MEMORY



PROJECT : NA1
Quanta Computer Inc.

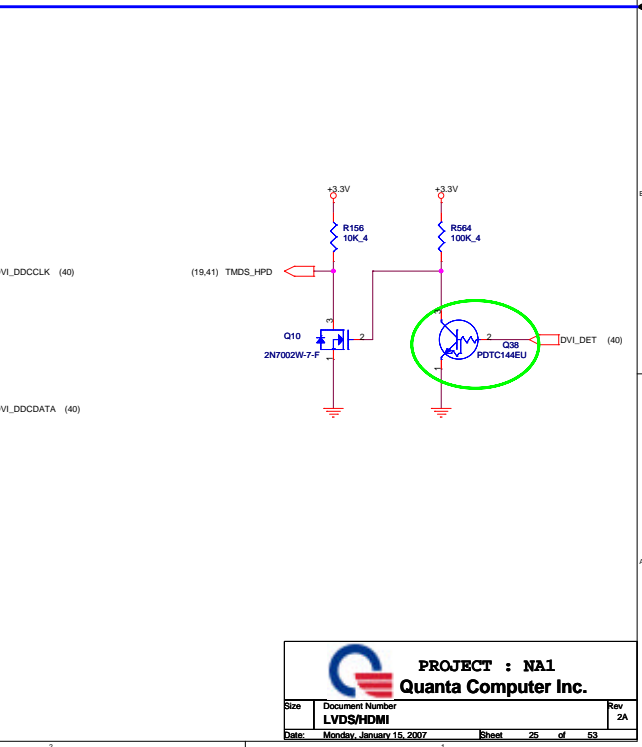
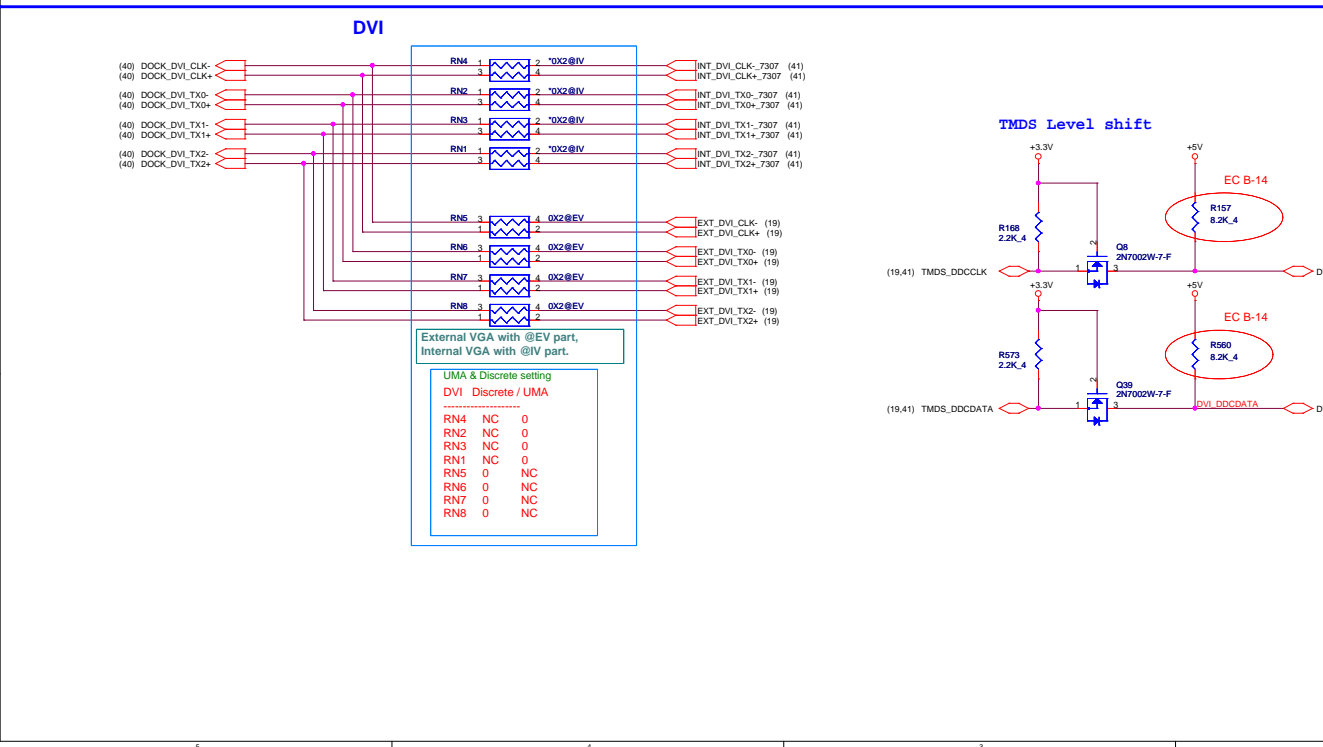
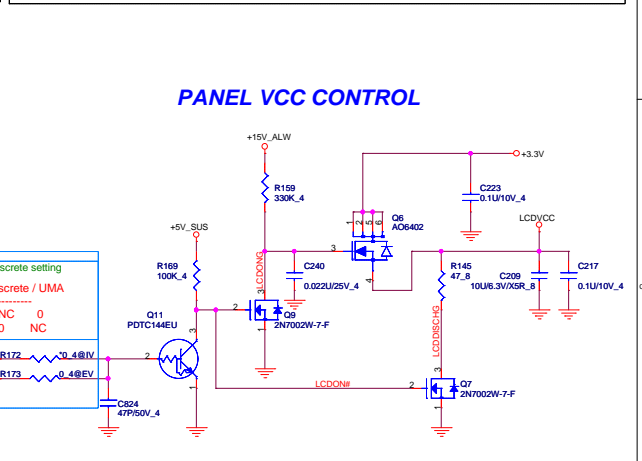
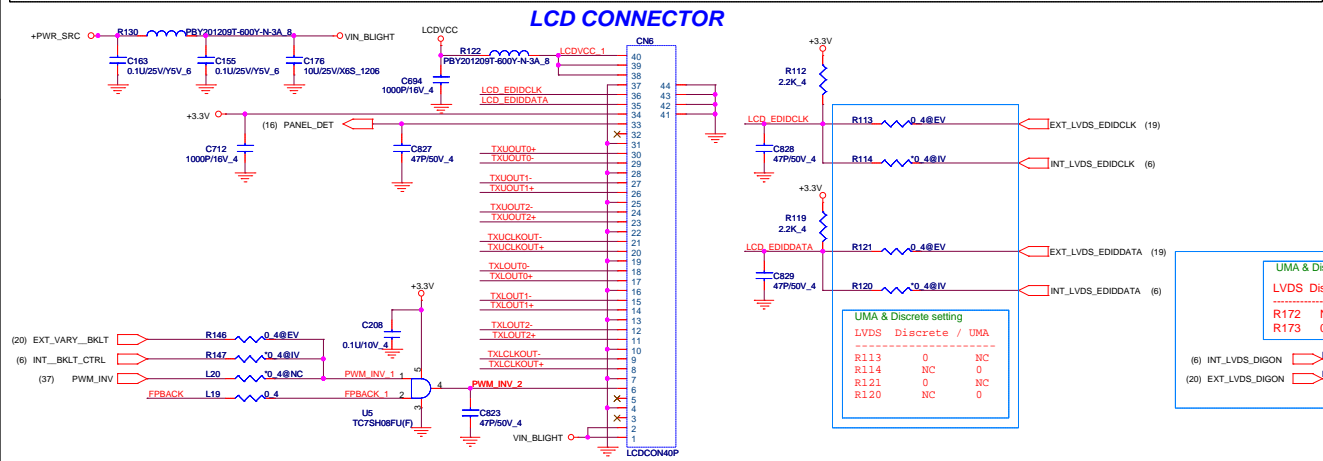
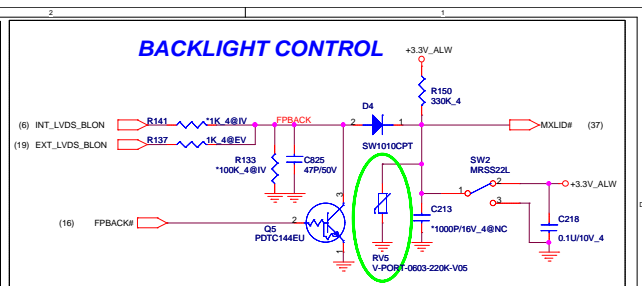
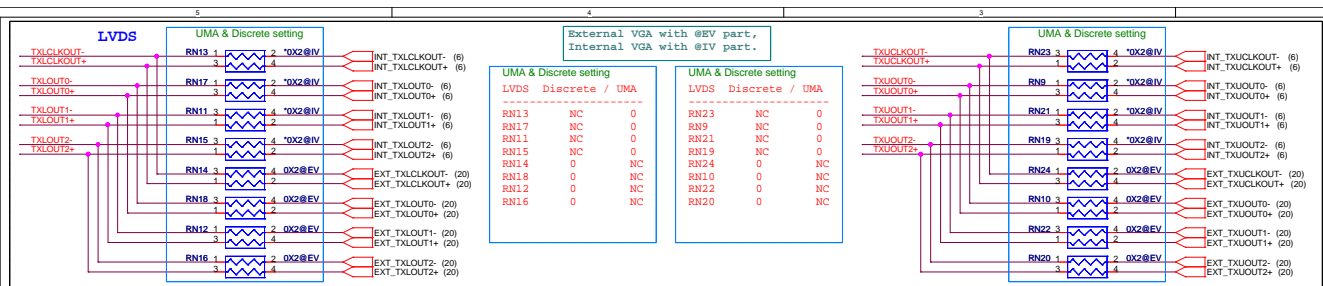
Size	Document Number	Rev
	MEM_A0	1A
Date:	Monday, January 15, 2007	Sheet 23 of 53

DDR2 BGA MEMORY

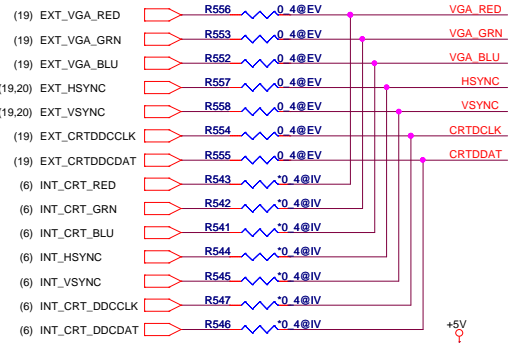


PROJECT : NA1
Quanta Computer Inc.

Size	Document Number	Rev
	MEM_B0	1A
Date:	Monday, January 15, 2007	Sheet 24 of 53



CRT SWITCH

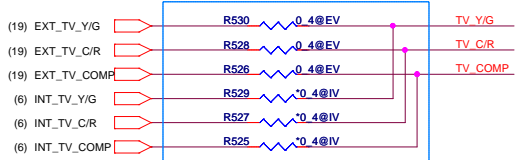
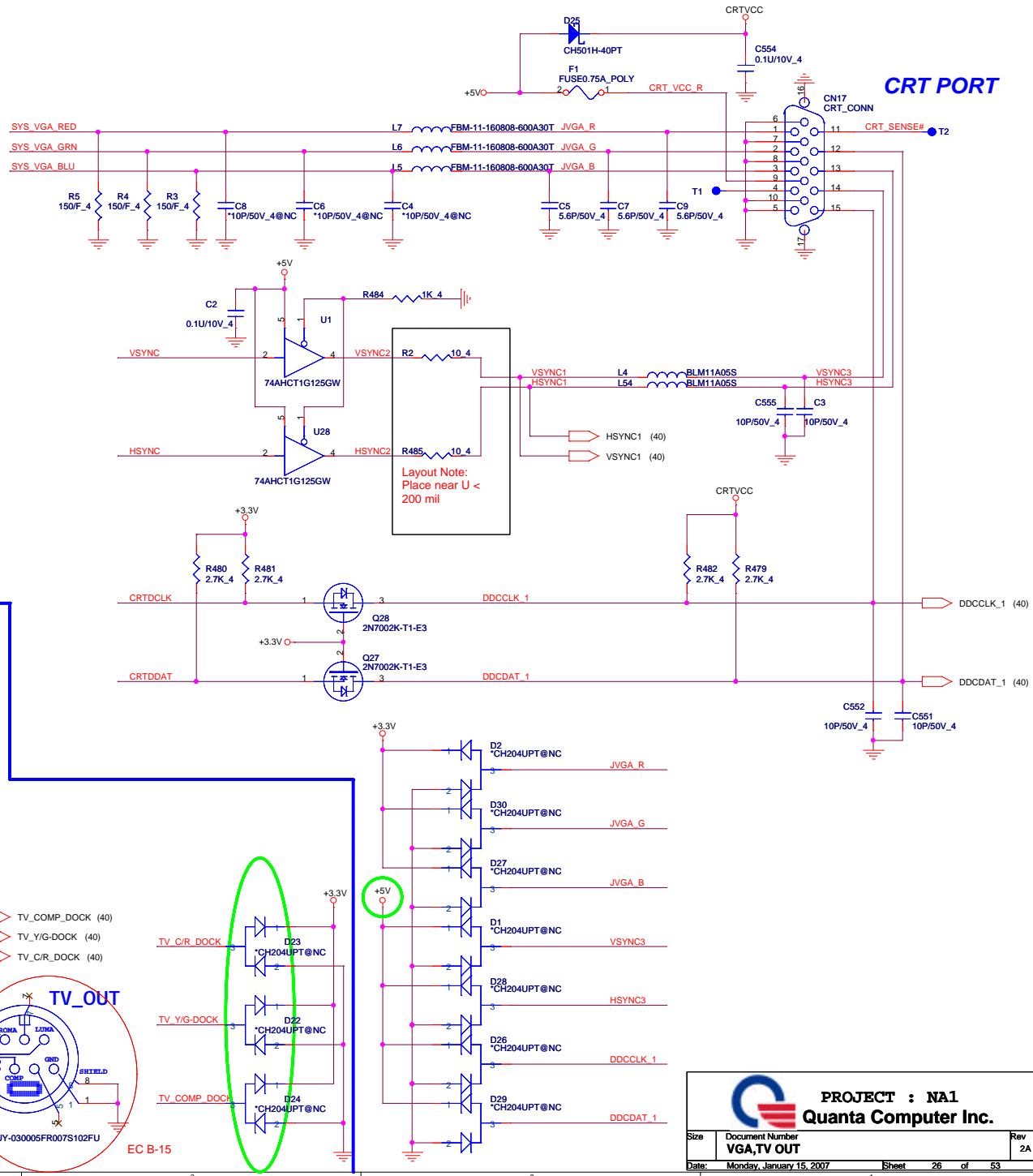


UMA & Discrete setting
LVDS Discrete / UMA

R536	0	NC
R533	0	NC
R552	0	NC
R557	0	NC
R558	0	NC
R554	0	NC
R555	0	NC
R543	NC	0
R542	NC	0
R541	NC	0
R544	NC	0
R545	NC	0
R547	NC	0
R546	NC	0

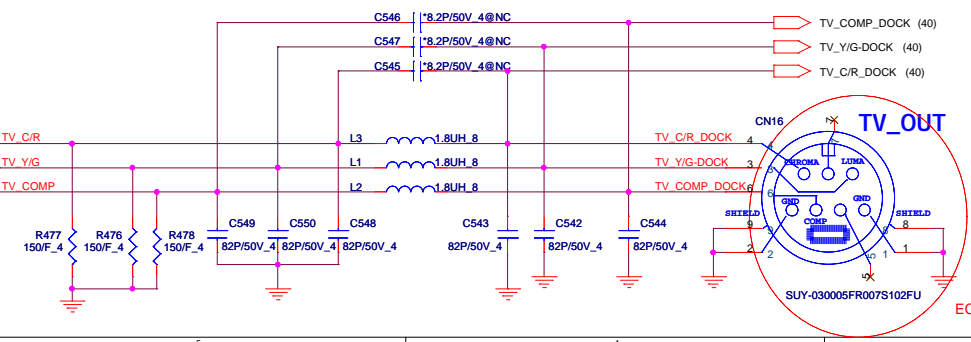
SEL	FUNCTION(COM)
LOW	IN_x0
HIGH	IN_x1

CRT PORT



UMA & Discrete setting
LVDS Discrete / UMA

R530	0	NC
R528	0	NC
R526	0	NC
R529	NC	0
R527	NC	0
R525	NC	0



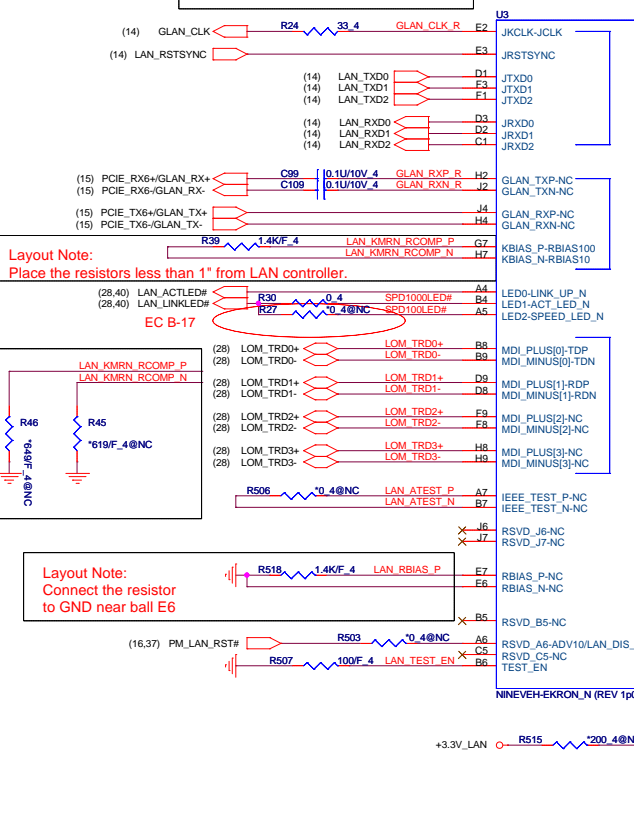
PROJECT : NA1
Quanta Computer Inc.

Size	Document Number	Rev
Date: Monday, January 15, 2007	VGA, TV OUT	2A
Sheet	26	of 53

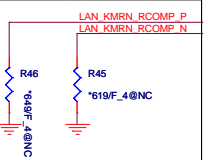
LAN

JKCLK Pin	0MHz
Power down	5MHz
10Mbps	50MHz
100Mbps	62.5MHz
1000Mbps	

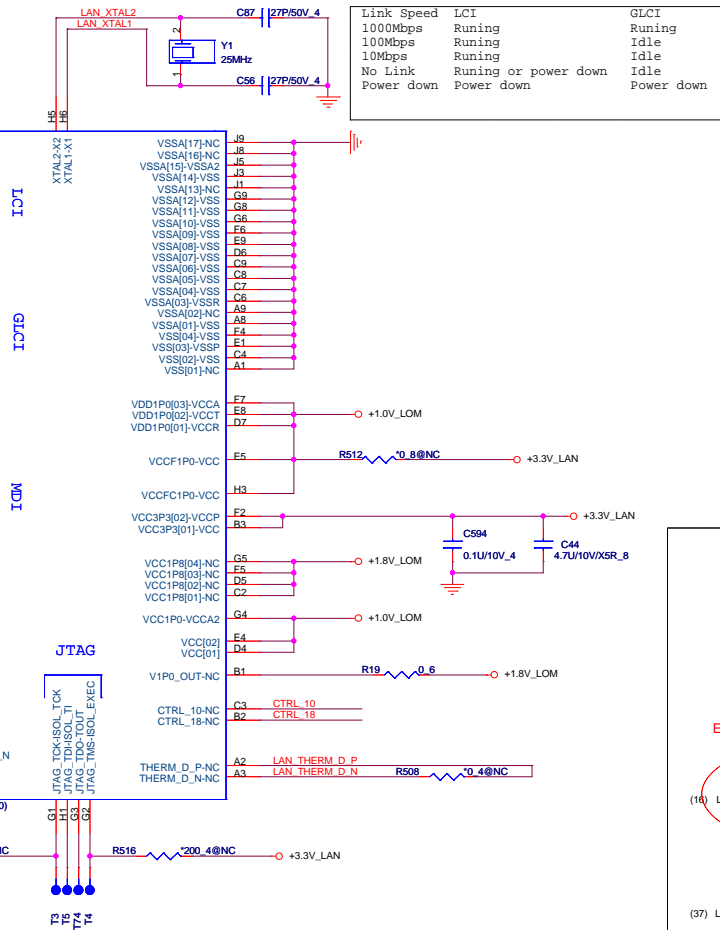
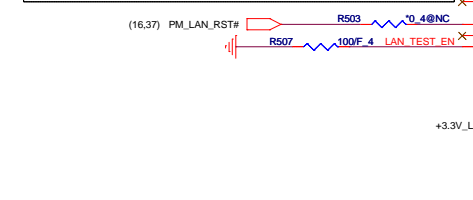
Layout Note:
Place series resistor close to LAN controller.



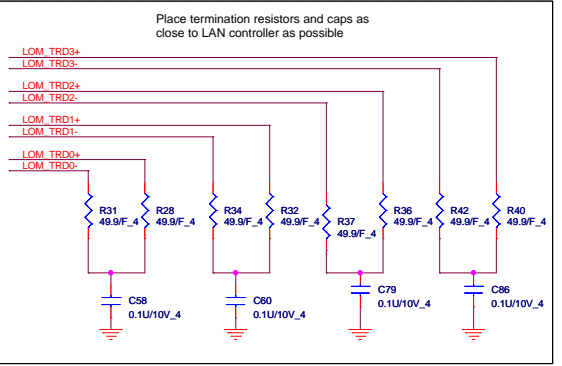
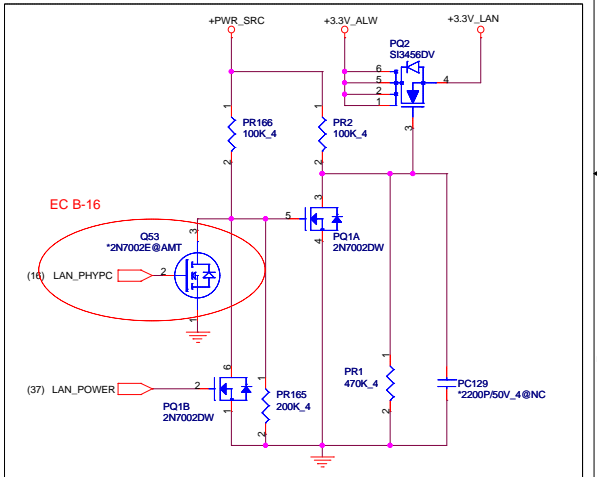
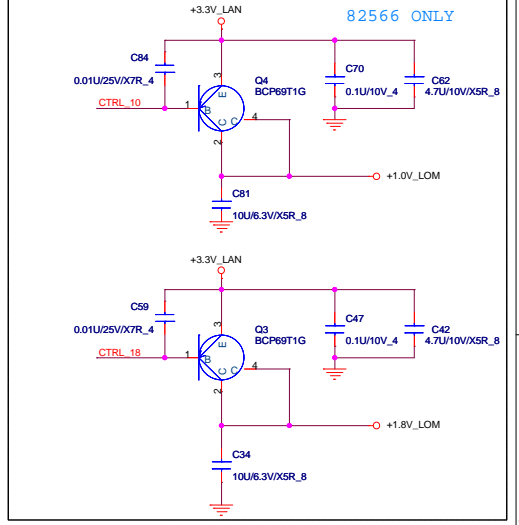
Layout Note:
Place the resistors less than 1" from LAN controller.



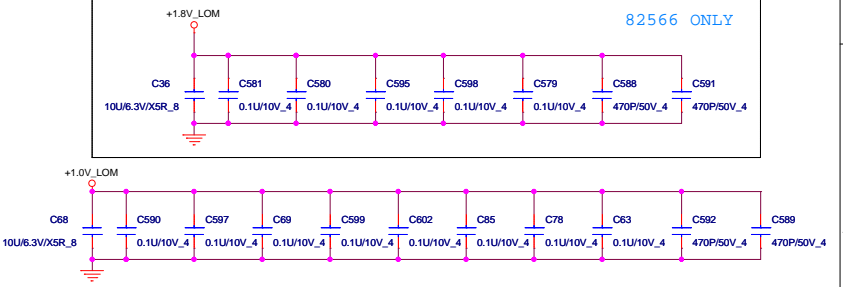
Layout Note:
Connect the resistor to GND near ball E6

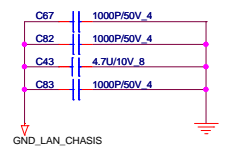
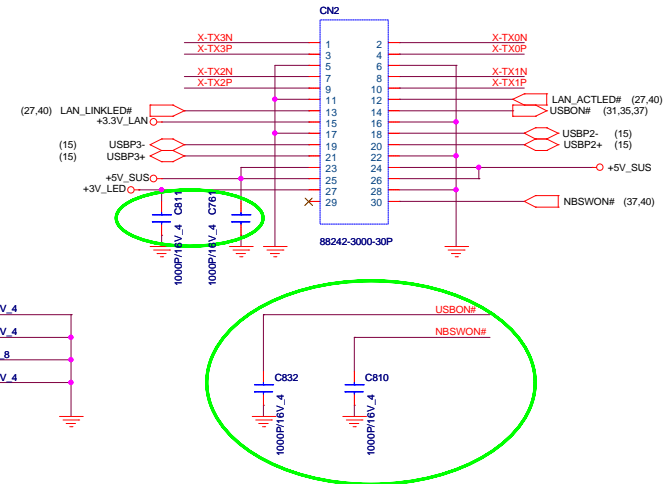
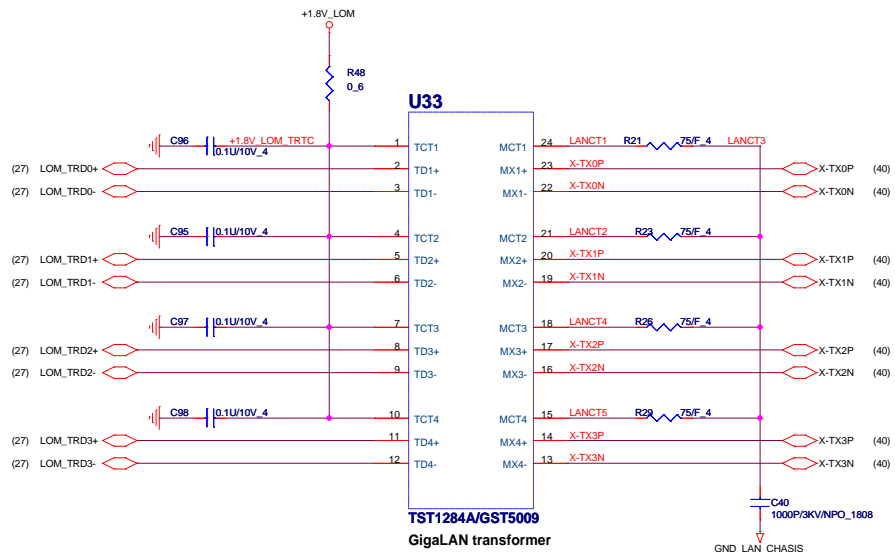


Link Speed	LCI	GLCI
1000Mbps	Running	Running
100Mbps	Running	Idle
10Mbps	Running	Idle
No Link	Running or power down	Idle
Power down	Power down	Power down



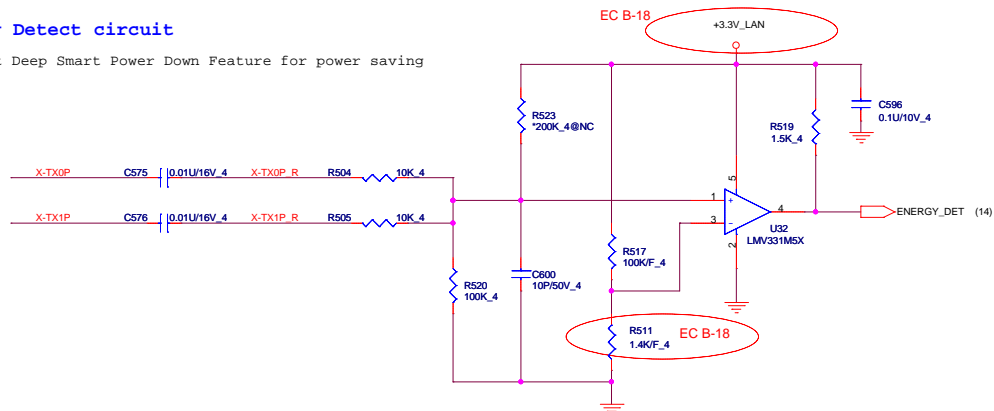
Place termination resistors and caps as close to LAN controller as possible

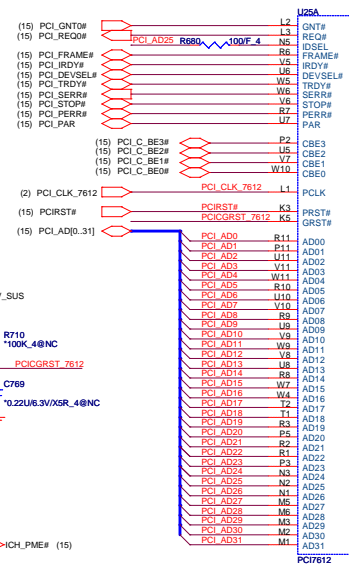
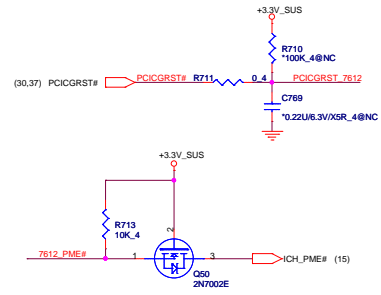
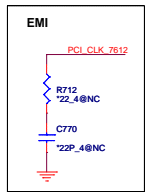




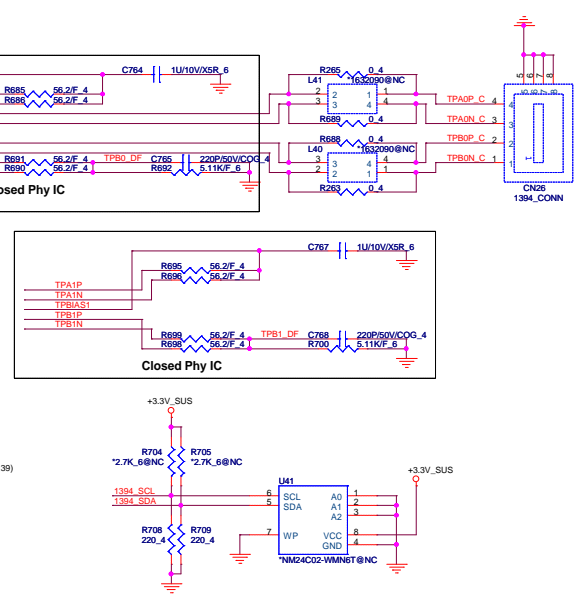
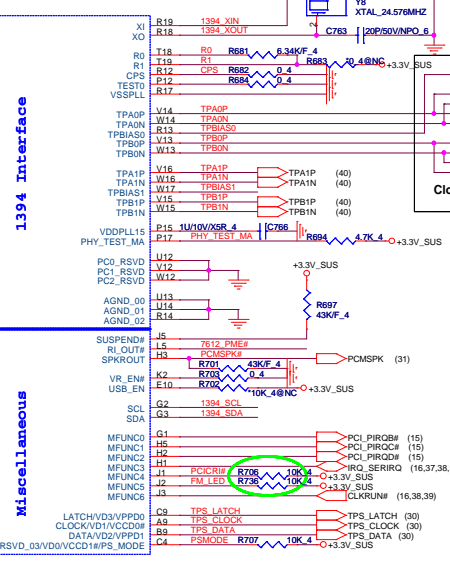
LAN Energy Detect circuit

82556 Support Deep Smart Power Down Feature for power saving

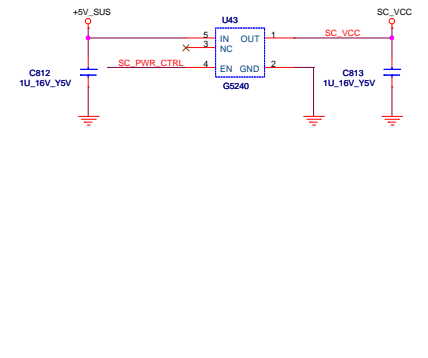
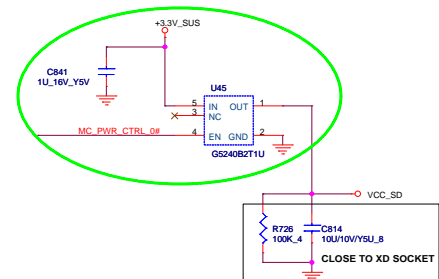
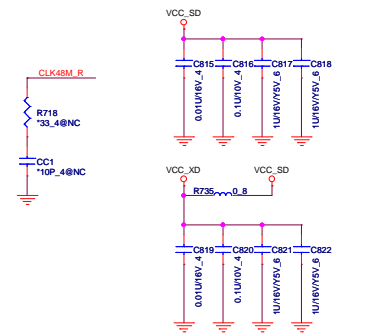
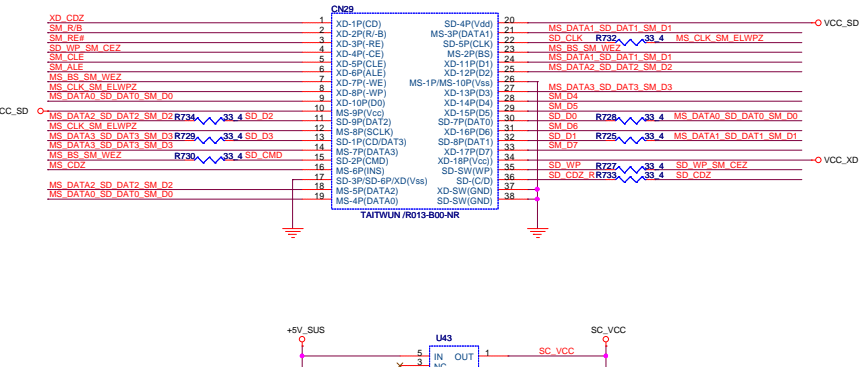
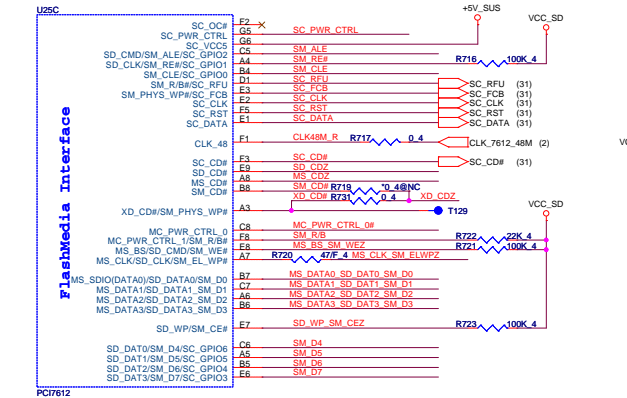


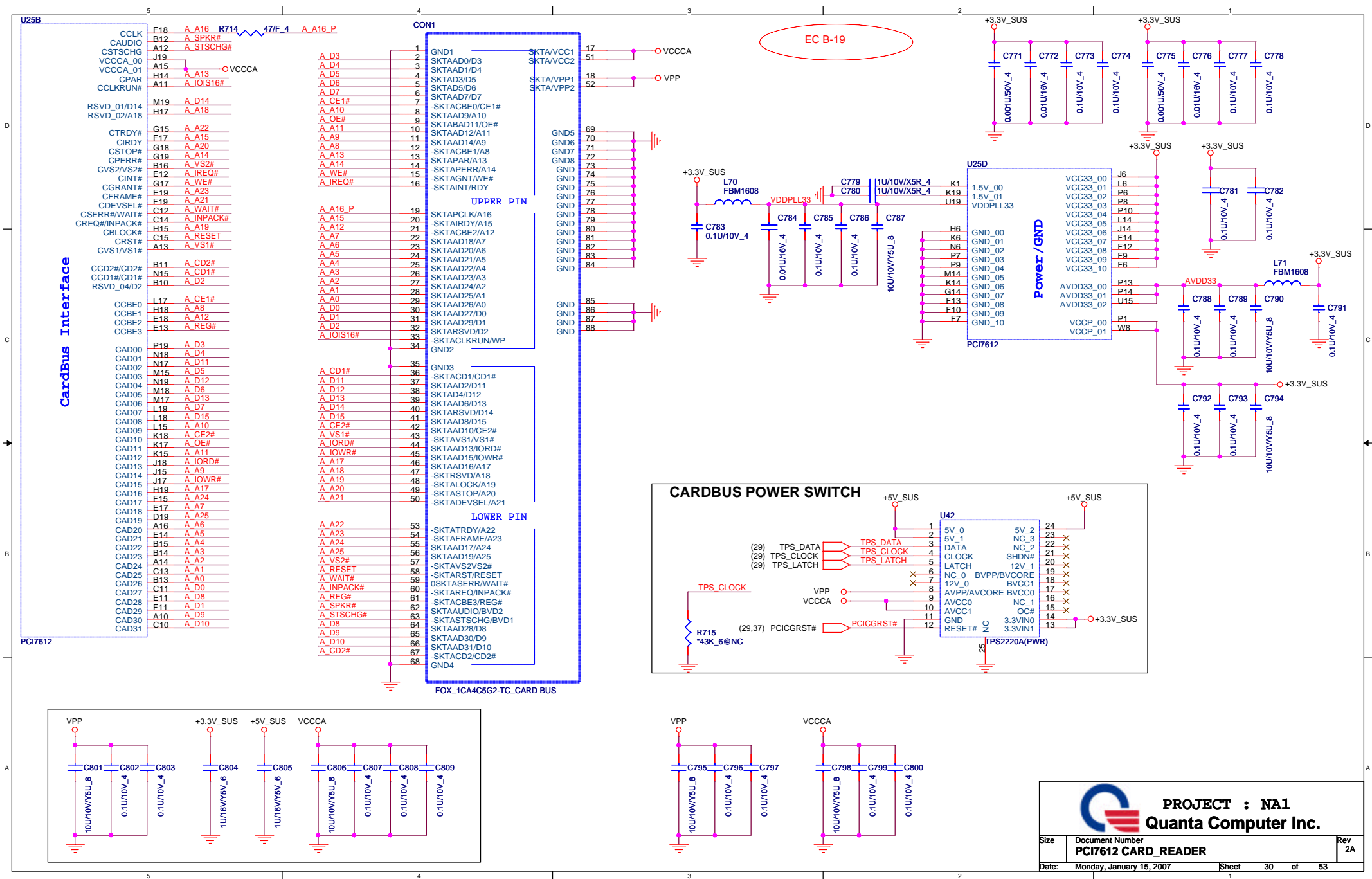


PCI Interface
Miscellaneous



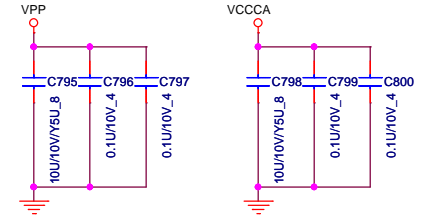
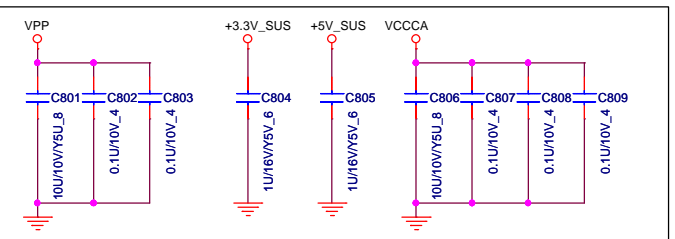
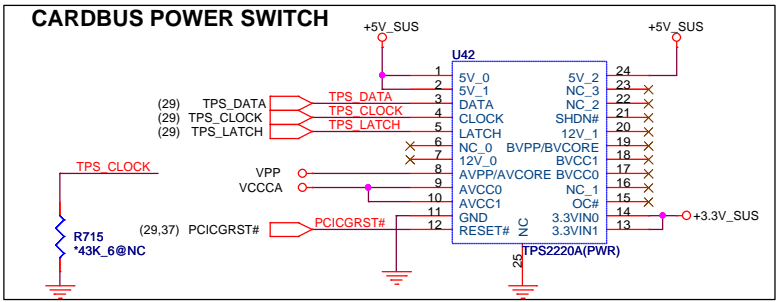
4 IN1 CARD READER Supporting MMC/SD/MS/XD Cards





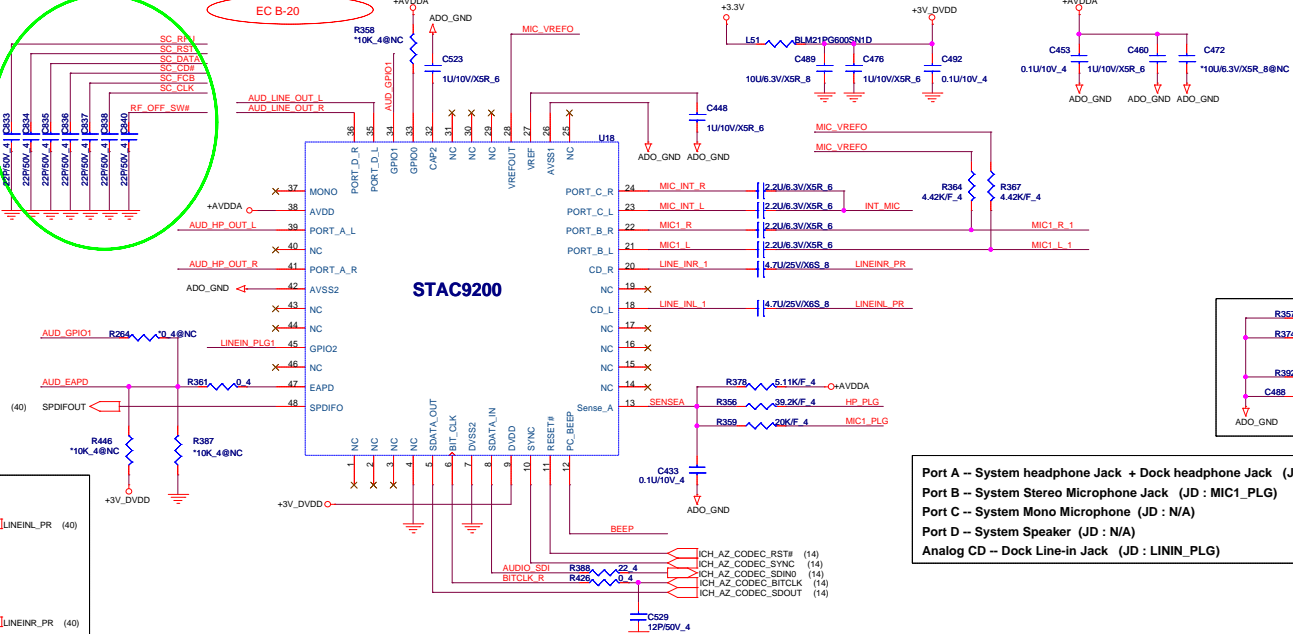
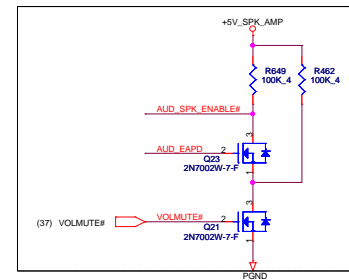
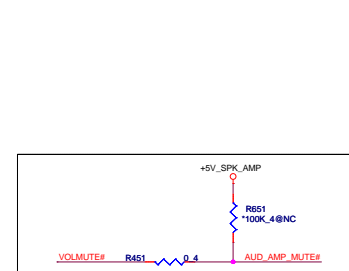
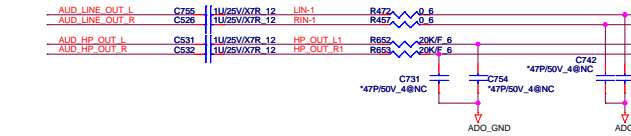
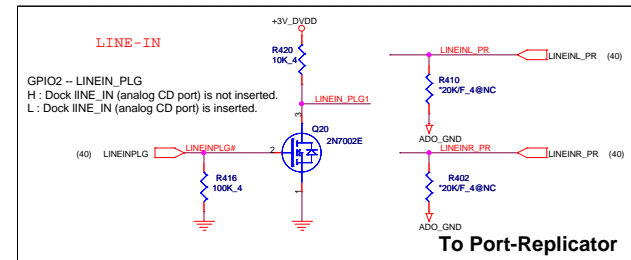
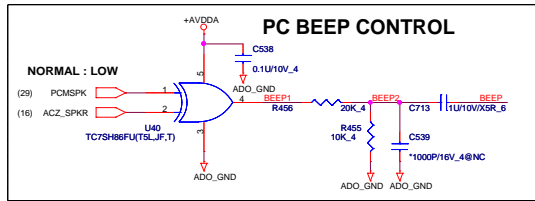
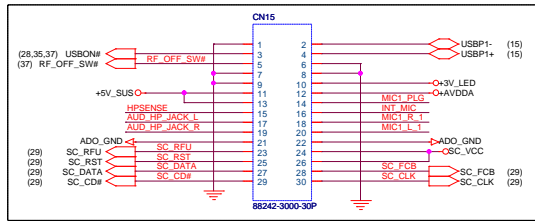
EC B-19

CardBus Interface

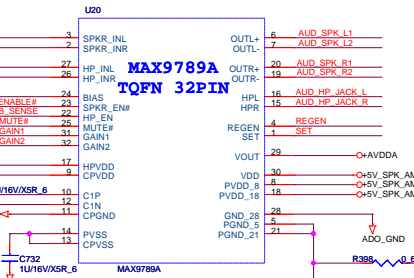


PROJECT : NA1
Quanta Computer Inc.

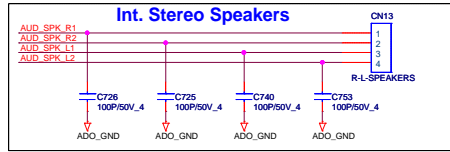
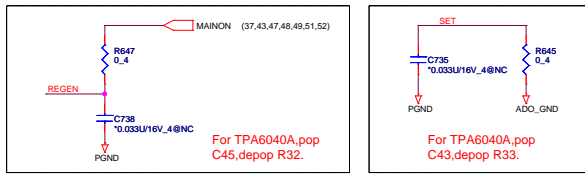
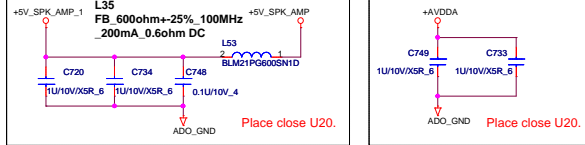
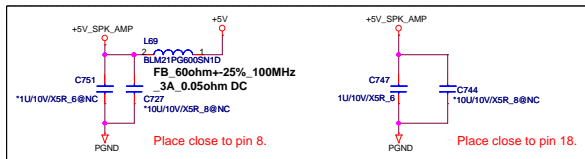
Size	Document Number	Rev
	PCI7612_CARD_READER	2A
Date:	Monday, January 15, 2007	Sheet 30 of 53



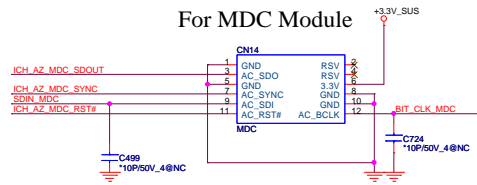
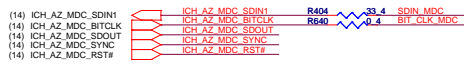
AUDIO AMPLIFIER

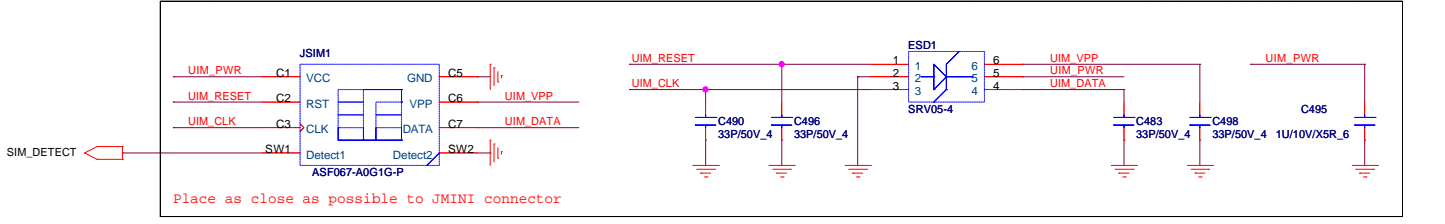
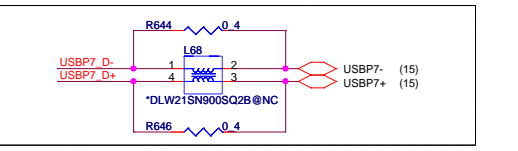
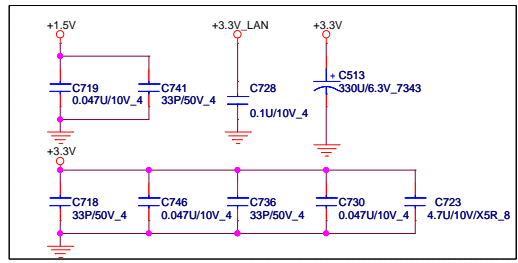
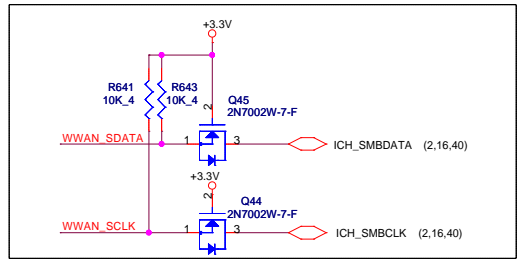
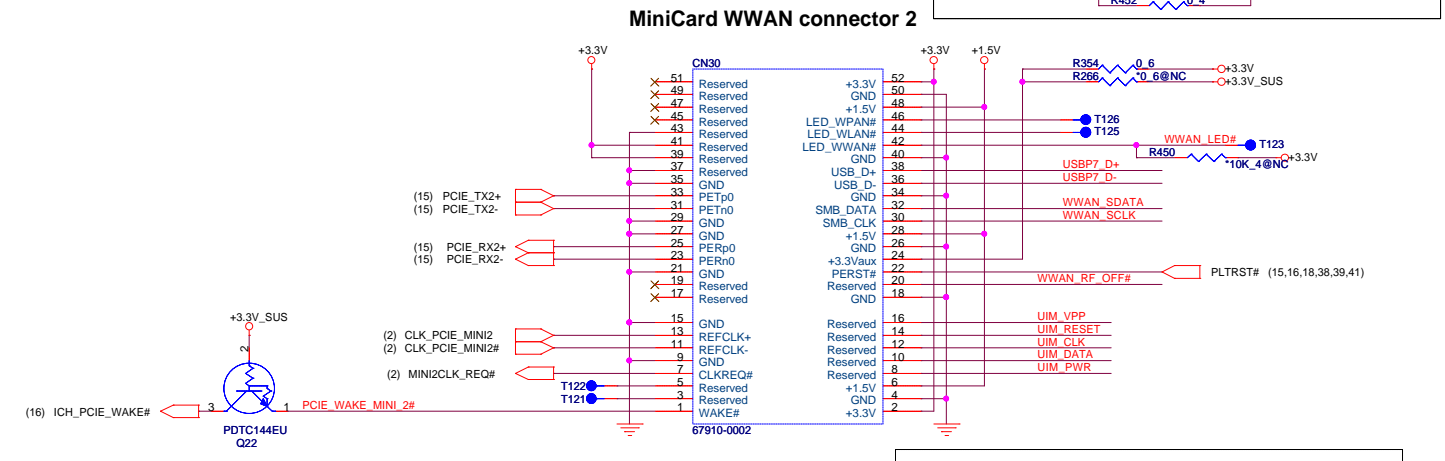
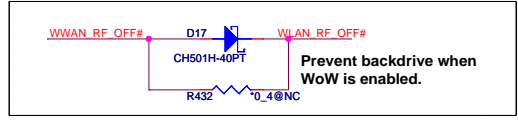
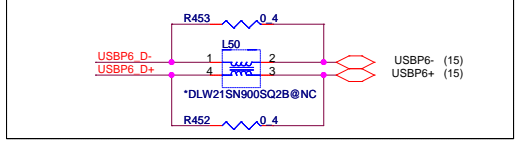
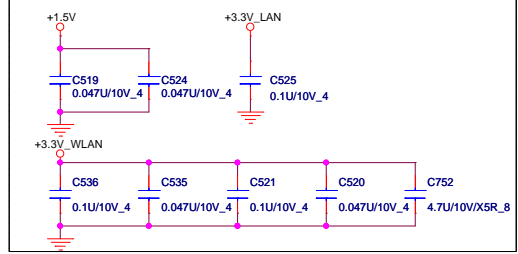
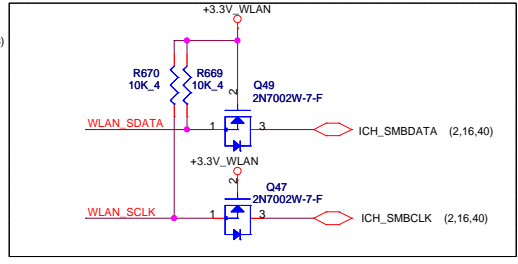
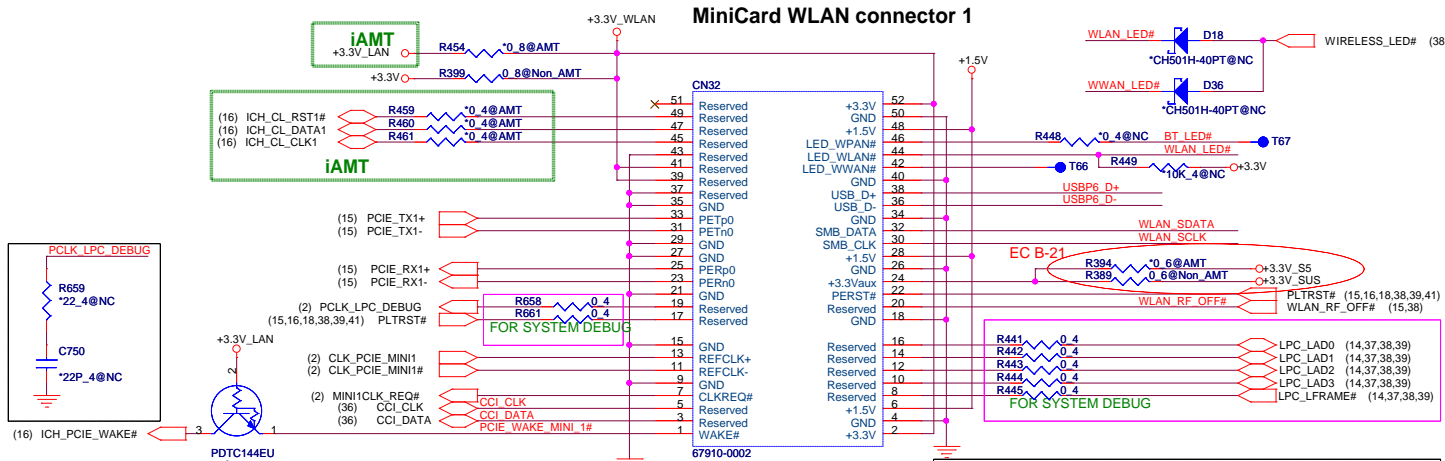


Port A -- System headphone Jack + Dock headphone Jack (JD : HP_PLG)
 Port B -- System Stereo Microphone Jack (JD : MIC1_PLG)
 Port C -- System Mono Microphone (JD : N/A)
 Port D -- System Speaker (JD : N/A)
 Analog CD -- Dock Line-in Jack (JD : LININ_PLG)

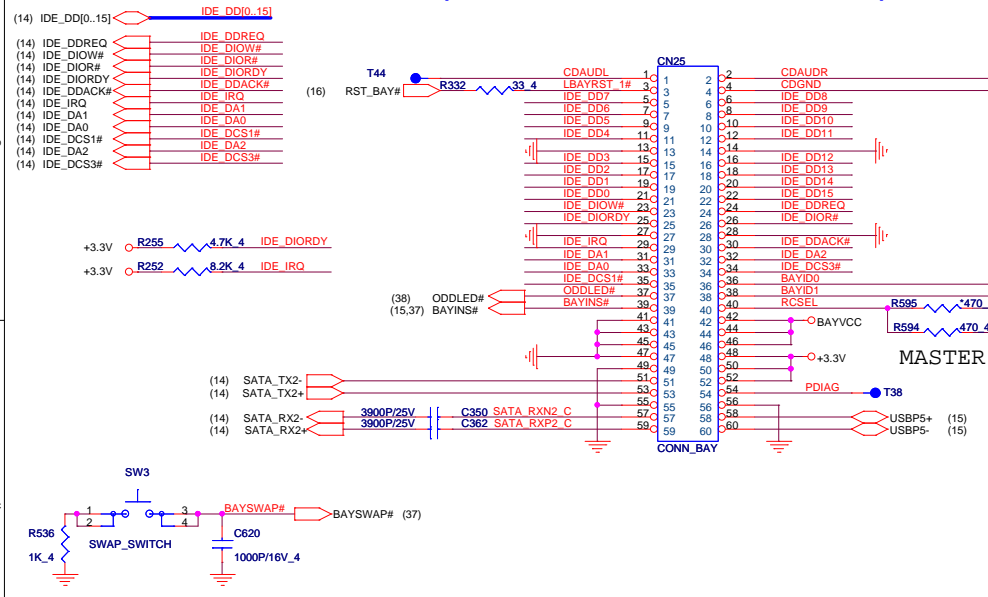


GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB





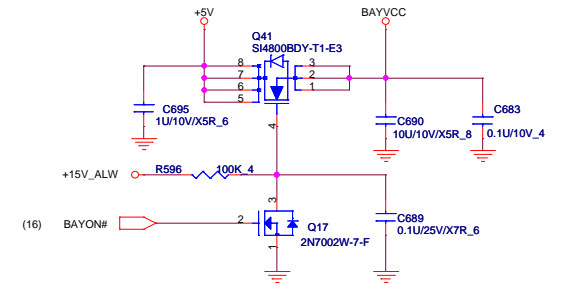
LEFT BAY(CD-ROM, HDD-PATA/SATA, FDD,)



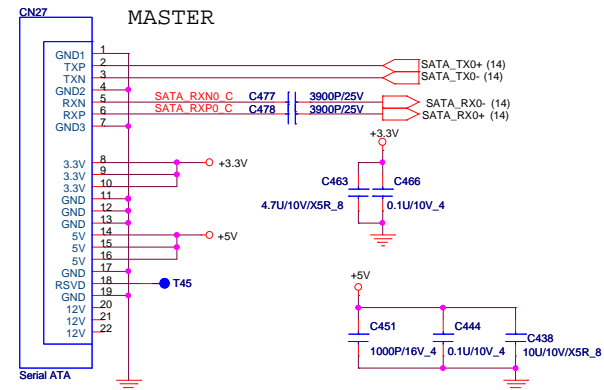
LBAY ID STATUS

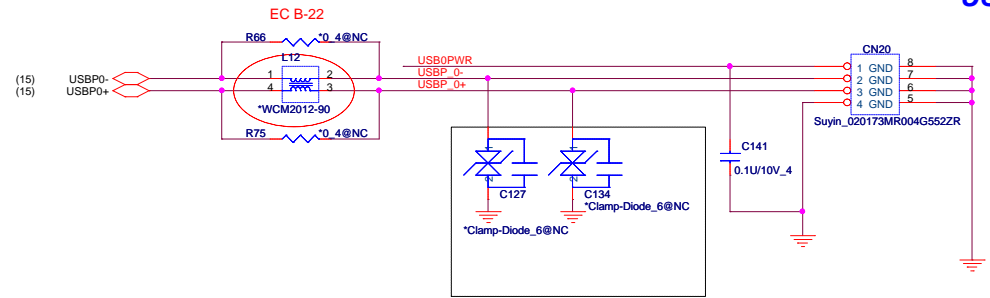
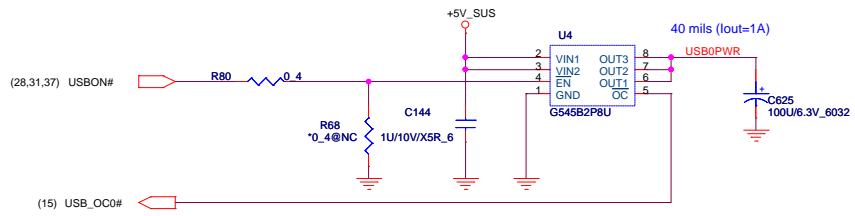
LEFT BAYID1	LEFT BAYID0	STATUS
0	0	HDD (PATA)
0	1	ODD
1	0	HDD (SATA)
1	1	Reserve

BAY POWER CONTROL

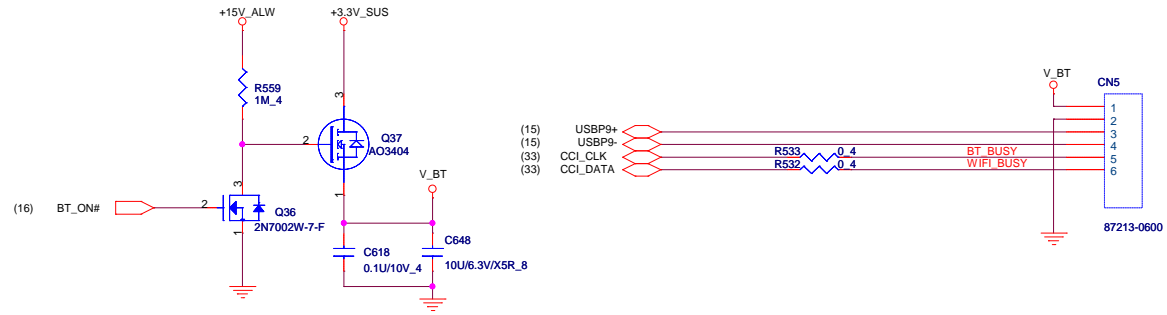


SATA CONNECTOR





BLUETOOTH CONNECTOR

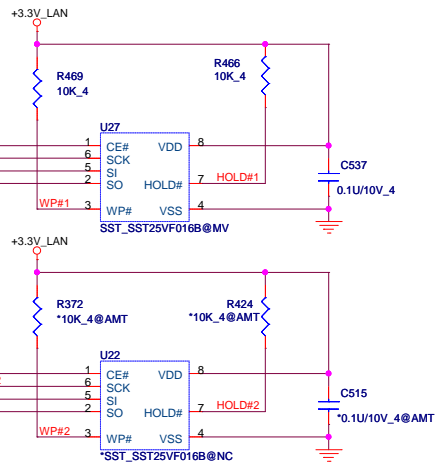


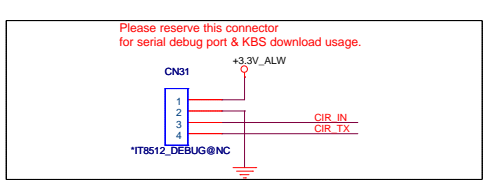
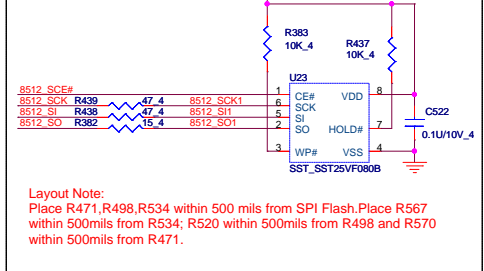
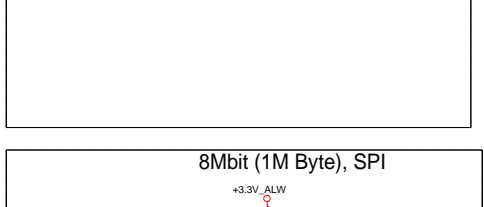
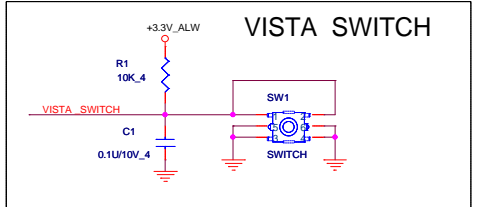
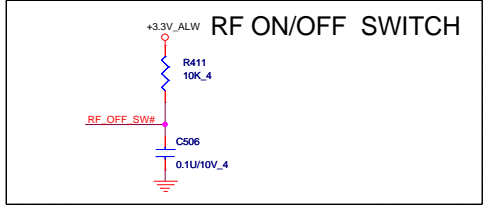
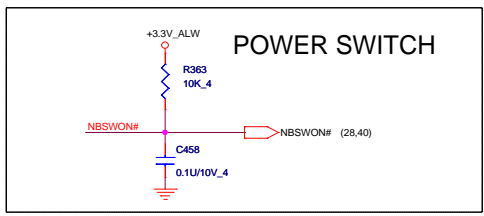
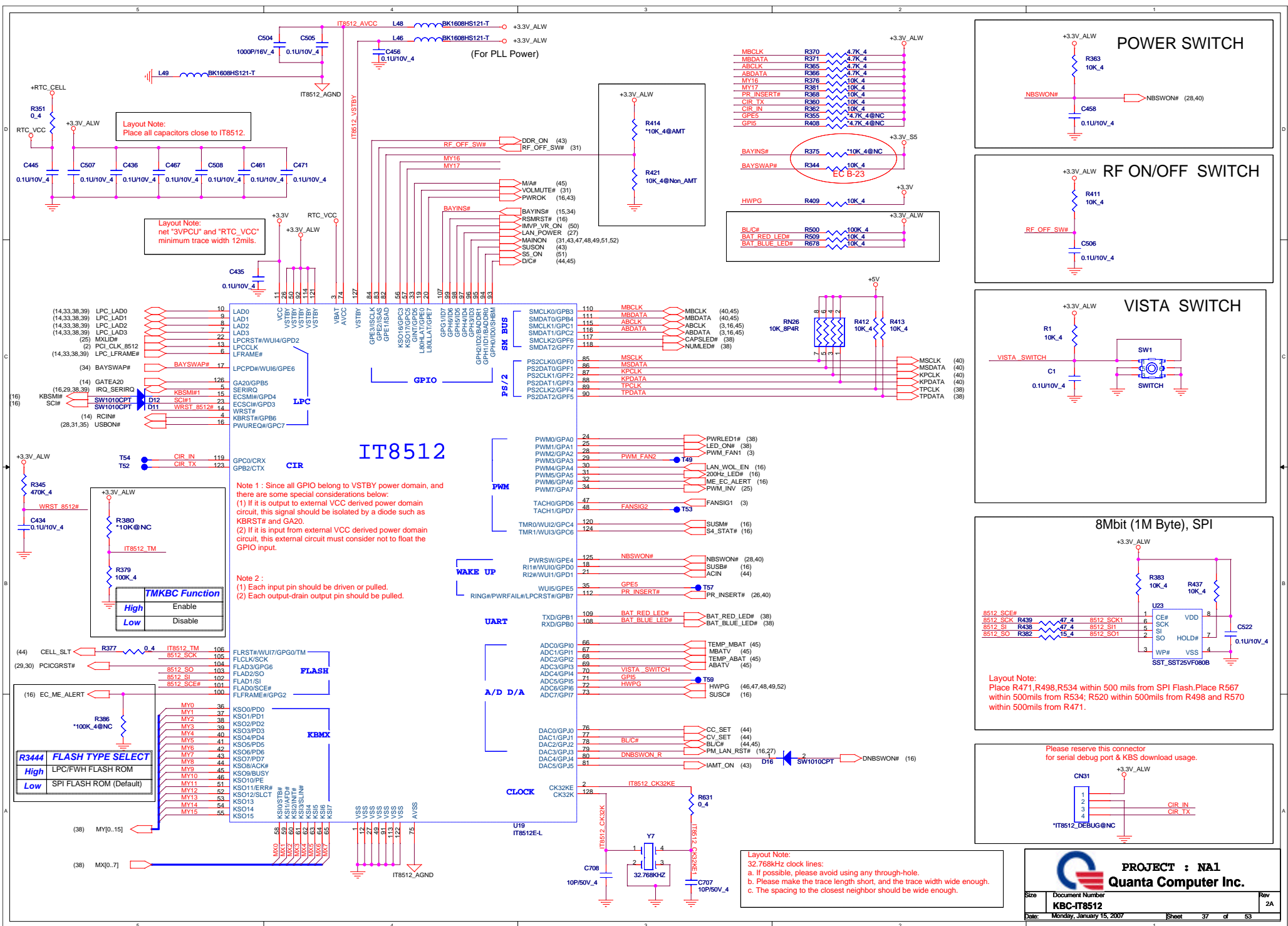
16Mbit (2M Byte), SPI iAMT

Layout Note:
 Place R471,R498,R534 within 500 mils from SPI
 Flash. Place R567 within 500mils from R534;
 R520 within 500mils from R498 and R570 within
 500mils from R471.

- (15) ICH_SPI_CS0#
- (15) ICH_SPI_CLK
- (15) ICH_SPI_DIN
- (15) ICH_SPI_DO

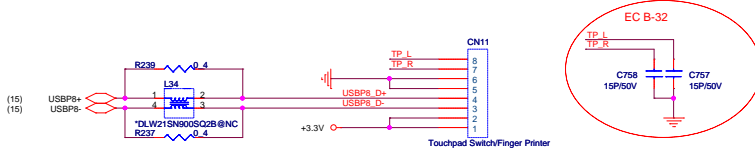
- (15) ICH_SPI_CS1#



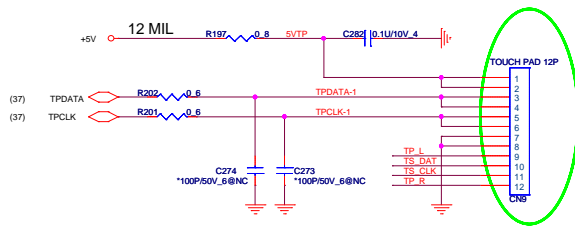


Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.

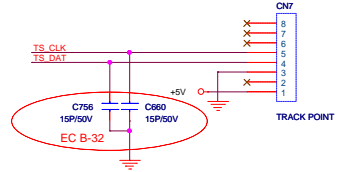
TOUCHPAD Switch / FINGER PRINT CONN



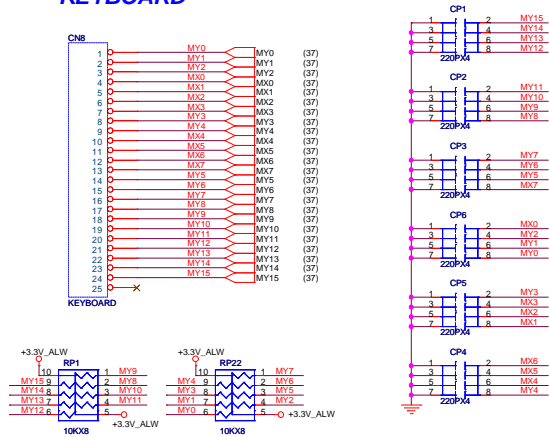
TOUCHPAD CONN



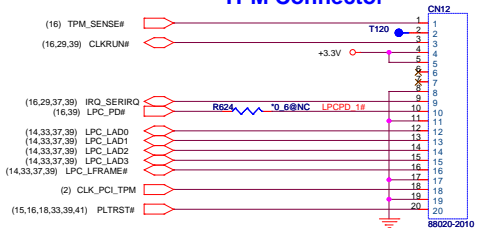
TRACK POINT



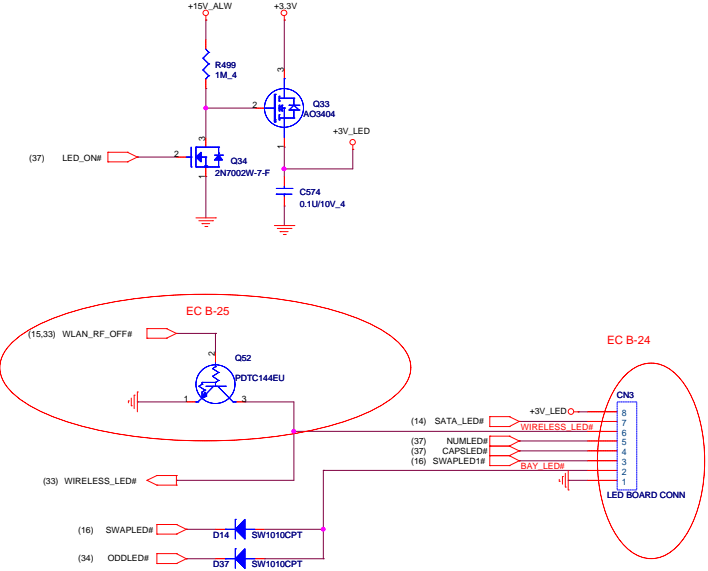
KEYBOARD



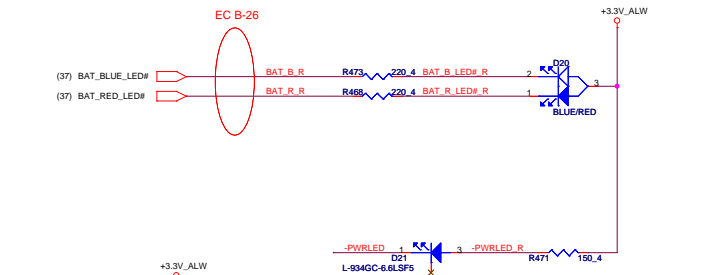
TPM Connector



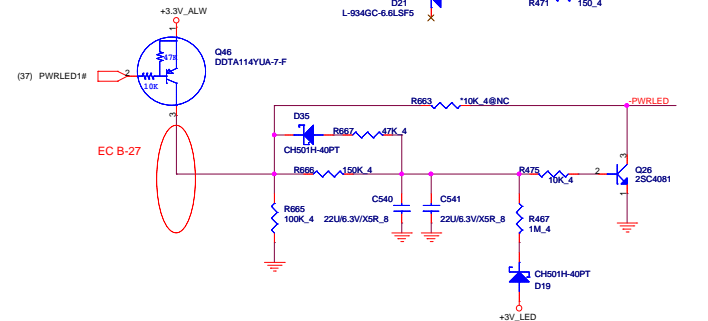
LED INDIACTOR



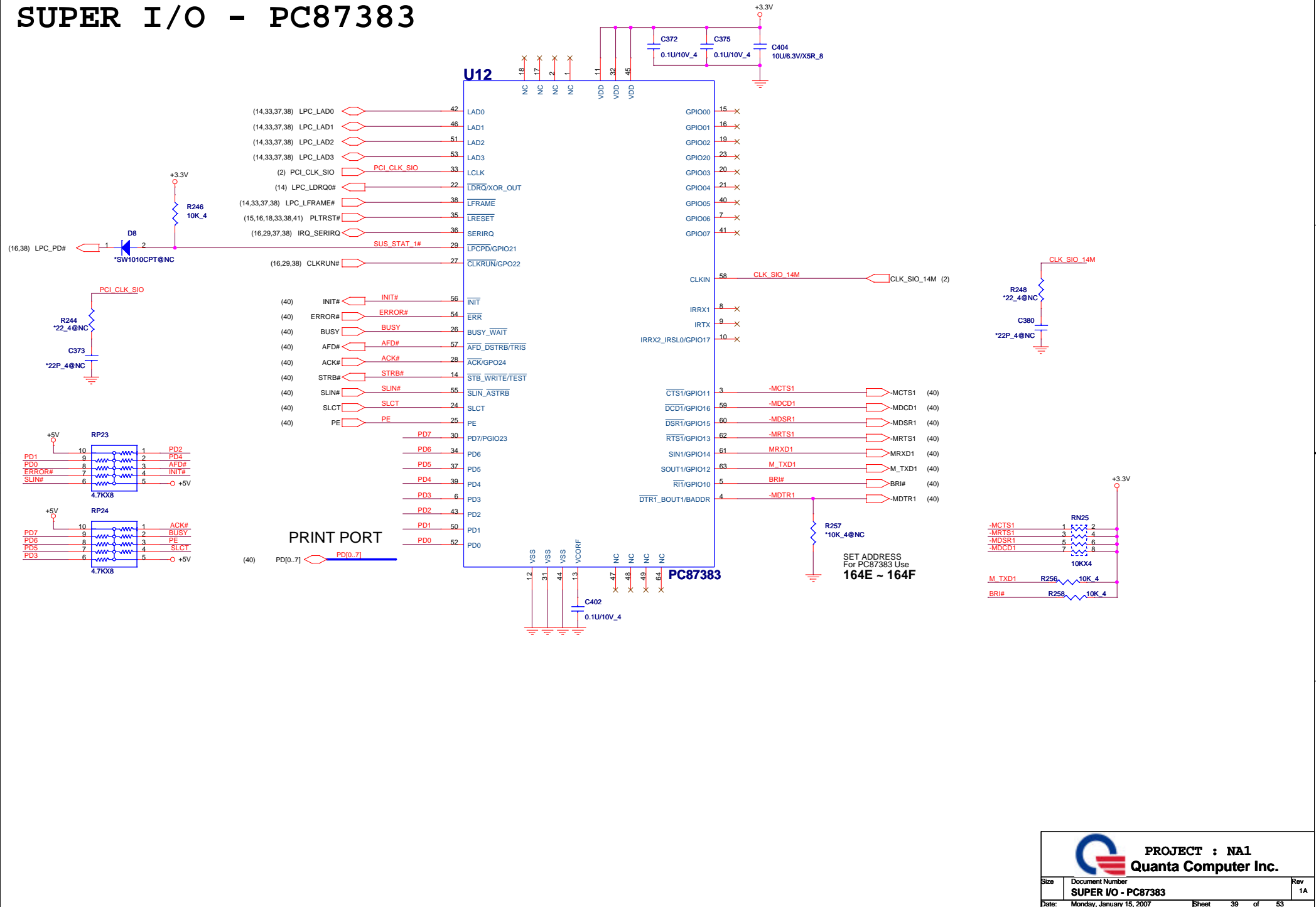
EC B-26

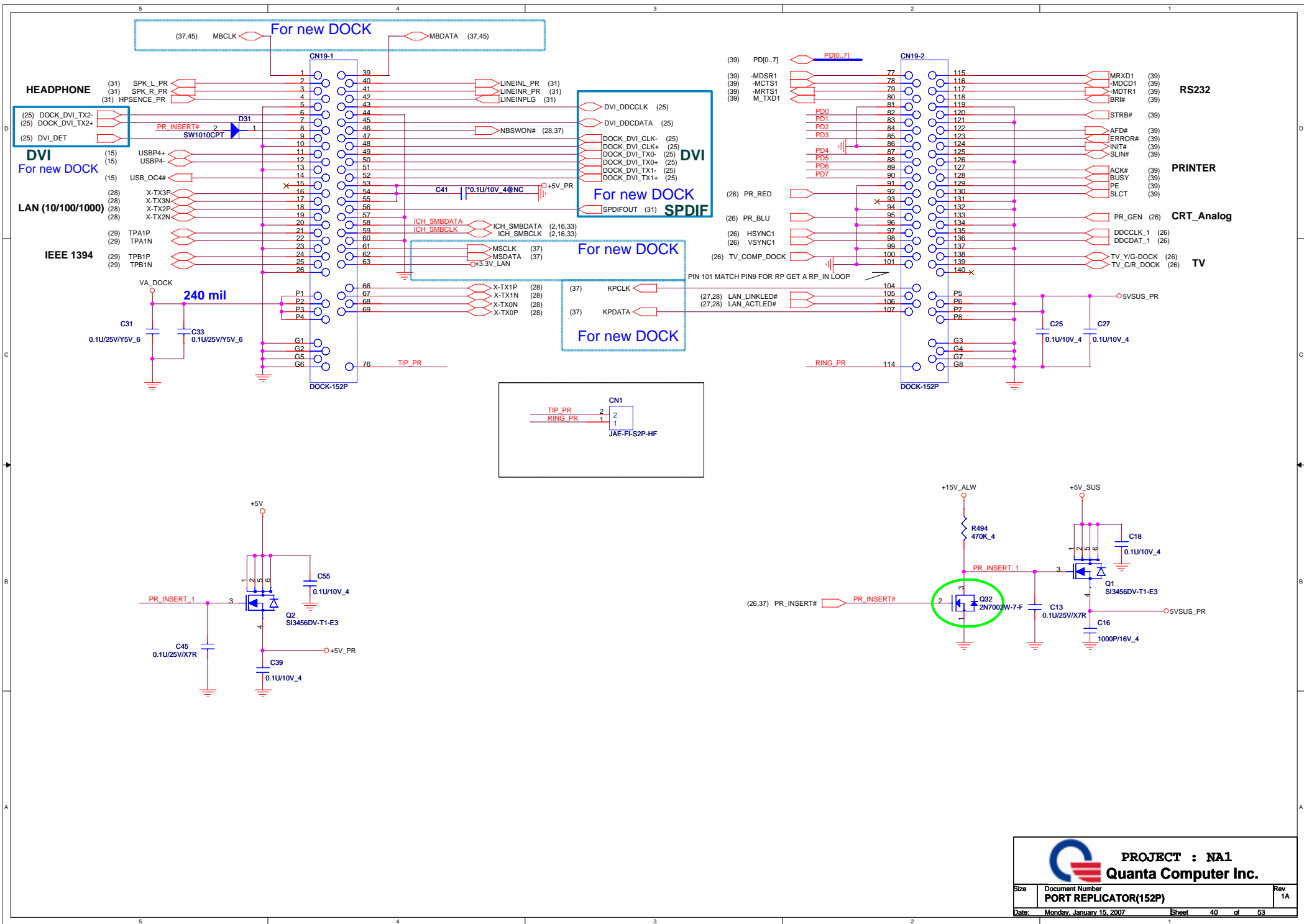


EC B-27

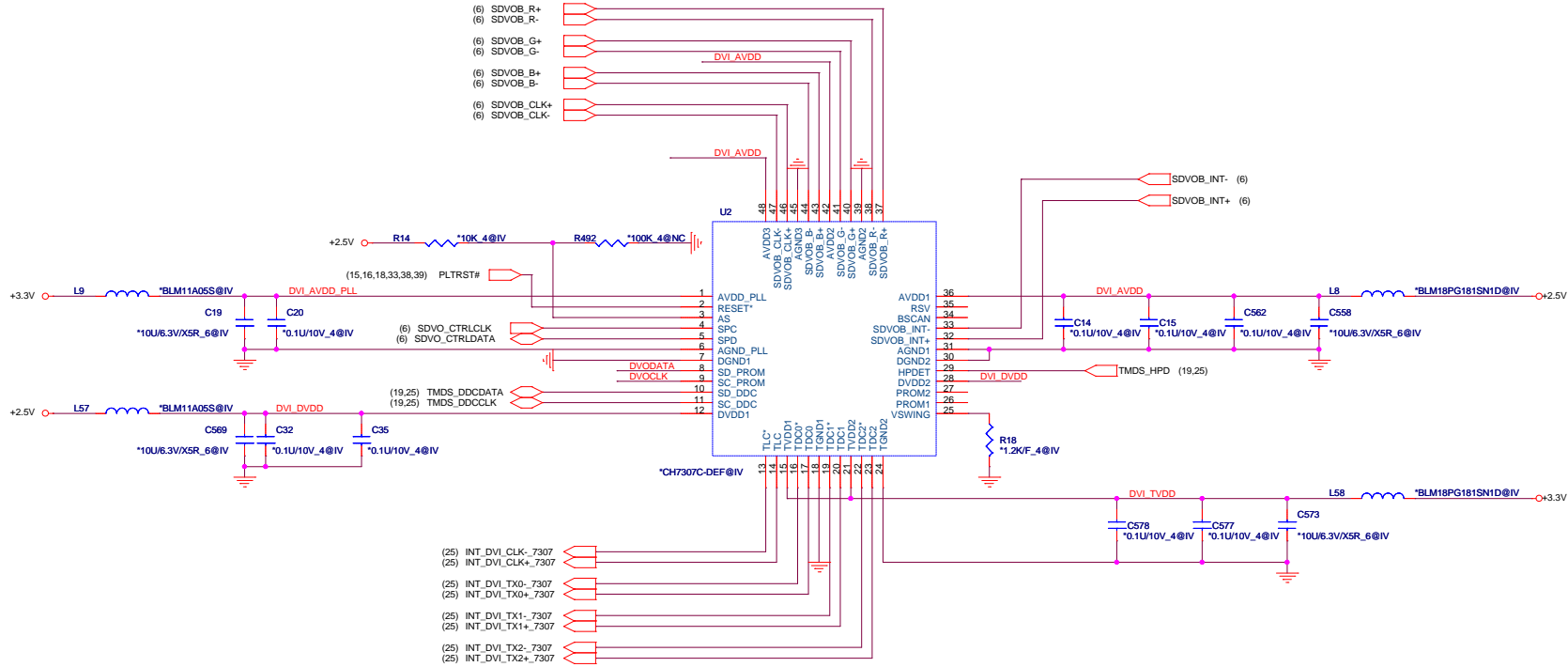


SUPER I/O - PC87383

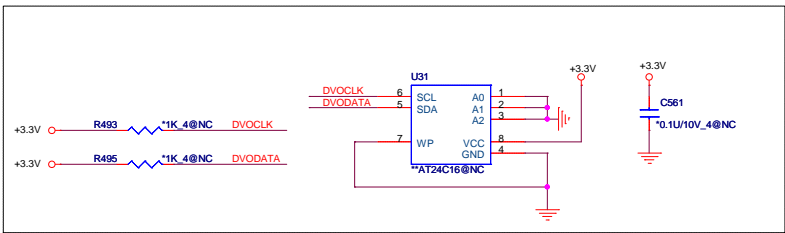
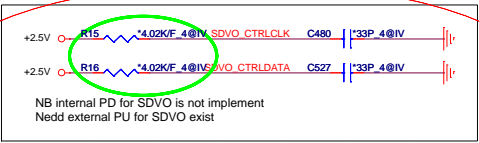


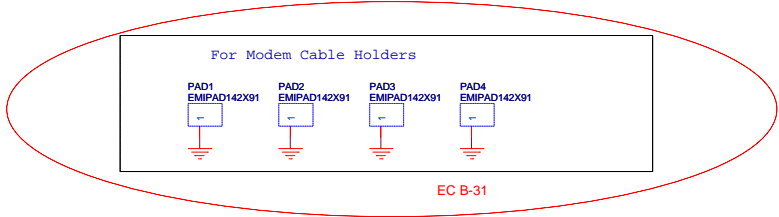
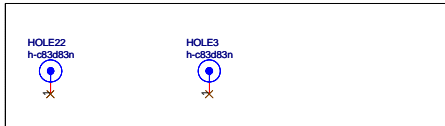
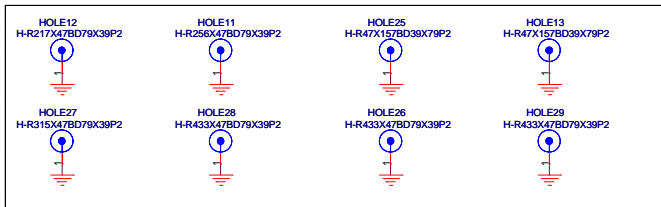
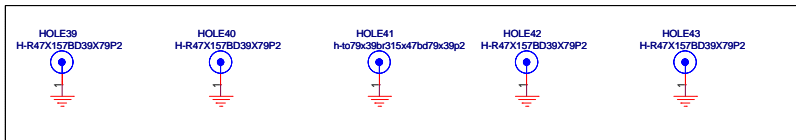
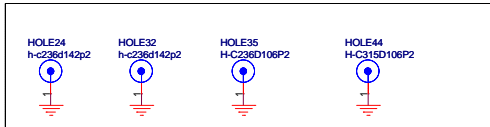
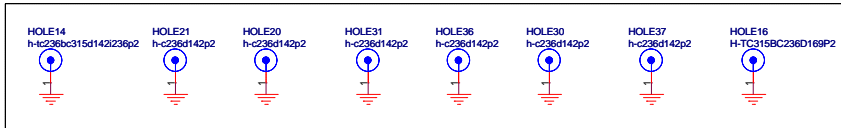
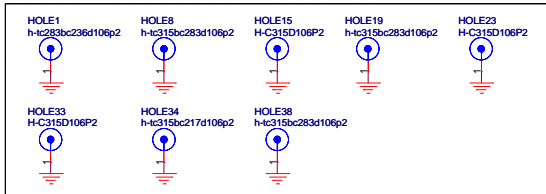
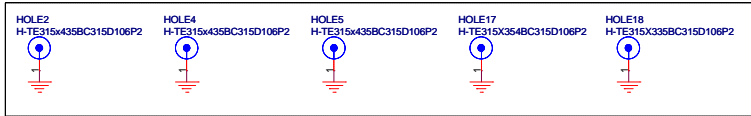
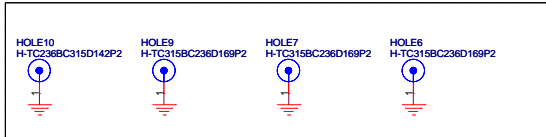


SDVO-DVI

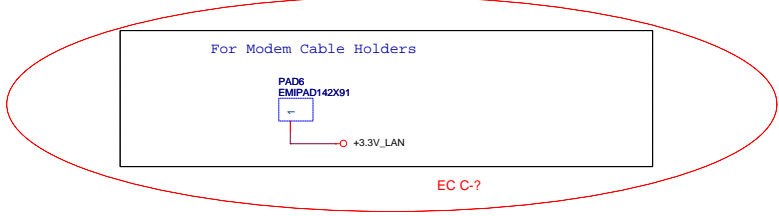


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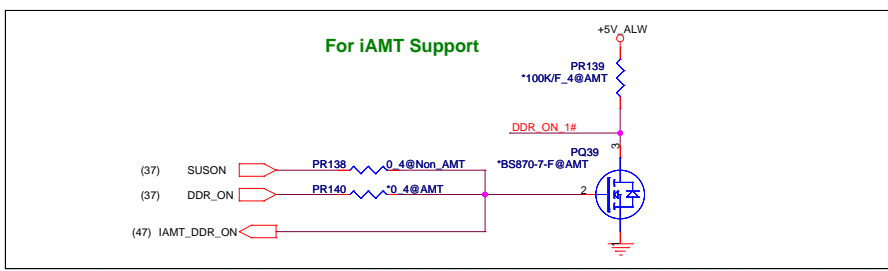
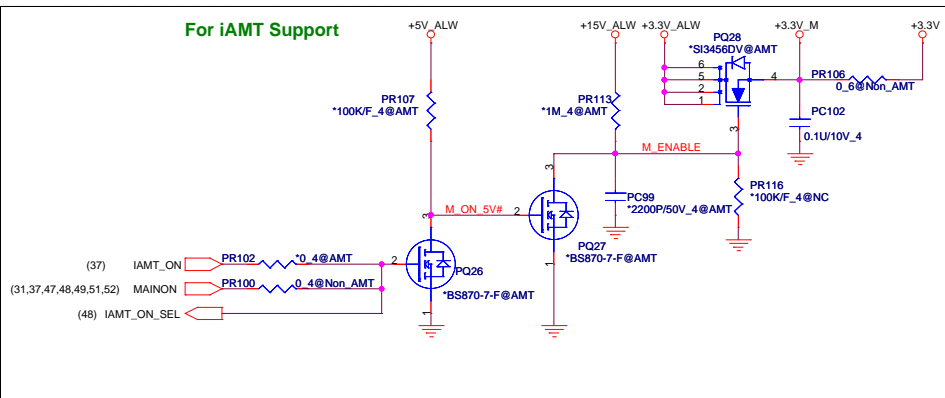
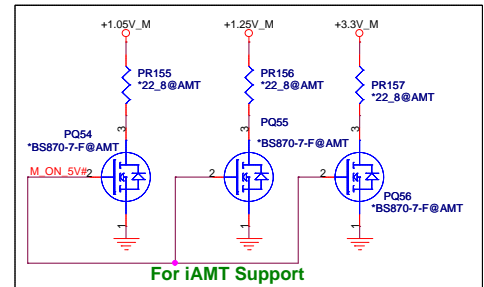
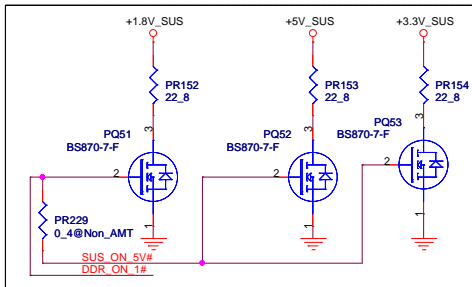
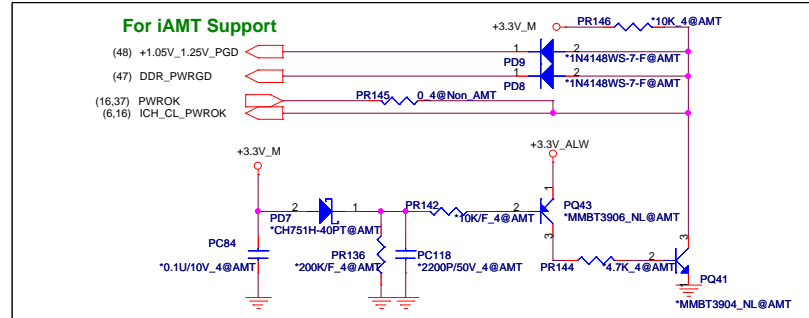
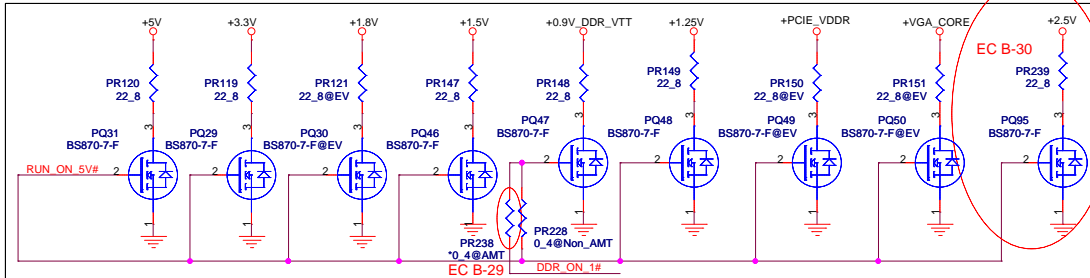
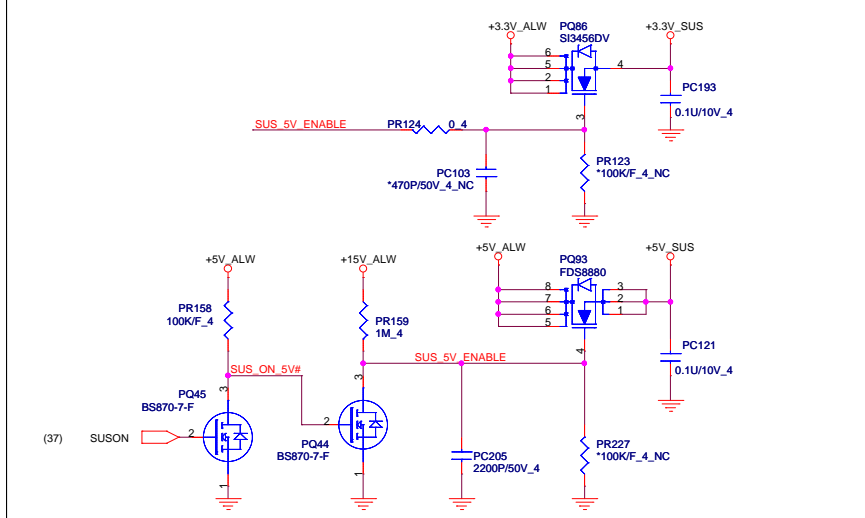
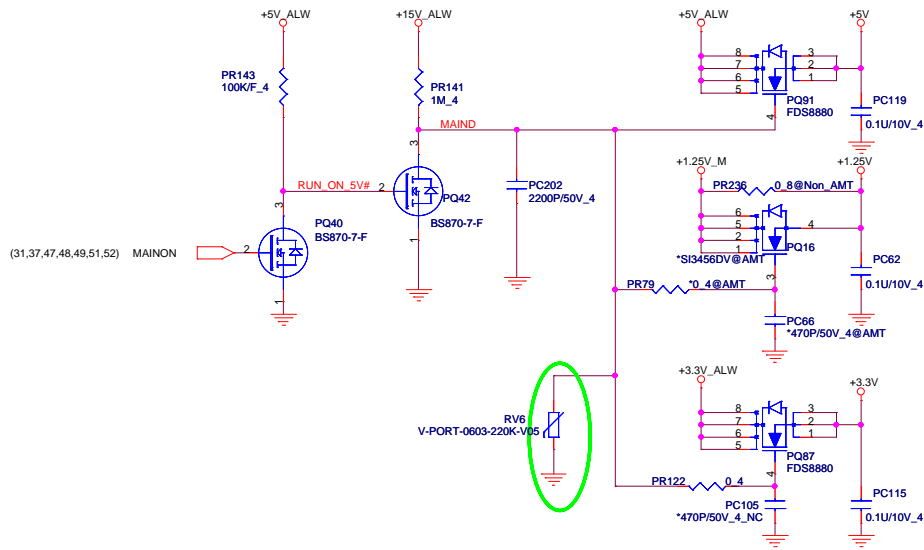




EC B-31

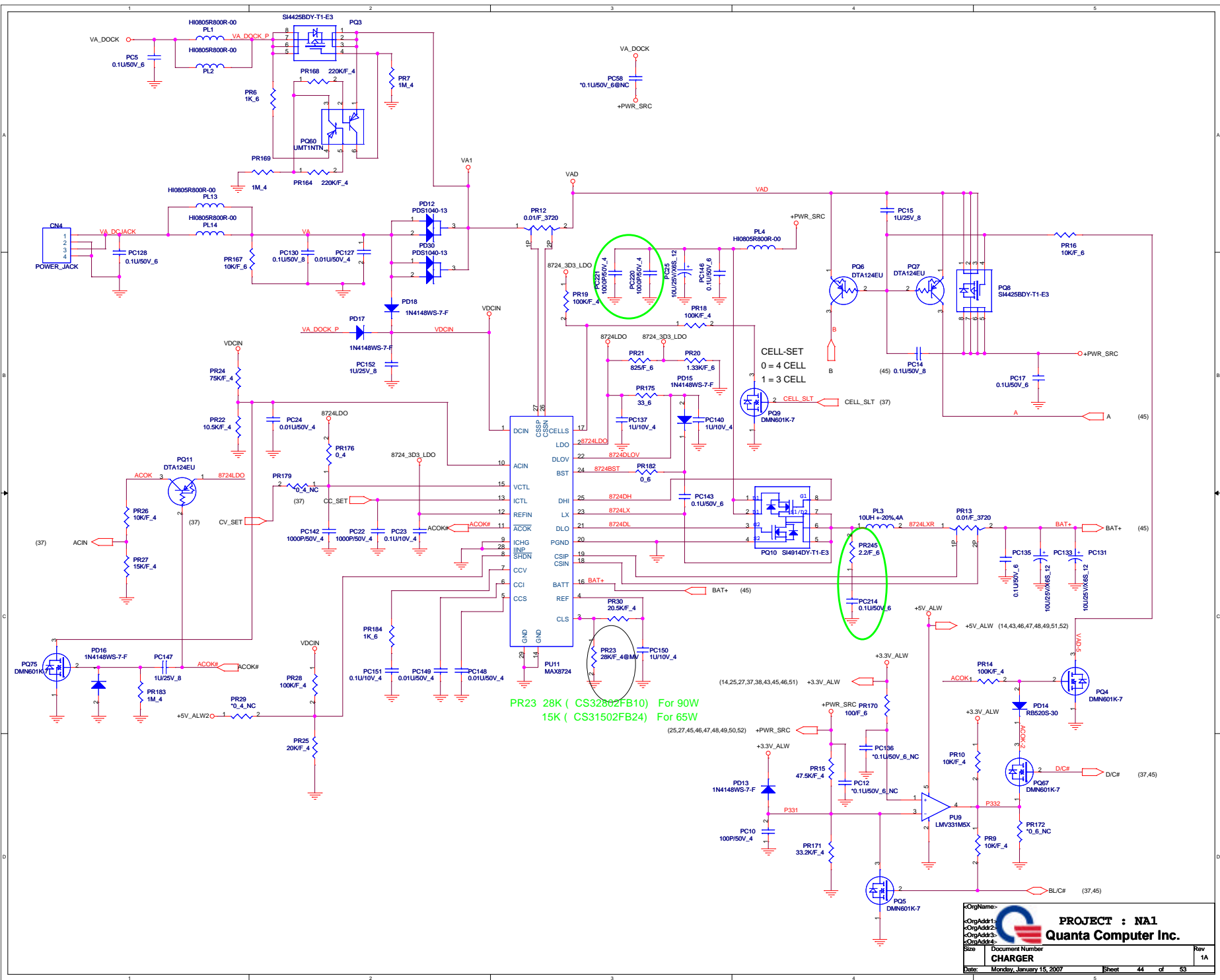


EC C-?

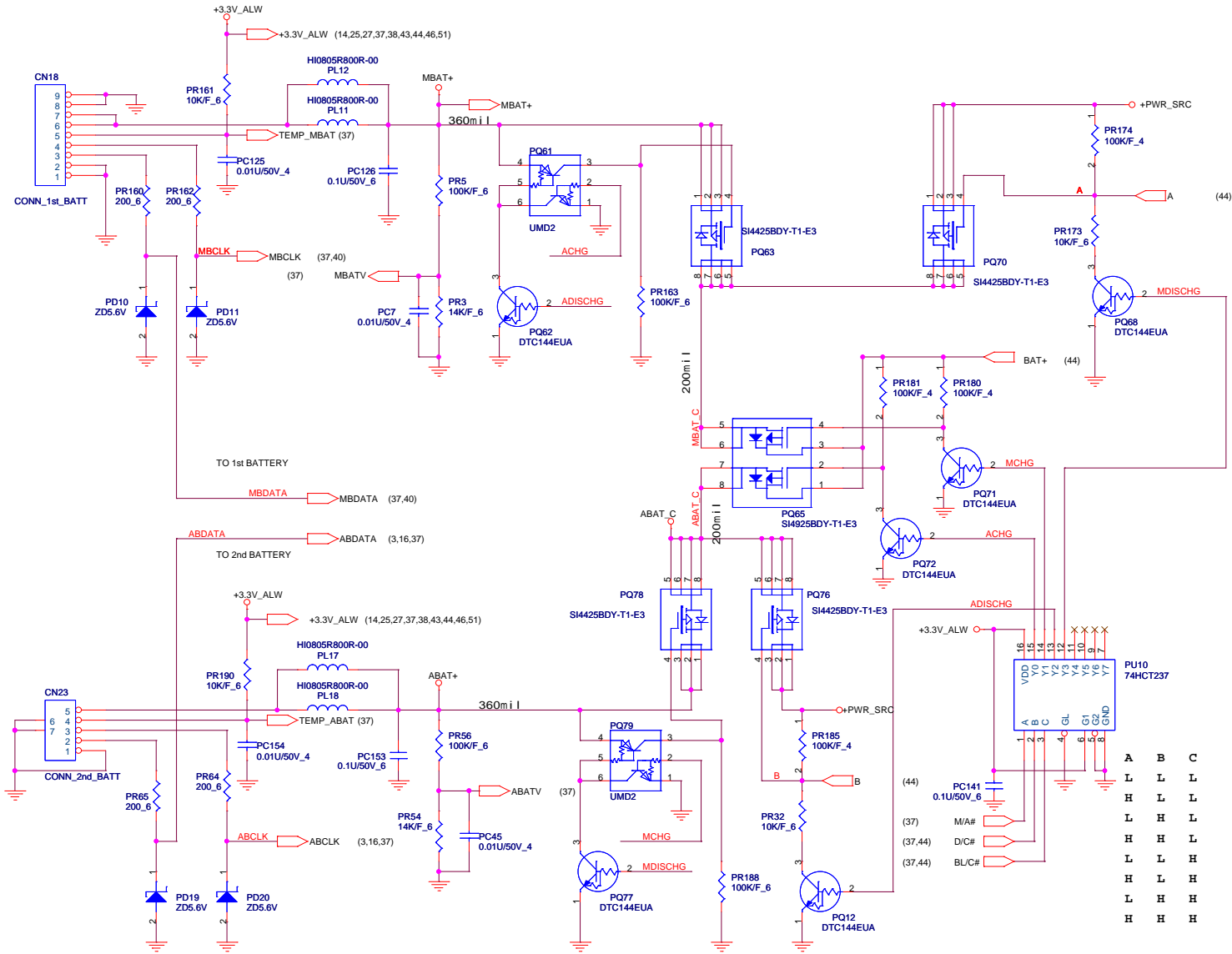


PROJECT : NA1
Quanta Computer Inc.

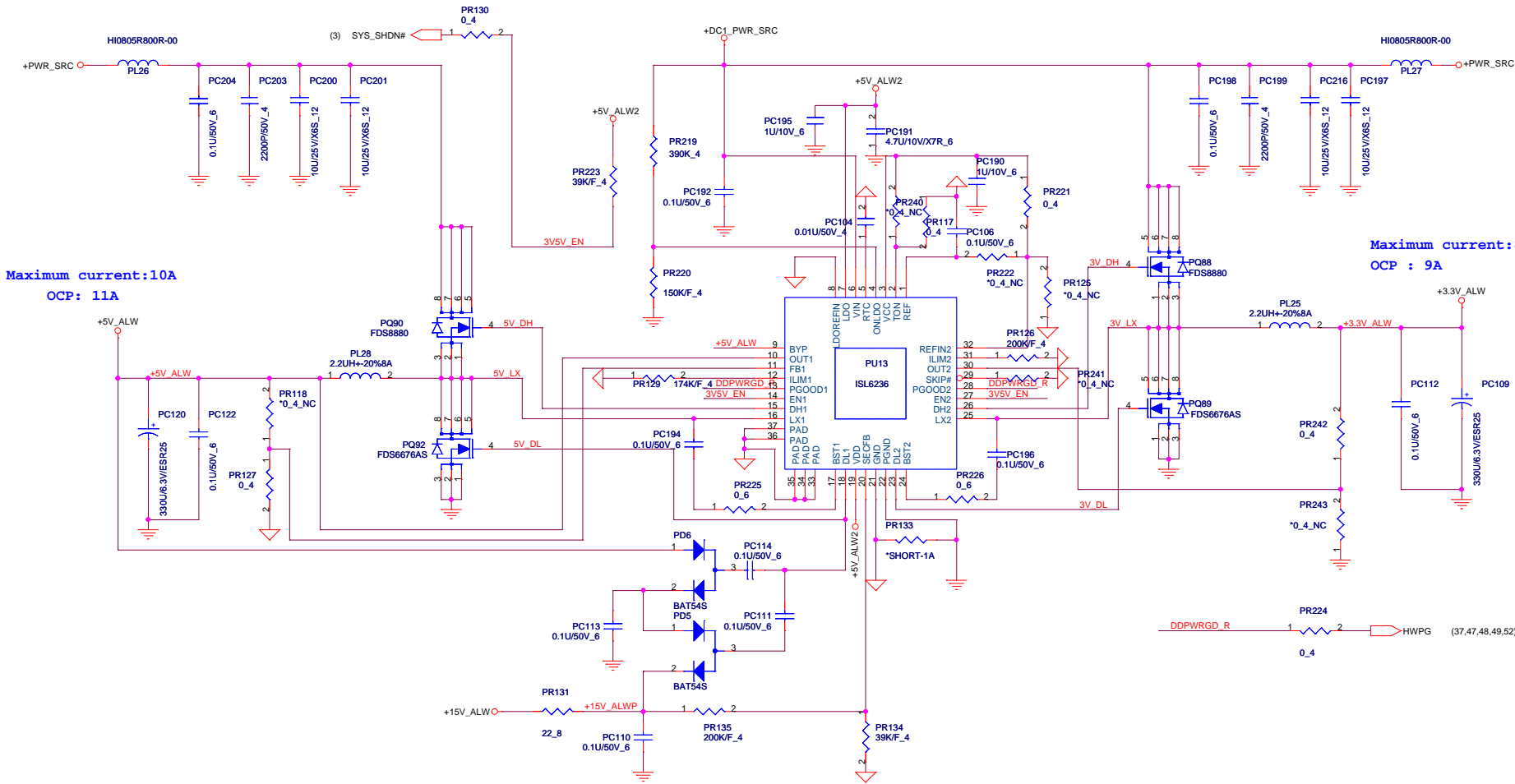
Size	Document Number	Rev
	RUN POWER SW & DISCHARGE	2A
Date:	Monday, January 15, 2007	Sheet 43 of 53



PROJECT : NA1
Quanta Computer Inc.




	A	B	C	Y0	Y1	Y2	Y3
(44)	L	L	L	H	L	L	L
(37)	H	L	L	L	H	L	L
(37,44)	L	H	L	L	L	H	L
(37,44)	H	H	L	L	L	L	H
(37,44)	L	L	H	L	L	L	L
	H	L	H	L	L	L	L
	L	H	H	L	L	L	L
	H	H	H	L	L	L	L



Maximum current:10A
OCP: 11A

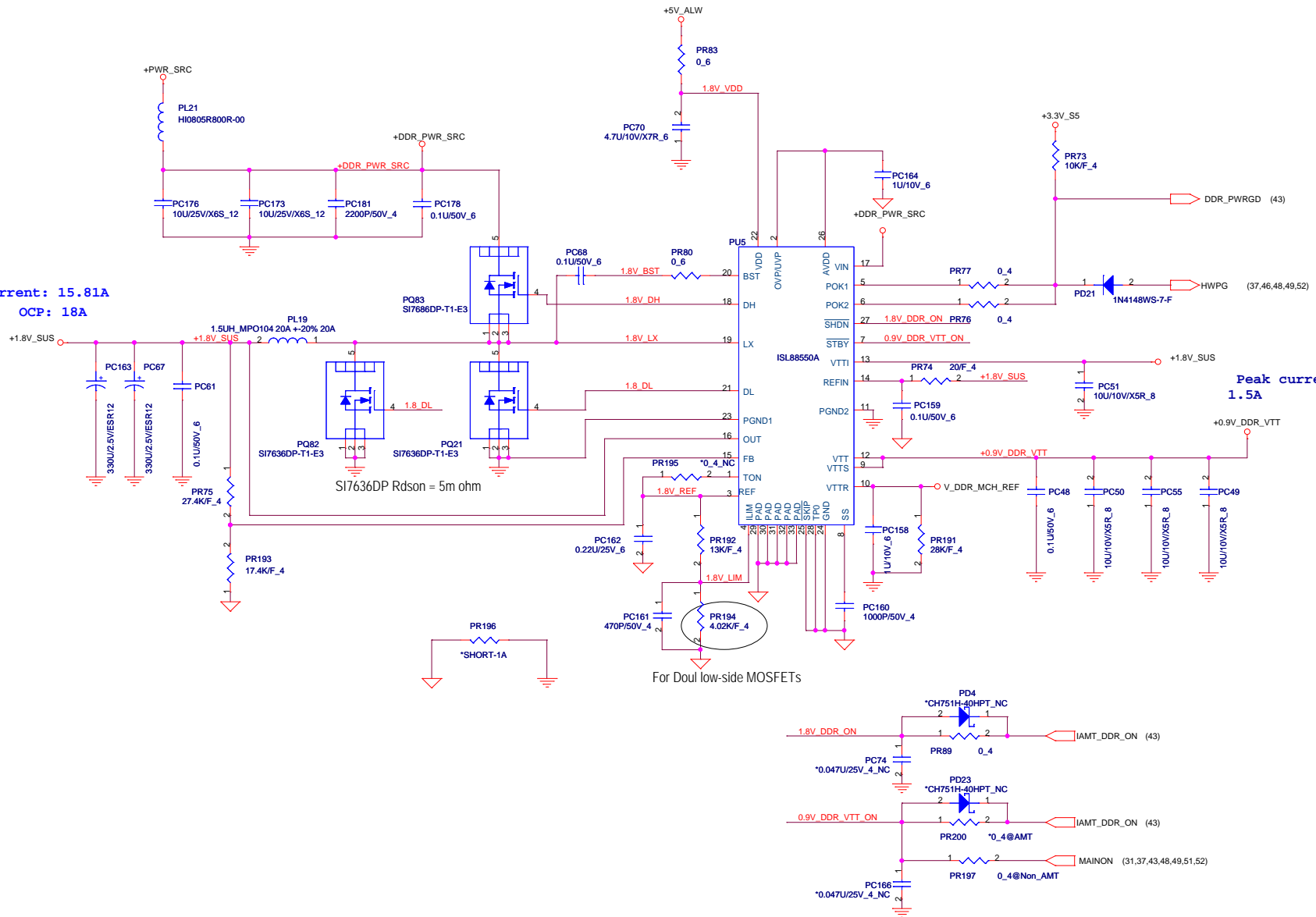
Maximum current:8.5A
OCP : 9A

 PROJECT : NA1 Quanta Computer Inc.		Size	Document Number	Rev
			+3.3V & +5V	1A
Date:	Monday, January 15, 2007	Sheet	46	of 53

Maximum current: 15.81A
 OCP: 18A

Peak current
 1.5A

For Doul low-side MOSFETs



PROJECT : NA1
Quanta Computer Inc.

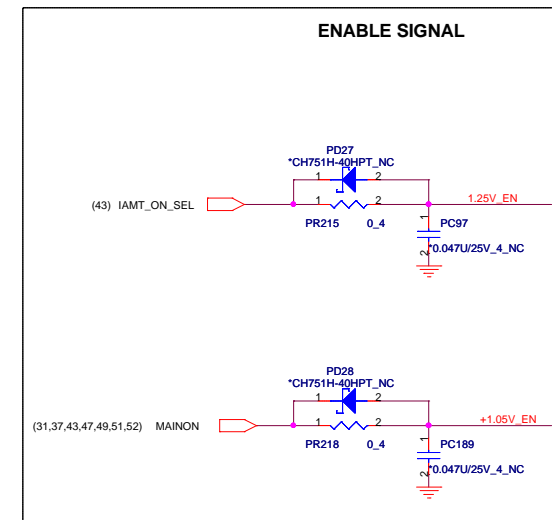
Size	Document Number	Rev
	1.8V_SUS & 0.9V_VTT	1A
Date:	Monday, January 15, 2007	Sheet 47 of 53

Maximum Current: 5A
OCP: 6A

Maximum Current: 17.81A
OCP: 20A

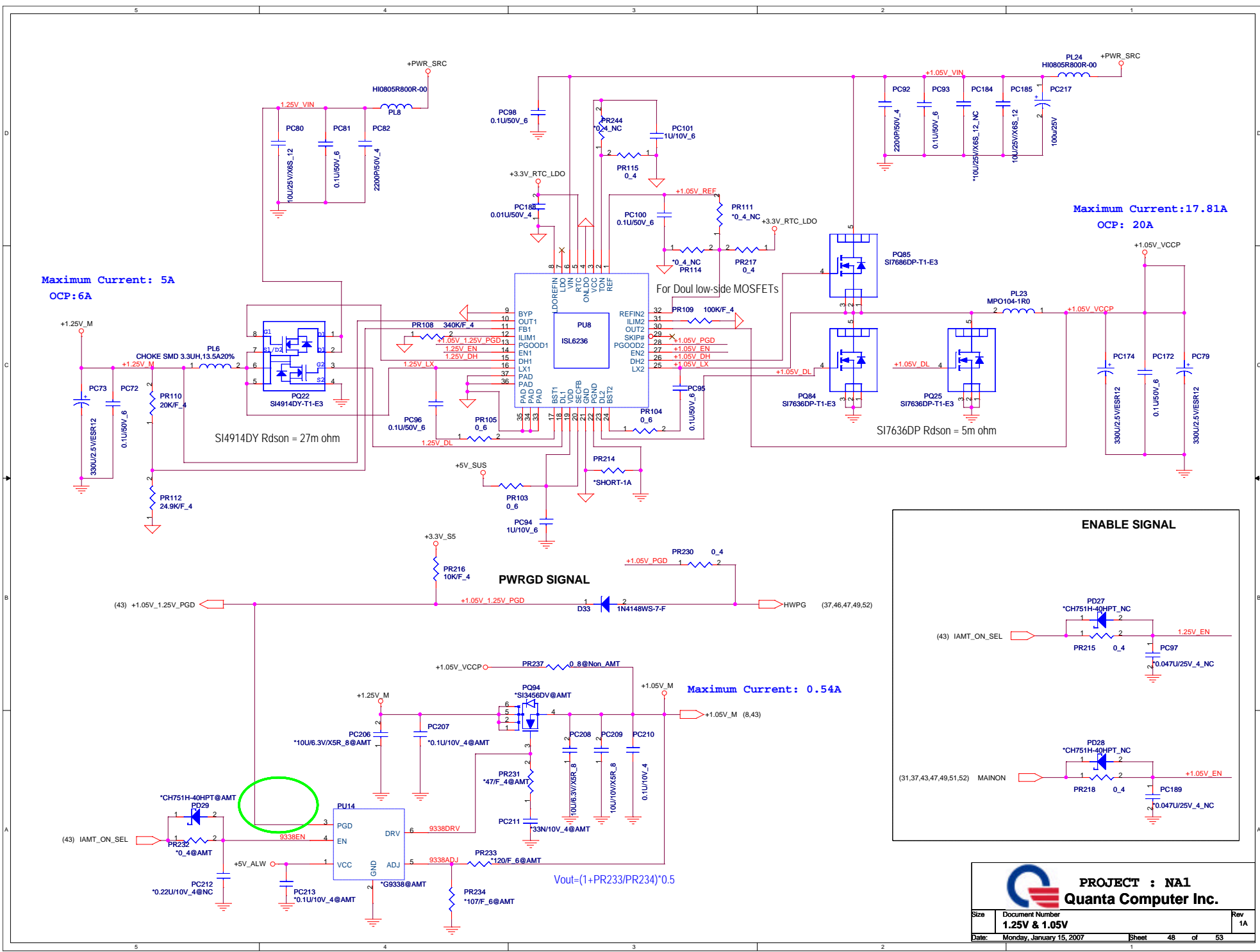
Maximum Current: 0.54A

$$V_{out} = (1 + PR233/PR234) * 0.5$$



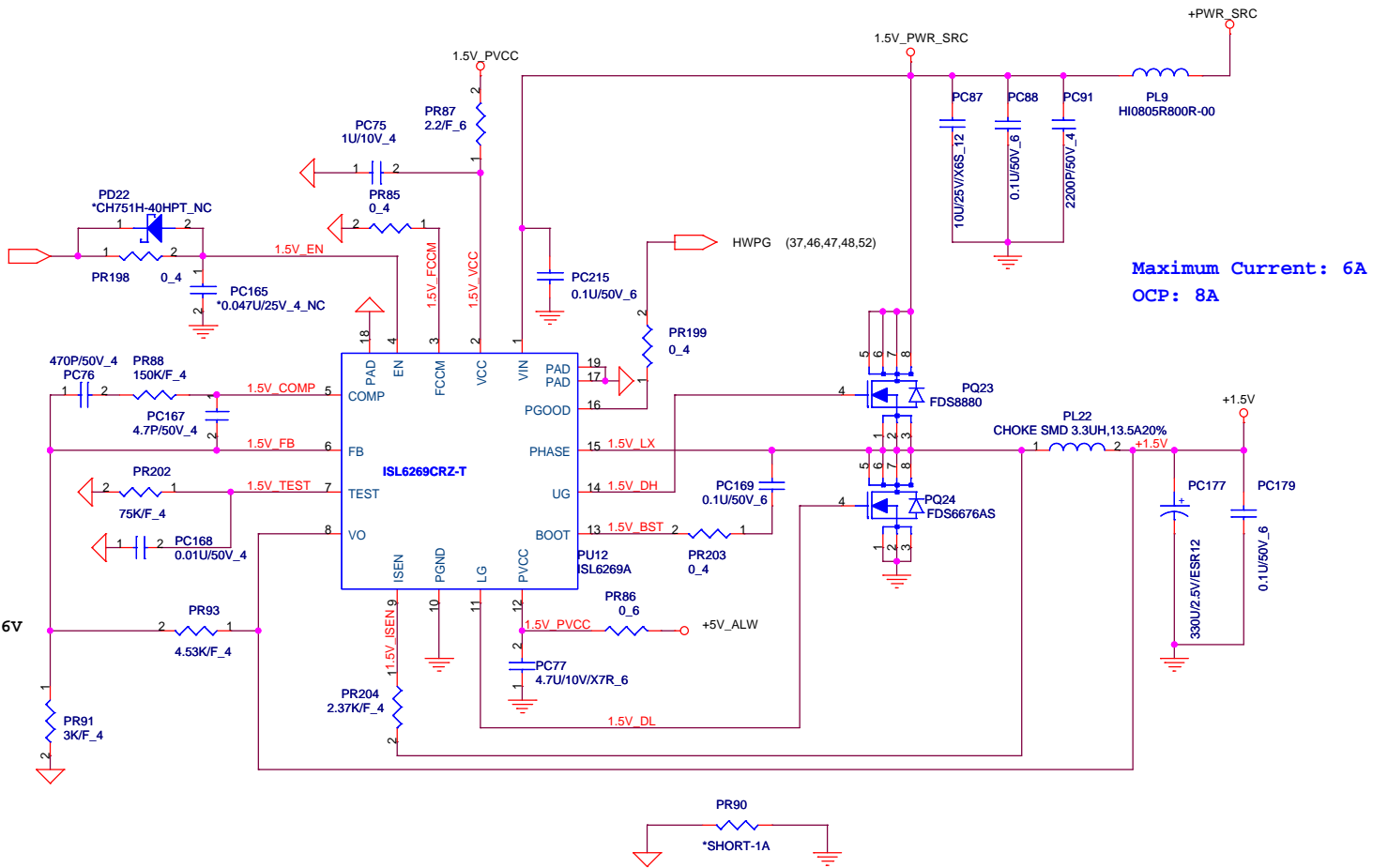
PROJECT : NA1
Quanta Computer Inc.

Size	Document Number	Rev
	1.25V & 1.05V	1A
Date:	Monday, January 15, 2007	Sheet 48 of 53



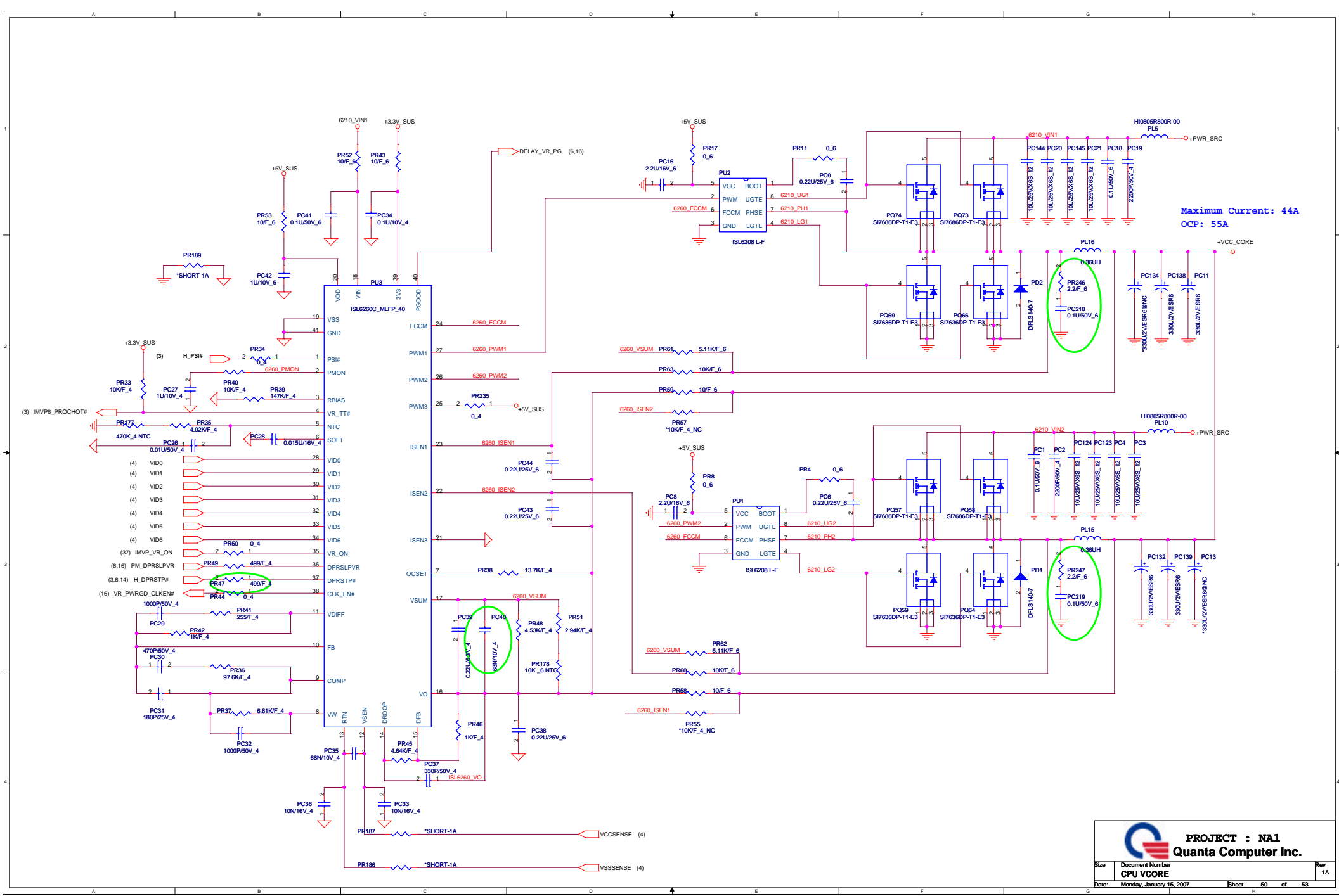
(31,37,43,47,48,51,52) MAINON

Vref=0.6V




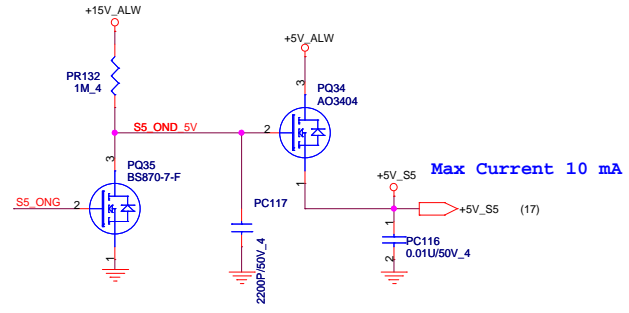
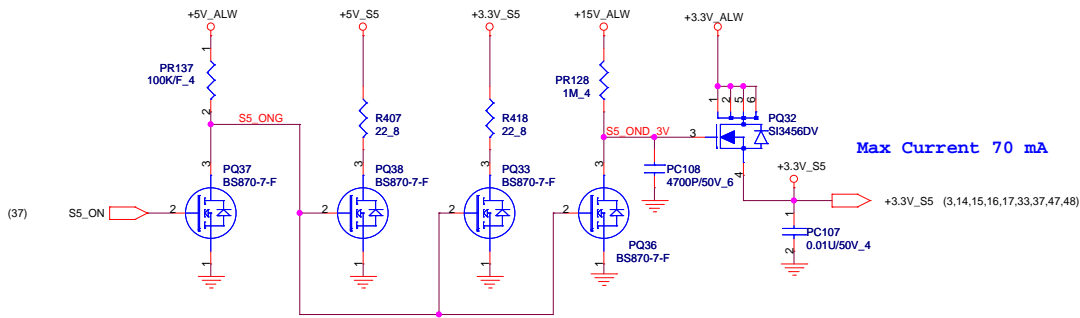
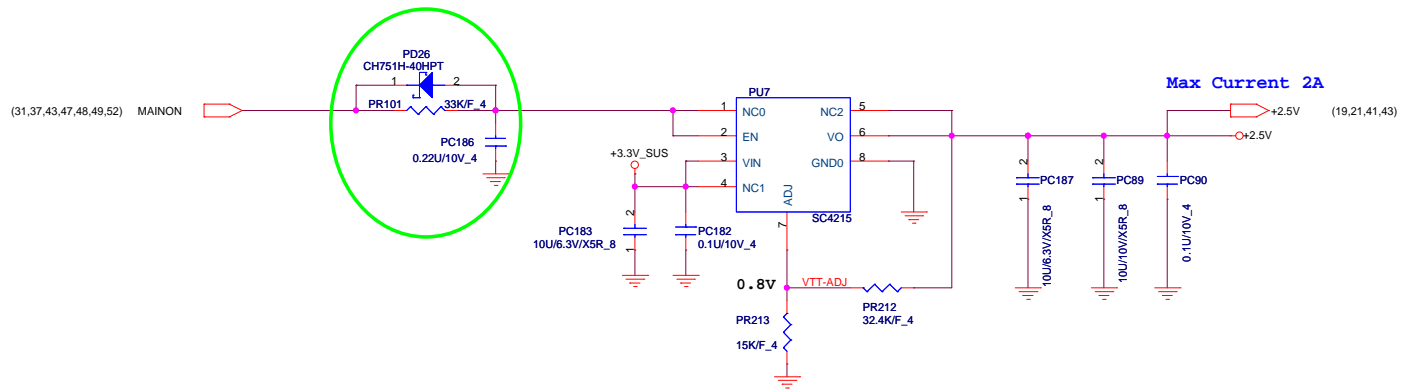
PROJECT : NA1
Quanta Computer Inc.

Size	Document Number	Rev
	1.5V	1A
Date:	Monday, January 15, 2007	Sheet 49 of 53

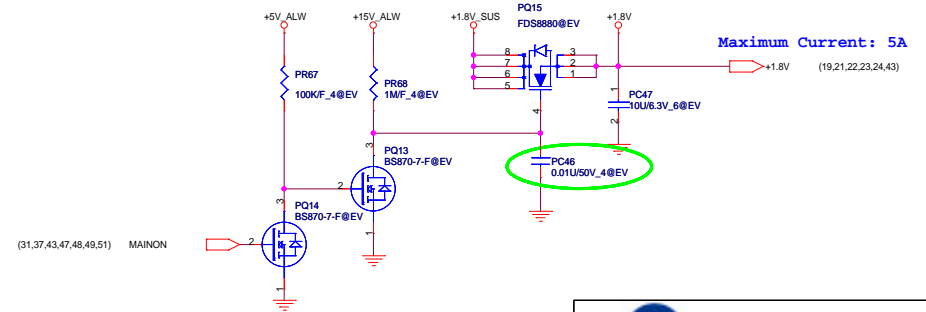
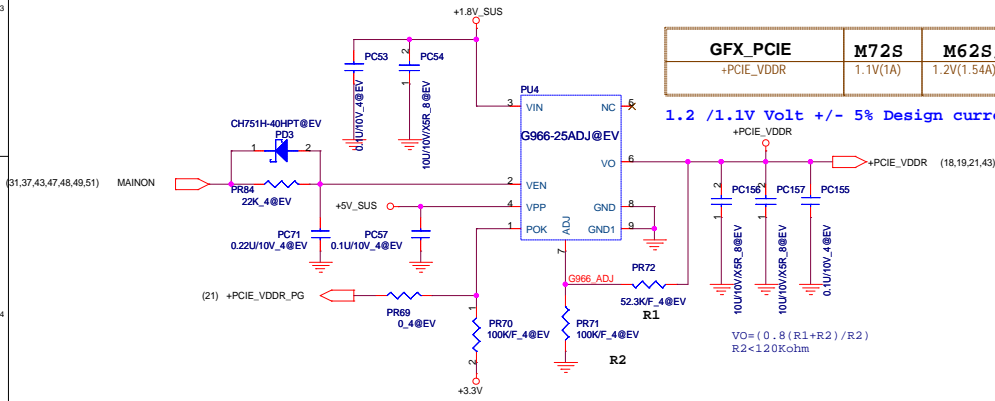
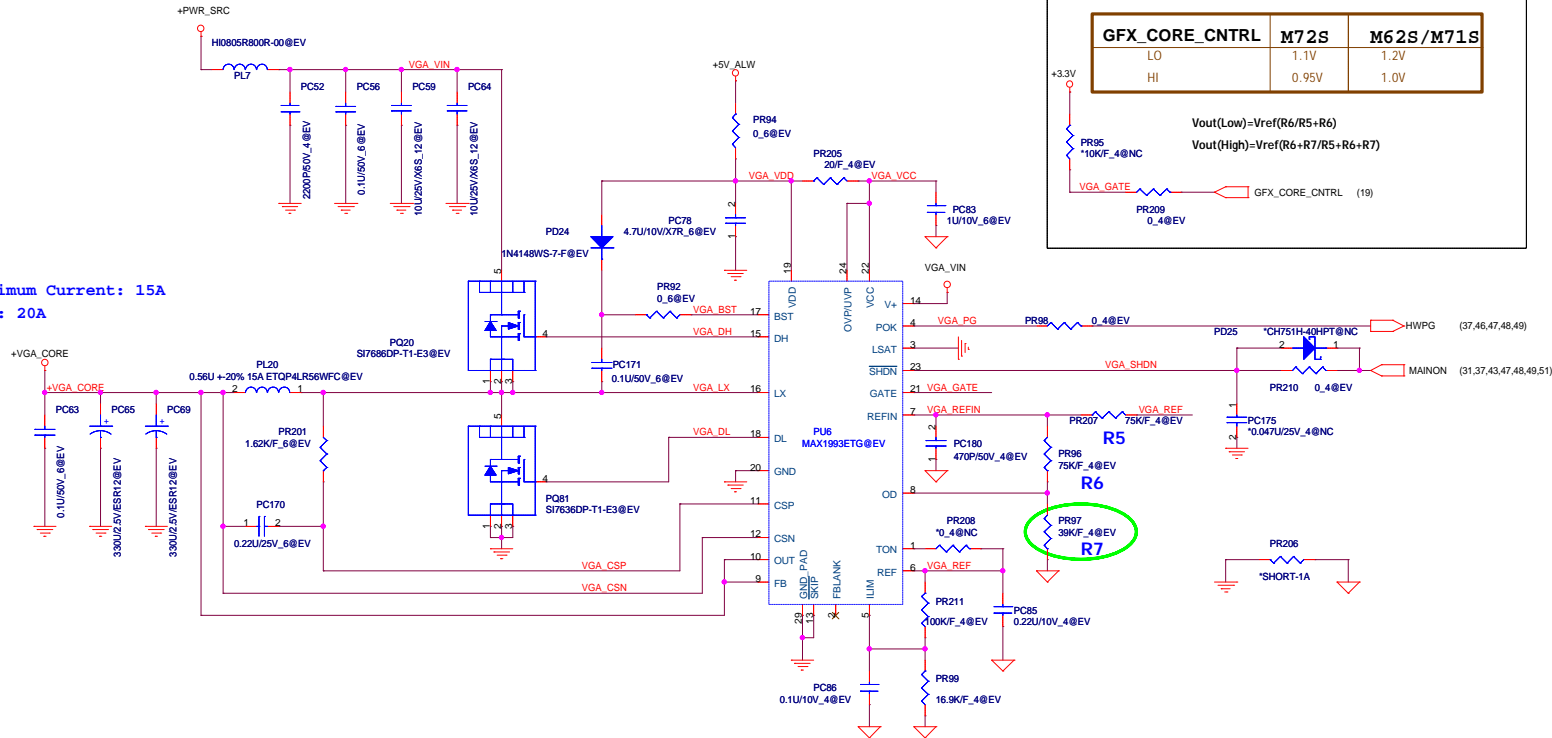
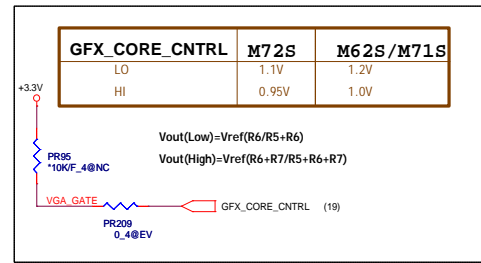


Maximum Current: 44A
OCP: 55A

 PROJECT : NA1 Quanta Computer Inc.		Rev	1A
		Doc Number	CPU CORE
Date:	Monday, January 15, 2007	Sheet	50 of 53



Maximum Current: 15A
OCF: 20A



NA1/QA1 Schematic EC Tracking Record B (for A --> B) Nov. 22, 2006

EC #/Page/Description/Part Affected

- EC B-01 /02/ Add C528,C530,C534,C830 33pF for EMI issue.
EC B-02 /03/ No_stuff R105_51O on H_RESET# signal for Intel platform request(ITP port unused).
EC B-03 /06/ Change R106,R116 connect From GND to +1.05V_VCCP for Intel design guide Rev_1.3 recommend.
EC B-04 /08/ Delete R496 for PCB layout issue.
EC B-05 /09/ Delete R17,R245 for PCB layout issue.
EC B-06 /09/ Change L60 to 100O and add C481/0.1uF for TV/CRT power VCCD_QDAC ripple issue.
EC B-07 /09/ No_stuff D3,R136 for Double stuff the between +1.05V_VCCP and +3.3V.
EC B-08 /14/ Add R642_0O of reserve for IAMT function request.
EC B-09 /15/ Change BAYINS# signal from GPIO12 to GPIO31pin for IAMT function request.
EC B-10 /16/ Add pull up resistor R434,R440_10KO of reserve on STP_PCl# & CPU_PCl# signals for IAMT function request.
EC B-11 /16/ Add signal "LAN_PHYPC" on GPIO12 pin for IAMT function request.
EC B-12 /16/ Stuff R607_0Ofor SATA HDD Modularity.
EC B-13 /19/ Add R245_10KO for ATI request.
EC B-14 /25/ Change R157 & R560 from 10KO to 8.2KO for ATI request.
EC B-15 /26/ Modify CN16 footprint for correct layout.
EC B-16 /27/ Add Q53 for IAMT function request.
EC B-17 /27/ No_Stuff R27 for correct LAN LED indicator.
EC B-18 /28/ Change R511 from 3.92KO to 1.4KO for Intel platform LAN energy detect circuit request.
EC B-19 /29,30/ Change cardbus controller from Ricoh-R5C853 to TI-PCI7612.
EC B-20 /31/ Move Audio codec & amplifier circuit from Audio board to M/B for EMI issue.
EC B-21 /33/ Add R394 MiniCard WLAN_AUX power connection to +3.3V_S5 for IAMT function request.
EC B-22 /35/ Add EMI filter L12 for EMI issue.
EC B-23 /37/ Change BAYSWAP# signal connection from +3.3V to +3.3V_S5 for Modularity Bay detect.
EC B-24 /38/ Change CN3 Pin definitions for cable assembly issue.
EC B-25 /01/ Add Q52 for correct WLAN LED indicator.
EC B-26 /38/ DeleteQ24,Q25 for correct battery LED indicator.
EC B-27 /01/ Delete R664 for correct power LED indicator.
EC B-28 /41/ Add C480 & C527_33pF for EMI request.
EC B-29 /43/ Add PR238_0O for IAMT function request.
EC B-30 /43/ Add PR239 & PQ95 for +2.5V discharger.
EC B-31 /42/ Add PAD1~PAD5 for modem cable holders.
EC B-32 /38/ Add C660,C756~C758 for EMI request.