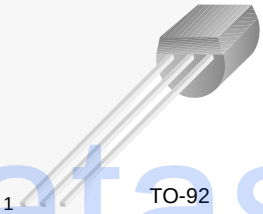
FAIRCHILD SEMICONDUCTOR®

November 2013

2N7000BU / 2N7000TA
Advanced Small-Signal MOSFET

Features

- Fast Switching Times
- Improved Inductive Ruggedness
- Lower Input Capacitance
- Extended Safe Operating Area
- Improved High-Temperature Reliability



TO-92

1. Source 2. Gate 3. Drain

Description

These N-channel enhancement mode field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. These products minimize on-state resistance while providing rugged, reliable, and fast switching performance. They can be used in most applications requiring up to 400 mA DC and can deliver pulsed currents up to 2 A. These products are particularly suited for low-voltage, low-current applications, such as small servo motor control, power MOSFET gate drivers, and other switching applications.

Ordering Information

Part Number	Marking	Package	Packing Method
2N7000BU	2N7000	TO-92 3L	Bulk
2N7000TA	2N7000	TO-92 3L	Ammo

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at T_C = 25°C unless otherwise noted.

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-to-Source Voltage	60	V
I_D	Continuous Drain Current (T_C = 25°C)	200	mA
	Continuous Drain Current (T_C = 100°C)	110	
I_{DM}	Drain Current Pulsed[1]	1000	mA
V_{GS}	Gate-to-Source Voltage	±30	V
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	°C
T_L	Maximum Lead Temperature for Soldering Purposes, 1/8-inch from Case for 5 Seconds	300	°C

Note:

1. Repetitive rating: pulse width limited by maximum junction temperature.

Thermal Characteristics[2]

Values are at T_C = 25°C unless otherwise noted.

Symbol	Parameter	Value	Unit
P_D	Total Power Dissipation (T_C = 25°C)	400	mW
	Linear Derating Factor	3.2	mW/°C
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	312.5	°C/W

Note:

2. Device mounted on FR-4 PCB, board size = 101.5 mm x 114.5 mm.

Electrical Characteristics

Values are at T_C = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	60			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	0.3		3.9	V
		V_{DS} = V_{GS}, I_D = 1 mA	0.4		2.2	
I_{GSS}	Gate-Source Leakage, Forward	V_{GS} = 15 V			100	nA
	Gate-Source Leakage, Reverse	V_{GS} = -15 V			-100	
I_{DSS}	Drain-to-Source Leakage Current	V_{DS} = 60 V			1	µA
		V_{DS} = 45 V, T_C = 125°C			1000	
$R_{DS(ON)}$	Static Drain-Source On-State Resistance[3]	V_{GS} = 10 V, I_D = 0.5 A			5.0	Ω
g_{fs}	Forward Transconductance[3]	V_{DS} = 15 V, I_D = 0.5 A	0.1	0.3		S
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		30		pF
C_{oss}	Output Capacitance			12		pF
C_{rss}	Reverse Transfer Capacitance			3.0		pF
$t_{d(on)}$	Turn-On Delay	V_{DD} = 30 V, I_D = 0.5 A, R_G = 15 Ω[3,4]			10	ns
t_r	Rise Time				10	ns
$t_{d(off)}$	Turn-Off Delay				10	ns
t_f	Fall Time				10	ns

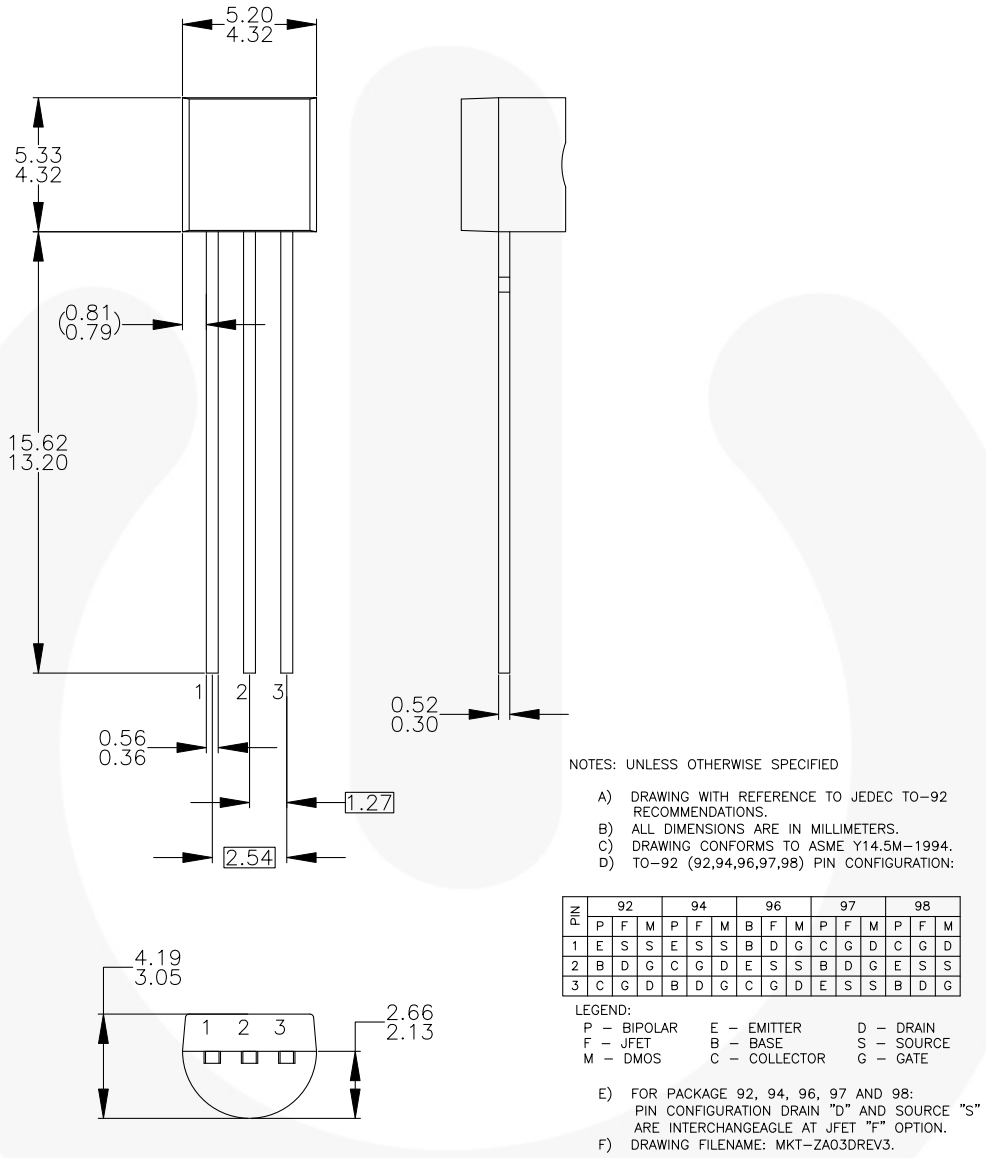
Notes:

3. Pulse test: pulse width = 250 µs, duty cycle ≤ 2%.

4. Essentially independent of operating temperature.

Physical Dimensions

TO-92



NOTES: UNLESS OTHERWISE SPECIFIED

A) DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DRAWING CONFORMS TO ASME Y14.5M-1994.
D) TO-92 (92,94,96,97,98) PIN CONFIGURATION:

PIN	92			94			96			97			98		
	P	F	M	P	F	M	B	F	M	P	F	M	P	F	M
1	E	S	S	E	S	S	B	D	G	C	G	D	C	G	D
2	B	D	G	C	G	D	E	S	S	B	D	G	E	S	S
3	C	G	D	B	D	G	C	G	D	E	S	S	B	D	G

LEGEND:
P – BIPOLAR
F – JFET
M – DMOS
E – EMITTER
B – BASE
C – COLLECTOR
D – DRAIN
S – SOURCE
G – GATE

E) FOR PACKAGE 92, 94, 96, 97 AND 98: PIN CONFIGURATION DRAIN "D" AND SOURCE "S" ARE INTERCHANGEAGLE AT JFET "F" OPTION.
F) DRAWING FILENAME: MKT-ZA03DREV3.

Figure 1. 3-LEAD, TO-92, JEDEC TO-92 COMPLIANT STRAIGHT LEAD CONFIGURATION

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Physical Dimensions (Continued)

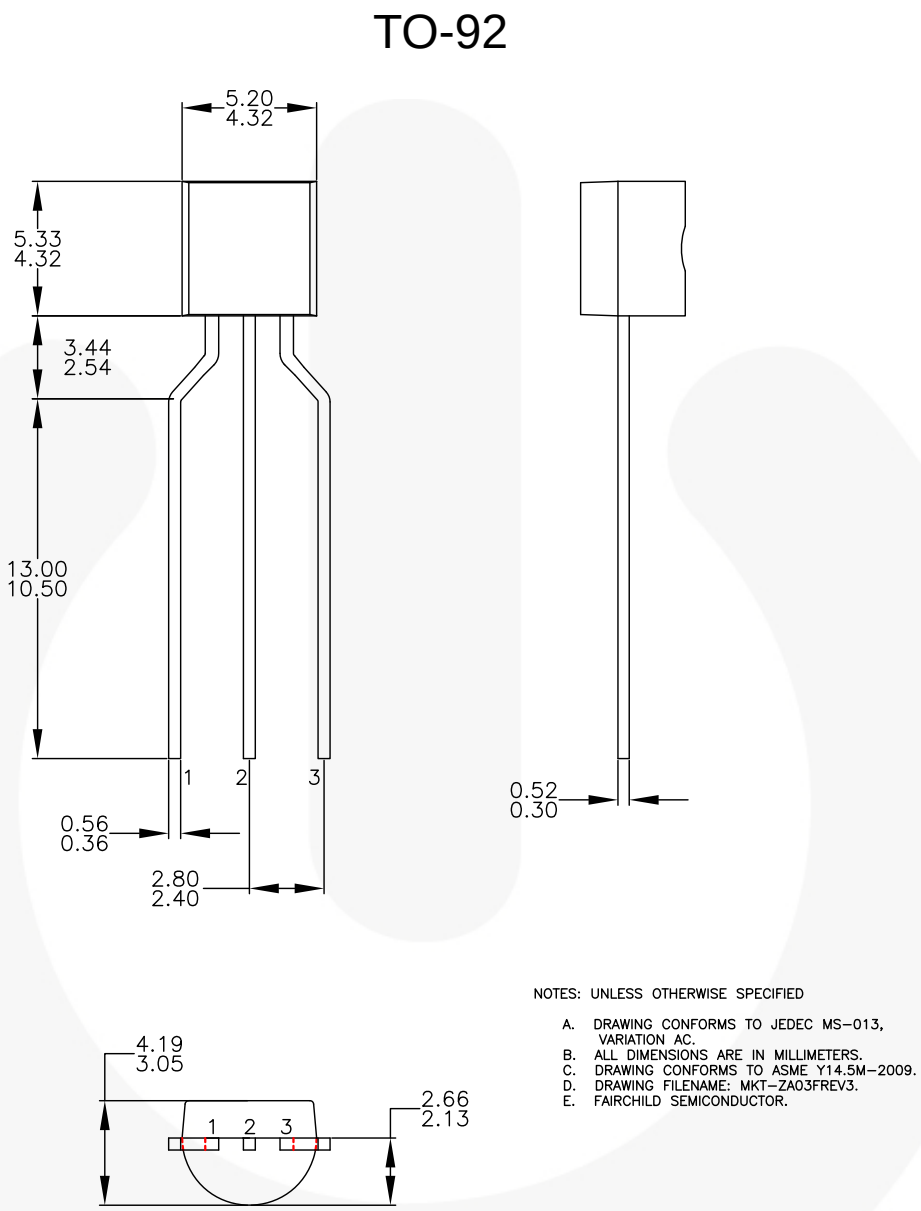

Figure 2. 3-LEAD, TO-92, MOLDED 0.200 IN LINE SPACING LD FORM (J61Z OPTION) (ACTIVE)

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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