3 to 5 Cells Li-ion Battery Protector IC

NO.EA-263-1600711

OUTLINE

The R5432V is a high voltage CMOS-based protection IC for overcharge /discharge of rechargeable three-cell / four-cell / five-cell Lithium-ion / Lithium- polymer battery, further include a short circuit and the protection circuits against the excess discharge current and excess charge current.

Each of these ICs is composed of eighteen voltage detectors (fourteen for 3cell protection type, sixteen for 4cell protection type), a reference circuit, a delay circuit, a short detector circuit, an oscillator, a counter and a logic circuit.

The output of COUT is P-channel open-drain type, and DOUT is CMOS type.

If the overcharge voltage or overcharge current is detected by the R5432V, after the preset output delay time, the output of COUT becomes Hi-Z.

While the overdischarge voltage or current is detected, after the preset output delay time, the output of DOUT becomes ”L”. After detecting overcharge voltage, when the cell voltage returns lower than the overcharge released voltage, then overcharge is released and the output of COUT becomes “H”. After detecting overcharge current, by disconnecting a charger and connecting a load, then overcharge current is released and the output of COUT becomes “H”.

After detecting overdischarge voltage, when the cell voltage becomes the released voltage from overdischarge or more, then overdischarge is released and the output of DOUT becomes “H”. After detecting overdischarge current and short circuit, by disconnecting the load, the function of the output of DRAIN pin, the external NMOSFET turns on, and VMP pin voltage is pulled down by the resistance connected to GND and released overdischarge current or short and the output of DOUT becomes “H”.

By forcing a certain voltage to SEL1 and SEL2 pins, the testing time of protection circuits can be short. Specifically, overcharge, discharge, over current delay time can be shortening into approximately 1/80.

The R5432V can protect 6-cell or more by connecting 2 pieces of the R5432V in cascade. High side IC’s COUT and DOUT must connect to CTLC and CTLD respectively of the low side IC. As a result, the signal of the high side of COUT and DOUT is transmit to the lower side IC, and control FETs for charge and discharge.

The R5432V has cell-balance function to solve the unbalance condition of serially connected cells. If cell voltage is beyond the cell balance detector threshold, by the output of the cell balance control pin, the external NMOSFET turns on, and a current path is made, and during charge, charge current is bypassed, otherwise, cell is discharged until the cell voltage becomes the released voltage from cell-balance operation.

If the connection between a cell and a protection board is broken, the open-wire condition is detected by the R5432V, and the output of COUT becomes Hi-Z. After detecting the open-wire, when the cell and the protection board is connected again, the open-wire detector is released and the output of COUT becomes “H”.

FEATURES

- Absolute Maximum Rating 30V
- Supply Current ..... Typ. 12.0μA

Detector thresholds range and accuracy

- Overcharge detector threshold ..... 3.6V to 4.5V (5mV step) (n=1, 2, 3, 4, 5) (±25mV)
- Overdischarge detector threshold ..... 2.0V to 3.0V (5mVstep) (n=1, 2, 3, 4, 5) (±2.5%)
- Excess discharge current threshold 1 ..... 0.1V to 0.3V (10mVstep) (±20mV) for BA/BB/BC ver.
  0.1V to 0.2V (10mV step) (±20mV) for AD/BD ver.
- Excess discharge current threshold 2 ..... 0.45V/0.60V for BA ver.
  0.25V to 0.40V for BB/BC ver.
  0.25V/0.3V(Vdet3-1+0.1V or more) for AD/BD ver.

- Short detector threshold ..... 1.00V for BA ver.
  0.75V for BB/BC ver.
  Vdet3-2 x 1.67 for AD/BD ver.
- Excess charge current threshold ..... -0.05V (±30mV), -0.1V (±30mV), -0.2V (±30mV), -0.4V (±40mV)
- Overcharge released voltage..... V_{DET1}n-0.1V to 0.4V (50mV steps) (n=1, 2, 3, 4, 5)
- Overdischarge released voltage ..... V_{DET2}n+0.2V to 0.7V (100mV steps) (n=1, 2, 3, 4, 5)
  up to 3.4V
- Cell-balance detector threshold ..... 3.45V to 4.45V (5mV steps) (n=1, 2, 3, 4, 5)
- Cell-balance released voltage ..... CB_{DET}n-0.0V to 0.4V (50mV steps) (n=1, 2, 3, 4, 5)

Output delay time

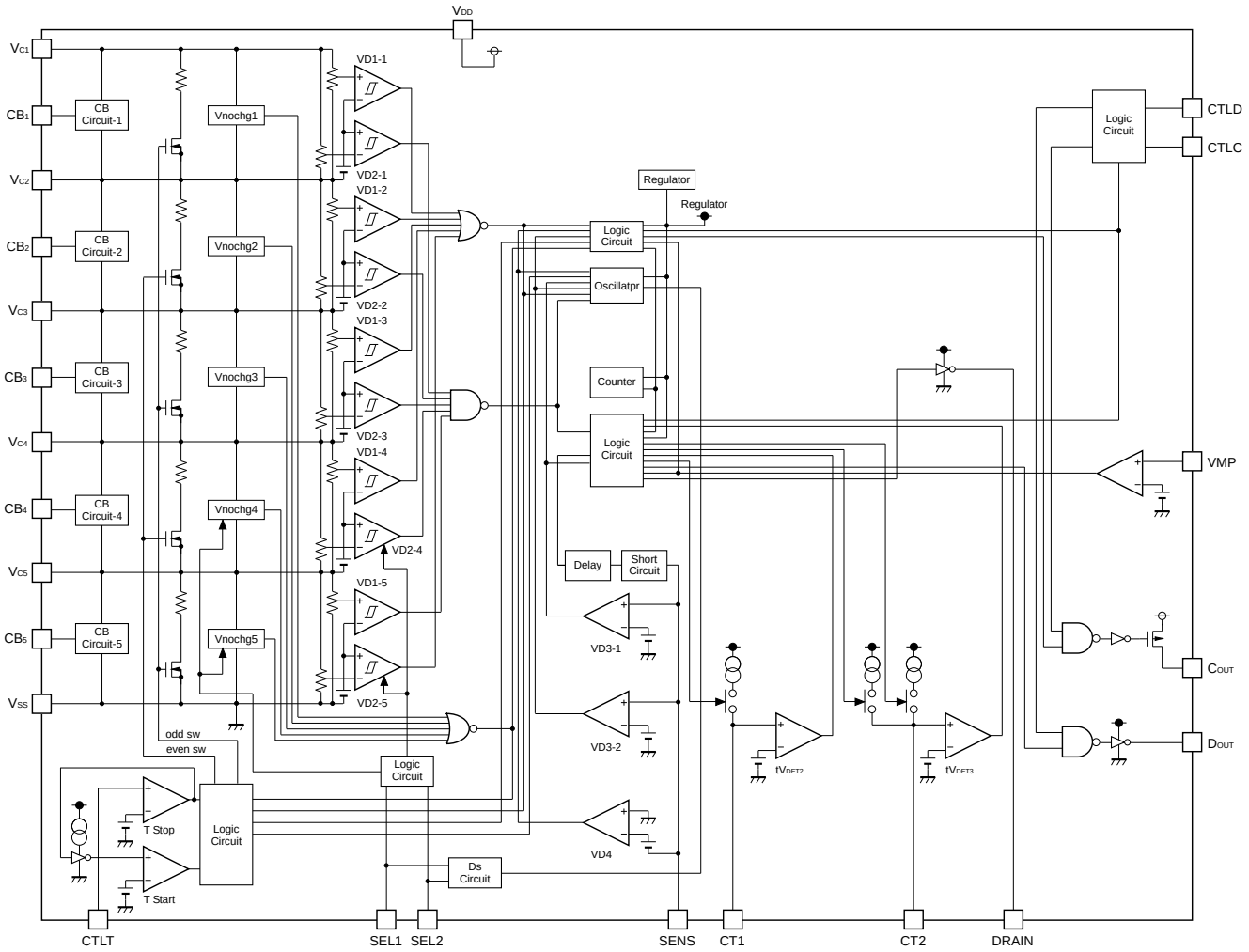
- Overcharge detector Output Delay 1.0s
- Overdischarge detector Output Delay ..... Settable by Ext.Capacitance1
- Excess discharge current detector Output Delay 1/2..... Settable by Ext.Capacitance2
- Excess charge current detector Output Delay 8ms
- Short detector Output Delay 300μs

Functions

- 0V-battery charger .... acceptable/unacceptable options
- Cascade connection .... Available. Refer to the typical application.
- 3/4/5 cell protection .... Selectable
- Output Delay Time Shortening Function..... By forcing a certain voltage to SEL pin, overcharge, discharge voltage and current is reduced approximately 1/80. Overcharge delay time can be shorten into around 4ms for testing.
- Cell-balance function ..... Available
- Cell-unbalance condition ..... If either of cells detects overcharge and either of cells detects overdischarge, the output of COUT becomes “Hi-Z”, the output of DOUT becomes “L”.
- Overcharge/Overdischarge released condition..... By voltage condition.
- Output of COUT/DOUT ..... COUT: VDD source P-channel open drain output. Normal state “H”(VDD), Detected state “Hi-Z”.
  DOUT: 12V regulator source CMOS output. Normal state “H”(12V), Detected state “L”.
- Open-wire detection ..... Open-wire between VDD, VSS, VCx pin and the pack is supervised.
- Small Package..... SSOP-24

BLOCK DIAGRAMS

R5432VxxxBA



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SELECTION GUIDE

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R5432Vxxx$*	SSOP-24	3000	Yes	Yes

xxx :Serial Number for the R5432V designating voltages such as overcharge threshold, overcharge released voltage, Cell-balance threshold, Cell-balance released voltage, overdischarge threshold, overdischarge released voltage, overdischarge current1/2, overcharge current, short voltage.

$: Designation of Output delay option.

	Overcharge Delay time (s)	Overdischarge Delay time (ms)	Overdischarge Current Delay time1 (ms)	Overdischarge Current Delay time2 (ms)	Overcharge Current Delay time (ms)	Short Delay time (μs)
A	1.0	$3.64\times C_{CT1}$ (nF)	$3.05\times C_{CT2}$ (nF)	$tV_{DET}31/100$	8	300
B	1.0	$3.88\times C_{CT1}$ (nF)	$3.26\times C_{CT2}$ (nF)	$tV_{DET}31/6$	8	300

*capacitor for CT1: C_{CT1}, capacitor for CT2:C_{CT2}.

* : Designation of Output delay option.

	Overcharge Released condition	Overdischarge Released condition	0V battery Charge	Short detector Threshold	Open-wire detection	Cascade connection
A	Auto Release	Auto Release	Acceptable	1.0V	Available	Available
B	Auto Release	Auto Release	Unacceptable	0.75V	Available	Available
C	Auto Release	Auto Release	Acceptable	0.75V	Available	Available
D	Auto Release with hysteresis cancellation	Auto Release	Acceptable	VDET32 x 1.67	Available	Available

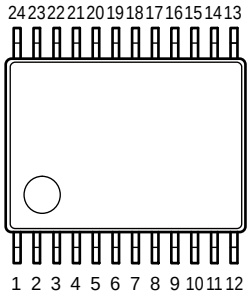
1) Product Code List

Code	VDET1n (V) *1	VREL1n (V) *1	VCBDn (V) *1	VCBRn (V) *1	VDET2n (V) *1	VREL2n (V) *1	VDET31 (V)	VDET32 (V)	VSHORT (V)	VDET4 (V)
R5432V402BA	4.350	4.050	4.200	4.200	2.400	2.700	0.200	0.600	1.000	-0.100
R5432V403BA	3.900	3.800	3.500	3.500	2.500	3.000	0.100	0.600	1.000	-0.100
R5432V404BA	4.250	4.100	4.200	4.200	2.500	3.000	0.200	0.600	1.000	-0.200
R5432V405BA	3.900	3.800	3.650	3.650	2.000	2.300	0.100	0.600	1.000	-0.200
R5432V406BA	3.650	3.550	3.500	3.500	2.500	3.000	0.300	0.600	1.000	-0.200
R5432V407BA	4.200	4.000	3.900	3.900	2.700	2.850	0.200	0.450	1.000	-0.200
R5432V408BA	3.800	3.600	3.450	3.450	2.000	2.300	0.200	0.450	1.000	-0.100
R5432V409BA	4.100	4.000	3.900	3.900	3.000	3.100	0.200	0.600	1.000	-0.200
R5432V410BC	4.200	4.000	4.150	4.150	2.750	2.950	0.100	0.250	0.750	-0.050
R5432V412BA	4.300	4.050	4.200	4.200	2.700	3.000	0.200	0.600	1.000	-0.100
R5432V413BA	4.250	4.100	4.200	4.200	2.500	3.000	0.100	0.600	1.000	-0.100
R5432V416BA	4.200	4.100	4.170	4.170	2.500	3.000	0.200	0.450	1.000	-0.100
R5432V417BC	4.200	4.100	4.180	4.180	2.500	3.000	0.100	0.400	0.750	-0.050
R5432V418BC	4.180	4.080	4.180	4.180	2.500	3.000	0.100	0.400	0.750	-0.050
R5432V419BD	3.900	3.800	3.500	3.500	2.500	3.000	0.100	0.300	0.500	-0.100
R5432V420BD	4.350	4.050	4.200	4.200	2.400	2.700	0.100	0.250	0.418	-0.100
R5432V501BA	3.900	3.700	3.800	3.600	2.000	2.300	0.200	0.600	1.000	-0.200
R5432V502BA	4.250	4.100	4.200	4.190	2.800	3.000	0.100	0.450	1.000	-0.050
R5432V503BB	4.250	4.150	4.150	4.140	2.700	3.000	0.150	0.300	0.750	-0.050
R5432V504BD	4.250	4.100	4.200	4.190	2.800	3.000	0.100	0.250	0.418	-0.050
R5432V505BD	4.250	4.100	4.200	4.190	2.500	3.000	0.100	0.250	0.418	-0.050
R5432V506BD	3.900	3.800	3.650	3.640	2.000	2.300	0.100	0.250	0.418	-0.050
R5432V507BD	4.215	4.100	4.200	4.180	2.800	3.000	0.100	0.250	0.418	-0.100
R5432V508BA	3.800	3.700	3.600	3.580	2.800	2.900	0.200	0.600	1.000	-0.100
R5432V509BD	3.900	3.800	3.650	3.640	2.000	2.300	0.100	0.250	0.418	-0.100
R5432V510BD	3.900	3.800	3.475	3.465	2.000	2.300	0.100	0.250	0.418	-0.100

*1 : n＝1,2,3,4,5

PIN DESCRIPTIONS

SSOP-24



Pin No	Symbol	Pin Description
1	CTLC	C_{OUT} control pin
2	CTLD	D_{OUT} control pin
3	C_{OUT}	Output pin of overcharge detection, Pch OPEN DRAIN output
4	VMP	Pin for charger negative input
5	DRAIN	Release from Excess discharge-current threshold Pin
6	D_{OUT}	Output pin of overdischarge detection,CMOS output
7	SENS	Current sense pin
8	CTLT	Disconnection detection movement interval setting capacitance pin
9	V_{SS}	V_{SS} pin. Ground pin for the IC
10	CT1	tV_{DET2} setting capacitance connection pin
11	CT2	tV_{DET3} setting capacitance connection pin
12	SEL1	3cell/4cell/5cell alternative pin1
13	SEL2	3cell/4cell/5cell alternative pin2
14	CB5	CELL5 Cell balance Control pin
15	V_{C5}	Positive terminal pin for Cell5
16	CB4	CELL4 Cell balance Control pin
17	V_{C4}	Positive terminal pin for Cell4
18	CB3	CELL3 Cell balance Control pin
19	V_{C3}	Positive terminal pin for Cell3
20	CB2	CELL2 Cell balance Control pin
21	V_{C2}	Positive terminal pin for Cell2
22	CB1	CELL1 Cell balance Control pin
23	V_{C1}	Positive terminal pin for Cell1
24	V_{DD}	V_{DD} pin

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating	Unit
V_{DD}	Supply voltage	-0.3 to 30	V
Input voltage			
V_{C1}	Positive input pin for Cell1	V_{C2}-0.3 to V_{C2}+6.5	V
V_{C2}	Positive input pin for Cell2	V_{C3}-0.3 to V_{C3}+6.5	V
V_{C3}	Positive input pin for Cell3	V_{C4}-0.3 to V_{C4}+6.5	V
V_{C4}	Positive input pin for Cell4	V_{C5}-0.3 to V_{C5}+6.5	V
V_{C5}	Positive input pin for Cell5	-0.3 to 6.5	V
VMP	Charger negative terminal input pin	-0.3 to 30.0	V
V_{SEL1}	3Cell/4Cell/5Cell alternative pin1	-0.3 to V_{DD}+0.3	V
V_{SEL2}	3Cell/4Cell/5Cell alternative pin2	-0.3 to V_{DD}+0.3	V
V_{CTLC}	C_{OUT} control pin	-0.3 to V_{DD}+25 -0.3 to 48	V
V_{CTLD}	D_{OUT} control pin	-0.3 to V_{DD}+25 -0.3 to 48	V
V_{SENSE}	Current sense pin	-0.3 to V_{DD}+0.3	V
V_{CT1}	Delay time setting pin1	-0.3 to 3.5	V
V_{CT2}	Delay time setting pin2	-0.3 to 3.5	V
V_{CTLT}	Disconnection detection movement interval setting capacitance pin	-0.3 to 3.5	V
Output voltage			
V_{COUT}	Output pin of overcharge detection,CMOS output	V_{DD}-30 to V_{DD}+0.3	V
V_{DOUT}	Output pin of overdischarge detection,CMOS output	-0.3 to V_{OH2}+0.3	V
V_{DRAIN}	Release from Excess discharge-current threshold Pin	-0.3 to V_{OH3}+0.3	V
V_{CB1}	Cell balance Control pin for Cell1	V_{C2}-0.3 to V_{C2}+6.5	V
V_{CB2}	Cell balance Control pin for Cell2	V_{C3}-0.3 to V_{C3}+6.5	V
V_{CB3}	Cell balance Control pin for Cell3	V_{C4}-0.3 to V_{C4}+6.5	V
V_{CB4}	Cell balance Control pin for Cell4	V_{C5}-0.3 to V_{C5}+6.5	V
V_{CB5}	Cell balance Control pin for Cell5	-0.3 to 6.5	V
P_D	Power dissipation(1)	770	mW
Ta	Operating temperature range	-40 to 85	°C
Tstg	Storage temperature range	-55 to 125	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field.
The functional operations at or over these absolute maximum ratings are not assured.

(1) Refer to *POWER DISSIPATION* for detailed information.

ELECTRICAL CHARACTERISTICS

- **R5432VxxxBA**

Unless otherwise specified, Ta=25°C

Symbol	Items	Conditions	Min.	Typ.	Max.	Unit	Circuit
V_{DD1}	Operating input voltage	V_{DD}-V_{SS}	2		25	V	-
$V_{DET1}n$	CELLn Overcharge threshold (n=1,2,3,4,5)	Detect rising edge of supply voltage	$V_{DET1}n$ -0.025	$V_{DET1}n$	$V_{DET1}n$ +0.025	V	A
$V_{REL1}n$	CELLn Overcharge released Voltage (n=1,2,3,4,5)	Detect falling edge of supply voltage	$V_{REL1}n$ -0.050	$V_{REL1}n$	$V_{REL1}n$ +0.050	V	A
tV_{DET1}	Output delay of overcharge	V_{DD}=V_{C1},$V_{CELL}n$=3.5V (n=2,3,4,5), V_{CELL1}=3.5V→4.5V	0.7	1.0	1.3	s	B
tV_{REL1}	Output delay of release from overcharge	V_{DD}=V_{C1}, $V_{CELL}n$=3.5V (n=2,3,4,5), V_{CELL1}=4.5V→3.5V	11	16	21	ms	B
$V_{CBD}n$	CELLn balance threshold (n=1,2,3,4,5)	Detect rising edge of supply voltage	$V_{CBD}n$ -0.025	$V_{CBD}n$	$V_{CBD}n$ +0.025	V	C
$V_{CBR}n$	CELLn balance released threshold (n=1,2,3,4,5)	Detect falling edge of supply voltage	$V_{CBR}n$ -0.050	$V_{CBR}n$	Lower of $V_{CBR}n$ +0.050 or $V_{CBD}n$ +0.025	V	C
$V_{DET2}n$	CELLn Overdischarge threshold (n=1,2,3,4,5)	Detect falling edge of supply voltage	$V_{DET2}n$ ×0.975	$V_{DET2}n$	$V_{DET2}n$ ×1.025	V	D
$V_{REL2}n$	CELLn Overdischarge released Voltage (n=1,2,3,4,5)	Detect rising edge of supply voltage	$V_{REL2}n$ ×0.975	$V_{REL2}n$	$V_{REL2}n$ ×1.025	V	D
I_{CT1}	CT1 charge Current	V_{DD}=V_{C1}, $V_{CELL}n$=3.5V (n=2, 3, 4, 5), V_{CELL1}=3.5V→1.5V	350	500	650	nA	E
V_{DCT1}	CT1 detector voltage	V_{DD}=V_{C1}, $V_{CELL}n$=3.5V (n=2, 3, 4, 5), V_{CELL1}=1.5V	1.48	1.85	2.22	V	F
tV_{DET2}	Output delay of overdischarge	tV_{DET2}=C_{CT1}×V_{DCT1}/I_{CT1} C_{CT1}=33nF	89	128	167	ms	-
tV_{REL2}	Output delay of release from overdischarge	V_{DD}=V_{C1}, $V_{CELL}n$=3.5V (n=1,2,3,4,5), VMP=4.0V V_{CELL1}=1.5V→3.5V	0.7	1.2	1.7	ms	G
V_{DET31}	Excess discharge-current threshold1	V_{DD}=V_{C1}, $V_{CELL}n$=3.5V (n=1,2,3,4,5), VMP=4.0V Detect rising edge of supply voltage	V_{DET31} -0.020	V_{DET31}	V_{DET31} +0.020	V	H
V_{DET32}	Excess discharge-current Threshold2	V_{DD}=V_{C1}, $V_{CELL}n$=3.5V (n=1,2,3,4,5), VMP=4.0V Detect rising edge of supply voltage	0.500	0.600	0.700	V	I
V_{REL3}	Output delay of release from Excess discharge-current threshold	V_{DD}=V_{C1}, $V_{CELL}n$=3.5V (n=1,2,3,4,5), SENSE=0V Detect falling edge of supply voltage	V_{DET31} ×0.50	V_{DET31} ×0.75	V_{DET31} ×1.00	V	H
I_{CT231}	CT2 Charge Current1	V_{DD}=V_{C1}, $V_{CELL}n$ =3.5V (n=1,2,3,4,5) SENSE=V_{SS}→0.4V	350	500	650	nA	I
I_{CT232}	CT2 Charge Current2	V_{DD}=V_{C1}, $V_{CELL}n$ =3.5V (n=1,2,3,4,5) SENSE=V_{SS}→0.7V	2.0	3.0	4.0	μA	I
V_{DCT2}	CT2 Charge voltage	V_{DD}=V_{C1}, $V_{CELL}n$ =3.5V (n=2,3,4,5) SENSE=0.4V, VMP=4.0V	1.23	1.55	1.87	V	J
tV_{DET31}	Output delay of Excess discharge-current threshold1	t_{VDET31}=C_{CT2}×V_{DCT2}/I_{CT231} C_{CT2}=3.3nF	7.3	10.8	14.7	ms	-
tV_{DET32}	Output delay of Excess discharge-current Threshold2	t_{VDET32}=C_{CT2}×V_{DCT2}/I_{CT232} C_{CT2}=3.3nF	1.25	1.8	2.4	ms	-
tV_{REL3}	Output delay of release from Excess discharge-current Threshold	V_{DD}=V_{C1}, $V_{CELL}n$=3.5V (n=1,2,3,4,5) SENS=0.4V, VMP= 4.0V	0.7	1.2	1.7	ms	H

Symbol	Items	Conditions	Min.	Typ.	Max.	Unit	Circuit
Vshort	Short protection voltage	V_{DD}=V_{C1}, V_{CELL}n=3.5V (n=1,2,3,4,5), VMP=4.0V Detect rising of supply voltage	0.7	1.0	1.7	V	K
tshort	Output Delay of Short protection	V_{DD}=V_{C1}, V_{CELL}n =3.5V (n=1,2,3,4,5) SENS=0.0V→2.0V, VMP=4.0V	180	300	550	μs	K
V_{DET4}	Excess charge-current threshold	V_{DD}=V_{C1}, V_{CELL}n=3.5V (n=1,2,3,4,5), VMP=-1.0V Detect falling edge of supply voltage	V_{DET4} -0.030	V_{DET4}	V_{DET4} +0.030	V	L
tV_{DET4}	Output delay of Excess charge-current threshold	V_{DD}=V_{C1}, V_{CELL}n =3.5V (n=1,2,3,4,5) SENS=0.0V→-1.0V	5	8	11	ms	L
tV_{rel4}	Output delay of release from Excess charge-current threshold	V_{DD}=V_{C1}, V_{CELL}n =3.5V (n=1,2,3,4,5) SENS=V_{SS},VMP=-1.0V→1.0V	0.7	1.2	1.7	ms	L
V_{IH1}	SEL1 pin “H” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{DD} -0.3		V_{DD} +0.3	V	M
V_{IM1}	SEL1 pin “M” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	4.0		V_{DD}/2 -0.5V	V	M
V_{IL1}	SEL1 pin “L” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{SS} -0.3		V_{SS} +1.0	V	M
V_{IH2}	SEL2 pin “H” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{DD} -0.3		V_{DD} +0.3	V	N
V_{IM2}	SEL2 pin “M” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	4.0		V_{DD}/2 -0.5V	V	N
V_{IL2}	SEL2 pin “L” input voltage	V_{DD}=V_{C}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{SS} -0.3		V_{SS} +0.3	V	N
C_{TLC1H}	C_{TLC} pin “H1” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{DD} +2.0			V	O
C_{TLC2H}	C_{TLC} pin “H2” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{DD} -0.3		V_{DD} +0.3	V	O
C_{TLC1L}	C_{TLC} pin “L” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{SS} -0.3		V_{SS} +0.3	V	O
C_{TLD1H}	C_{TLD} pin “H1” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{DD} +2.0			V	P
C_{TLD2H}	C_{TLD} pin “H2” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{DD} -0.3		V_{DD} +0.3	V	P
C_{TLD1L}	C_{TLD} pin “L” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{SS} -0.3		V_{SS} +0.3	V	P
V_{OL2}	D_{OUT} Nch ON voltage	I_{OL}=50μA, V_{DD}=V_{C1}, C_{TLD}=V_{DD} V_{CELL}n =3.2V (n=1,2,3,4,5)		0.1	0.5	V	Q
V_{OL3}	DRAIN Nch ON voltage	I_{OL}=50μA, V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)		0.1	0.5	V	R
V_{OL4}	CB1 Nch ON voltage	I_{OL}=50μA, V_{DD}=V_{C1}, V_{CELL}n=3.2V (n=1,2,3,4,5)		V_{C2} +0.2	V_{C2} +0.5	V	S
V_{OL5}	CB2 Nch ON voltage	I_{OL}=50μA, V_{DD}=V_{C1}, V_{CELL}n=3.2V (n=1,2,3,4,5)		V_{C3} +0.2	V_{C3} +0.5	V	S
V_{OL6}	CB3 Nch ON voltage	I_{OL}=50μA, V_{DD}=V_{C1}, V_{CELL}n=3.2V (n=1,2,3,4,5)		V_{C4} +0.2	V_{C4} +0.5	V	S
V_{OL7}	CB4 Nch ON voltage	I_{OL}=50μA, V_{DD}=V_{C1}, V_{CELL}n=3.2V (n=1,2,3,4,5)		V_{C5} +0.2	V_{C5} +0.5	V	S
V_{OL8}	CB5 Nch ON voltage	I_{OL}=50μA, V_{DD}=V_{C1}, V_{CELL}n=3.2V (n=1,2,3,4,5)		0.2	0.5	V	S

Symbol	Items	Conditions	Min.	Typ.	Max.	Unit	Circuit
V_{OH1}	C_{OUT} Pch ON voltage	I_{OH}=-50μA, V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5) C_{TLC}=V_{SS}	V_{DD} -0.5	V_{DD} -0.1		V	T
V_{VR12}	VR 12V output voltage (*1)	I_{OH}=-5μA, V_{DD}=V_{C1}, C_{TLD}=V_{SS}, V_{CELL}=3.2V (n=1, 2, 3, 4, 5) Measured to draw the current through D_{OUT}	10	12	14	V	U
V_{OH2}	D_{OUT} Pch ON voltage (*1)	I_{OH}=-50μA, V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5) C_{TLD}= V_{SS}	V_{VR12} -0.5V	V_{VR12} -0.1V		V	U
V_{OH3}	DRAIN Pch ON voltage (*1)	I_{OH}=-50μA, V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5) SENS =VMP =4.0V	V_{VR12} -0.5V	V_{VR12} -0.1V		V	V
V_{OH4}	CB1 Pch ON voltage	I_{OH}=-50μA, V_{DD}=V_{C1}, V_{C1}=4.5V, V_{CELL}n=3.2V (n=2, 3, 4, 5)	V_{C1} -0.5	V_{C1} -0.3		V	W
V_{OH5}	CB2 Pch ON voltage	I_{OH}=-50μA, V_{DD}=V_{C1}, V_{C1}=4.5V, V_{CELL}n=3.2V (n=1, 3, 4, 5)	V_{C2} -0.5	V_{C2} -0.3		V	W
V_{OH6}	CB3 Pch ON voltage	I_{OH}=-50μA, V_{DD}=V_{C1}, V_{C1}=4.5V, V_{CELL}n=3.2V (n=1, 2, 4, 5)	V_{C3} -0.5	V_{C3} -0.3		V	W
V_{OH7}	CB4 Pch ON voltage	I_{OH}=-50μA, V_{DD}=V_{C1}, V_{C1}=4.5V, V_{CELL}n=3.2V (n=1, 2, 3, 5)	V_{C4} -0.5	V_{C4} -0.3		V	W
V_{OH8}	CB5 Pch ON voltage	I_{OH}=-50μA, V_{DD}=V_{C1}, V_{C1}=4.5V, V_{CELL}n=3.2V (n=1, 2, 3, 4)	V_{C5} -0.5	V_{C5} -0.3		V	W
I_{LCOUT}	C_{OUT} pin off leak current	V_{DD}=V_{C1}, V_{CELL}n=3.2V (n=1, 2, 3, 4, 5) C_{TLC}=V_{DD}, C_{OUT}=-14V	-0.1			μA	X
I_{CTLT}	C_{TLT} Charge Current	V_{DD}=V_{C1}, V_{CELL}n=3.2V (n=1, 2, 3, 4, 5)	145	205	264	nA	Y
V_{DTLT}	C_{TLT} detector threshold	V_{DD}=V_{C1}, V_{CELL}n=3.2V (n=1, 2, 4, 5) V_{C3}=V_{D1}+0.2V	1.58	2.00	2.42	V	Z
V_{RTLT}	C_{TLT} released voltage	V_{DD}=V_{C1}, V_{CELL}n=3.2V (n=1, 2, 3, 4, 5)	0.07	0.13	0.19	V	Z
tLT	Disconnection detection Test Interval	C_{CTLT}×(V_{DTLT}-V_{RTLT})/I_{CTLT} C_{CTLT} =3.3μF	21	30	39	s	-
I_{SS1}	Supply Currnt1	V_{DD}=V_{C1},C_{OUT}=OPEN V_{CELL}n=V_{DET1}n-0.4V (n=1, 2, 3, 4, 5)		12	30	μA	a
I_{SS2}	Supply Currnt2	V_{DD}=V_{C1},C_{OUT}=OPEN V_{CELL}n=1.5V (n=1, 2, 3, 4, 5)		10	25	μA	a

∗ V_{CELL}n=CELLn voltage n=1, 2, 3, 4, 5

(*1) If VDD pin voltage becomes lower than the output of the regulator, the output voltage becomes almost equal to VDD.

RECOMMENDED OPERATING CONDITIONS (ELECTRICAL CHARACTERISTICS)

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. The semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

- **R5432VxxxBB/BC**

Unless otherwise specified, Ta=25°C

Symbol	Items	Conditions	Min.	Typ.	Max.	Unit	Circuit
V_{DD1}	Operating input voltage	V_{DD}-V_{SS}	2		25	V	-
$V_{DET1}n$	CELLn Overcharge threshold (n=1,2,3,4,5)	Detect rising edge of supply voltage	$V_{DET1}n$ -0.025	$V_{DET1}n$	$V_{DET1}n$ +0.025	V	A
$V_{REL1}n$	CELLn Overcharge released Voltage (n=1,2,3,4,5)	Detect falling edge of supply voltage	$V_{REL1}n$ -0.050	$V_{REL1}n$	$V_{REL1}n$ +0.050	V	A
tV_{DET1}	Output delay of overcharge	V_{DD}=V_{C1},$V_{CELL}n$=3.5V (n=2,3,4,5), V_{CELL1}=3.5V→4.5V	0.7	1.0	1.3	s	B
tV_{REL1}	Output delay of release from overcharge	V_{DD}=V_{C1}, $V_{CELL}n$=3.5V (n=2,3,4,5), V_{CELL1}=4.5V→3.5V	11	16	21	ms	B
$V_{CBD}n$	CELLn balance threshold (n=1,2,3,4,5)	Detect rising edge of supply voltage	$V_{CBD}n$ -0.025	$V_{CBD}n$	$V_{CBD}n$ +0.025	V	C
$V_{CBR}n$	CELLn balance released threshold (n=1,2,3,4,5)	Detect falling edge of supply voltage	$V_{CBR}n$ -0.050	$V_{CBR}n$	Lower of $V_{CBR}n$ +0.050 or $V_{CBD}n$ +0.025	V	C
$V_{DET2}n$	CELLn Overdischarge threshold (n=1,2,3,4,5)	Detect falling edge of supply voltage	$V_{DET2}n$ ×0.975	$V_{DET2}n$	$V_{DET2}n$ ×1.025	V	D
$V_{REL2}n$	CELLn Overdischarge released Voltage (n=1,2,3,4,5)	Detect rising edge of supply voltage	$V_{REL2}n$ ×0.975	$V_{REL2}n$	$V_{REL2}n$ ×1.025	V	D
I_{CT1}	CT1 charge Current	V_{DD}=V_{C1}, $V_{CELL}n$=3.5V (n=2, 3, 4, 5), V_{CELL1}=3.5V→1.5V	350	500	650	nA	E
V_{DCT1}	CT1 detector voltage	V_{DD}=V_{C1}, $V_{CELL}n$=3.5V (n=2, 3, 4, 5), V_{CELL1}=1.5V	1.48	1.85	2.22	V	F
tV_{DET2}	Output delay of overdischarge	tV_{DET2}=C_{CT1}×V_{DCT1}/I_{CT1} C_{CT1}=33nF	89	128	167	ms	-
tV_{REL2}	Output delay of release from overdischarge	V_{DD}=V_{C1}, $V_{CELL}n$=3.5V (n=1,2,3,4,5), VMP=4.0V V_{CELL1}=1.5V→3.5V	0.7	1.2	1.7	ms	G
V_{DET31}	Excess discharge-current threshold1	V_{DD}=V_{C1}, $V_{CELL}n$=3.5V (n=1,2,3,4,5), VMP=4.0V Detect rising edge of supply voltage	V_{DET31} -0.020	V_{DET31}	V_{DET31} +0.020	V	H
V_{DET32}	Excess discharge-current Threshold2	V_{DD}=V_{C1}, $V_{CELL}n$=3.5V (n=1,2,3,4,5), VMP=4.0V Detect rising edge of supply voltage	V_{DET32} -0.070	V_{DET32}	V_{DET32} +0.070	V	I
V_{REL3}	Output delay of release from Excess discharge-current threshold	V_{DD}=V_{C1}, $V_{CELL}n$=3.5V (n=1,2,3,4,5), SENSE=0V Detect falling edge of supply voltage	V_{DET31} ×0.50	V_{DET31} ×0.75	V_{DET31} ×1.00	V	H
I_{CT231}	CT2 Charge Current1	V_{DD}=V_{C1}, $V_{CELL}n$ =3.5V (n=1,2,3,4,5) SENSE=V_{SS}→0.4V	350	500	650	nA	I
I_{CT232}	CT2 Charge Current2	V_{DD}=V_{C1}, $V_{CELL}n$ =3.5V (n=1,2,3,4,5) SENSE=V_{SS}→0.7V	2.0	3.0	4.0	μA	I
V_{DCT2}	CT2 Charge voltage	V_{DD}=V_{C1}, $V_{CELL}n$ =3.5V (n=2,3,4,5) SENSE=0.4V, VMP=4.0V	1.23	1.55	1.87	V	J
tV_{DET31}	Output delay of Excess discharge-current threshold1	t_{VDET31}=C_{CT2}×V_{DCT2}/I_{CT231} C_{CT2}=3.3nF	7.3	10.8	14.7	ms	-
tV_{DET32}	Output delay of Excess discharge-current Threshold2	t_{VDET32}=C_{CT2}×V_{DCT2}/I_{CT232} C_{CT2}=3.3nF	1.25	1.80	2.40	ms	-
tV_{REL3}	Output delay of release from Excess discharge-current Threshold	V_{DD}=V_{C1}, $V_{CELL}n$=3.5V (n=1,2,3,4,5) SENS=0.4V, VMP= 4.0V	0.7	1.2	1.7	ms	H

Symbol	Items	Conditions	Min.	Typ.	Max.	Unit	Circuit
Vshort	Short protection voltage	V_{DD}=V_{C1}, V_{CELL}n=3.5V (n=1,2,3,4,5), VMP=4.0V Detect rising of supply voltage	0.7	1.0	1.7	V	K
tshort	Output Delay of Short protection	V_{DD}=V_{C1}, V_{CELL}n =3.5V (n=1,2,3,4,5) SENS=0.0V→2.0V,VMP=4.0V	180	300	550	µs	K
V_{DET4}	Excess charge-current threshold	V_{DD}=V_{C1}, V_{CELL}n=3.5V (n=1,2,3,4,5), VMP=-1.0V Detect falling edge of supply voltage	V_{DET4} -0.030	V_{DET4}	V_{DET4} +0.030	V	L
tV_{DET4}	Output delay of Excess charge-current threshold	V_{DD}=V_{C1}, V_{CELL}n =3.5V (n=1,2,3,4,5) SENS=0.0V→-1.0V	5	8	11	ms	L
tV_{rel4}	Output delay of release from Excess charge-current threshold	V_{DD}=V_{C1}, V_{CELL}n =3.5V (n=1,2,3,4,5) SENS=V_{SS},VMP=-1.0V→1.0V	0.7	1.2	1.7	ms	L
V_{IH1}	SEL1 pin “H” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{DD} -0.3		V_{DD} +0.3	V	M
V_{IM1}	SEL1 pin “M” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	4.0		V_{DD}/2 -0.5V	V	M
V_{IL1}	SEL1 pin “L” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{SS} -0.3		V_{SS} +1.0	V	M
V_{IH2}	SEL2 pin “H” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{DD} -0.3		V_{DD} +0.3	V	N
V_{IM2}	SEL2 pin “M” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	4.0		V_{DD}/2 -0.5V	V	N
V_{IL2}	SEL2 pin “L” input voltage	V_{DD}=V_{C}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{SS} -0.3		V_{SS} +0.3	V	N
C_{TLC1H}	C_{TLC} pin “H1” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{DD} +2.0			V	O
C_{TLC2H}	C_{TLC} pin “H2” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{DD} -0.3		V_{DD} +0.3	V	O
C_{TLC1L}	C_{TLC} pin “L” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{SS} -0.3		V_{SS} +0.3	V	O
C_{TLD1H}	C_{TLD} pin “H1” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{DD} +2.0			V	P
C_{TLD2H}	C_{TLD} pin “H2” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{DD} -0.3		V_{DD} +0.3	V	P
C_{TLD1L}	C_{TLD} pin “L” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{SS} -0.3		V_{SS} +0.3	V	P
V_{OL2}	D_{OUT} Nch ON voltage	I_{OL}=50µA, V_{DD}=V_{C1}, C_{TLD}=V_{DD} V_{CELL}n =3.2V (n=1,2,3,4,5)		0.1	0.5	V	Q
V_{OL3}	DRAIN Nch ON voltage	I_{OL}=50µA, V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)		0.1	0.5	V	R
V_{OL4}	CB1 Nch ON voltage	I_{OL}=50µA, V_{DD}=V_{C1}, V_{CELL}n=3.2V (n=1,2,3,4,5)		V_{C2} +0.2	V_{C2} +0.5	V	S
V_{OL5}	CB2 Nch ON voltage	I_{OL}=50µA, V_{DD}=V_{C1}, V_{CELL}n=3.2V (n=1,2,3,4,5)		V_{C3} +0.2	V_{C3} +0.5	V	S
V_{OL6}	CB3 Nch ON voltage	I_{OL}=50µA, V_{DD}=V_{C1}, V_{CELL}n=3.2V (n=1,2,3,4,5)		V_{C4} +0.2	V_{C4} +0.5	V	S
V_{OL7}	CB4 Nch ON voltage	I_{OL}=50µA, V_{DD}=V_{C1}, V_{CELL}n=3.2V (n=1,2,3,4,5)		V_{C5} +0.2	V_{C5} +0.5	V	S
V_{OL8}	CB5 Nch ON voltage	I_{OL}=50µA, V_{DD}=V_{C1}, V_{CELL}n=3.2V (n=1,2,3,4,5)		0.2	0.5	V	S
V_{OH1}	C_{OUT} Pch ON voltage	I_{OH}=-50µA, V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5) C_{TLC}=V_{SS}	V_{DD}-0.5	V_{DD}-0.1		V	T

Symbol	Items	Conditions	Min.	Typ.	Max.	Unit	Circuit
V_{VR12}	VR 12V output voltage(*1)	I_{OH}=-5μA, V_{DD}=V_{C1}, C_{TLD}=V_{SS}, V_{CELL}=3.2V (n=1, 2, 3, 4, 5) Measured to draw the current through D_{OUT}	10	12	14	V	U
V_{OH2}	D_{OUT} Pch ON voltage(*1)	I_{OH}=-50μA, V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5) C_{TLD}= V_{SS}	V_{VR12} -0.5V	V_{VR12} -0.1V		V	U
V_{OH3}	DRAIN Pch ON voltage(*1)	I_{OH}=-50μA, V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5) SENS =VMP =4.0V	V_{VR12} -0.5V	V_{VR12} -0.1V		V	V
V_{OH4}	CB1 Pch ON voltage	I_{OH}=-50μA, V_{DD}=V_{C1}, V_{C1}=4.5V, V_{CELL}n=3.2V (n=2, 3, 4, 5)	V_{C1} -0.5	V_{C1} -0.3		V	W
V_{OH5}	CB2 Pch ON voltage	I_{OH}=-50μA, V_{DD}=V_{C1}, V_{C1}=4.5V, V_{CELL}n=3.2V (n=1, 3, 4, 5)	V_{C2} -0.5	V_{C2} -0.3		V	W
V_{OH6}	CB3 Pch ON voltage	I_{OH}=-50μA, V_{DD}=V_{C1}, V_{C1}=4.5V, V_{CELL}n=3.2V (n=1, 2, 4, 5)	V_{C3} -0.5	V_{C3} -0.3		V	W
V_{OH7}	CB4 Pch ON voltage	I_{OH}=-50μA, V_{DD}=V_{C1}, V_{C1}=4.5V, V_{CELL}n=3.2V (n=1, 2, 3, 5)	V_{C4} -0.5	V_{C4} -0.3		V	W
V_{OH8}	CB5 Pch ON voltage	I_{OH}=-50μA, V_{DD}=V_{C1}, V_{C1}=4.5V, V_{CELL}n=3.2V (n=1, 2, 3, 4)	V_{C5} -0.5	V_{C5} -0.3		V	W
I_{LCOUT}	C_{OUT} pin off leak current	V_{DD}=V_{C1}, V_{CELL}n=3.2V (n=1, 2, 3, 4, 5) C_{TLC}=V_{DD}, C_{OUT}=-14V	-0.1			μA	X
I_{CTLT}	C_{TLT} Charge Current	V_{DD}=V_{C1}, V_{CELL}n=3.2V (n=1, 2, 3, 4, 5)	145	205	264	nA	Y
V_{DTLT}	C_{TLT} detector threshold	V_{DD}=V_{C1}, V_{CELL}n=3.2V (n=1, 2, 4, 5) V_{C3}=V_{D1}+0.2V	1.58	2.00	2.42	V	Z
V_{RTLT}	C_{TLT} released voltage	V_{DD}=V_{C1}, V_{CELL}n=3.2V (n=1, 2, 3, 4, 5)	0.07	0.13	0.19	V	Z
tLT	Disconnection detection Test Interval	C_{CTLT}×(V_{DTLT}-V_{RTLT})/I_{CTLT} C_{CTLT} =3.3μF	21	30	39	s	-
Vnochgn	CELLn charge inhibit maximum voltage (n=1,2,3,4,5)-for R5432V4xxxB	VDD=VC1			1.100	V	A
I_{SS1}	Supply Currnt1	V_{DD}=V_{C1},C_{OUT}=OPEN V_{CELL}n=V_{DET1}n-0.4V (n=1, 2, 3, 4, 5)		12	30	μA	a
I_{SS2}	Supply Currnt2	V_{DD}=V_{C1},C_{OUT}=OPEN V_{CELL}n=1.5V (n=1, 2, 3, 4, 5)		10	25	μA	a

∗ V_{CELL}n=CELLn voltage n=1, 2, 3, 4, 5

(*1) If VDD pin voltage becomes lower than the output of the regulator, the output voltage becomes almost equal to VDD.

- **R5432VxxxBD**

Unless otherwise specified, Ta=25°C

Symbol	Items	Conditions	Min.	Typ.	Max.	Unit	Circuit
V_{DD1}	Operating input voltage	V_{DD}-V_{SS}	2		25	V	-
$V_{DET1}n$	CELLn Overcharge threshold (n=1,2,3,4,5)	Detect rising edge of supply voltage	$V_{DET1}n$ -0.025	$V_{DET1}n$	$V_{DET1}n$ +0.025	V	A
$V_{REL1}n$	CELLn Overcharge released Voltage (n=1,2,3,4,5)	Detect falling edge of supply voltage	$V_{REL1}n$ -0.050	$V_{REL1}n$	$V_{REL1}n$ +0.050	V	A
tV_{DET1}	Output delay of overcharge	V_{DD}=V_{C1},$V_{CELL}n$=3.5V (n=2,3,4,5), V_{CELL1}=3.5V→4.5V	0.7	1.0	1.3	s	B
tV_{REL1}	Output delay of release from overcharge	V_{DD}=V_{C1}, $V_{CELL}n$=3.5V (n=2,3,4,5), V_{CELL1}=4.5V→3.5V	11	16	21	ms	B
$V_{CBD}n$	CELLn balance threshold (n=1,2,3,4,5)	Detect rising edge of supply voltage	$V_{CBD}n$ -0.025	$V_{CBD}n$	$V_{CBD}n$ +0.025	V	C
$V_{CBR}n$	CELLn balance released threshold (n=1,2,3,4,5)	Detect falling edge of supply voltage	$V_{CBR}n$ -0.050	$V_{CBR}n$	Lower of $V_{CBR}n$ +0.050 or $V_{CBD}n$ +0.025	V	C
$V_{DET2}n$	CELLn Overdischarge threshold (n=1,2,3,4,5)	Detect falling edge of supply voltage	$V_{DET2}n$ ×0.975	$V_{DET2}n$	$V_{DET2}n$ ×1.025	V	D
$V_{REL2}n$	CELLn Overdischarge released Voltage (n=1,2,3,4,5)	Detect rising edge of supply voltage	$V_{REL2}n$ ×0.975	$V_{REL2}n$	$V_{REL2}n$ ×1.025	V	D
I_{CT1}	CT1 charge Current	V_{DD}=V_{C1}, $V_{CELL}n$=3.5V (n=2, 3, 4, 5), V_{CELL1}=3.5V→1.5V	350	500	650	nA	E
V_{DCT1}	CT1 detector voltage	V_{DD}=V_{C1}, $V_{CELL}n$=3.5V (n=2, 3, 4, 5), V_{CELL1}=1.5V	1.48	1.85	2.22	V	F
tV_{DET2}	Output delay of overdischarge	tV_{DET2}=C_{CT1}×V_{DCT1}/I_{CT1} C_{CT1}=33nF	89	128	167	ms	-
tV_{REL2}	Output delay of release from overdischarge	V_{DD}=V_{C1}, $V_{CELL}n$=3.5V (n=1,2,3,4,5), VMP=4.0V V_{CELL1}=1.5V→3.5V	0.7	1.2	1.7	ms	G
V_{DET31}	Excess discharge-current threshold1	V_{DD}=V_{C1}, $V_{CELL}n$=3.5V (n=1,2,3,4,5), VMP=4.0V Detect rising edge of supply voltage	V_{DET31} -0.020	V_{DET31}	V_{DET31} +0.020	V	H
V_{DET32}	Excess discharge-current Threshold2	V_{DD}=V_{C1}, $V_{CELL}n$=3.5V (n=1,2,3,4,5), VMP=4.0V Detect rising edge of supply voltage	V_{DET32} -0.055	V_{DET32}	V_{DET32} +0.055	V	I
V_{REL3}	Output delay of release from Excess discharge-current threshold	V_{DD}=V_{C1}, $V_{CELL}n$=3.5V (n=1,2,3,4,5), SENSE=0V Detect falling edge of supply voltage	V_{DET31} ×0.50	V_{DET31} ×0.75	V_{DET31} ×1.00	V	H
I_{CT231}	CT2 Charge Current1	V_{DD}=V_{C1}, $V_{CELL}n$ =3.5V (n=1,2,3,4,5) SENSE=V_{SS}→0.4V	350	500	650	nA	I
I_{CT232}	CT2 Charge Current2	V_{DD}=V_{C1}, $V_{CELL}n$ =3.5V (n=1,2,3,4,5) SENSE=V_{SS}→0.7V	2.0	3.0	4.0	μA	I
V_{DCT2}	CT2 Charge voltage	V_{DD}=V_{C1}, $V_{CELL}n$ =3.5V (n=2,3,4,5) SENSE=0.4V, VMP=4.0V	1.23	1.55	1.87	V	J
tV_{DET31}	Output delay of Excess discharge-current threshold1	t_{VDET31}=C_{CT2}×V_{DCT2}/I_{CT231} C_{CT2}=3.3nF	7.3	10.8	14.7	ms	-
tV_{DET32}	Output delay of Excess discharge-current Threshold2	t_{VDET32}=C_{CT2}×V_{DCT2}/I_{CT232} C_{CT2}=3.3nF	1.25	1.80	2.40	ms	-
tV_{REL3}	Output delay of release from Excess discharge-current Threshold	V_{DD}=V_{C1}, $V_{CELL}n$=3.5V (n=1,2,3,4,5) SENS=0.4V, VMP= 4.0V	0.7	1.2	1.7	ms	H

Symbol	Items	Conditions	Min.	Typ.	Max.	Unit	Circuit
Vshort	Short protection voltage	V_{DD}=V_{C1}, V_{CELL}n=3.5V (n=1,2,3,4,5), VMP=4.0V Detect rising of supply voltage	Vshort -0.12	V_{DET32} x1.67	Vshort +0.17	V	K
tshort	Output Delay of Short protection	V_{DD}=V_{C1}, V_{CELL}n =3.5V (n=1,2,3,4,5) SENS=0.0V→2.0V, VMP=4.0V	180	300	550	µs	K
V_{DET4}	Excess charge-current threshold	V_{DD}=V_{C1}, V_{CELL}n=3.5V (n=1,2,3,4,5), VMP=-1.0V Detect falling edge of supply voltage	V_{DET4} -0.030	V_{DET4}	V_{DET4} +0.030	V	L
tV_{DET4}	Output delay of Excess charge-current threshold	V_{DD}=V_{C1}, V_{CELL}n =3.5V (n=1,2,3,4,5) SENS=0.0V→-1.0V	5	8	11	ms	L
tV_{rel4}	Output delay of release from Excess charge-current threshold	V_{DD}=V_{C1}, V_{CELL}n =3.5V (n=1,2,3,4,5) SENS=V_{SS},VMP=-1.0V→1.0V	0.7	1.2	1.7	ms	L
V_{IH1}	SEL1 pin “H” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{DD} -0.3		V_{DD} +0.3	V	M
V_{IM1}	SEL1 pin “M” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	4.0		V_{DD}/2 -0.5V	V	M
V_{IL1}	SEL1 pin “L” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{SS} -0.3		V_{SS} +1.0	V	M
V_{IH2}	SEL2 pin “H” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{DD} -0.3		V_{DD} +0.3	V	N
V_{IM2}	SEL2 pin “M” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	4.0		V_{DD}/2 -0.5V	V	N
V_{IL2}	SEL2 pin “L” input voltage	V_{DD}=V_{C}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{SS} -0.3		V_{SS} +0.3	V	N
C_{TLC1H}	C_{TLC} pin “H1” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{DD} +2.0			V	O
C_{TLC2H}	C_{TLC} pin “H2” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{DD} -0.3		V_{DD} +0.3	V	O
C_{TLC1L}	C_{TLC} pin “L” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{SS} -0.3		V_{SS} +0.3	V	O
C_{TLD1H}	C_{TLD} pin “H1” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{DD} +2.0			V	P
C_{TLD2H}	C_{TLD} pin “H2” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{DD} -0.3		V_{DD} +0.3	V	P
C_{TLD1L}	C_{TLD} pin “L” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{SS} -0.3		V_{SS} +0.3	V	P
V_{OL2}	D_{OUT} Nch ON voltage	I_{OL}=50µA, V_{DD}=V_{C1}, C_{TLD}=V_{DD} V_{CELL}n =3.2V (n=1,2,3,4,5)		0.1	0.5	V	Q
V_{OL3}	DRAIN Nch ON voltage	I_{OL}=50µA, V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)		0.1	0.5	V	R
V_{OL4}	CB1 Nch ON voltage	I_{OL}=50µA, V_{DD}=V_{C1}, V_{CELL}n=3.2V (n=1,2,3,4,5)		V_{C2} +0.2	V_{C2} +0.5	V	S
V_{OL5}	CB2 Nch ON voltage	I_{OL}=50µA, V_{DD}=V_{C1}, V_{CELL}n=3.2V (n=1,2,3,4,5)		V_{C3} +0.2	V_{C3} +0.5	V	S
V_{OL6}	CB3 Nch ON voltage	I_{OL}=50µA, V_{DD}=V_{C1}, V_{CELL}n=3.2V (n=1,2,3,4,5)		V_{C4} +0.2	V_{C4} +0.5	V	S
V_{OL7}	CB4 Nch ON voltage	I_{OL}=50µA, V_{DD}=V_{C1}, V_{CELL}n=3.2V (n=1,2,3,4,5)		V_{C5} +0.2	V_{C5} +0.5	V	S
V_{OL8}	CB5 Nch ON voltage	I_{OL}=50µA, V_{DD}=V_{C1}, V_{CELL}n=3.2V (n=1,2,3,4,5)		0.2	0.5	V	S
V_{OH1}	C_{OUT} Pch ON voltage	I_{OH}=-50µA, V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5) C_{TLC}=V_{SS}	V_{DD} -0.5	V_{DD} -0.1		V	T

Symbol	Items	Conditions	Min.	Typ.	Max.	Unit	Circuit
V_{VR12}	VR 12V output voltage(*1)	I_{OH}=-5μA, V_{DD}=V_{C1}, C_{TLD}=V_{SS}, V_{CELL}=3.2V (n=1, 2, 3, 4, 5) Measured to draw the current through D_{OUT}	10	12	14	V	U
V_{OH2}	D_{OUT} Pch ON voltage(*1)	I_{OH}=-50μA, V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5) C_{TLD}= V_{SS}	V_{VR12} -0.5V	V_{VR12} -0.1V		V	U
V_{OH3}	DRAIN Pch ON voltage(*1)	I_{OH}=-50μA, V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5) SENS =VMP =4.0V	V_{VR12} -0.5V	V_{VR12} -0.1V		V	V
V_{OH4}	CB1 Pch ON voltage	I_{OH}=-50μA, V_{DD}=V_{C1}, V_{C1}=4.5V, V_{CELL}n=3.2V (n=2, 3, 4, 5)	V_{C1} -0.5	V_{C1} -0.3		V	W
V_{OH5}	CB2 Pch ON voltage	I_{OH}=-50μA, V_{DD}=V_{C1}, V_{C1}=4.5V, V_{CELL}n=3.2V (n=1, 3, 4, 5)	V_{C2} -0.5	V_{C2} -0.3		V	W
V_{OH6}	CB3 Pch ON voltage	I_{OH}=-50μA, V_{DD}=V_{C1}, V_{C1}=4.5V, V_{CELL}n=3.2V (n=1, 2, 4, 5)	V_{C3} -0.5	V_{C3} -0.3		V	W
V_{OH7}	CB4 Pch ON voltage	I_{OH}=-50μA, V_{DD}=V_{C1}, V_{C1}=4.5V, V_{CELL}n=3.2V (n=1, 2, 3, 5)	V_{C4} -0.5	V_{C4} -0.3		V	W
V_{OH8}	CB5 Pch ON voltage	I_{OH}=-50μA, V_{DD}=V_{C1}, V_{C1}=4.5V, V_{CELL}n=3.2V (n=1, 2, 3, 4)	V_{C5} -0.5	V_{C5} -0.3		V	W
I_{LCOUT}	C_{OUT} pin off leak current	V_{DD}=V_{C1}, V_{CELL}n=3.2V (n=1, 2, 3, 4, 5) C_{TLC}=V_{DD}, C_{OUT}=-14V	-0.1			μA	X
I_{CTLT}	C_{TLT} Charge Current	V_{DD}=V_{C1}, V_{CELL}n=3.2V (n=1, 2, 3, 4, 5)	145	205	264	nA	Y
V_{DTLT}	C_{TLT} detector threshold	V_{DD}=V_{C1}, V_{CELL}n=3.2V (n=1, 2, 4, 5) V_{C3}=V_{D1}+0.2V	1.58	2.00	2.42	V	Z
V_{RTLT}	C_{TLT} released voltage	V_{DD}=V_{C1}, V_{CELL}n=3.2V (n=1, 2, 3, 4, 5)	0.07	0.13	0.19	V	Z
tLT	Disconnection detection Test Interval	C_{CTLT}×(V_{DTLT}-V_{RTLT})/I_{CTLT} C_{CTLT} =3.3μF	21	30	39	s	-
I_{SS1}	Supply Currnt1	V_{DD}=V_{C1},C_{OUT}=OPEN V_{CELL}n=V_{DET1}n-0.4V (n=1, 2, 3, 4, 5)		12	30	μA	a
I_{SS2}	Supply Currnt2	V_{DD}=V_{C1},C_{OUT}=OPEN V_{CELL}n=1.5V (n=1, 2, 3, 4, 5)		10	25	μA	a

∗ V_{CELL}n=CELLn voltage n=1, 2, 3, 4, 5

(*1) If VDD pin voltage becomes lower than the output of the regulator, the output voltage becomes almost equal to VDD.

- **R5432VxxxAD**

Unless otherwise specified, Ta=25°C

Symbol	Items	Conditions	Min.	Typ.	Max.	Unit	Circuit
V_{DD1}	Operating input voltage	V_{DD}-V_{SS}	2		25	V	-
$V_{DET1}n$	CELLn Overcharge threshold (n=1,2,3,4,5)	Detect rising edge of supply voltage	$V_{DET1}n$ -0.025	$V_{DET1}n$	$V_{DET1}n$ +0.025	V	A
$V_{REL1}n$	CELLn Overcharge released Voltage (n=1,2,3,4,5)	Detect falling edge of supply voltage	$V_{REL1}n$ -0.050	$V_{REL1}n$	$V_{REL1}n$ +0.050	V	A
tV_{DET1}	Output delay of overcharge	V_{DD}=V_{C1},$V_{CELL}n$=3.5V (n=2,3,4,5), V_{CELL1}=3.5V→4.5V	0.7	1.0	1.3	S	B
tV_{REL1}	Output delay of release from overcharge	V_{DD}=V_{C1}, $V_{CELL}n$=3.5V (n=2,3,4,5), V_{CELL1}=4.5V→3.5V	11	16	21	ms	B
$V_{CBD}n$	CELLn balance threshold (n=1,2,3,4,5)	Detect rising edge of supply voltage	$V_{CBD}n$ -0.025	$V_{CBD}n$	$V_{CBD}n$ +0.025	V	C
$V_{CBR}n$	CELLn balance released threshold (n=1,2,3,4,5)	Detect falling edge of supply voltage	$V_{CBR}n$ -0.050	$V_{CBR}n$	Lower of $V_{CBR}n$ +0.050 or $V_{CBD}n$ +0.025	V	C
$V_{DET2}n$	CELLn Overdischarge threshold (n=1,2,3,4,5)	Detect falling edge of supply voltage	$V_{DET2}n$ ×0.975	$V_{DET2}n$	$V_{DET2}n$ ×1.025	V	D
$V_{REL2}n$	CELLn Overdischarge released Voltage (n=1,2,3,4,5)	Detect rising edge of supply voltage	$V_{REL2}n$ ×0.975	$V_{REL2}n$	$V_{REL2}n$ ×1.025	V	D
I_{CT1}	CT1 charge Current	V_{DD}=V_{C1}, $V_{CELL}n$=3.5V (n=2, 3, 4, 5), V_{CELL1}=3.5V→1.5V	350	500	650	nA	E
V_{DCT1}	CT1 detector voltage	V_{DD}=V_{C1}, $V_{CELL}n$=3.5V (n=2, 3, 4, 5), V_{CELL1}=1.5V	1.48	1.85	2.22	V	F
tV_{DET2}	Output delay of overdischarge	tV_{DET2}=C_{CT1}×V_{DCT1}/I_{CT1} C_{CT1}=330nF	840	1200	1560	ms	-
tV_{REL2}	Output delay of release from overdischarge	V_{DD}=V_{C1}, $V_{CELL}n$=3.5V (n=1,2,3,4,5), VMP=4.0V V_{CELL1}=1.5V→3.5V	0.7	1.2	1.7	ms	G
V_{DET31}	Excess discharge-current threshold1	V_{DD}=V_{C1}, $V_{CELL}n$=3.5V (n=1,2,3,4,5), VMP=4.0V Detect rising edge of supply voltage	V_{DET31} -0.020	V_{DET31}	V_{DET31} +0.020	V	H
V_{DET32}	Excess discharge-current Threshold2	V_{DD}=V_{C1}, $V_{CELL}n$=3.5V (n=1,2,3,4,5), VMP=4.0V Detect rising edge of supply voltage	V_{DET32} -0.055	V_{DET32}	V_{DET32} +0.055	V	I
V_{REL3}	Output delay of release from Excess discharge-current threshold	V_{DD}=V_{C1}, $V_{CELL}n$=3.5V (n=1,2,3,4,5), SENSE=0V Detect falling edge of supply voltage	V_{DET31} ×0.50	V_{DET31} ×0.75	V_{DET31} ×1.00	V	H
I_{CT231}	CT2 Charge Current1	V_{DD}=V_{C1}, $V_{CELL}n$ =3.5V (n=1,2,3,4,5) SENSE=V_{SS}→0.4V	350	500	650	nA	I
I_{CT232}	CT2 Charge Current2	V_{DD}=V_{C1}, $V_{CELL}n$ =3.5V (n=1,2,3,4,5) SENSE=V_{SS}→0.7V	3.5	5.0	6.5	μA	I
V_{DCT2}	CT2 Charge voltage	V_{DD}=V_{C1}, $V_{CELL}n$ =3.5V (n=2,3,4,5) SENSE=0.4V, VMP=4.0V	1.23	1.55	1.87	V	J
tV_{DET31}	Output delay of Excess discharge-current threshold1	t_{VDET31}=C_{CT2}×V_{DCT2}/I_{CT231} C_{CT2}=330nF	700	1000	1300	ms	-
tV_{DET32}	Output delay of Excess discharge-current Threshold2	t_{VDET32}=C_{CT2}×V_{DCT2}/I_{CT232} C_{CT2}=330nF	7	10	13	ms	-
tV_{REL3}	Output delay of release from Excess discharge-current Threshold	V_{DD}=V_{C1}, $V_{CELL}n$=3.5V (n=1,2,3,4,5) SENS=0.4V, VMP= 4.0V	0.7	1.2	1.7	ms	H

Symbol	Items	Conditions	Min.	Typ.	Max.	Unit	Circuit
Vshort	Short protection voltage	V_{DD}=V_{C1}, V_{CELL}n=3.5V (n=1,2,3,4,5), VMP=4.0V Detect rising of supply voltage	Vshort -0.12	V_{DET32} x1.67	Vshort +0.17	V	K
tshort	Output Delay of Short protection	V_{DD}=V_{C1}, V_{CELL}n =3.5V (n=1,2,3,4,5) SENS=0.0V→2.0V, VMP=4.0V	180	300	550	µs	K
V_{DET4}	Excess charge-current threshold	V_{DD}=V_{C1}, V_{CELL}n=3.5V (n=1,2,3,4,5), VMP=-1.0V Detect falling edge of supply voltage	V_{DET4} -0.030	V_{DET4}	V_{DET4} +0.030	V	L
tV_{DET4}	Output delay of Excess charge-current threshold	V_{DD}=V_{C1}, V_{CELL}n =3.5V (n=1,2,3,4,5) SENS=0.0V→-1.0V	5	8	11	ms	L
tV_{rel4}	Output delay of release from Excess charge-current threshold	V_{DD}=V_{C1}, V_{CELL}n =3.5V (n=1,2,3,4,5) SENS=V_{SS},VMP=-1.0V→1.0V	0.7	1.2	1.7	ms	L
V_{IH1}	SEL1 pin “H” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{DD} -0.3		V_{DD} +0.3	V	M
V_{IM1}	SEL1 pin “M” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	4.0		V_{DD}/2 -0.5V	V	M
V_{IL1}	SEL1 pin “L” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{SS} -0.3		V_{SS} +0.3	V	M
V_{IH2}	SEL2 pin “H” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{DD} -0.3		V_{DD} +0.3	V	N
V_{IM2}	SEL2 pin “M” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	4.0		V_{DD}/2 -0.5V	V	N
V_{IL2}	SEL2 pin “L” input voltage	V_{DD}=V_C, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{SS} -0.3		V_{SS} +0.3	V	N
C_{TLC1H}	C_{TLC} pin “H1” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{DD} +2.0			V	O
C_{TLC2H}	C_{TLC} pin “H2” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{DD} -0.3		V_{DD} +0.3	V	O
C_{TLC1L}	C_{TLC} pin “L” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{SS} -0.3		V_{SS} +0.3	V	O
C_{TLD1H}	C_{TLD} pin “H1” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{DD} +2.0			V	P
C_{TLD2H}	C_{TLD} pin “H2” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{DD} -0.3		V_{DD} +0.3	V	P
C_{TLD1L}	C_{TLD} pin “L” input voltage	V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)	V_{SS} -0.3		V_{SS} +0.3	V	P
V_{OL2}	D_{OUT} Nch ON voltage	I_{OL}=50µA, V_{DD}=V_{C1}, C_{TLD}=V_{DD} V_{CELL}n =3.2V (n=1,2,3,4,5)		0.1	0.5	V	Q
V_{OL3}	DRAIN Nch ON voltage	I_{OL}=50µA, V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5)		0.1	0.5	V	R
V_{OL4}	CB1 Nch ON voltage	I_{OL}=50µA, V_{DD}=V_{C1}, V_{CELL}n=3.2V (n=1,2,3,4,5)		V_{C2} +0.2	V_{C2} +0.5	V	S
V_{OL5}	CB2 Nch ON voltage	I_{OL}=50µA, V_{DD}=V_{C1}, V_{CELL}n=3.2V (n=1,2,3,4,5)		V_{C3} +0.2	V_{C3} +0.5	V	S
V_{OL6}	CB3 Nch ON voltage	I_{OL}=50µA, V_{DD}=V_{C1}, V_{CELL}n=3.2V (n=1,2,3,4,5)		V_{C4} +0.2	V_{C4} +0.5	V	S
V_{OL7}	CB4 Nch ON voltage	I_{OL}=50µA, V_{DD}=V_{C1}, V_{CELL}n=3.2V (n=1,2,3,4,5)		V_{C5} +0.2	V_{C5} +0.5	V	S
V_{OL8}	CB5 Nch ON voltage	I_{OL}=50µA, V_{DD}=V_{C1}, V_{CELL}n=3.2V (n=1,2,3,4,5)		0.2	0.5	V	S
V_{OH1}	C_{OUT} Pch ON voltage	I_{OH}=-50µA, V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5) C_{TLC}=V_{SS}	V_{DD} -0.5	V_{DD} -0.1		V	T

Symbol	Items	Conditions	Min.	Typ.	Max.	Unit	Circuit
V_{VR12}	VR 12V output voltage(*1)	I_{OH}=-5μA, V_{DD}=V_{C1}, C_{TLD}=V_{SS}, V_{CELL}=3.2V (n=1, 2, 3, 4, 5) Measured to draw the current through D_{OUT}	10	12	14	V	U
V_{OH2}	D_{OUT} Pch ON voltage(*1)	I_{OH}=-50μA, V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5) C_{TLD}= V_{SS}	V_{VR12} -0.5V	V_{VR12} -0.1V		V	U
V_{OH3}	DRAIN Pch ON voltage(*1)	I_{OH}=-50μA, V_{DD}=V_{C1}, V_{CELL}n =3.2V (n=1,2,3,4,5) SENS =VMP =4.0V	V_{VR12} -0.5V	V_{VR12} -0.1V		V	V
V_{OH4}	CB1 Pch ON voltage	I_{OH}=-50μA, V_{DD}=V_{C1}, V_{C1}=4.5V, V_{CELL}n=3.2V (n=2, 3, 4, 5)	V_{C1} -0.5	V_{C1} -0.3		V	W
V_{OH5}	CB2 Pch ON voltage	I_{OH}=-50μA, V_{DD}=V_{C1}, V_{C1}=4.5V, V_{CELL}n=3.2V (n=1, 3, 4, 5)	V_{C2} -0.5	V_{C2} -0.3		V	W
V_{OH6}	CB3 Pch ON voltage	I_{OH}=-50μA, V_{DD}=V_{C1}, V_{C1}=4.5V, V_{CELL}n=3.2V (n=1, 2, 4, 5)	V_{C3} -0.5	V_{C3} -0.3		V	W
V_{OH7}	CB4 Pch ON voltage	I_{OH}=-50μA, V_{DD}=V_{C1}, V_{C1}=4.5V, V_{CELL}n=3.2V (n=1, 2, 3, 5)	V_{C4} -0.5	V_{C4} -0.3		V	W
V_{OH8}	CB5 Pch ON voltage	I_{OH}=-50μA, V_{DD}=V_{C1}, V_{C1}=4.5V, V_{CELL}n=3.2V (n=1, 2, 3, 4)	V_{C5} -0.5	V_{C5} -0.3		V	W
I_{LCOUT}	C_{OUT} pin off leak current	V_{DD}=V_{C1}, V_{CELL}n=3.2V (n=1, 2, 3, 4, 5) C_{TLC}=V_{DD}, C_{OUT}=-14V	-0.1			μA	X
I_{CTLT}	C_{TLT} Charge Current	V_{DD}=V_{C1}, V_{CELL}n=3.2V (n=1, 2, 3, 4, 5)	145	205	264	nA	Y
V_{DTLT}	C_{TLT} detector threshold	V_{DD}=V_{C1}, V_{CELL}n=3.2V (n=1, 2, 4, 5) V_{C3}=V_{D1}+0.2V	1.58	2.00	2.42	V	Z
V_{RTLT}	C_{TLT} released voltage	V_{DD}=V_{C1}, V_{CELL}n=3.2V (n=1, 2, 3, 4, 5)	0.07	0.13	0.19	V	Z
tLT	Disconnection detection Test Interval	C_{CTLT}×(V_{DTLT}-V_{RTLT})/I_{CTLT} C_{CTLT} =3.3μF	21	30	39	s	-
I_{SS1}	Supply Currnt1	V_{DD}=V_{C1},C_{OUT}=OPEN V_{CELL}n=V_{DET1}n-0.4V (n=1, 2, 3, 4, 5)		12	30	μA	a
I_{SS2}	Supply Currnt2	V_{DD}=V_{C1},C_{OUT}=OPEN V_{CELL}n=1.5V (n=1, 2, 3, 4, 5)		10	25	μA	a

∗ V_{CELL}n=CELLn voltage n=1, 2, 3, 4, 5

(*1) If VDD pin voltage becomes lower than the output of the regulator, the output voltage becomes almost equal to VDD.

OPERATION

• $V_{DET1}n$ / Overcharge Detectors (n=1, 2, 3, 4, 5)

While the cell is charged, the voltage between V_{C1} pin and V_{C2} pin (voltage of the Cell-1), the voltage between V_{C2} pin and V_{C3} pin (voltage of the Cell-2), the voltage between V_{C3} pin and V_{C4} pin (voltage of the Cell-3), the voltage of V_{C4} pin and V_{C5} pin (voltage of Cell-4), and the voltage between V_{C5} pin and V_{SS} pin (voltage of the Cell-5) are supervised. If at least one of the cells' voltage becomes equal or more than the overcharge detector threshold, the overcharge is detected, and C_{OUT} pin connected to an external pull down resistance outputs "Hi-Z", and by turning off the external N-channel MOSFET by the pull-down resister, charge cycle stops.

BA/BB/BC ver.:

To reset the overcharge and make the C_{OUT} pin level to "H" again after detecting overcharge, in such condition that a time when all the cells' voltages become lower than the overcharge released voltage. Then, the output voltage of C_{OUT} pin becomes "H", and it makes an external N-channel MOSFET turn on, and charge cycle is available. The overcharge detectors have hysteresis.

AD/BD ver.:

To reset the overcharge, when all the cell voltage become lower than the released voltage from overcharge, COUT pin becomes "H", charge is acceptable. After detecting overcharge, by connecting a load, and when all the cell voltage becomes lower than the overcharge voltage detector threshold, COUT voltage becomes "H" and charge will be possible.

Internal fixed output delay times for overcharge detection and release from overcharge exist. Even if one of cells' voltage keeps its level more than the overcharge detector threshold, and the output delay time passes, overcharge voltage is detected. Even if the voltage of each cell becomes equal or higher than V_{DET1} if these voltages would be back to be lower than the overcharge detector threshold within the output delay time, the overcharge is not detected. Besides, after detecting overcharge, each cell voltage is lower than the overcharge detector released voltage, even if just one of cells' voltage becomes equal or more than the overcharge released voltage within the released output delay time, overcharge is not released.

The output type of the C_{OUT} pin is P-channel open drain and "H" level of C_{OUT} pin is V_{DD} pin voltage.

• $V_{DET2}n$ / Overdischarge Detectors (n=1, 2, 3, 4, 5)

While the cells are discharged, the voltage between V_{C1} pin and V_{C2} pin (the voltage of Cell-1), the voltage between VC2 pin and V_{C3} pin (Cell-2 voltage), the voltage between V_{C3} pin and V_{C4} pin (Cell-3 voltage), the voltage between VC4 pin and V_{C5} pin (Cell-4 voltage), and the voltage between V_{C5} pin and Vss pin (Cell-5 voltage) are supervised. If at least one of the cells' voltage becomes equal or less than the overdischarge detector threshold, the overdischarge is detected and discharge stops by the external discharge control N-channel MOSFET turning off with the D_{OUT} pin being at "L".

The condition to release overdischarge voltage detector is that after detecting overdischarge voltage, all the cells' voltage becomes higher than the overdischarge released voltage, D_{OUT} pin becomes "H" level, and by turning on the external N-channel MOSFET, discharge becomes possible. The overdischarge detectors have hysteresis.

The output delay time for overdischarge detect is set with an external capacitor C_{CT1} connected to CT1 pin. If at least one of the cells' voltage becomes down to equal or lower than the overdischarge detector threshold, and the voltage of each cell would be back to higher than the overdischarge detector threshold within the output delay time, the overdischarge is not detected. The output delay time for release from overdischarge is also set internally.

After detecting overdischarge, supply current would be reduced and be into standby by halting unnecessary circuits and consumption current of the IC itself is made as small as possible.

When a cell voltage equals to zero, if the voltage of each cell is lower than the charge inhibit maximum voltage, charge is not acceptable. All the cell voltages are higher than the charge inhibit maximum voltage, C_{OUT} pin becomes "H" and the IC allows the system to charge.

The output type of D_{OUT} pin is CMOS having "H" level around 12V of the internal regulator and "L" level of V_{SS}.

• V_{DET3}-n (n=1, 2) /Excess discharge-current Detector, Short Circuit Protector

When the charge and discharge is acceptable, SENS pin voltage is supervised, if the load is short and SENS pin voltage becomes equal or more than excess discharge current threshold, and equal or less than the short detector threshold, the status becomes excess discharge current detected condition. If SENS pin voltage becomes equal or more than the short circuit detector threshold, the status becomes short circuit detected, then DOUT pin outputs "L" and by turning off the external MOSFET, the IC prevents the circuit from flowing large current. The excess discharge current detector has two thresholds, and each threshold has the output delay time. In terms of the output delay times, the delay time for the excess discharge current detector 2 is set shorter than the excess discharge current 1.

The output delay times for the excess discharge-current detectors are set by an external capacitor C_{CT2} connected to CT2 pin. A quick recovery of SENS pin level from a value between the excess discharge current detector and the short circuit detector threshold within the delay time, may keep the status as before excess discharge current detected. Output delay time for the release from excess discharge-current detection is also set internally.

When the short circuit protector is enabled, the delay time exists as well as other protection circuits.

Between the drain of the external FET connected to DRAIN pin, and the drain of an external FET connected to C_{OUT} and D_{OUT}, an external resistor should be mounted to release from overdischarge.

After an excess discharge-current or short circuit protection is detected, an external FET connected to DRAIN pin turns on and the resistance of release from the excess-discharge current is connected to V_{SS}. After detecting the excess discharge current or short circuit, load is removed and opened, VMP pin level is connected to the V_{SS} pin level, through the pulled down resistor for release from excess discharge, and when the VMP pin becomes equal or less than V_{REL3}, the circuit is released from excess discharge or short automatically. When the excess-discharge current is released, the external FET connected to DRAIN pin turns off and resisters for the release from excess-discharge current status is separated from V_{SS}.

• V_{DET4}/ Excess charge-current detector

When the battery pack is chargeable and discharge is also possible, V_{DET4} senses SENS pin voltage. For example, in case that a battery pack is charged by an inappropriate charger, excess current flows, then the voltage of SENS pin becomes equal or less than the excess charge-current detector threshold, then the output of C_{OUT} pin becomes "Hi-Z", and by turning off the external N-channel MOSFET with the pull-down resister, flowing excess current in the circuit is prevented.

Output delay of the excess charge current is internally fixed. Even the voltage level of SENS pin becomes equal or lower than the excess charge-current detector threshold, if the voltage becomes higher than the excess charge current threshold within the delay time, the excess charge current is not detected. Output delay for the release from excess charge current exists as well as other protection circuits.

V_{DET4} can be released by disconnecting a charger and connecting a load and when the VMP pin voltage becomes equal or more than V_{REL3}.

• Operation against cell unbalance

If one of the cells detects overcharge and either of the cells detects overdischarge, both outputs of C_{OUT} and D_{OUT} become "L".

• CTLC/CTLD pin

If the ICs are stacked and function with two chips, by connecting C_{OUT} and CTLC, and connecting D_{OUT} and CTLD shown as in the example circuit (10-cell protection), overcharge, overdischarge, open-wire state can be transferred. If stacked connection is unnecessary, CTLC/CTLD pins must be set at V_{SS} voltage level.

If CTLC/CTLD pins are in the range of $V_{SS} \pm 0.3V$, or larger than V_{DD}+2.0V, the IC operates in normal way.

By forcing V_{DD} voltage level (between V_{DD}-0.3V and V_{DD}+0.3V) to CTLC pin, the output of C_{OUT} connected an external pull-down resister can be forcibly set to "L". However, if short circuit is detected, the output of C_{OUT} cannot be made "L".

By forcing V_{DD} voltage level (between V_{DD}-1.0V and V_{DD}+3.0V) to CTLD pin, the output of D_{OUT} can be forcibly set to "L".

If the voltage in the range from Vss+0.3V to V_{DD}-0.3V is forced to the CTLC/CTLD pin, the operation may change by the voltage between V_{DD} and V_{SS}.
The voltage in the range from V_{SS} + 0.3V to V_{DD}-0.3V should not be forced to CTLC/CTLD continuously.

CTL pin input and outputs of COUT and DOUT

CTLC/CTLD pin input	C_{OUT}/D_{OUT} external FET
equal or more than V_{DD}+2.0	Normal Operation
V_{DD}-0.3V to V_{DD}+0.3V	Forced off
V_{SS}-0.3 to V_{SS}+0.3	Normal Operation
Open, other than the above	Indefinite

• SEL1, SEL2 pin

SEL1 and SEL2 pins are used as switch over 3-cell protector, 4-cell protector and 5-cell protector. If 4-cell protection is selected, by forcing VSS voltage level to SEL1 pin and forcing V_{DD} voltage
level to SEL2 pin, the operation of 5th cell's protection circuit, the signal is shut down, therefore, even if the VC5 is shortened to GND, overdischarge is not detected and operates as a 4-cell protector IC.
To select 3-cell protection mode, by forcing V_{DD} voltage level to SEL1 pin, V_{SS} voltage level to SEL2 pin, the operation of 5th cell and 4th cell stop, and the signal is cut off. Therefore, if V_{C4}, V_{C5} and V_{SS} are shorted, overdischarge is not detected and operates as a 3-cell protector IC.
SELn pins must be set as V_{DD} voltage or V_{SS} voltage level.
Depending on the combination of SEL1 pin and SEL2 pin input, delay time shortening function mode 1 (down to 1/100 delay) or delay time shortening function mode 2 (overcharge detector threshold delay time is shortened into 4ms) is realized.
Middle voltage of the table below means in the range from 4.0V to V_{DD}/2-0.5V.

SEL1 and SEL2 pin input combination, and the operation mode

SEL1 pin input	SEL2 pin input	Operation Mode
High	High	5-cell protector
Low	High	4-cell protector
High	Low	3-cell protector
Low	Low	Delay shortening mode 1 for 5-cell protector
Low	Middle	Delay shortening mode 1 for 4-cell protector
Middle	Low	Delay shortening mode 1 for 3-cell protector
Middle	Middle	Delay shortening mode 2 for 5-cell protector
Middle	High	Delay shortening mode 2 for 4-cell protector
High	Middle	Delay shortening mode 2 for 3-cell protector

• CT1, CT2 pin

CT1 and CT2 pins are used for setting the output delay time of overdischarge (tV_{DET2}), the excess discharge current 1 (tV_{DET31}), and the excess discharge current 2 (tV_{DET32}) by connecting external capacitors C_{CT1} and C_{CT2}.
tV_{DET2} can be set with CT1 pin. tV_{DET31} and tV_{DET32} can be set with CT2 pin.

(1) tV_{DET2} external capacitor C_{CT1} setting
tV_{DET2} can be set as in the next formula.
Delay time code : A $tV_{DET2}(msec) = 3.64 \times C_{CT1}(nF)$
Delay time code : B $tV_{DET2}(msec) = 3.88 \times C_{CT1}(nF)$

(2) tV_{DET31} and tV_{DET32} external capacitor C_{CT2} setting

tV_{DET31} and tV_{DET32} can be set as in the next formulas.

Delay time code : A $tV_{DET31}(msec) = 3.05 \times C_{CT2}(nF)$

$tV_{DET32}(msec) = tV_{DET31}/100$

Delay time code : B $tV_{DET31}(msec) = 3.26 \times C_{CT2}(nF)$

$tV_{DET32}(msec) = tV_{DET31}/6$

• Cell balance function CB circuit-n (n=1,2,3,4,5)

While a battery is being charged, and the cell voltage is beyond the cell balance voltage $V_{CBD}n$ (n=1,2,3,4,5) , against the cell which becomes equal or more than the cell balance voltage $V_{CBD}n$, the output of CBn pin (n=1,2,3,4,5) becomes "H" and an external N-channel transistor for cell balance turns on, and discharge path is connected in parallel with the cell and charge current is reduced. When the cell voltage becomes equal or less than the cell balance released voltage $V_{CBR}n$ (n=1,2,3,4,5), then cell balance function is released and the output of CBn pin (n=1,2,3,4,5) becomes "L".
The resister used for the discharge path, absolute ratings must be cared.
If the cell balance function is unnecessary, CBn pin must be left open.

Open-wire Detector Function
Open-wire detect of V_{DD} (V_{C1}) and V_{SS} for 5-cell protector

If V_{DD} line is cut, the voltage between V_{C1} and V_{C2} is less than 0V.
If V_{SS} line is cut, the voltage between V_{C5} and V_{SS} is less than 0V.
The voltage is detected by the 0V-detector circuit.
If open-wire is detected, the P-channel open drain of the C_{OUT} turns off.

• Open-wire detector for V_{C2}, V_{C3}, V_{C4}, V_{C5} for 5-cell protection

When using the 5-cell protection, the voltage of VDD (= VC1) becomes lower than VC2 voltage if the connection between the battery and VDD (= VC1) is open. And, the voltage of VSS becomes higher than VC5 voltage if the connection between the battery and VSS is open. The voltage variation is detected as “Open-wire”. When the open-wire is detected, the P-channel open drain of the COUT turns off.
In case of the 3.3μF capacitor is attached to the CTLT pin, open-wire detector operates every 30 seconds. The built in switch of VC1, VC3, VC5 cell, and the switch attached to the VC2 and VC4 turn on alternatively by the even_sw and the odd_sw signal.
The internal impedance of the cell whose switch turns on becomes low for about 1.2 seconds by the low resistance connected to the switch. If the wire is not broken, the capacitor of the CTLT is discharged and the next cycle starts for checking.
While the wire is broken, the difference of the internal impedance of the IC generated by the switch's tuning on makes VC shift and detected by the comparator for V_{DET1}. If the open-wire is detected and the condition continues for about 4ms, then even_sw and odd_sw turn off and the capacitor of CTLT is discharged and the P-channel open drain of the C_{OUT} turns off. While the overdischarge voltage is detected, the open-wire of V_{C2}, V_{C3}, V_{C4} and V_{C5} does not operate.

• Open-wire detector for V_{DD} (V_{C1}) and V_{SS} for 10-cell protection

If the ICs are connected in cascade, the V_{DD} of the high side IC and V_{SS} (V_{SS2}) of the low side IC, the open-wire detector is able to work as well as 5-cell protection type.
As for the V_{SS} (V_{SS1}) of high side IC and V_{DD} (V_{DD2}) of low side IC, if they are connected with common one wire from the battery, and if the wire is broken, two lines, V_{SS1} and V_{DD2}'s wire are broken, as a result, open-wire may not be able to be detected correctly.
As for the V_{SS1} and V_{DD2}, connect with two wires so that either V_{SS1} or V_{DD2} is connected to the battery, and by the pull-down

resistance of C_{OUT} of high side is connected to the V_{DD2} of the low side IC, if either of V_{SS1} or V_{DD2} breaks the wire, the open-wire detector is able to operate.
Refer to the typical application circuit. (10-cell, cell-balance, open-wire detector are in use.)

***Limitation of the** open-wire **detector for V_{C2}, V_{C3}, V_{C4}, V_{C5}.**

If the open-wire detecting function is necessary, confirm the limitations below;
External components must be

C_{CTLT}=3.3μF
C_{CT1} range: from 0.47μF to 1.0μF
C_{VCX}=0.1μF

Even if the protection IC does not detect overdischarge, if the cell voltage is low, depending on the distribution of the ICs, cell balance state, the operating environment, the characteristics of the external components, open-wire function may not operate correctly.

During the delay time of the overcharge voltage, if the open-wire is detected, the overcharge detect operation is once cancelled, and the open-wire operation will be dominant. During the open-wire detection, even if the cell voltage becomes equal or more than the overcharge detector threshold, overcharge is not detected. In this case, after detecting open-wire operation, if the cell voltage is still equal or more than the overcharge detector threshold, overcharge detector operation starts again. For this reason, overcharge detector output delay time may longer than 1s. (Refer to the timing chart.)

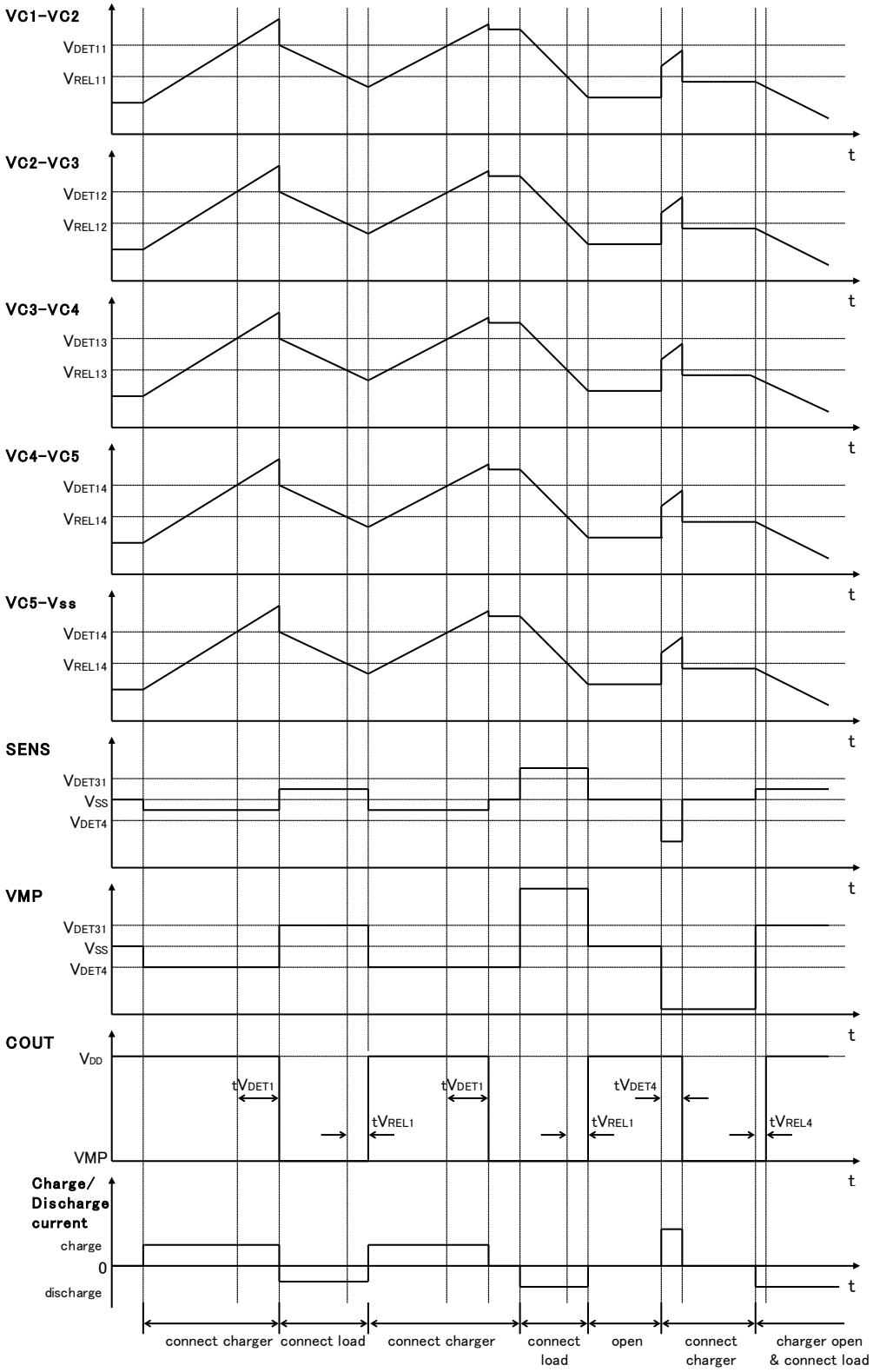
During the overdischarge delay time, if the open-wire detector's operation starts, the overdischarge detector's operation is once cancelled and the open-wire operation will be dominant. During the open-wire, detector's operation is active, even if the cell voltage becomes equal or less than the overdischarge detector threshold, the overdischarge detector does not start. In this case, after detecting open-wire operation, if the cell voltage is still equal or less than the overdischarge detector threshold, overdischarge detector operation starts again. For this reason, the output delay time of overdischarge detector may be longer than the preset value. (Refer to the timing chart.)

Charge Inhibit Detector Circuit Vnochg-n (n-1,2,3,4,5)

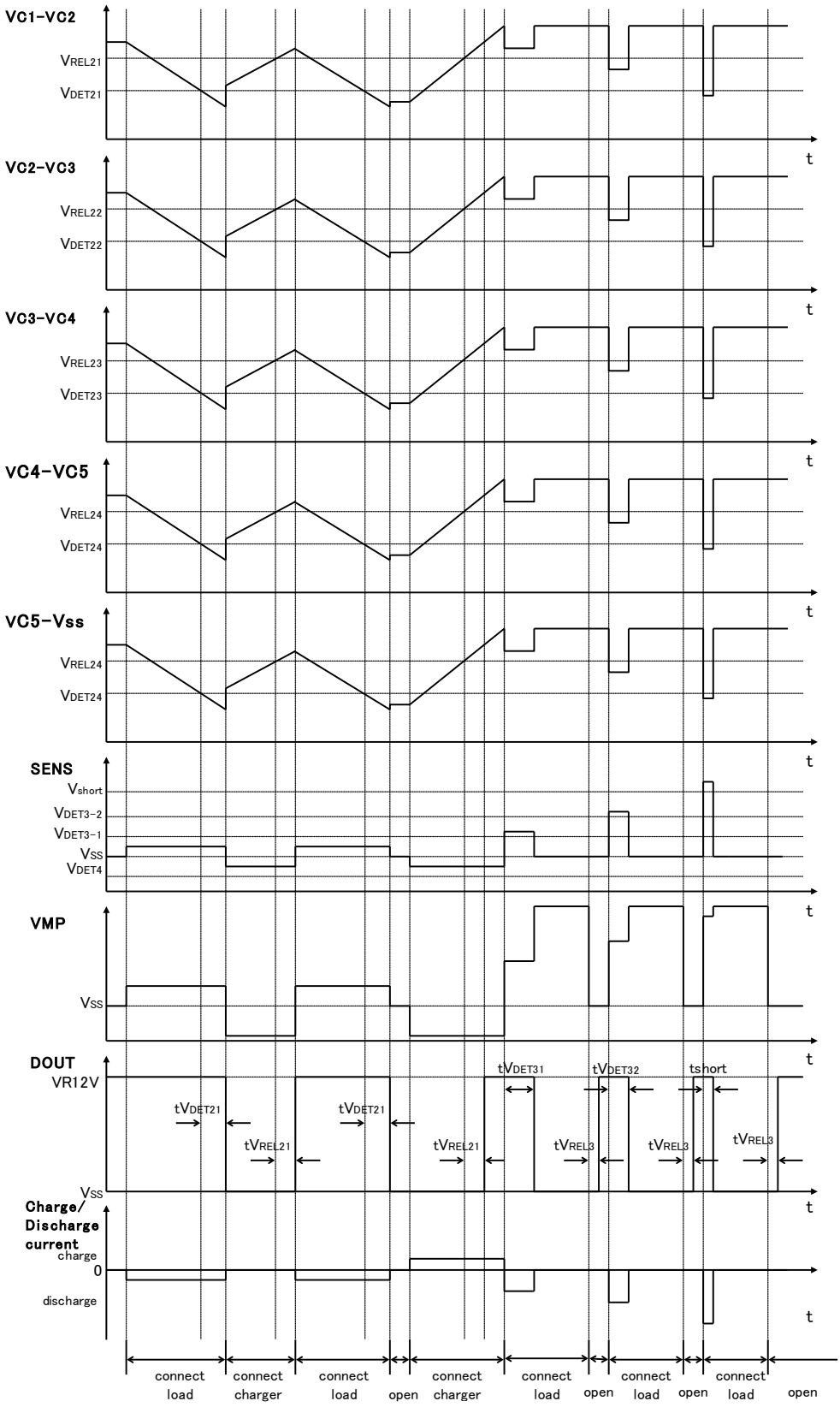
In the R5432VxxxBB, for each cell, charge inhibit detector is built-in. If either of cells' voltage is lower than the charge inhibit voltage, when a charger is connected to the battery pack, charge inhibit is detected and COUT with external pull-down becomes "Hi-Z" and an external MOSFET turns off by the pull-down resistance and charge stops.
When the charge inhibit is detected, the cell voltage which is inhibit charge is equal or lower than the overdischarge detector threshold, therefore the output of COUT becomes "Hi-Z", and the output of DOUT becomes "L", and both external FETs turn off.

TIMING CHART

- **Overcharge, Excess charge current**

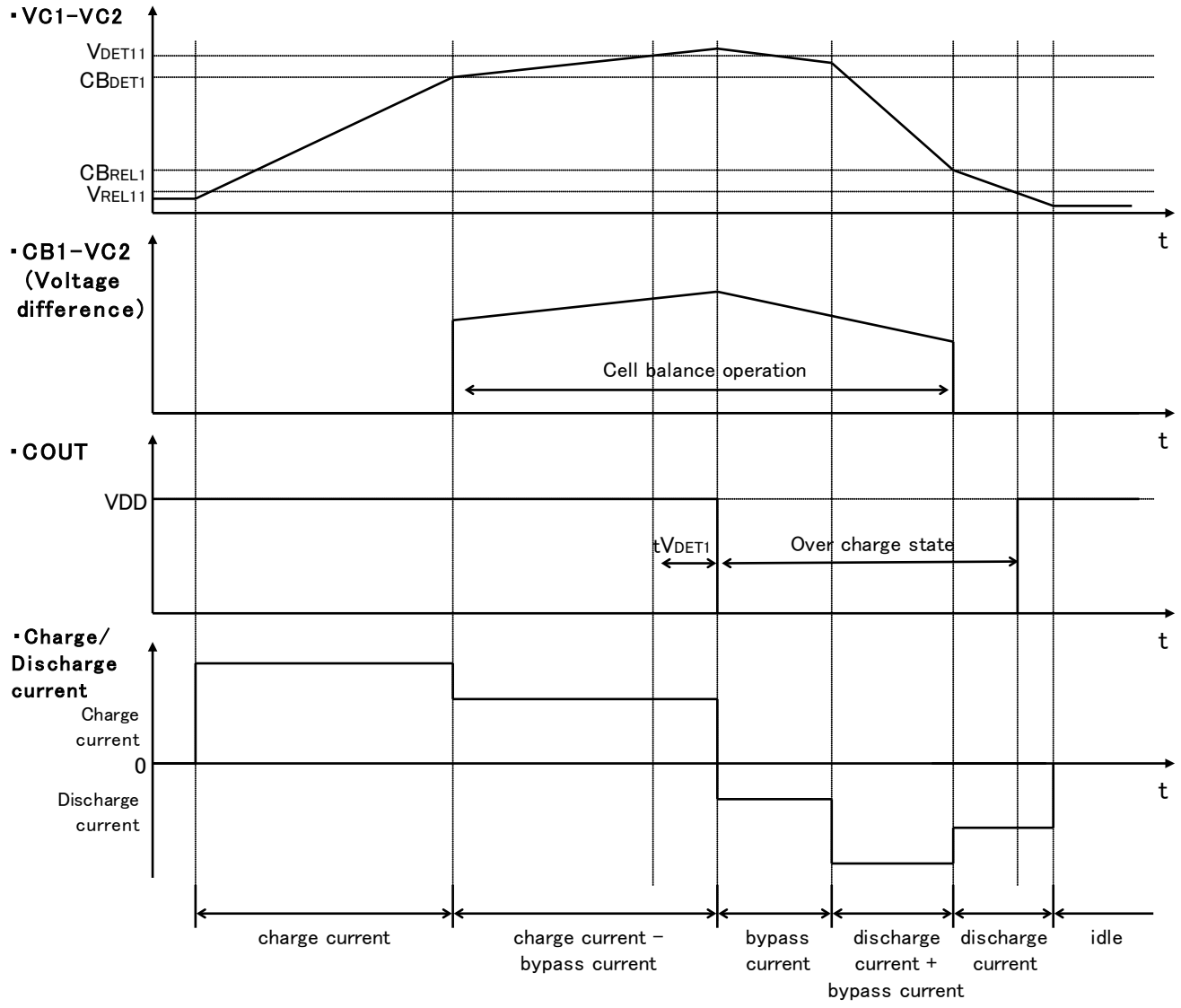


• Overdischarge, Excess discharge current1/2, Short detector

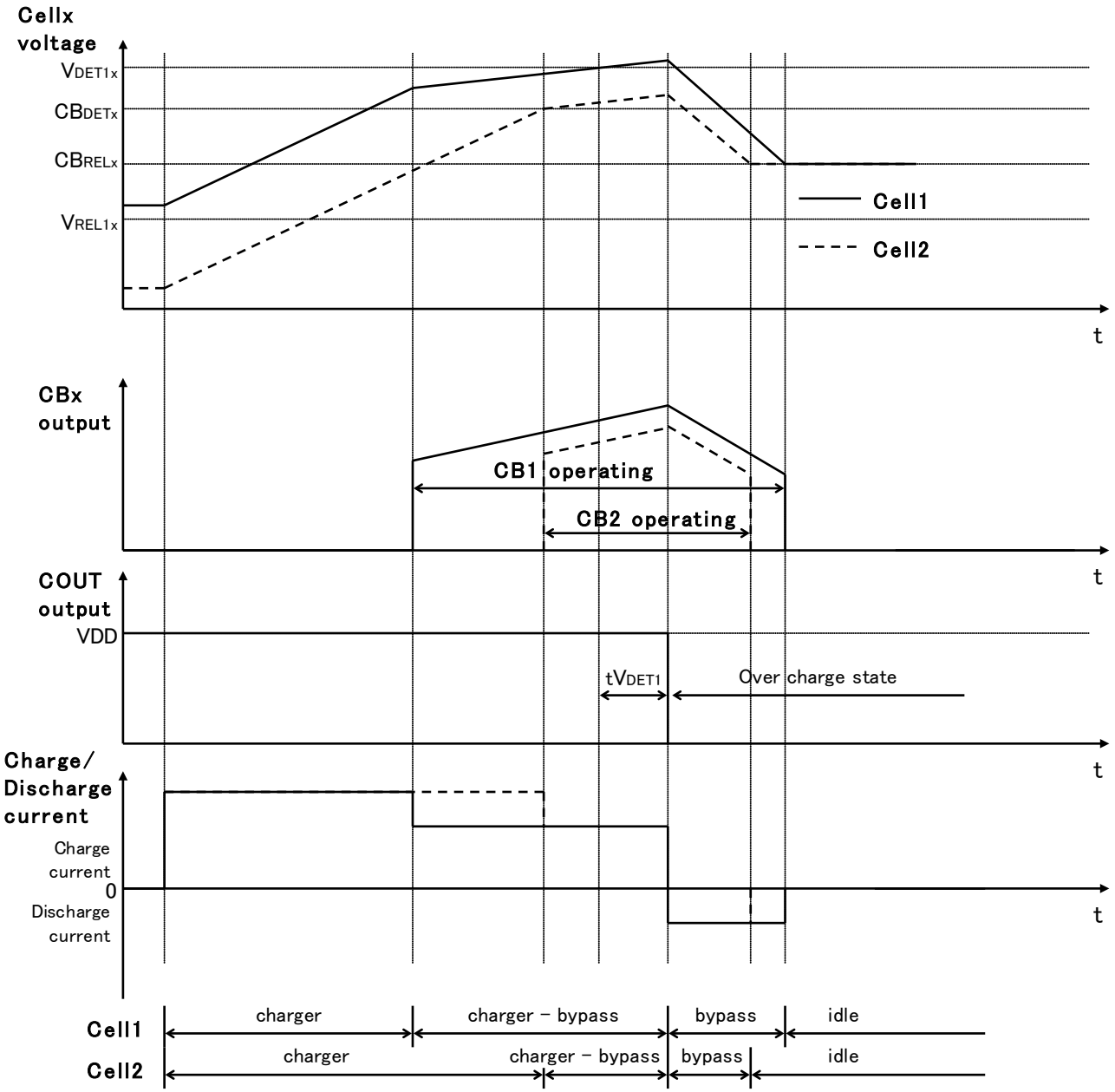


CELL BALANCE OPERATION

In the case that CELL1 operates CELL balance



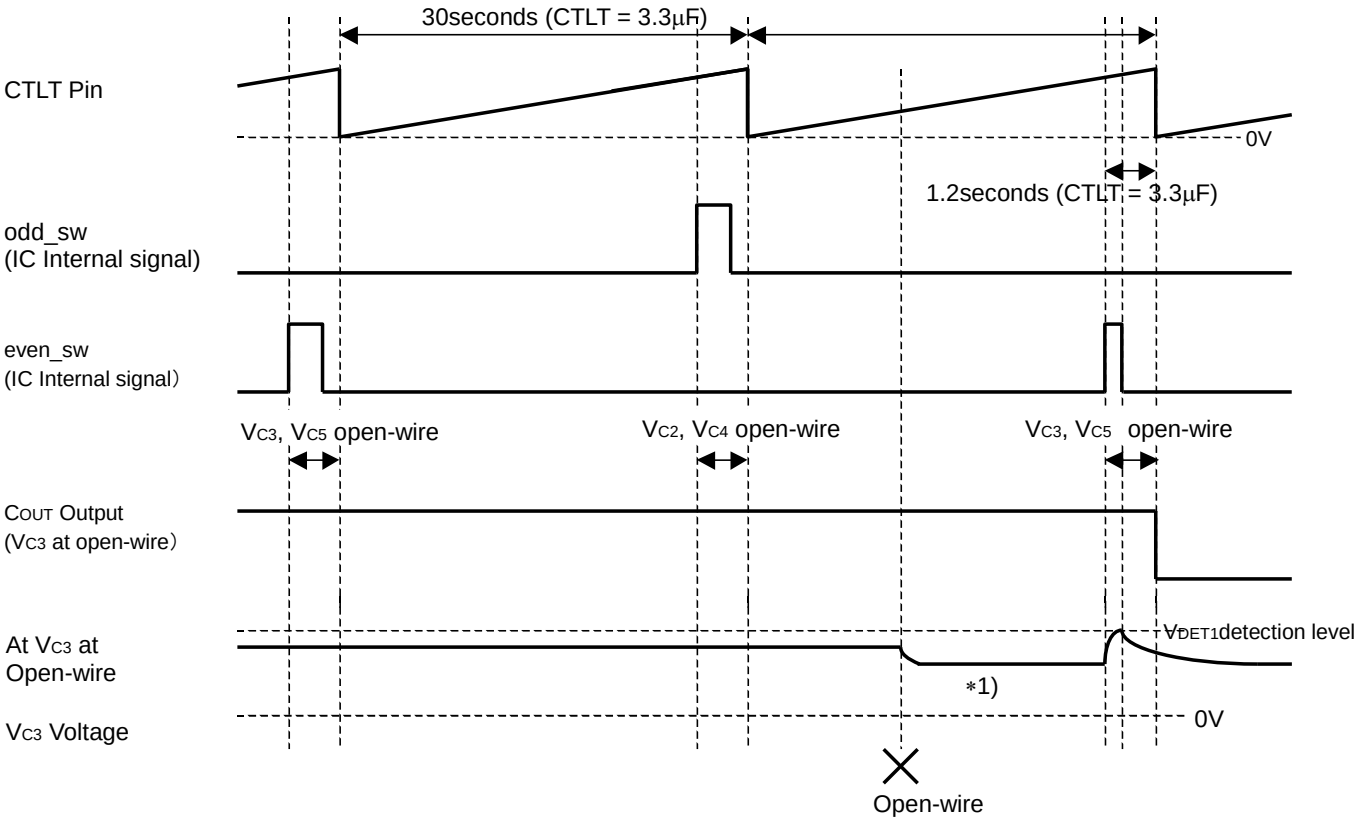
Balance operation with CELL1 and CELL2



• Open-wire Detection

Open-wire detector's operation of VC2, VC3, VC4, and VC5 for 5-cell protector
In case of the 3.3μF capacitor is attached to the CTLT pin, open-wire detection operates every 30 seconds. The built in switch of VC1, VC3, VC5 cell, and the switch attached to the VC2 and VC4 turn on alternatively by the even_sw and the odd_sw signal.
The internal impedance of the cell whose switch turns on becomes low for about 1.2 seconds by the low resistance connected to the switch in serial. If the wire is not open, the capacitor of the CTLT is discharged and the next cycle starts for checking.
While the wire is open, the difference of the internal impedance of the IC generated by the switch's tuning on makes VC shift and detected by the comparator for VDET1. If the open-wire is detected and the condition continues for about 4ms, then even_sw and odd_sw turn off and the capacitor of CTLT is discharged and the P-channel open drain of the COUT turns off. While the overdischarge voltage is detected, the open-wire of VC2, VC3, VC4 and VC5 does not operate.

The timing chart of open-wire of V_{C2}, V_{C3}, V_{C4}, V_{C5} is shown below:



∗1) The change of V_C is not always increasing. Depending on the cell balance or the internal impedance, the V_C increases or decreases.

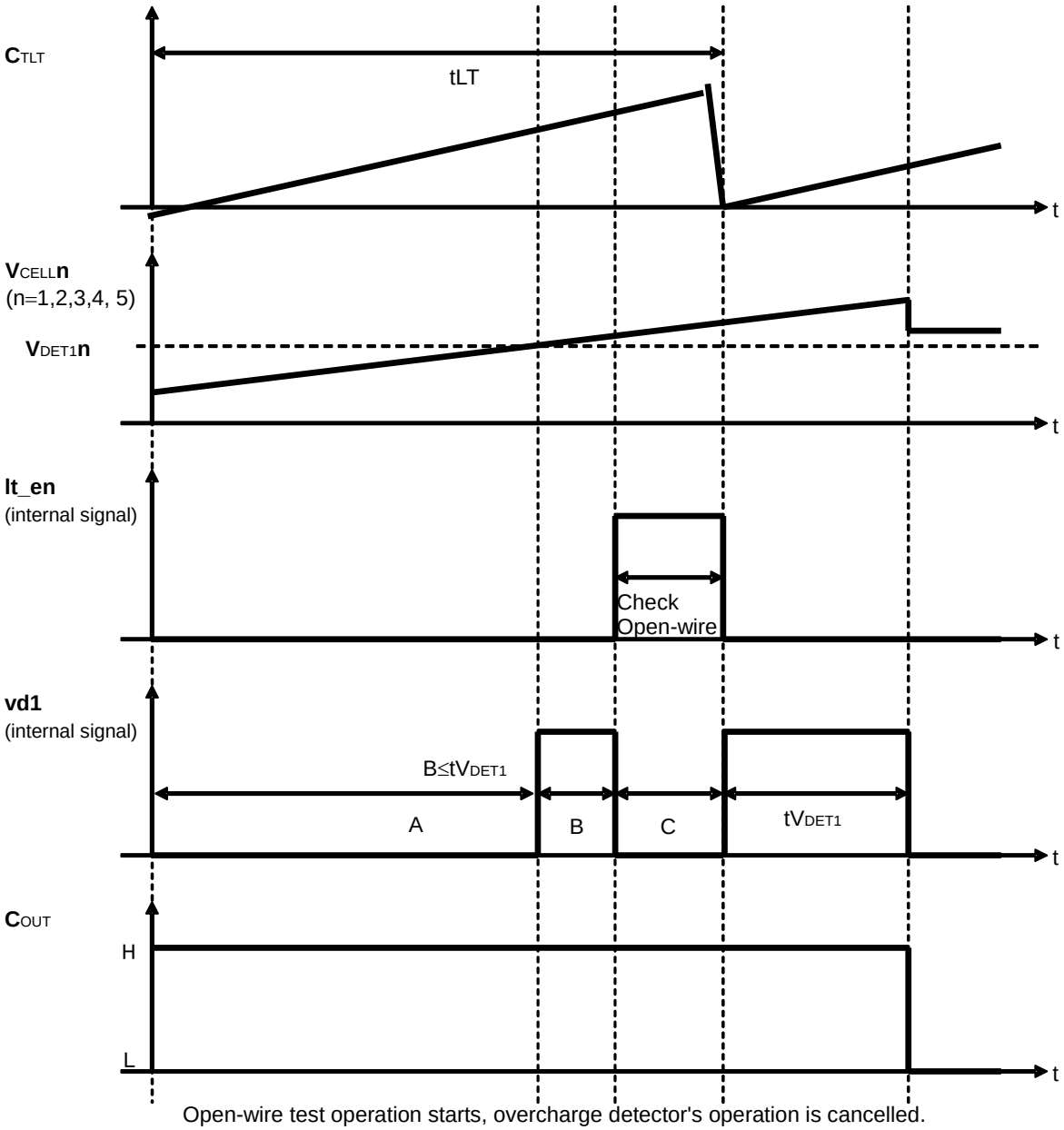
• Overcharge detector operation and Open-wire detector operation

The output delay time of overcharge is normally set at 1s, however, the effect of the open-wire detector, the output delay time may be longer than 1s.

Case 1: During the operation of detecting overcharge, if the open-wire is detected, once the operation of the overcharge detector is cancelled, and after detecting the open-wire, the operation of the overcharge detector starts again.

Case 2: During the operation of the open-wire detector, if the cell voltage becomes more than the overcharge detector threshold, after detecting the open-wire, the operation of the overcharge detector starts.

The timing chart shown below is for the operation of the case 1. When the overcharge is detected, internal node "vd1" becomes "H", then, if the open-wire is detected, the internal node "It_en" becomes "H", then "vd1" signal returns to "L". After the open-wire detector is released, then "It_en" returns to "L", then the "vd1" becomes "H", and overcharge detector's function restar.



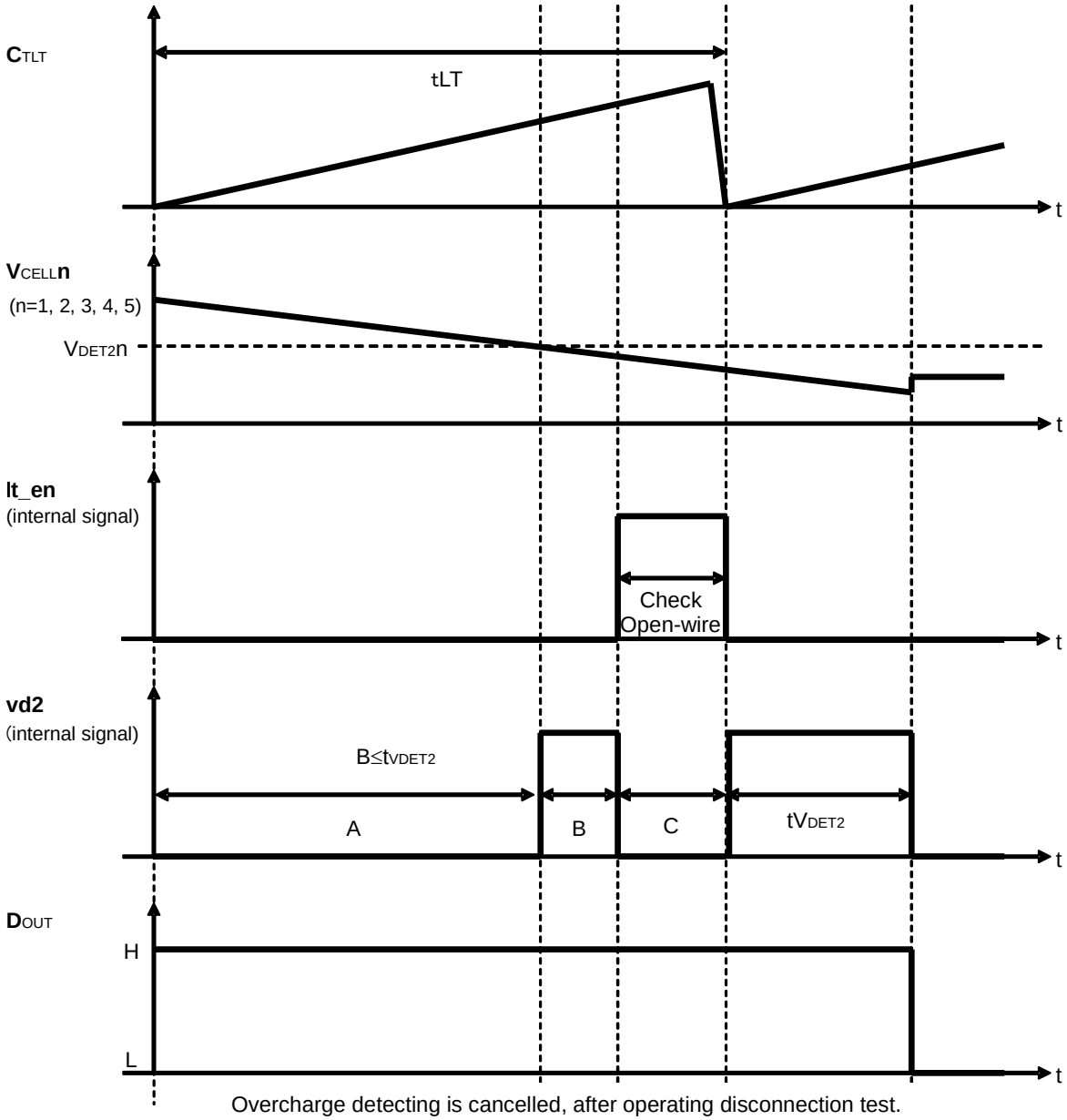
Open-wire test operation starts, overcharge detector's operation is cancelled.
Overcharge detector's maximum output delay : Max_tV_{DET1} = B＋C＋tV_{DET1}.

• Overdischarge operation and disconnection detector operation

The output delay time of the overcharge detector can be set by an external capacitor, but the delay time might be longer than the present value due to the open-wire detector's operation.

1. During the operation of detecting overdischarge, if the open-wire is detected, once the operation of the over discharge detector is cancelled, and after detecting the open-wire is detected, once the operation of the
2. Overdischarge can not be detected during disconnection detection. It can operate after disconnection detect.

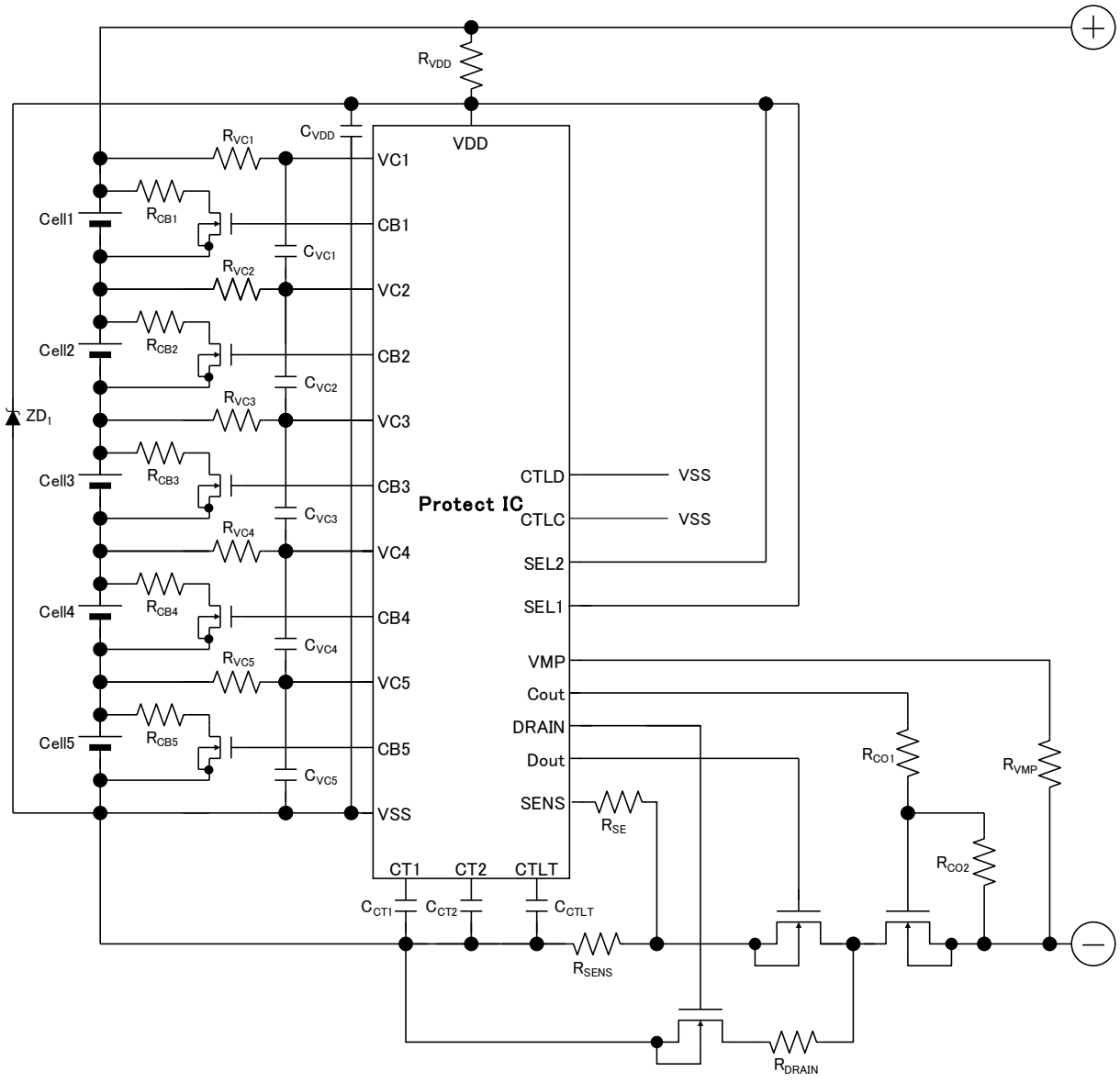
The timing chart which start to detect disconnect during overdischarge is displayed as follows.
The internal signal "vd1" become "H" after it is equal or less than overdischarge threshold. It comes back "L" after which is the detecting disconnection internal signal become "H". "vd1" become "H" after "It_en" comes back "L". . Overdischarge can be detected.



Overcharge detecting is cancelled, after operating disconnection test.
So max output of overcharge delay : Max_tV_{DET2} = B＋C＋tV_{DET2}

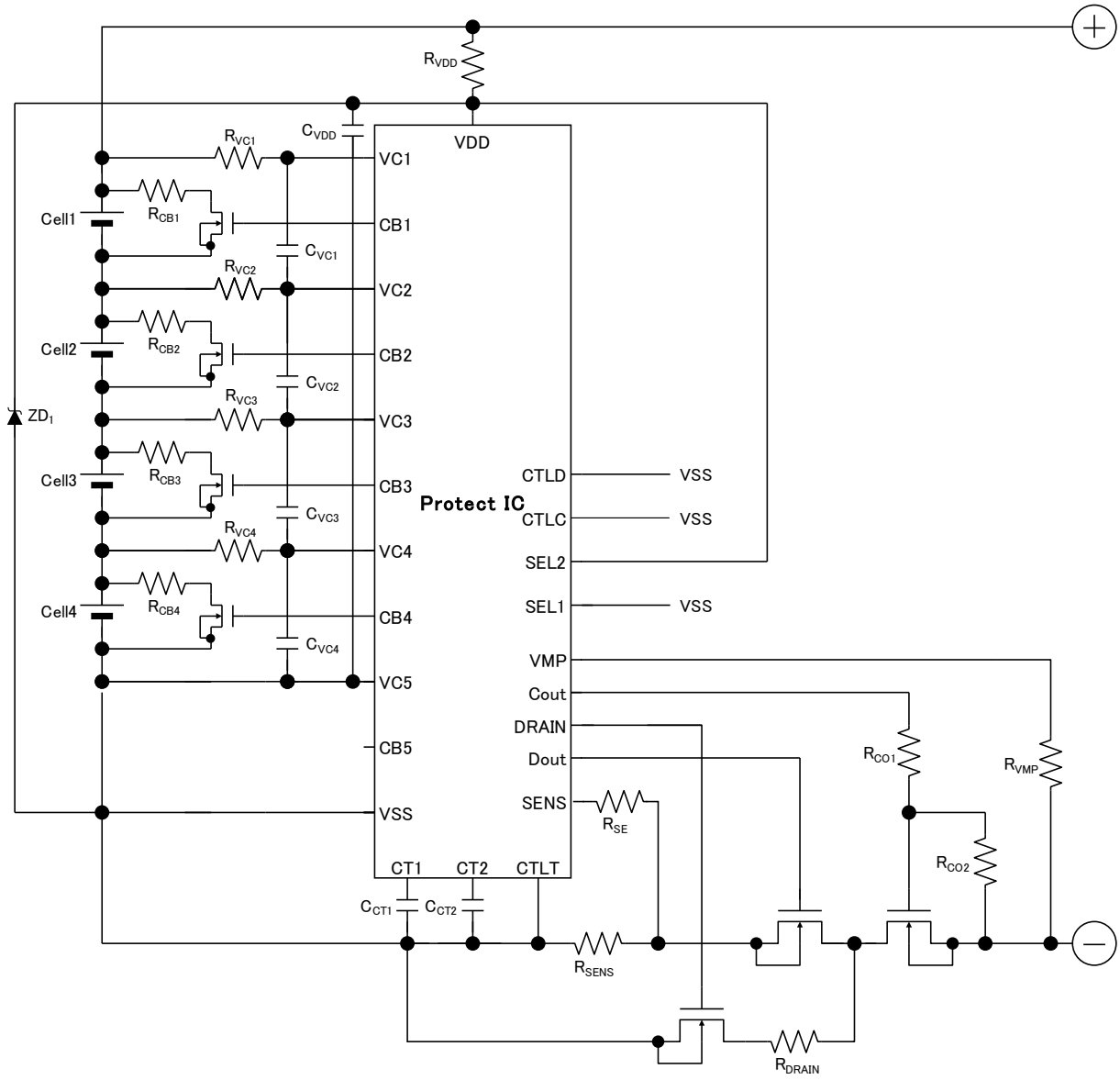
TYPICAL APPLICATION AND TECHNICAL NOTES (R5432VxxxBA)

- **Circuit example (for -5cell protection, detecting disconnection, at operating cell-balance function)**



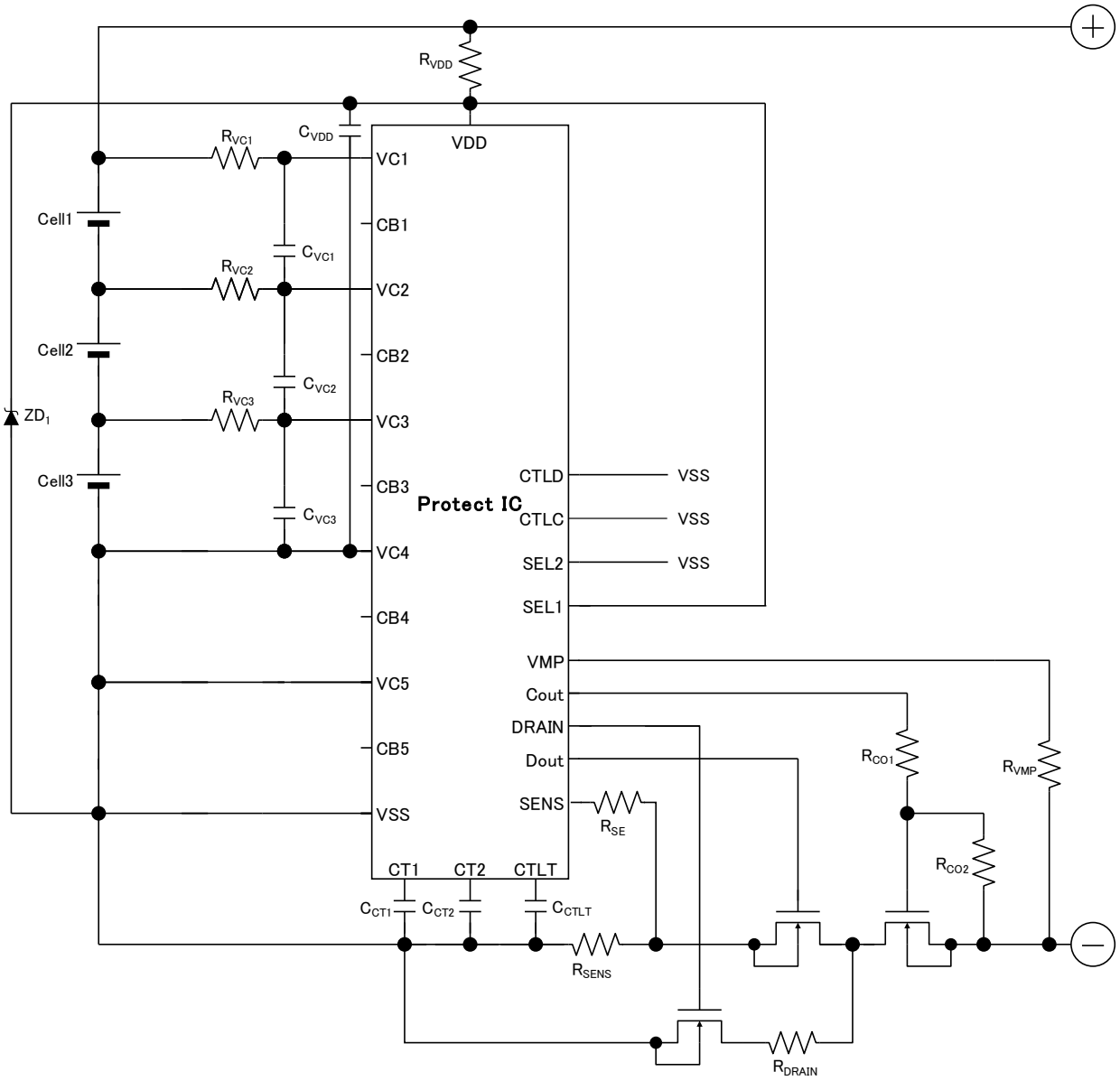
When the FET connected to Cout is OFF and the load is connected between Pack+ and Pack-, the discharge current flows through the parasitic diode of that FET, and when the FET connected to Dout is OFF and the charger is connected between Pack+ and Pack-, the charge current flows through the parasitic diode of that FET. Choose the FETs which can flow those current enough.

- **Circuit example (for 4cell protection, detecting disconnection, at not operating cell-balance function)**



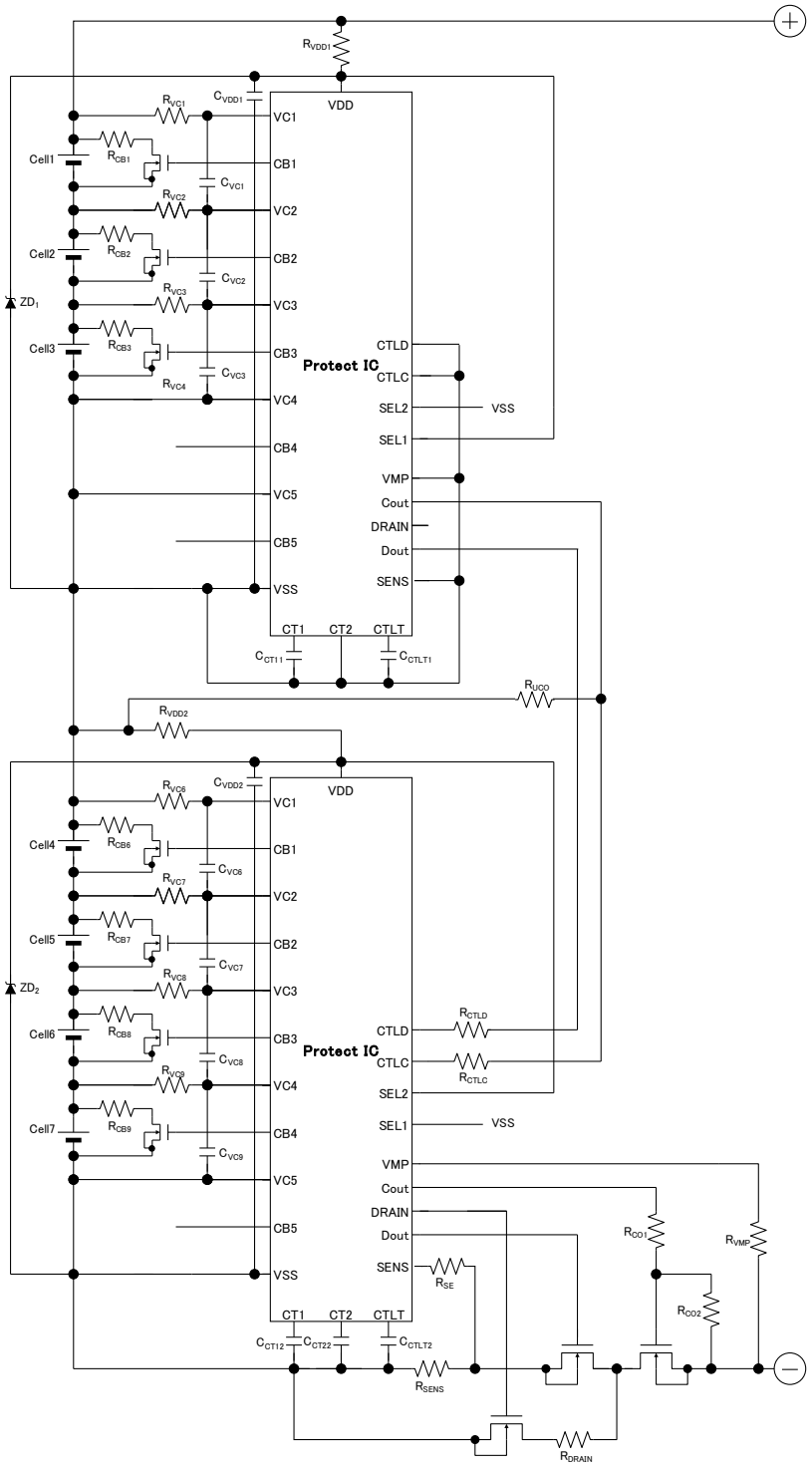
When the FET connected to Cout is OFF and the load is connected between Pack+ and Pack-, the discharge current flows through the parasitic diode of that FET, and when the FET connected to Dout is OFF and the charger is connected between Pack+ and Pack-, the charge current flows through the parasitic diode of that FET. Choose the FETs which can flow those current enough.

- **Circuit example (for 3cell, detecting disconnection, at not operating cell-balance function)**



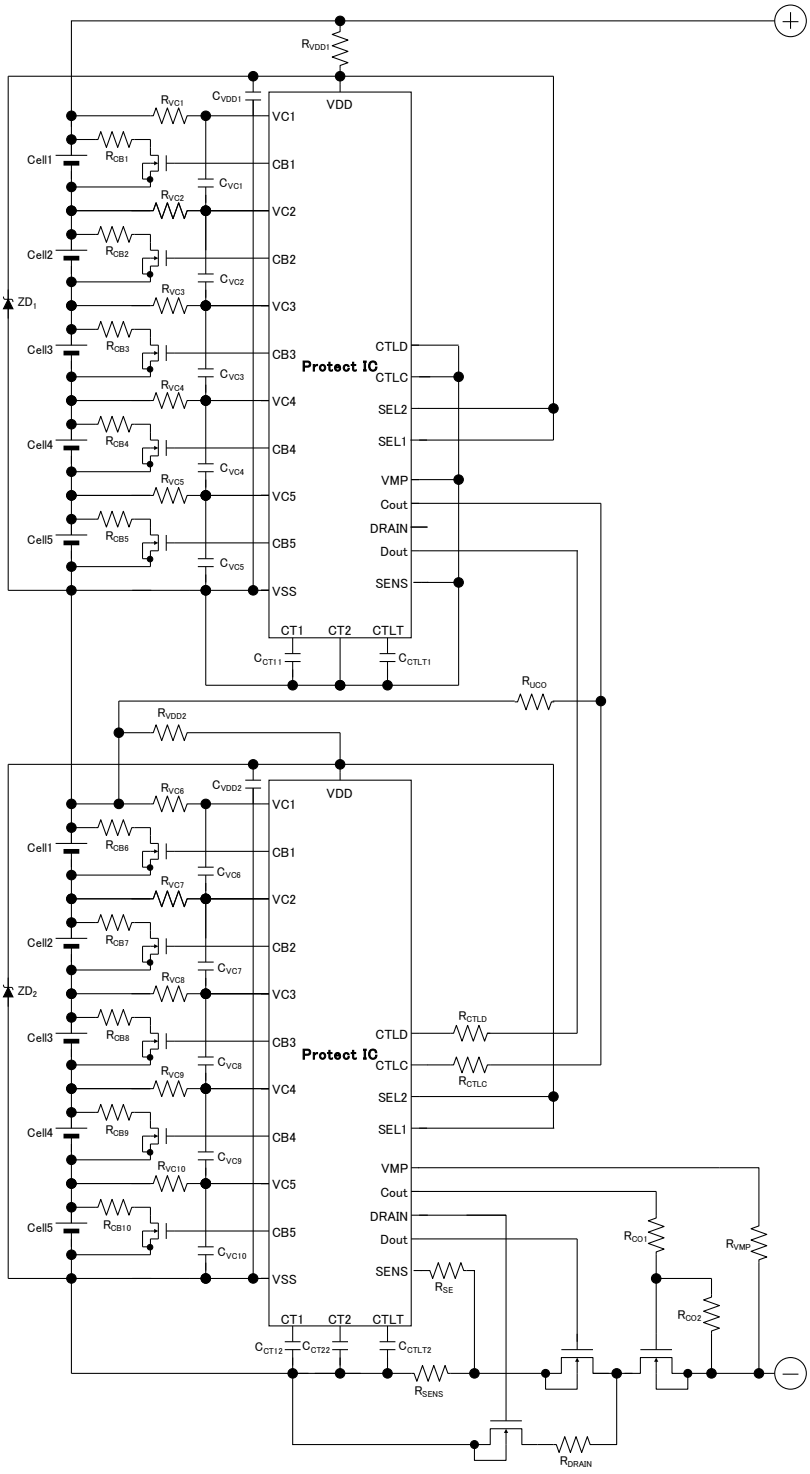
When the FET connected to Cout is OFF and the load is connected between Pack+ and Pack-, the discharge current flows through the parasitic diode of that FET, and when the FET connected to Dout is OFF and the charger is connected between Pack+ and Pack-, the charge current flows through the parasitic diode of that FET. Choose the FETs which can flow those current enough.

- **Circuit example (for 7cell, detecting disconnection, at operating cell-balance function)**



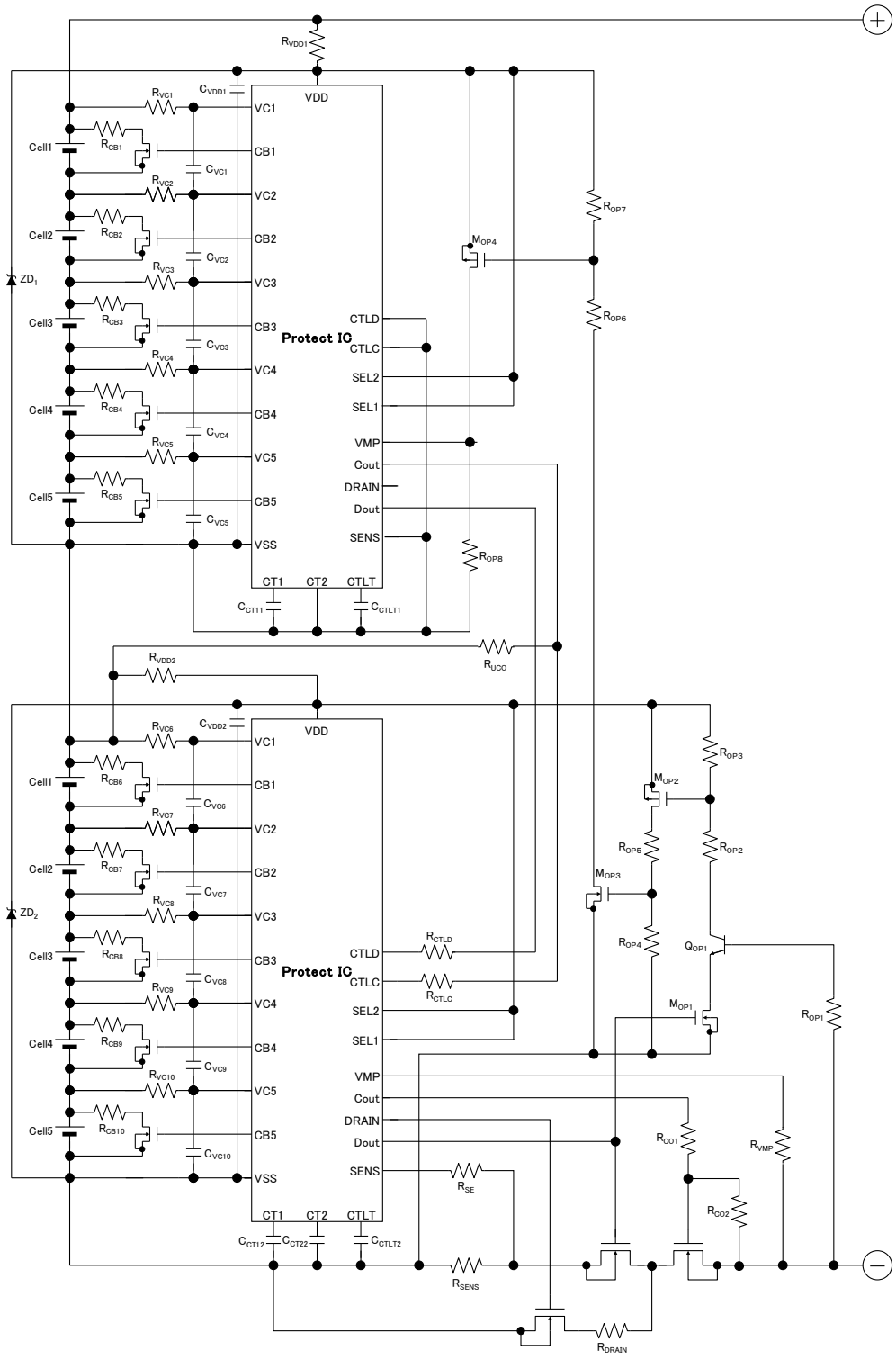
If the open-wire detector is used, for Vss of the high side IC or VDD of the low side IC, these two lines must be separated. If they are common, the both pins' open-wire cannot be detected. Refer to the operation explanation. When the FET connected to Cout is OFF and the load is connected between Pack+ and Pack-, the discharge current flows through the parasitic diode of that FET, and when the FET connected to Dout is OFF and the charger is connected between Pack+ and Pack-, the charge current flows through the parasitic diode of that FET. Choose the FETs which can flow those current enough.

Circuit example (for 10cell, detecting open-wire, with cell-balance function)



If the open-wire detector is used, for Vss of the high side IC or VDD of the low side IC, these two lines must be separated. If they are common, the both pins' open-wire cannot be detected. Refer to the operation explanation.
When the FET connected to Cout is OFF and the load is connected between Pack+ and Pack-, the discharge current flows through the parasitic diode of that FET, and when the FET connected to Dout is OFF and the charger is connected between Pack+ and Pack-, the charge current flows through the parasitic diode of that FET. Choose the FETs which can flow those current enough.

- **Circuit example (for 10-cell protection with cell-balance, open-wire, overcharge hysteresis cancellation: AD/BD ver.)**



If the open-wire detector is used, for Vss of the high side IC or VDD of the low side IC, these two lines must be separated. If they are common, the both pins' open-wire cannot be detected. Refer to the operation explanation.

- **External parts ratings**

Symbol	Typ.	Unit	Range	Remarks
R_{VDD}	330	Ω	330 to 1000	∗1
R_{VC1}	330	Ω	330 to 1000	∗2
R_{VC2}	330	Ω	330 to 1000	∗2
R_{VC3}	330	Ω	330 to 1000	∗2
R_{VC4}	330	Ω	330 to 1000	∗2
R_{VC5}	330	Ω	330 to 1000	∗2
R_{CB1}	100	Ω	40 or more	∗3
R_{CB2}	100	Ω	40 or more	∗3
R_{CB3}	100	Ω	40 or more	∗3
R_{CB4}	100	Ω	40 or more	∗3
R_{CB5}	100	Ω	40 or more	∗3
R_{SENS}	100	mΩ	1.0 or more	It is determined by the value of over current
R_{SE}	10	kΩ	1 to 10	∗4
R_{DRAIN}	∗5	MΩ	∗5	∗5 $R_{DRAIN}<V_{DET31}x(R_{CO1}+R_{CO2})/50$
R_{CO1}	1	MΩ	∗5	∗5
R_{CO2}	2	MΩ	∗5	∗5
R_{VMP}	10	MΩ	0.01 to 10	∗6
R_{CTLC}	1	kΩ	1 to 10	
R_{CTLD}	1	kΩ	1 to 10	
R_{UCO}	3	MΩ	0.1 to 10	∗7
C_{VDD}	1	μF	0.1 to 1	∗1
C_{VC1}	0.1	μF	0.1	∗2
C_{VC2}	0.1	μF	0.1	∗2
C_{VC3}	0.1	μF	0.1	∗2
C_{VC4}	0.1	μF	0.1	∗2
C_{VC5}	0.1	μF	0.1	∗2
C_{CT1}	0.47	μF	0.01 to 1.0	∗8
C_{CT2}	0.0033	μF	0.0022 or more	∗9
C_{CTLT}	3.3	μF	3.3	∗10
ZD_1	30	V	30 or less	∗11
R_{OP1}	10	kΩ	10 or more	Input resistance of Q_{OP1}
R_{OP2}	10	MΩ	5 or more	
R_{OP3}	10	MΩ	5 or more	
R_{OP4}	10	MΩ	5 or more	
R_{OP5}	10	MΩ	5 or more	
R_{OP6}	20	MΩ	10 or more	
R_{OP7}	10	MΩ	5 or more	
M_{OP1}				Consider the Voltage rating of V_{GS} and V_{DS}
M_{OP2}				Consider the Voltage rating of V_{GS} and V_{DS}
M_{OP3}				Consider the Voltage rating of V_{GS} and V_{DS}
M_{OP4}				Consider the Voltage rating of V_{GS} and V_{DS}
Q_{OP1}				Consider the Voltage rating of V_{GS} and V_{DS}

Please refer to the external circuits of next page for "∗" of remarks
Please confirm "Precautions before Use".

Technical Notes on External Circuits and Components

*1) The voltage fluctuation is stabilized with R_{VDD} and C_{VDD}. If a small R_{VDD} is set, in the case of the large transient may happen to the cell voltage, by the flowing current, the IC may be unstable. If a large R_{VDD} is set, by the consumption current of the IC itself, the voltage difference between V_{DD} pin and V_{C1} pin is generated, and unexpected operation may result. Therefore, the appropriate value range of R_{VDD} is from 330Ω to 1kΩ. To make a stable operation of the IC, the appropriate value range of C_{VDD} is from 0.1μF to 1.0μF.

*2) R_{VC1} to R_{VC10}, C_{VC1} to C_{VC10} stabilize the voltage fluctuation. If large R_{VC1} to R_{VC10} is set, the detector threshold will be high because of the internal conduction current of the IC. The operation error of open-wire detector function may happen easily by the distribution of the ICs or environment. If small R_{VC1} to R_{VC10} is set, the effect by noise will be large. Therefore the appropriate value range of R_{VC1} to R_{VC10} is from 330Ω to 1kΩ. To make stable operation, use 0.1μF as C_{VC1} to C_{VC10}.

*3) When the cell balance function is necessary, RCB1 to RCB10 must be chosen carefully with considering the bypass current, and consumption power by the bypass current, and the external MOSFET. Especially, if a small resistance (to set the large bypass current) is set, fully evaluation is necessary. If a large resistance (to set the small bypass current) is set, the time for cell balance will be long.

*4) When the cascade connection is used, if short circuit is happened, by the short current and the R_{SENS} enlarges the voltage, and as a result, if the voltage of SENS pin becomes larger than the V_{DD} of the IC, during the short circuit output delay time, the current flows into SENS pin. Therefore, if a small R_{SE} is set, a large current may flow into SENS pin. If a large R_{SE} is set, the overcurrent detector threshold may shift. Therefore the appropriate value is around 10kΩ.

*5) Choose appropriate values for R_{DRAIN}, R_{CO1}, and R_{CO2} to satisfy the next formula, otherwise, the release from excess discharge current and short may be impossible.

$R_{DRAIN} < V_{DET31} \times (R_{CO1}+R_{CO2})/50$

If small R_{CO1} or R_{CO2} is set, when the output of C_{OUT} is "H", the consumption current of protection circuit board increases. If large R_{CO1} or R_{CO2} is set, when the output of C_{OUT} is "Hi-Z", the speed for pull-down the gate of the charge FET becomes slow and turning off the FET will be slow. Not only that, by dividing between the "Hi-Z" output and the resistance, turning off the charge FET may be difficult.

If a small R_{DRAIN} is set, when the excess discharge current and short circuit is detected, the large current may flow until the load is removed.

*6) In terms of R_{VMP}, when the cascade connection is made, if D_{OUT} turns off, VMP pin is pulled up via R_{VMP} to the top cell. In this case, the current flows via R_{VMP} and the internal diode, therefore, appropriate value must be chosen. If the cascade connection is not used, around 10kΩ is acceptable.

*7) Set R_{UCO} to satisfy $R_{UCO}=R_{CO1}+R_{CO2}$. If a extremely large resistance is set, when the output of C_{OUT} is "Hi-Z", by the dividing resistance, CTLC pin may not be pulled down. If a small resistance is used, when the output of C_{OUT} is "H", the consumption current via R_{UCO} increases.

*8) If the open-wire detector function of V_{C2} to V_{C5} is used, use 0.47μF to 1μF as C_{CT1}. If the open-wire detector function is unnecessary, use a capacitor of 0.01μF or more.

*9) If a too small C_{CT2} is set, excess discharge current detector output delay time 2 becomes shorter than the short circuit output delay time. Therefore, use a capacitor with 0.0022μF or more.

*10) If the open-wire detector of V_{C2} to V_{C5} is used, use 3.3μF as C_{CTLT}. If the open-wire detector of V_{C2} to V_{C5} is not necessary, pull down to V_{SS}.

*11) Considering the break down of the resistors and capacitors to stabilize the fluctuation of the voltage, to avoid that the high voltage is directly forced to the IC, adding a zener diode is our recommendation. Connect the zener diode between V_{DD} pin of the IC and VSS pin directly. (Refer to the typical application circuits.)

To set the number of connecting cells, SEL1/SEL2 pin must be connected to V_{DD} level. In these cases, connect the pin inside the filter for stabilizing V_{DD} pin voltage. If SEL1/SEL2 is connected outside the filter, during the operation, the voltage difference between SEL1/SEL2 and V_{DD} may be generated, and unstable operation or excess current flow may result.

The typical application circuit diagrams are just examples. This circuit performance largely depends on the PCB layout and external components. In the actual application, fully evaluation is necessary.

Overvoltage and the over current beyond the absolute maximum rating should not be forced to the protection IC and external components. Especially, if the pack+ and Pack- are short, although the short protection circuit is built-in the IC, but during the output delay time, large current may flow through the FET. By the current during the output delay, in order not to destruct the FET, choose the FET with enough current rating.

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To connect the protection IC and cells, connect V_{SS} pin first. If the connect order is wrong, by flowing unexpected current, the IC may be damaged.

If charge control FET and discharge control FET are connected in serial, if the control FET for charge turns off and discharge big current, or when the FET for discharge turns off and if charge with big current is done without discharge control FET turning off, big current flows through the parasitic diode of the FET, the FET may be burnt. To avoid this, separate the charge and discharge current path and when the FET turns off, in order not to flow large current through parasitic diode, choose an FET with large current capacity.

TEST CIRCUITS

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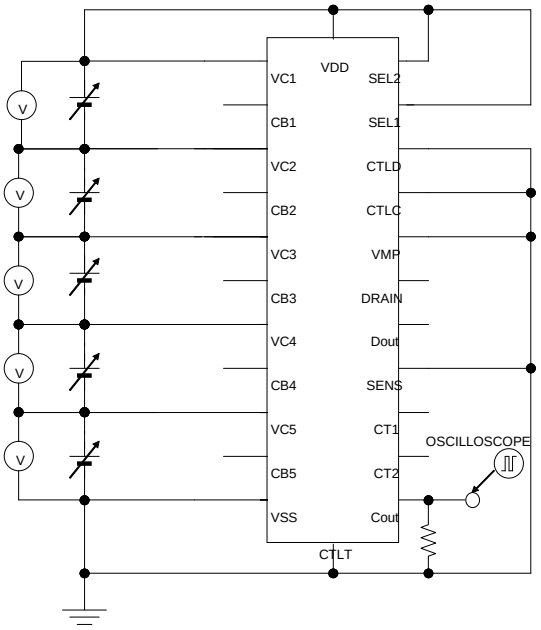

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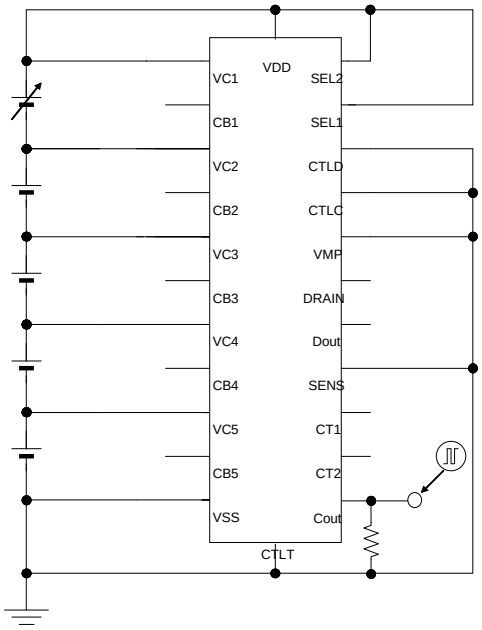

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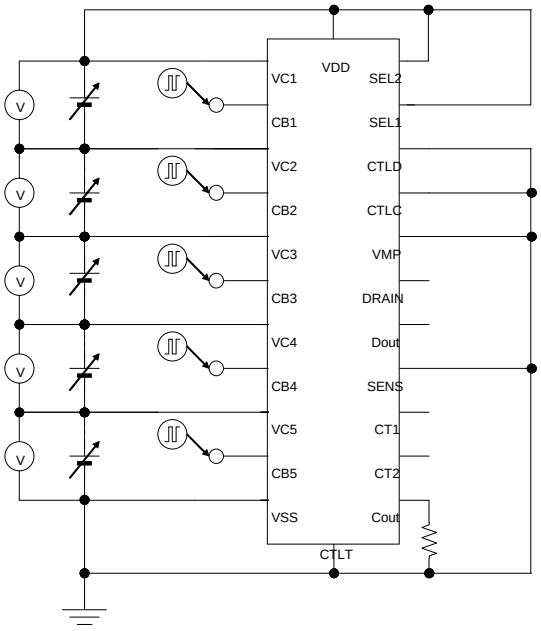

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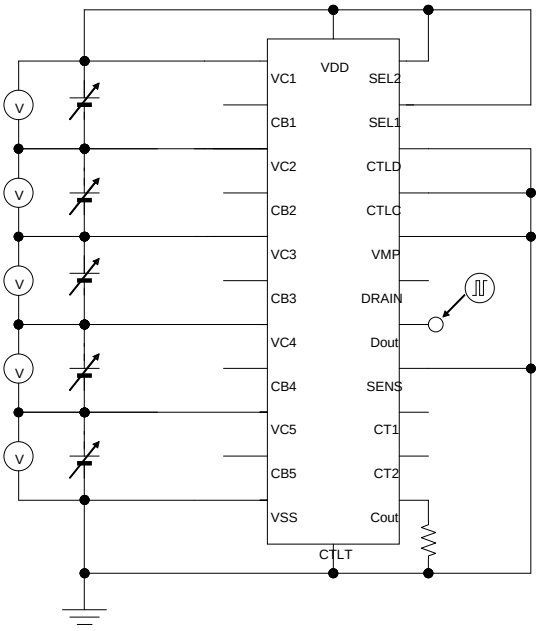

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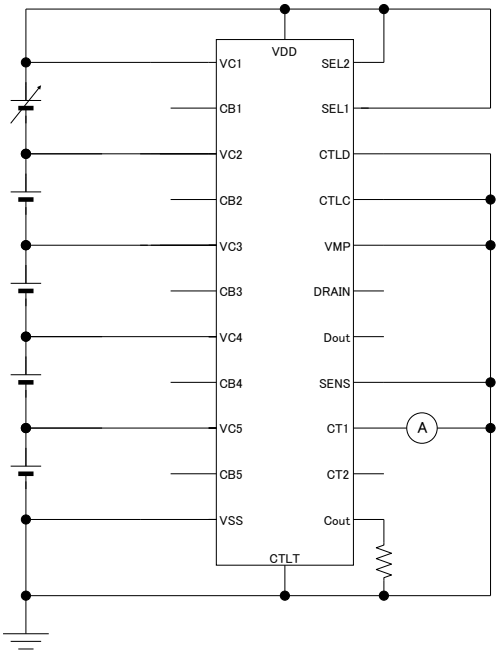
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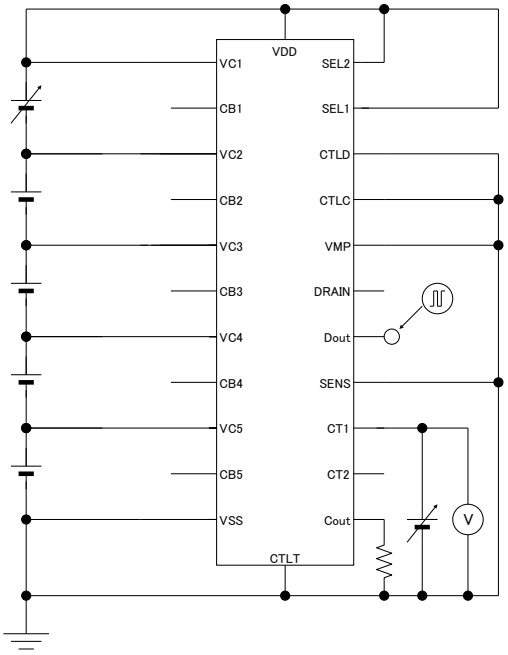
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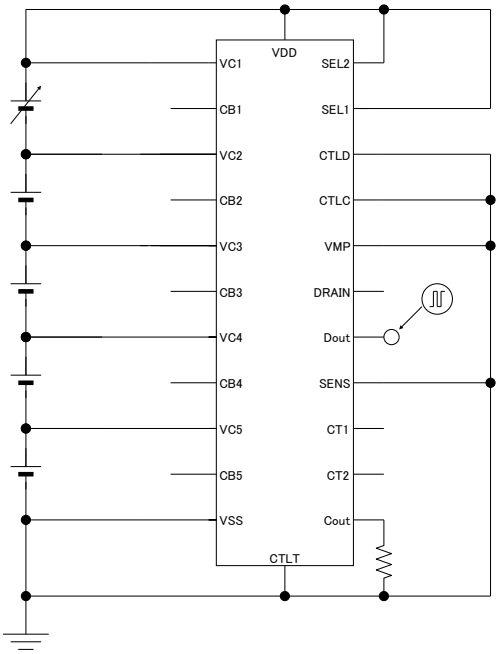
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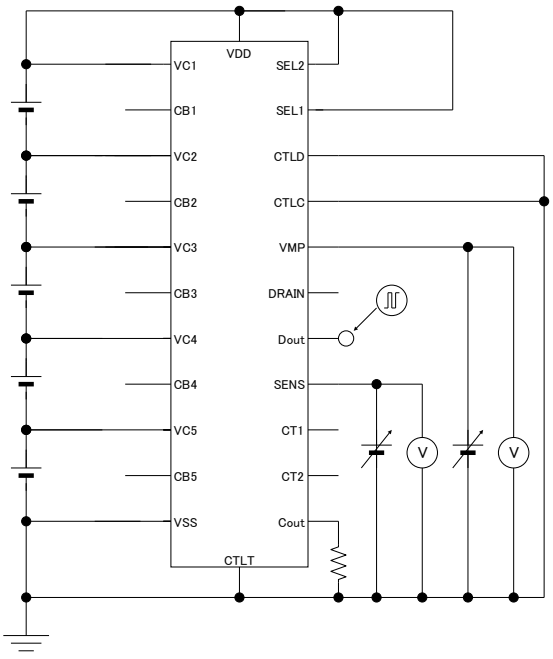
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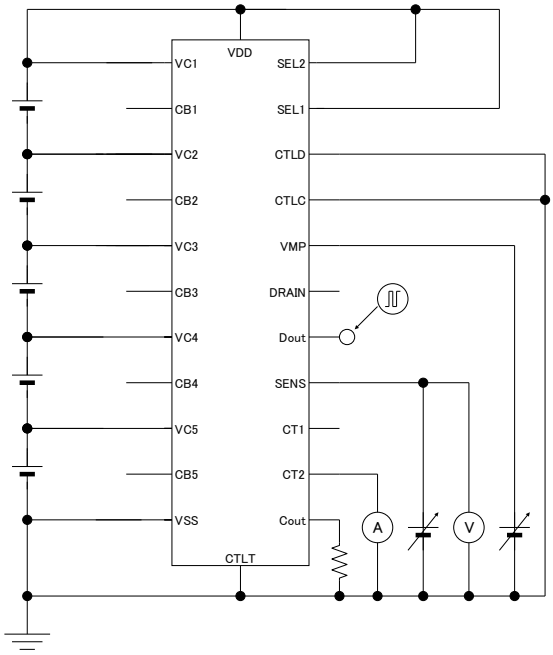
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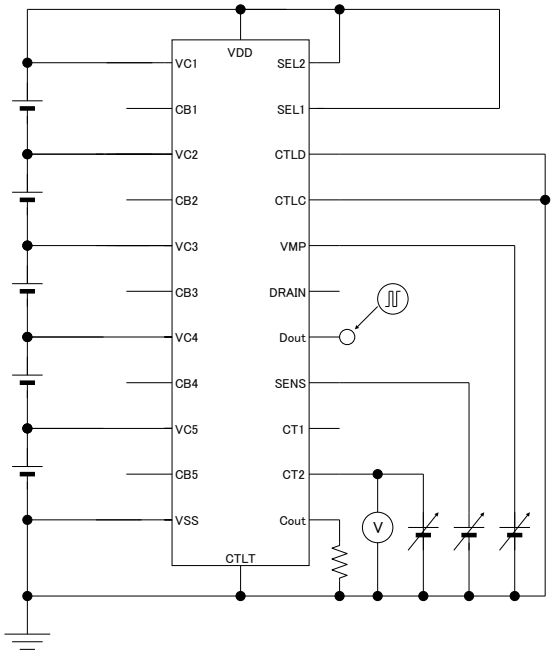
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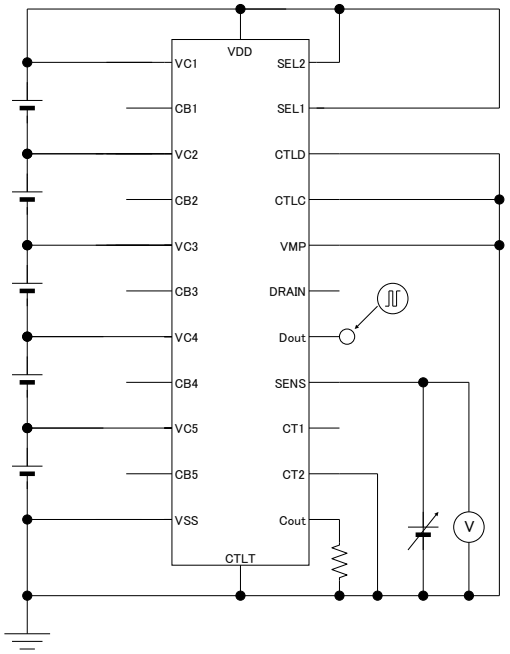
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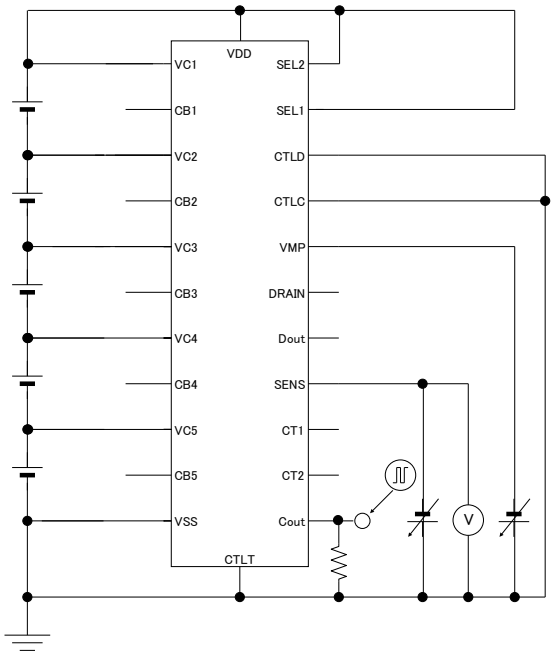
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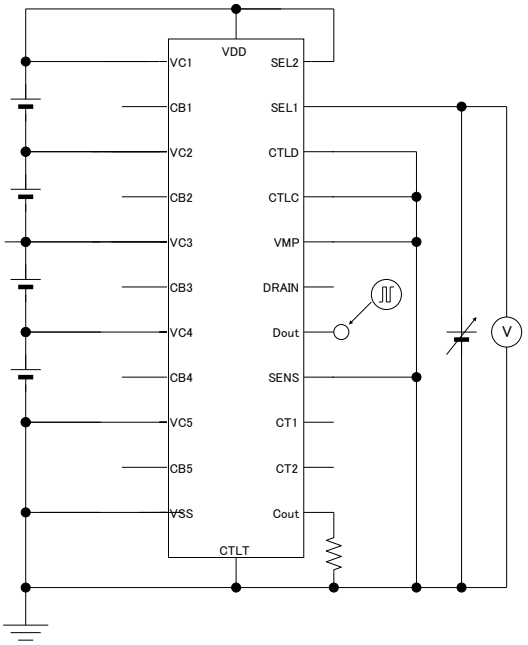
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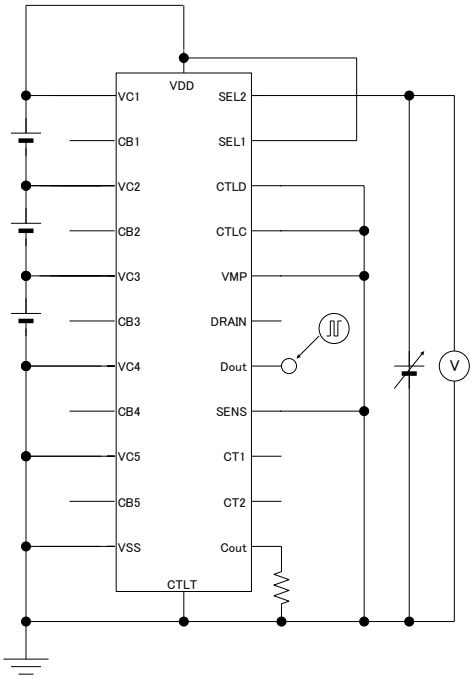
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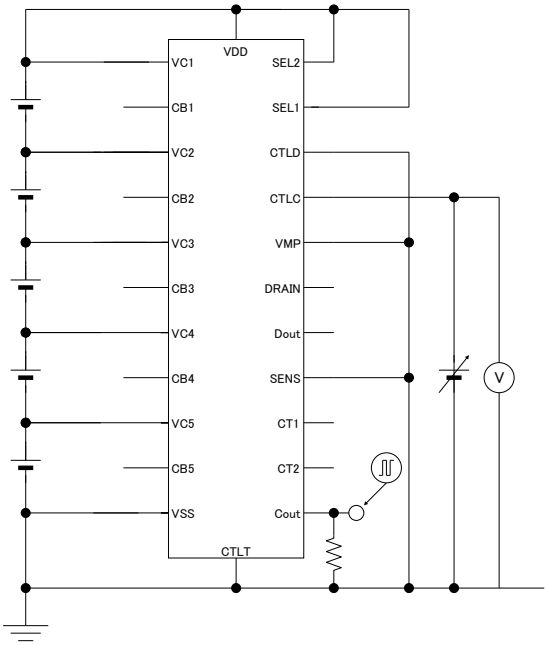
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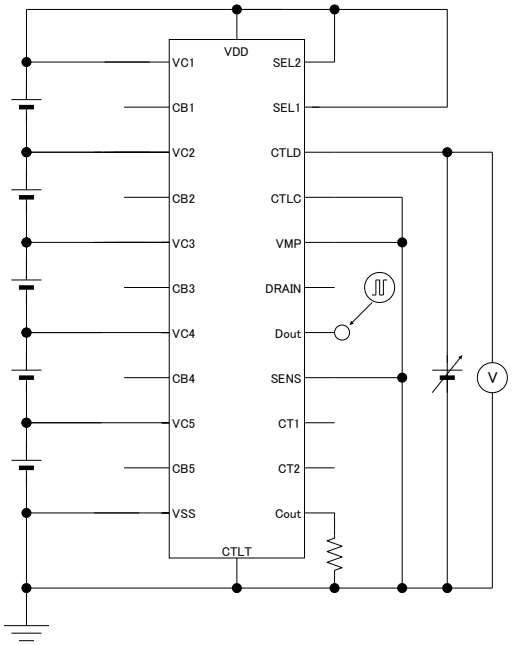
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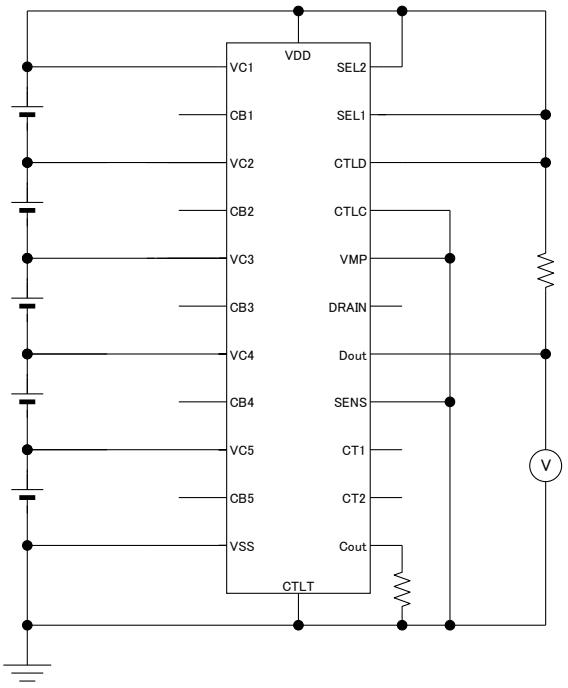
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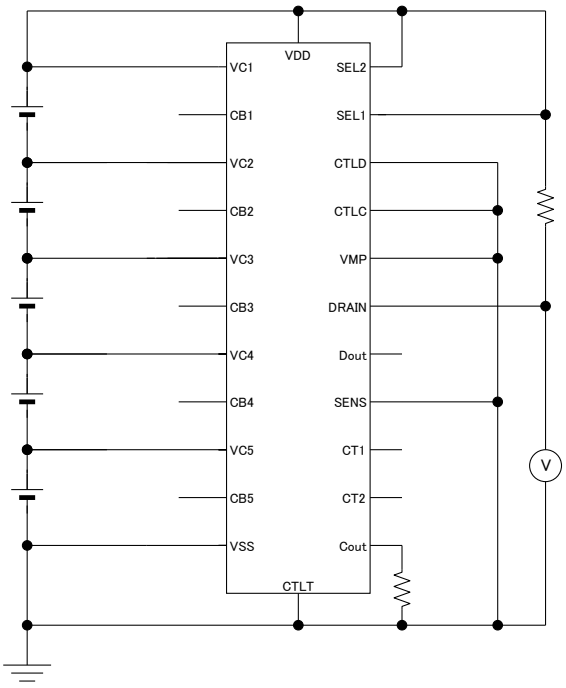
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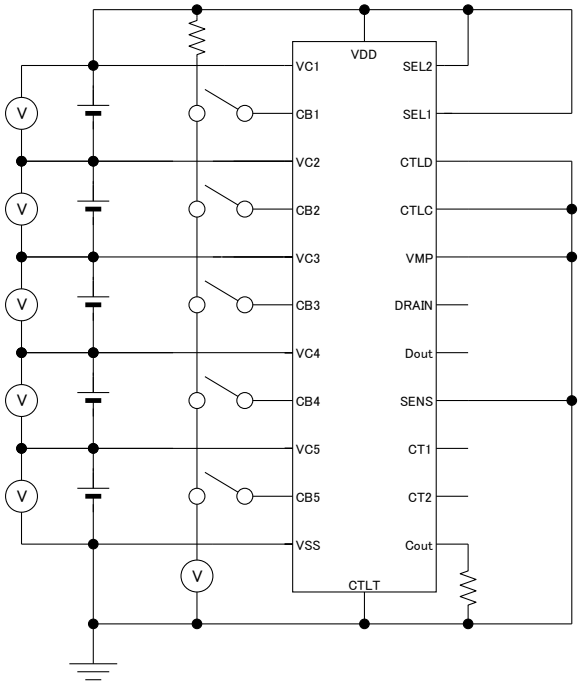
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VC1
CB1
VC2
CB2
VC3
CB3
VC4
CB4
VC5
CB5
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SEL2
SEL1
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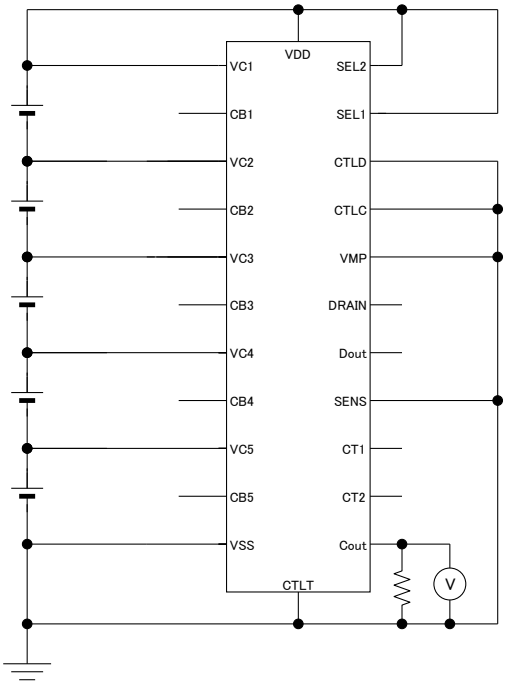
CTLC
VMP
DRAIN
Dout
SENS
CT1
CT2
Cout
CTLT
V

T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Dout
SENS
CT1
CT2
Cout
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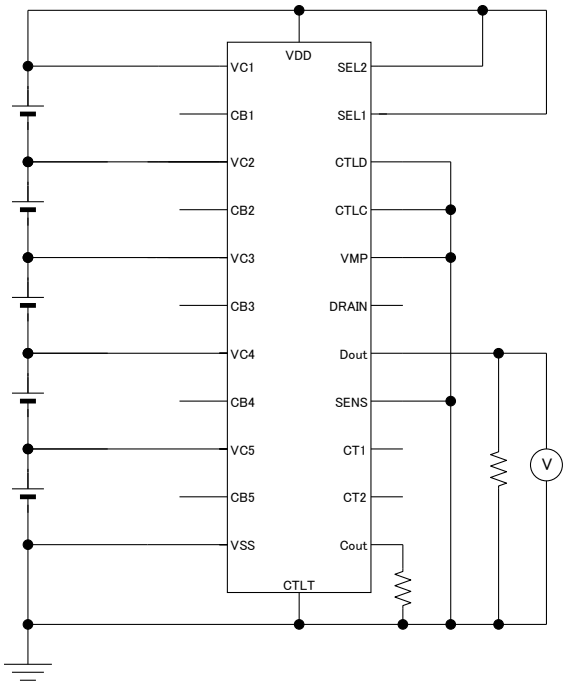
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CB2
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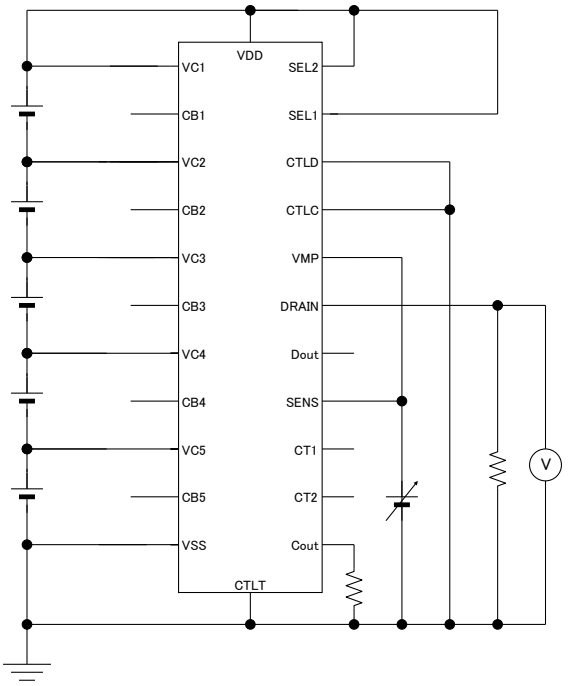
V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CTLT
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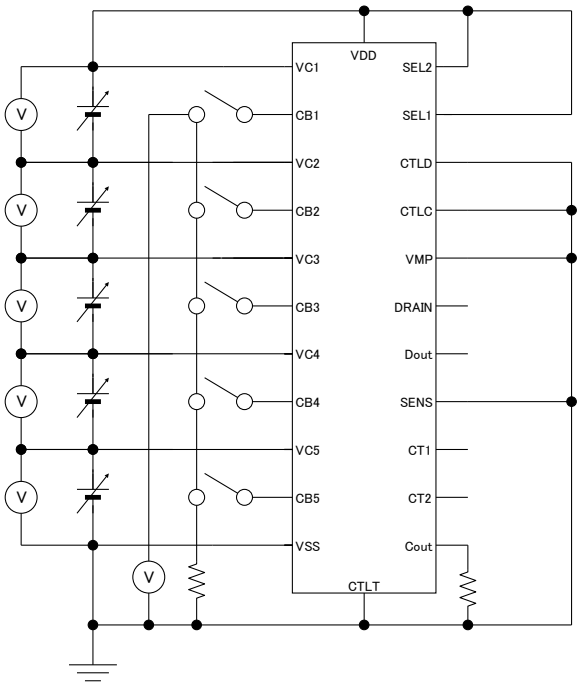
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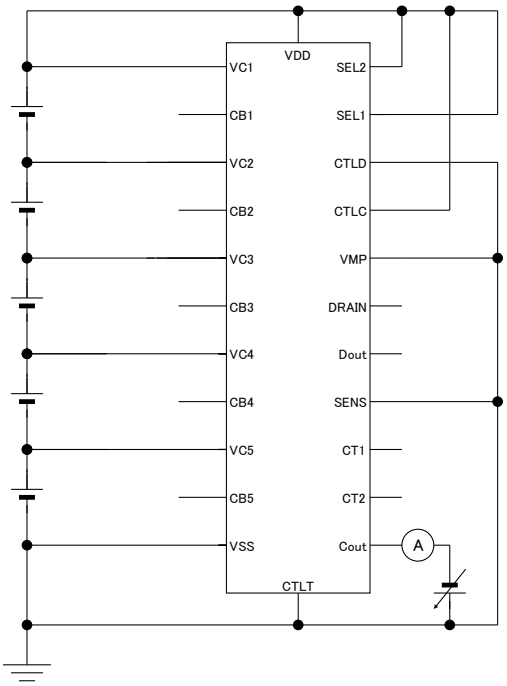
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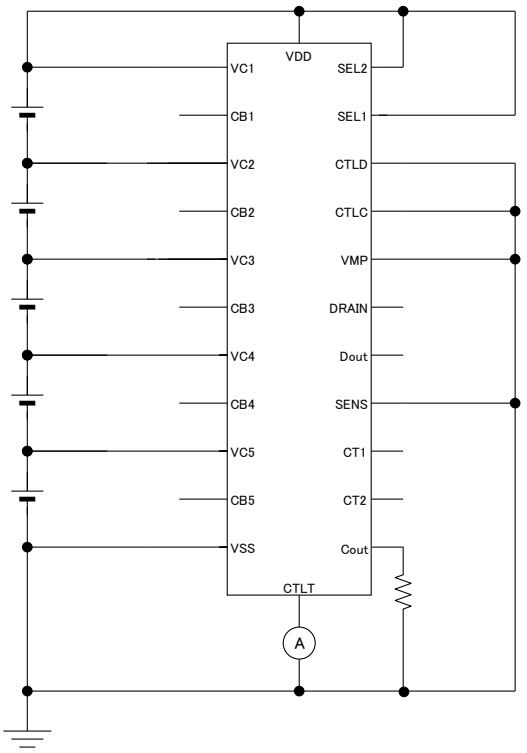
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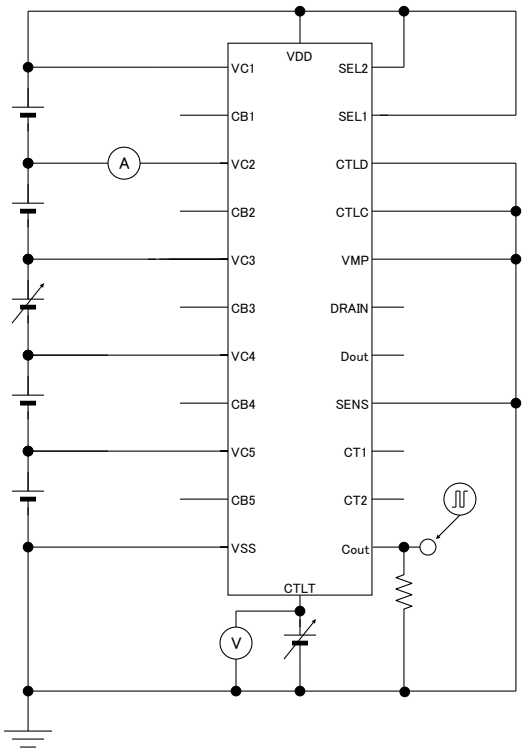
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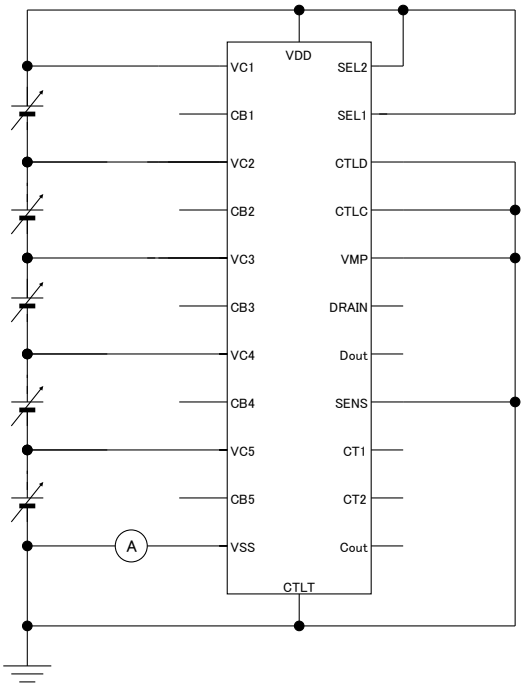
VDD
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VMP
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SENS
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Cout
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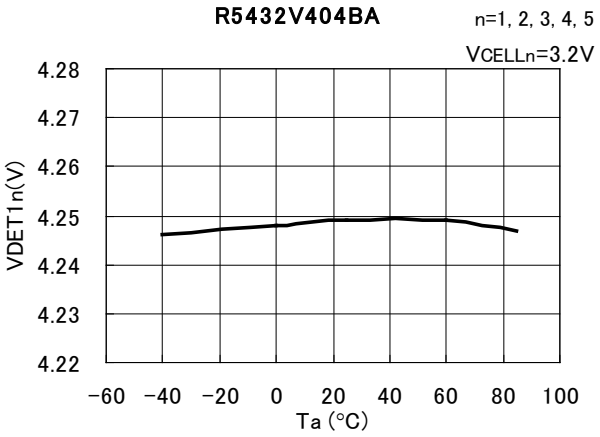
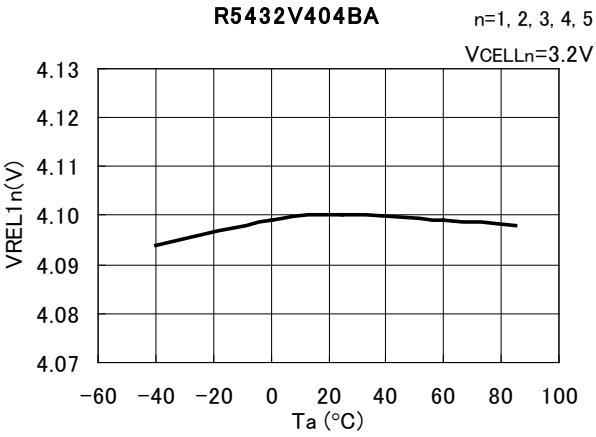
TYPICAL CHRACTERSTICS

Part1. Temperature Characteristics

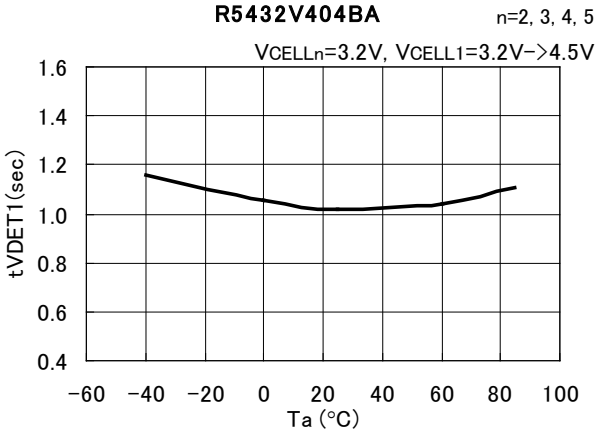
1) Overcharge voltage threshold (CELLn)



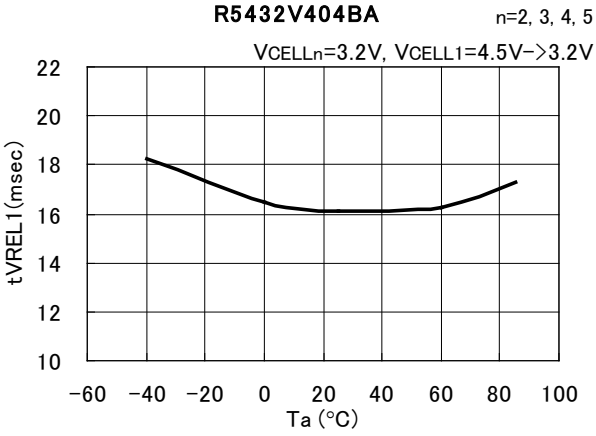
2) Overcharge Released Voltage (CELLn)



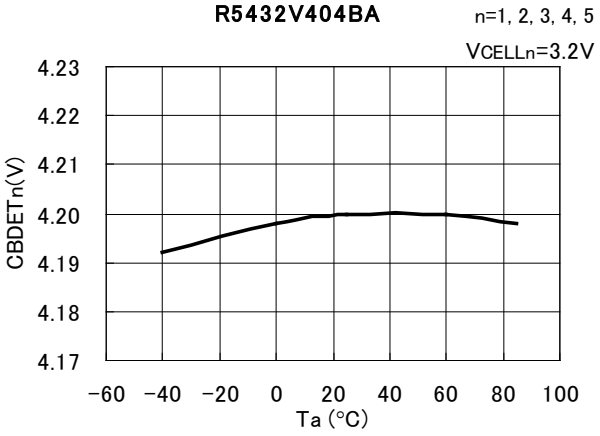
3) Overcharge Detector Delay



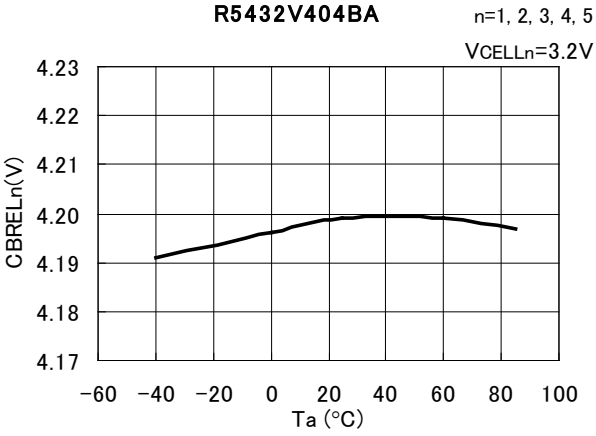
4) Released from Overcharged Delay time Temperature



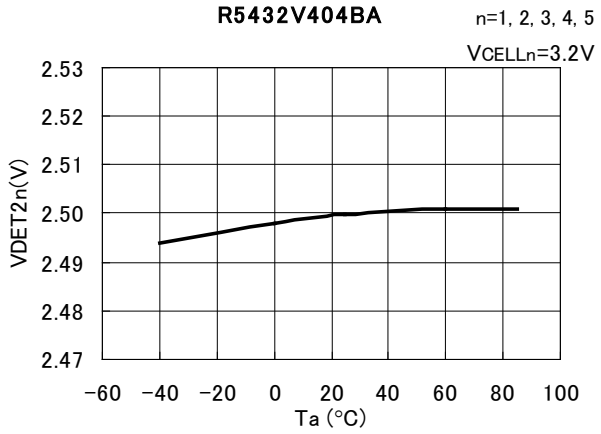
5) CELL balance detector (CELLn) threshold



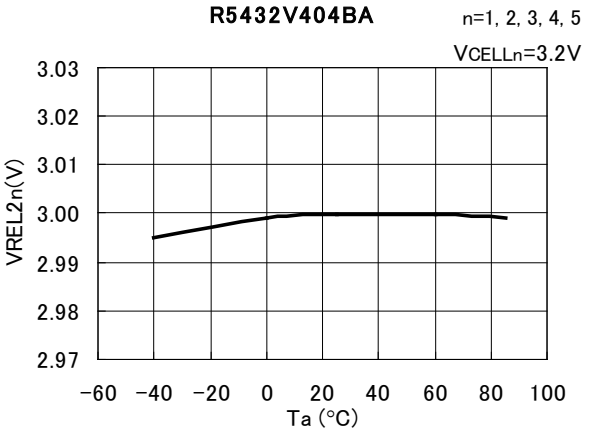
6) CELL balance released Voltage (CELLn)



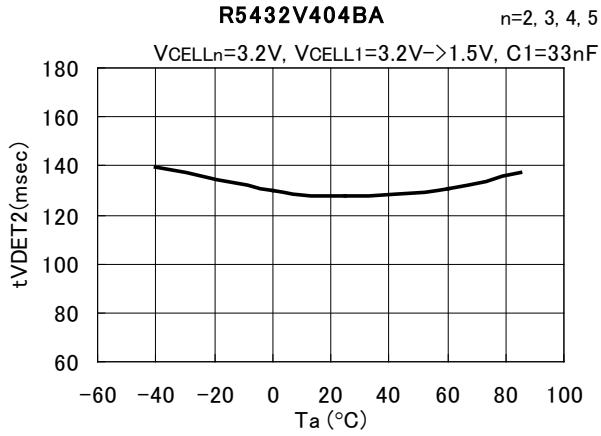
7) Overdischarge Detector Threshold (CELLn)



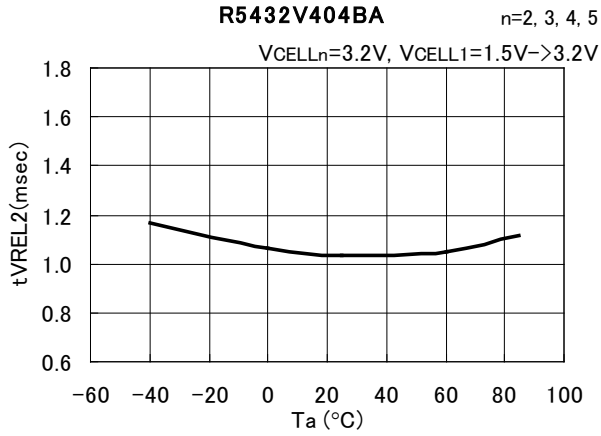
8) Released Voltage from overdischarge (CELLn)



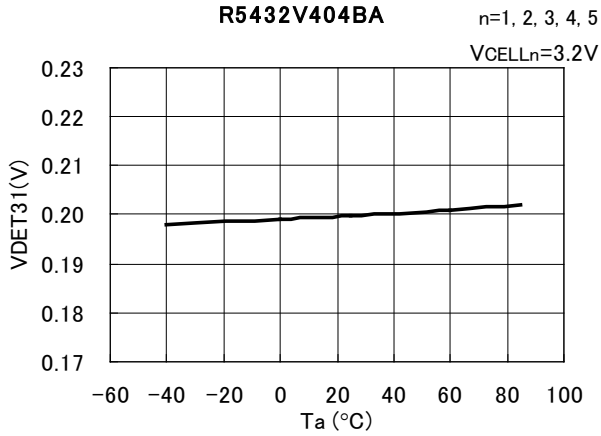
9) Output Delay time of Overdischarge (CELLn)



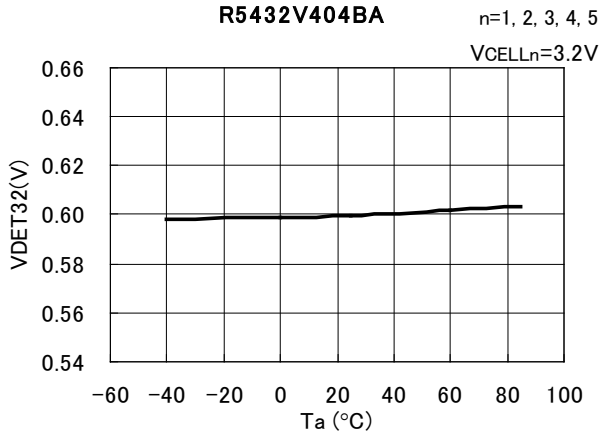
10) Output Delay Time of Released from Overdischarge (CELLn)



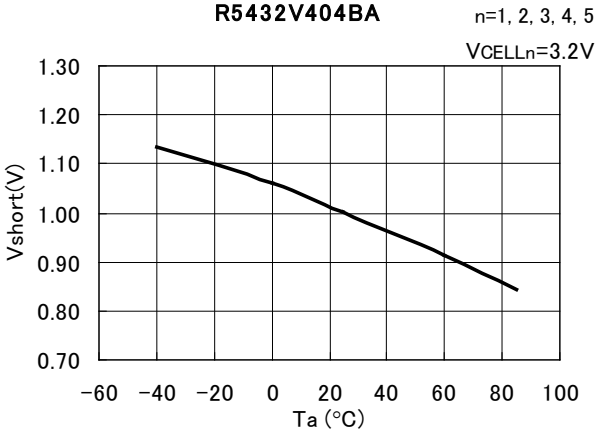
11) Excess Discharge Current Detector Thershold1



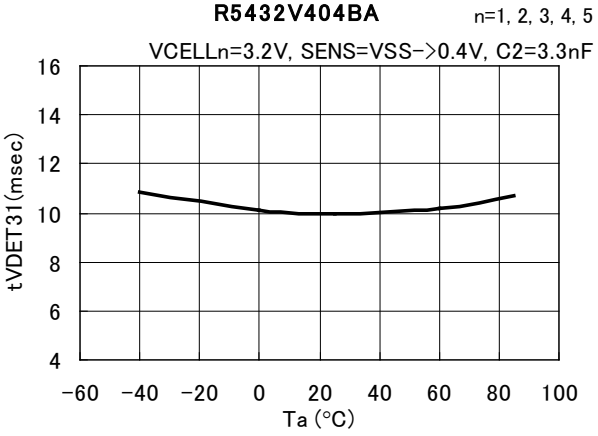
12) Excess Discharge Current Detector Thershold2



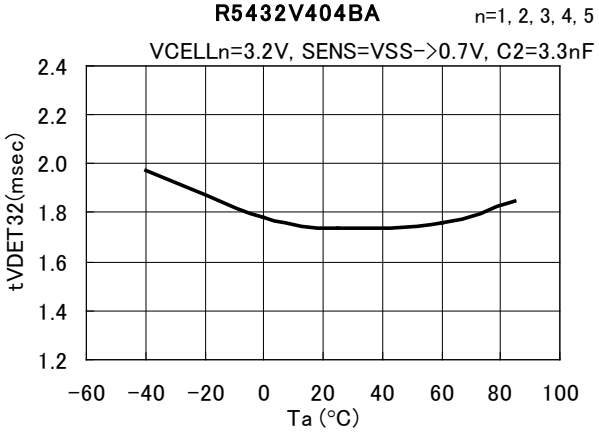
13) Short Detector Threshold



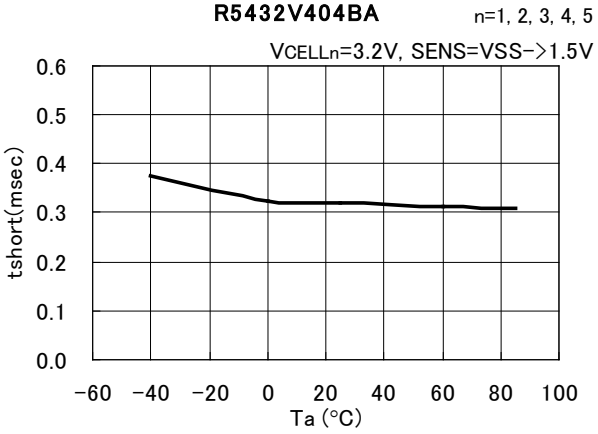
14) Excess discharge Current Detector Output Delay Time 1



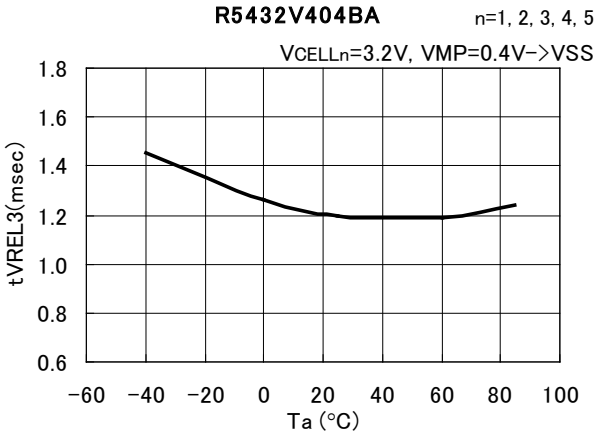
15) Excess discharge Current detector Output Delay Time2



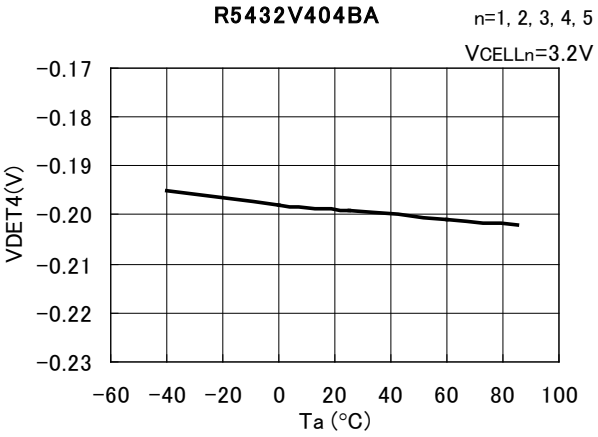
16) Short Detector Output Delay Time



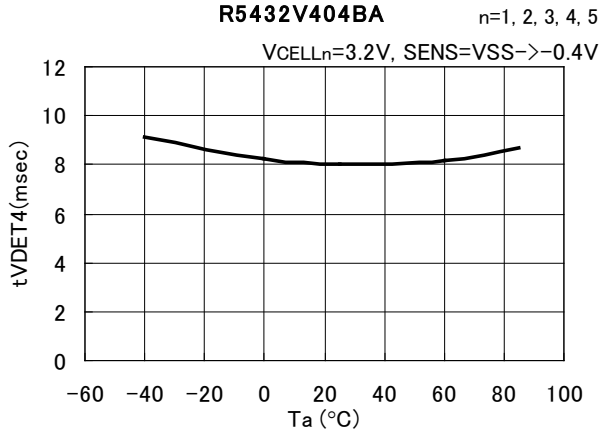
17) Excess discharge Current released delay time



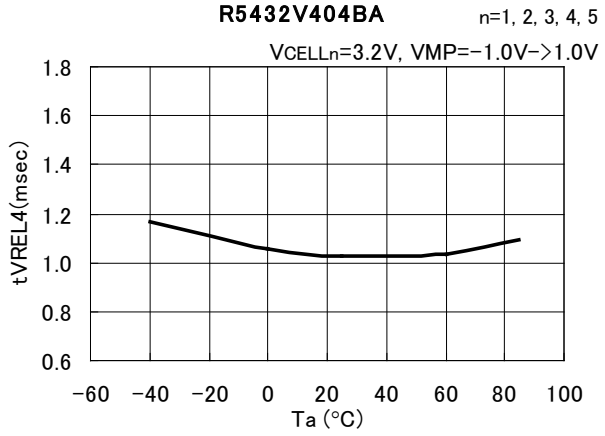
18) Excess charge Current Detector Threshold



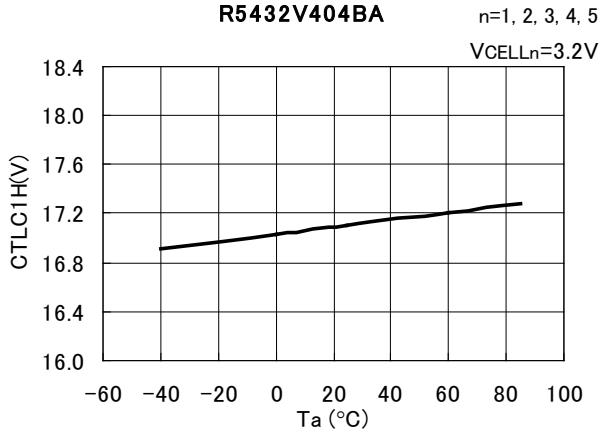
19) Excess Charge Current Output Delay Time



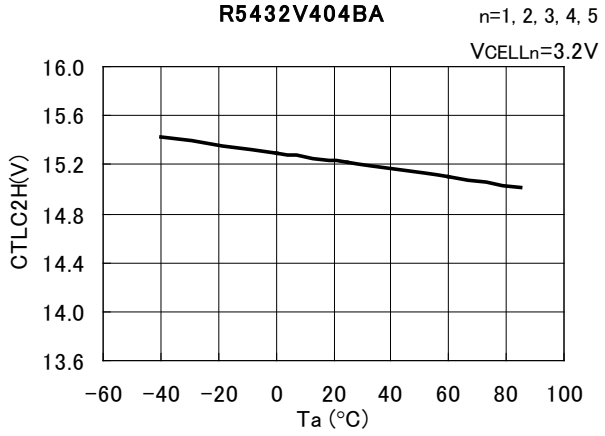
20) Excess Charge Current Delay Time of Released



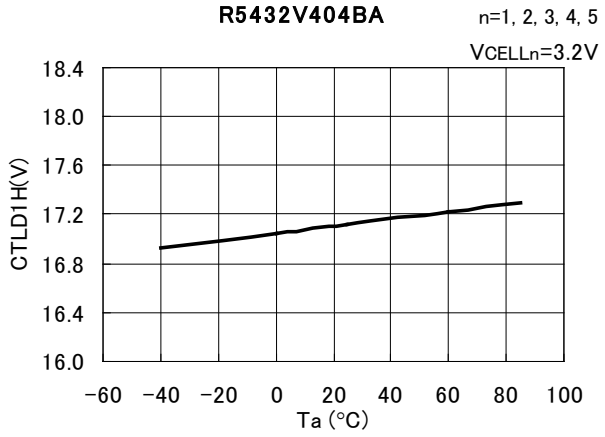
21) CTLC Pin "H" Input Voltage



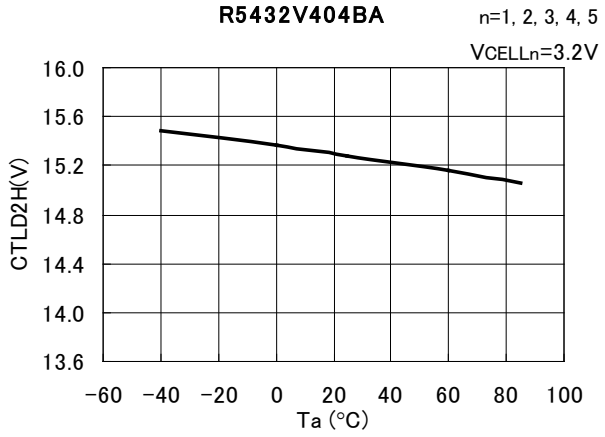
22) CTLC Pin "H2" Input Voltage



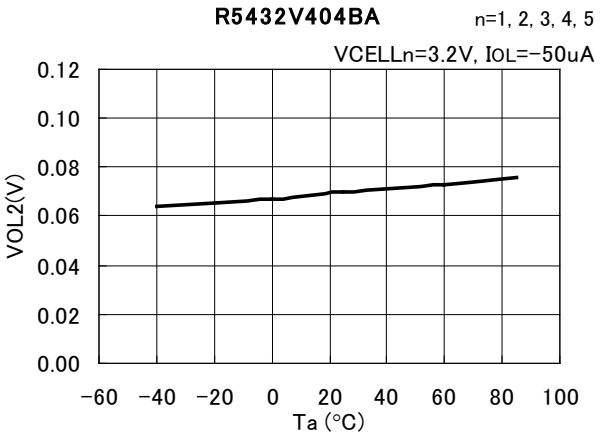
23) CTLD Pin "H1" Input Voltage



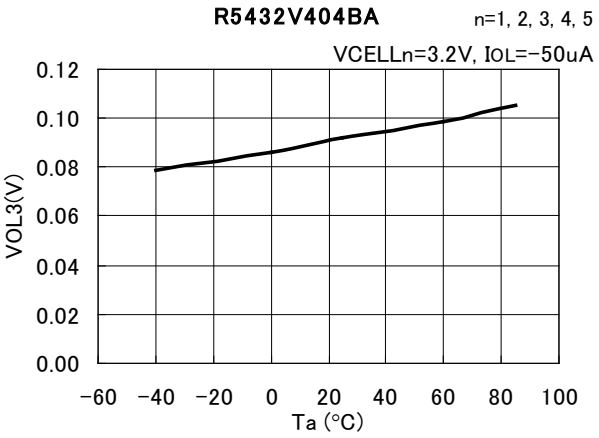
24) CTLD Pin "H2" Input Voltage



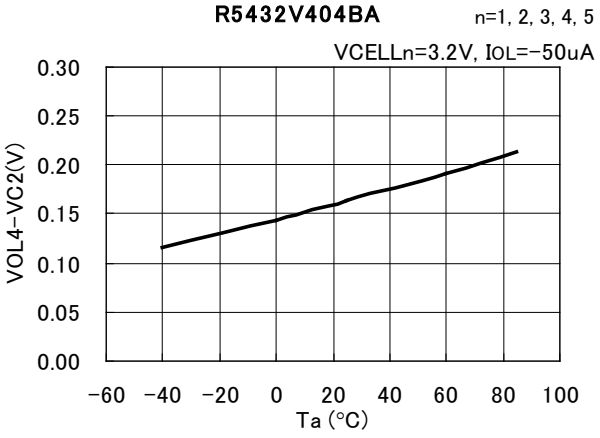
25) DOUT Nch ON Voltage



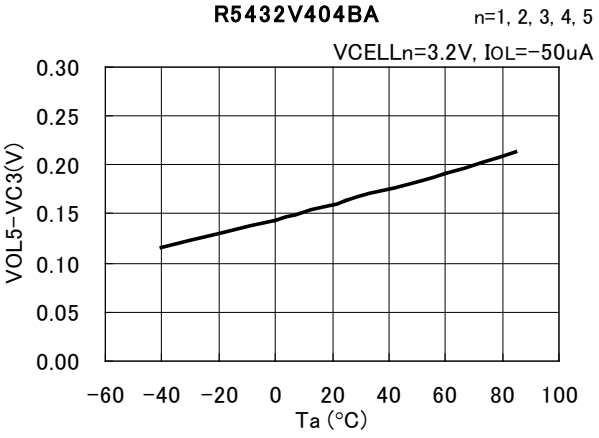
26) DRAIN Nch ON Voltage



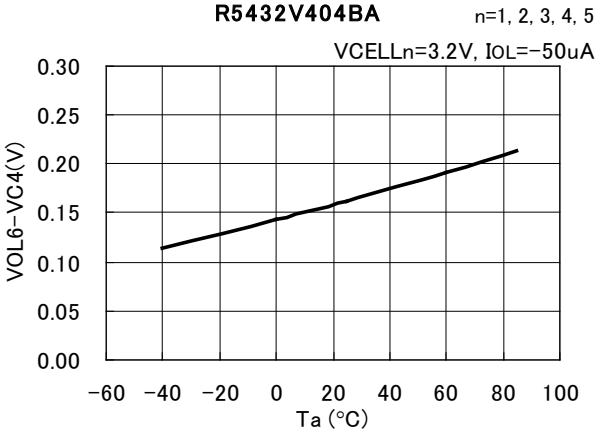
27) CB1 Nch ON Voltage



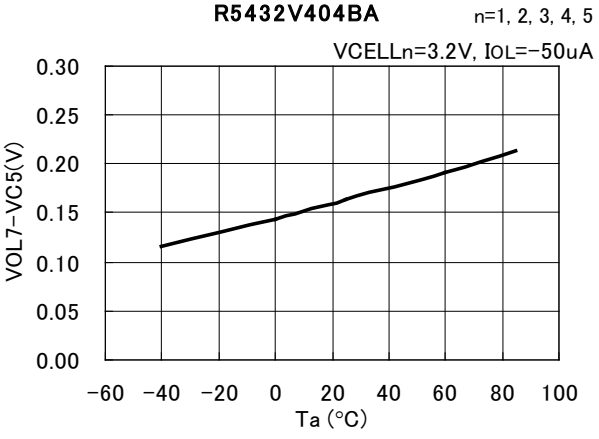
28) CB2 Nch ON Voltage



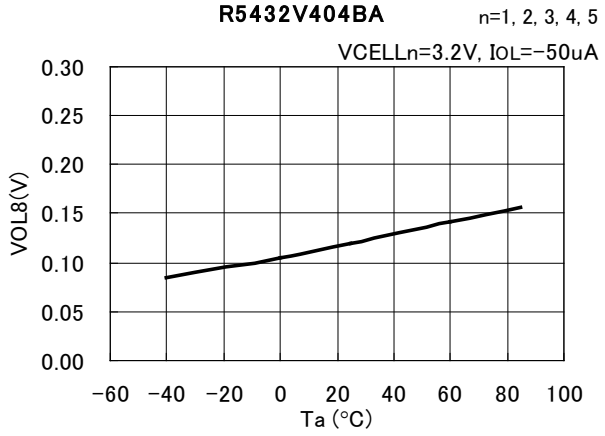
29) CB3 Nch ON Voltage



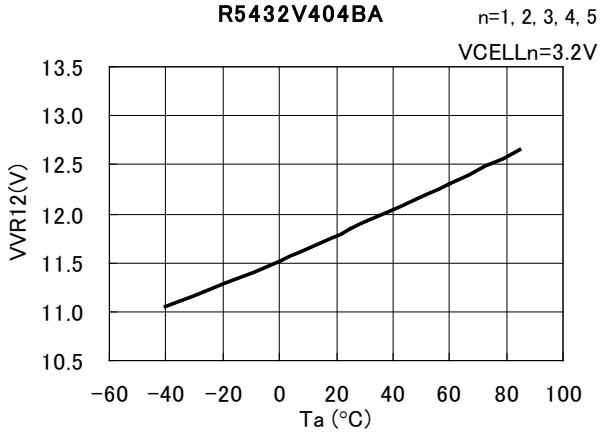
30) CB4 Nch ON Voltage



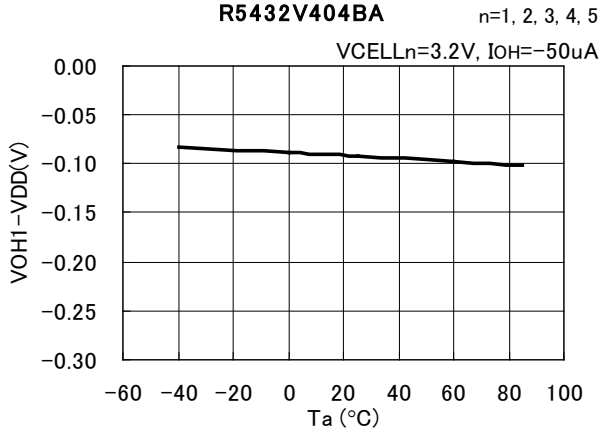
31) CB5 Nch ON Voltage



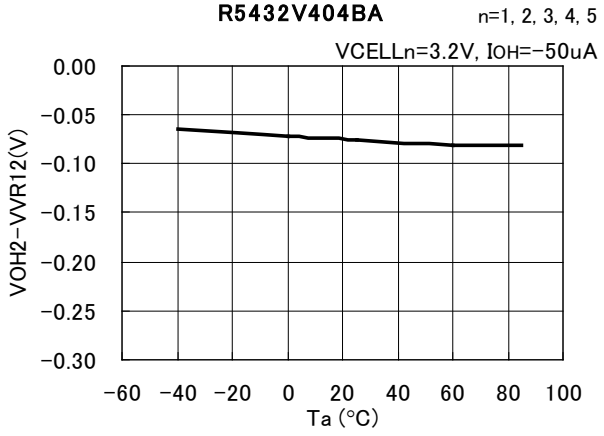
32) VR12V Output Voltage



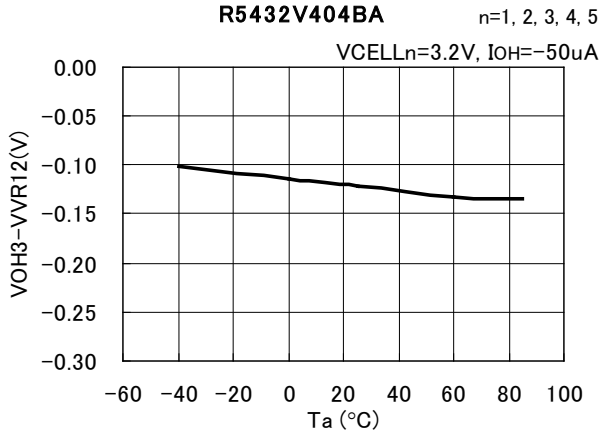
33) COUT Pch ON Voltage



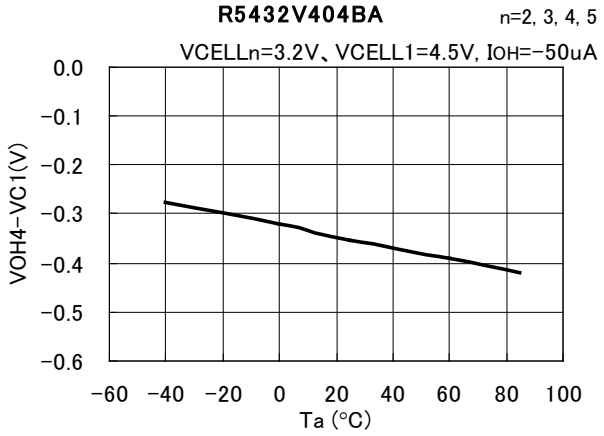
34) DOUT Pch ON Voltage



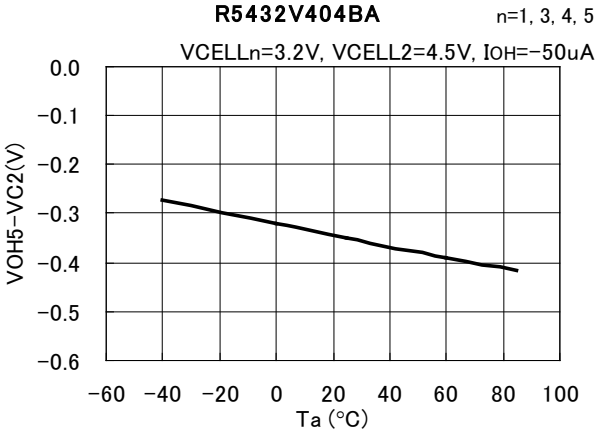
35) DRAIN Pch ON Voltage



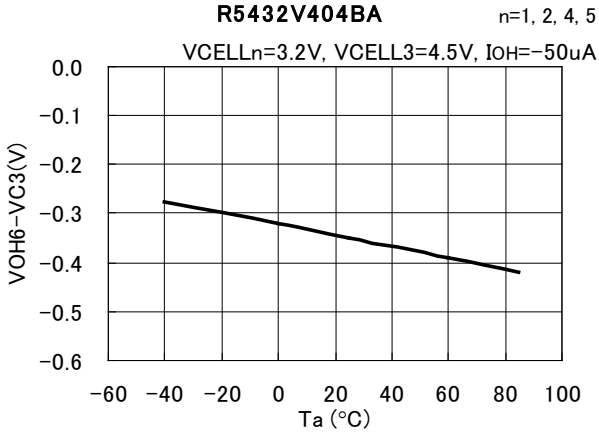
36) CB1 Pch ON Voltage



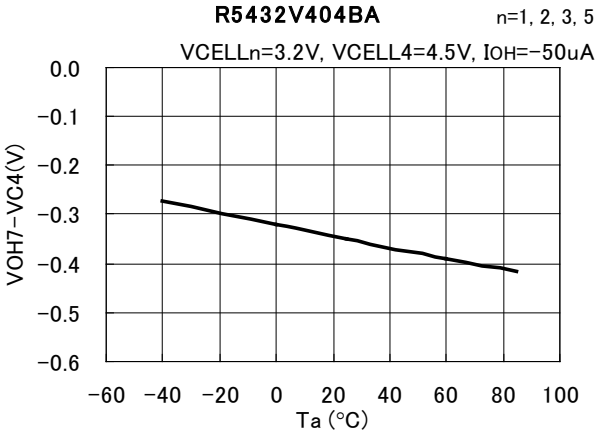
37) CB2 Pch ON Voltage



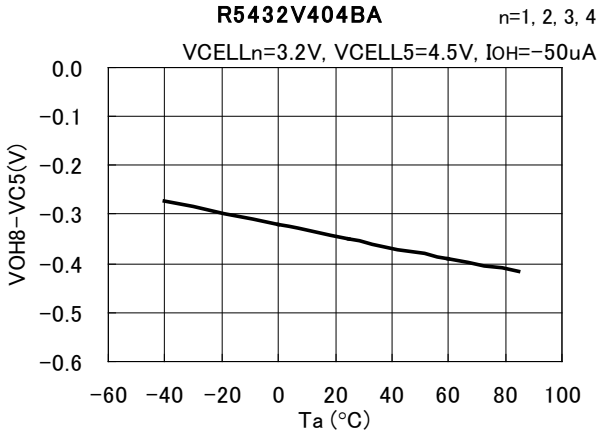
38) CB3 Pch ON Voltage



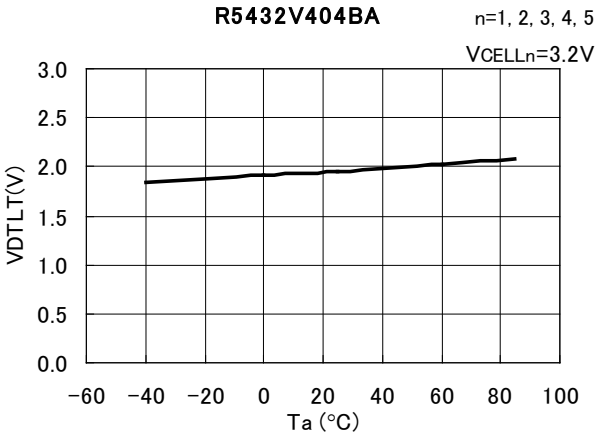
39) CB4 Pch ON Voltage



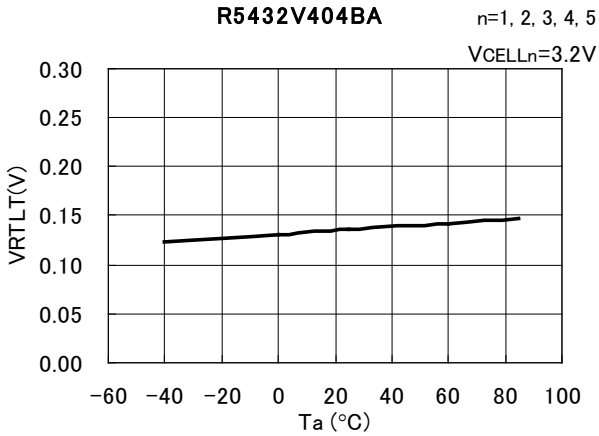
40) CB4 Pch ON Voltage



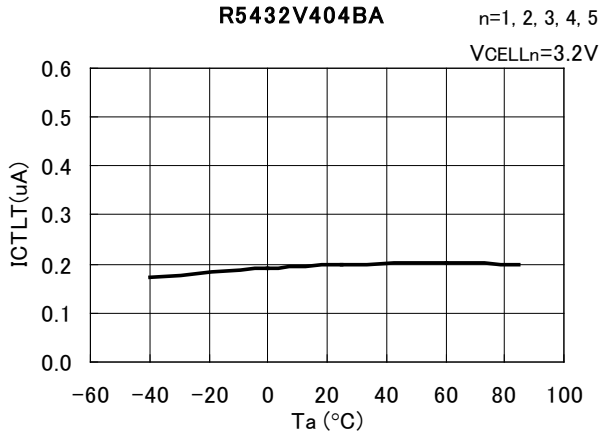
41) CTLT Detector threshold



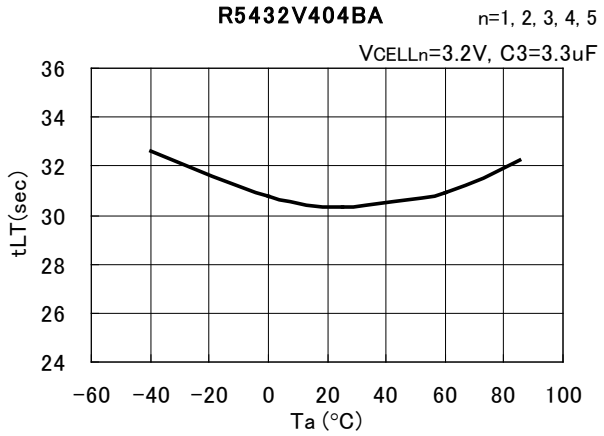
42) CTLT release Voltage



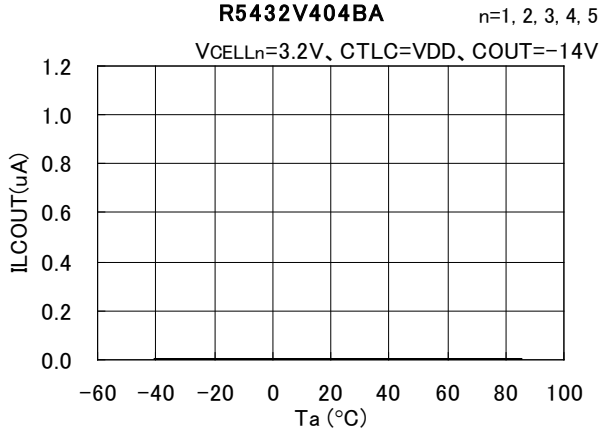
43) CTLT Excess charge Current



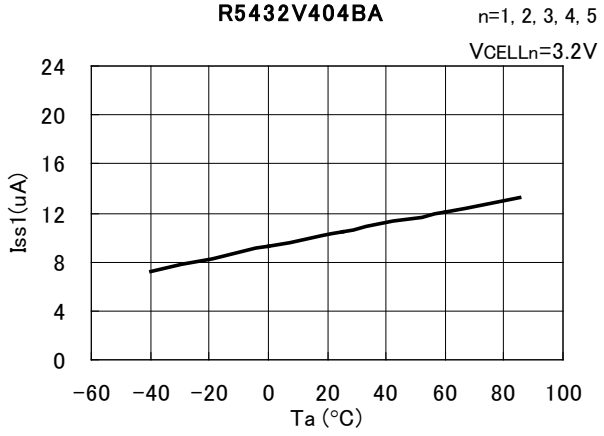
44) Open-wire test interval time



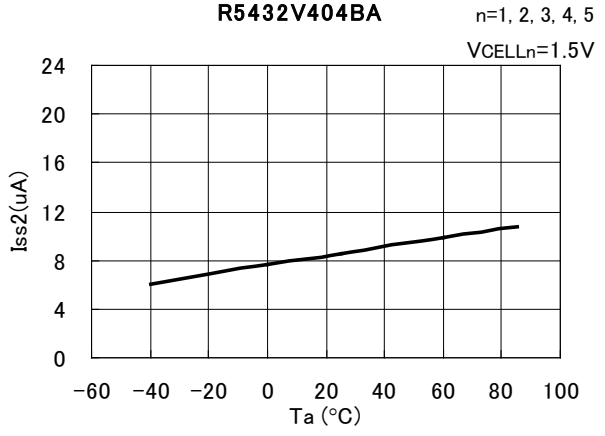
45) C_{OUT} Off leak current



46) Supply Current1

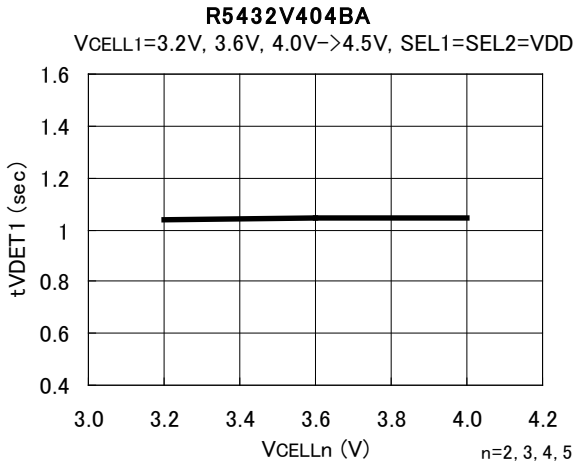


47) Supply Current2

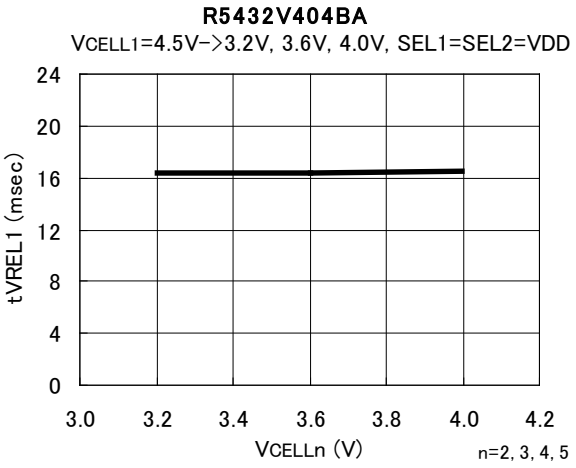


Part2.Output Delay Time V_{DD} dependence

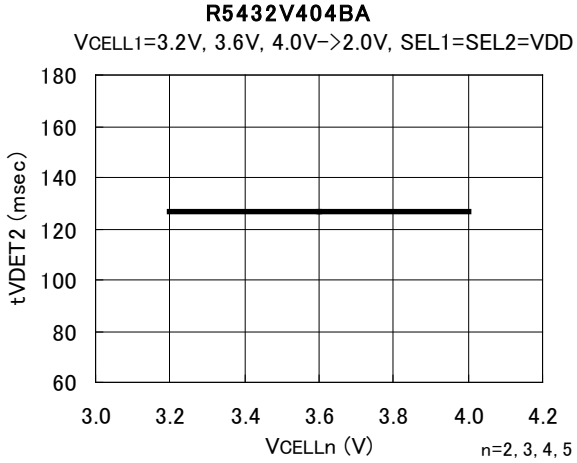
1) Overcharge detector output Delay Time



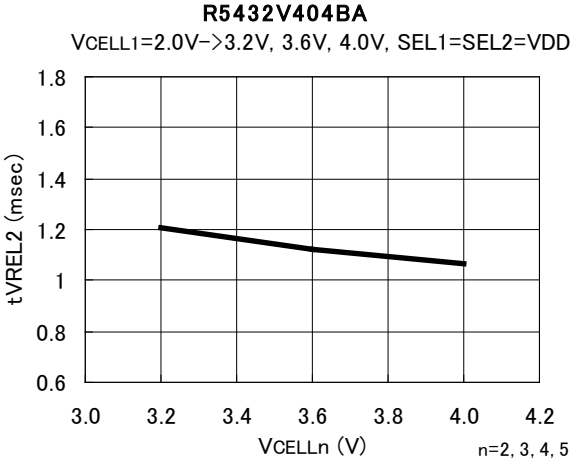
2) Overcharge Released Delay Time



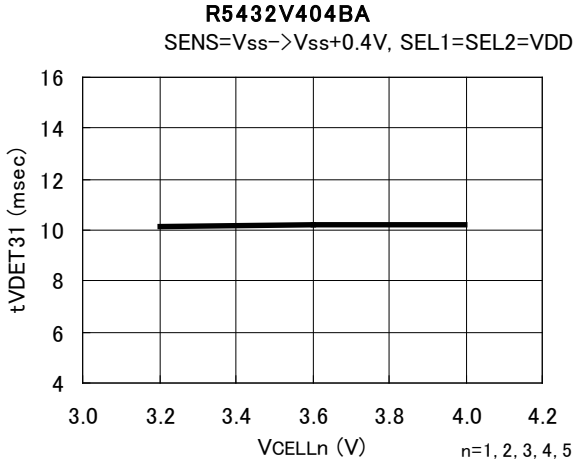
3) Overdischarge detector output Delay Time



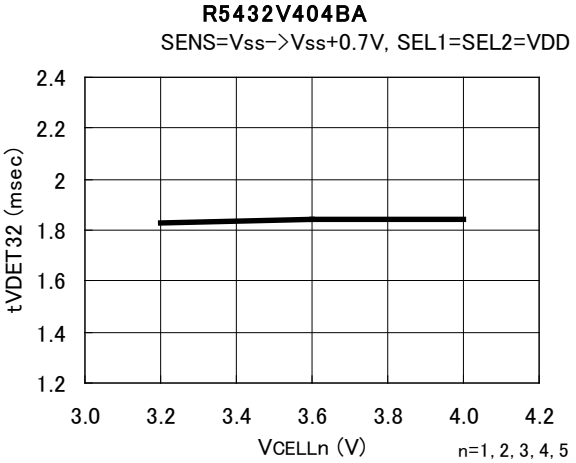
4) Overdischarge Released Delay Time



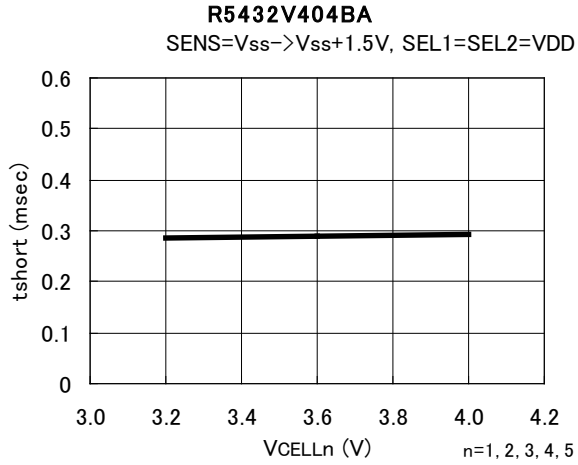
5) Excess discharge current detector Delay Time 1



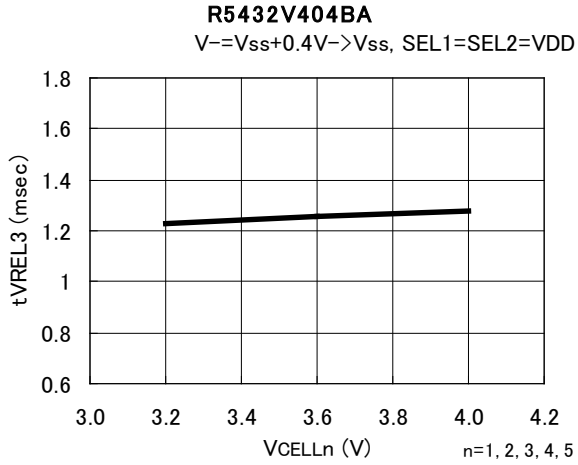
6) Excess discharge current detector Delay Time 2



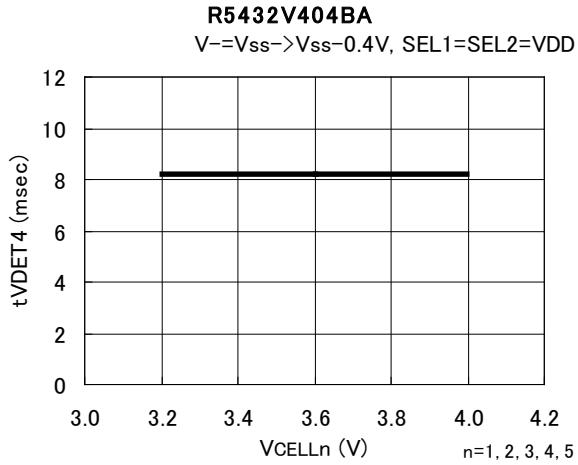
7) Short detector output delay time1



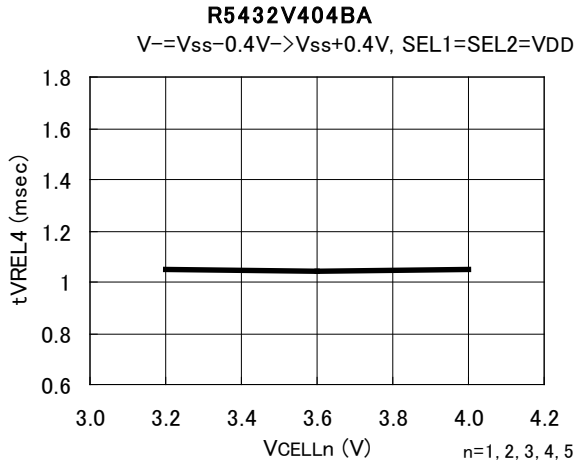
8) Excess discharge current released delay time2



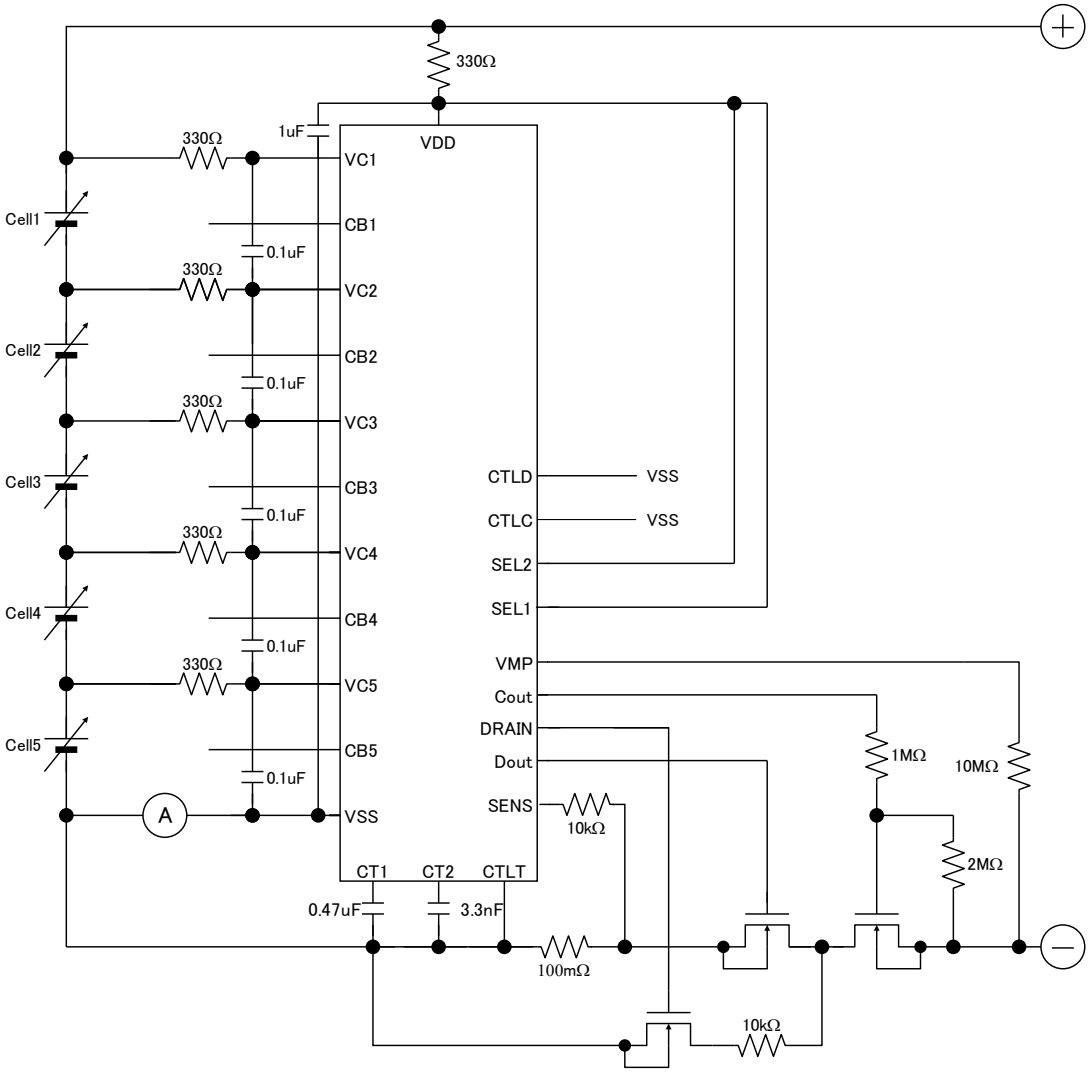
9) Excess charge current detector output Delay Time



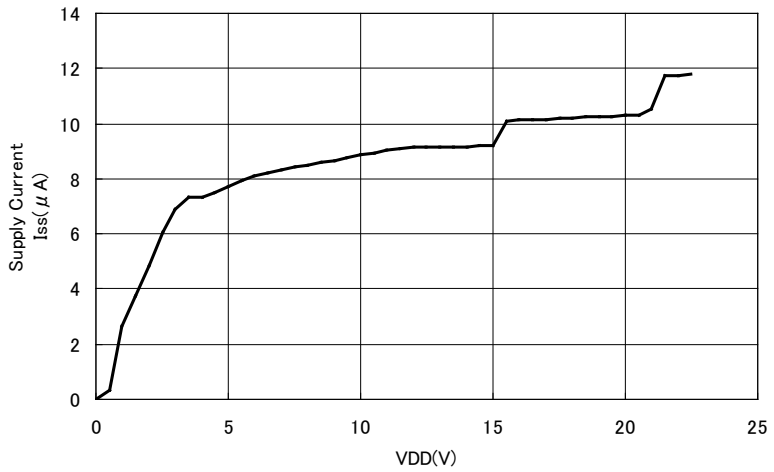
10) Excess charge current released delay time



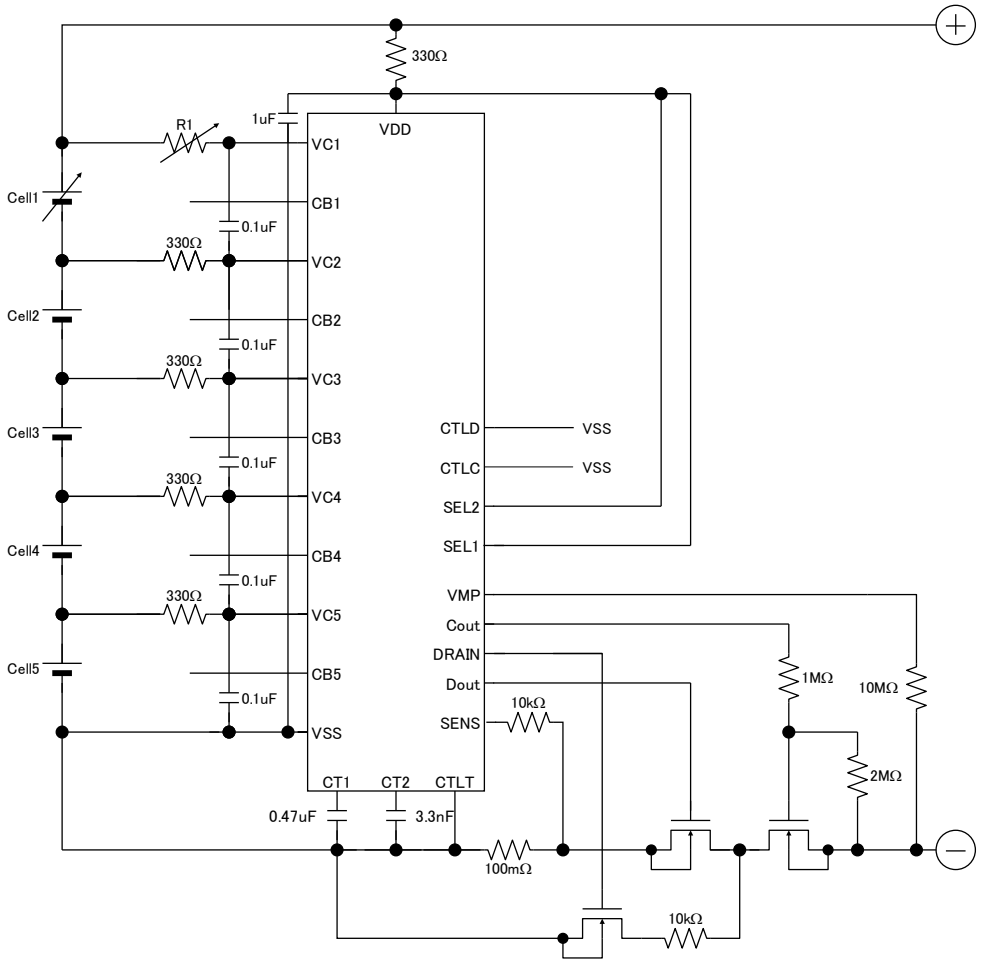
- **Part3. Supply Current V_{DD} dependence (R5432V404BA)**



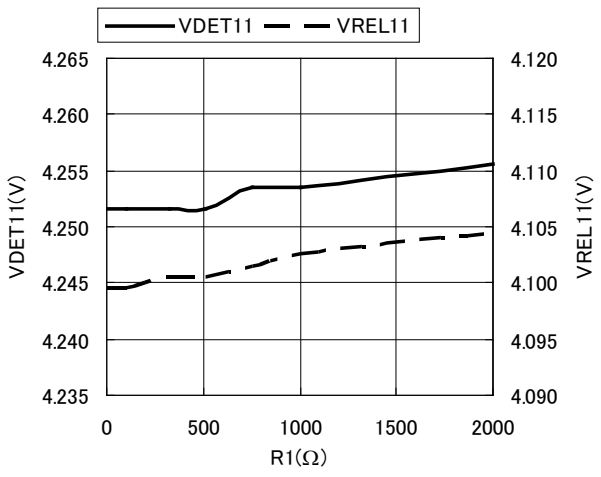
Supply Current for 5-cell protection



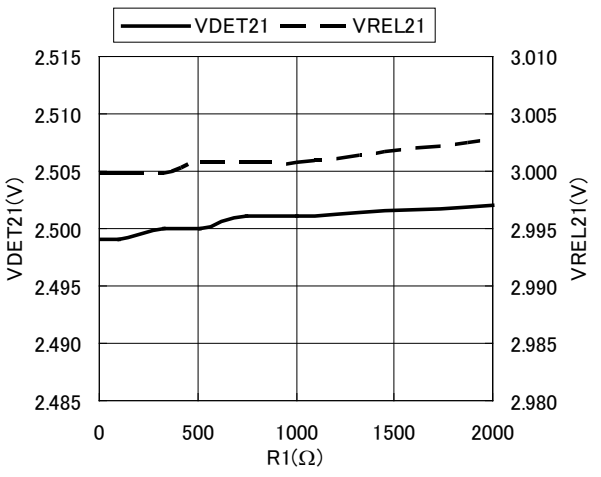
Part4. External resistance dependence (R5432V404BA)



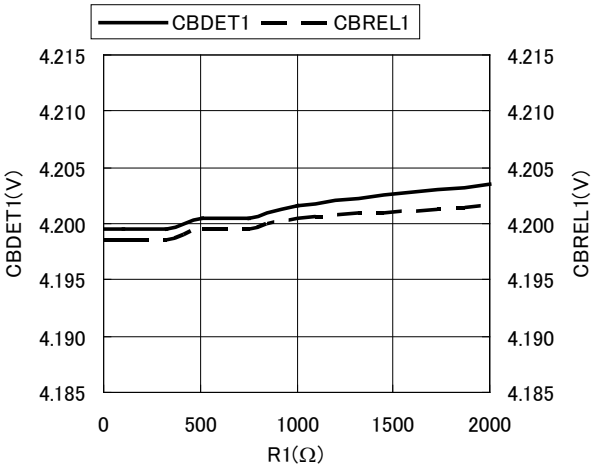
Overcharge Detector/Released Voltage from Overcharge vs. R1 (CELL1)



Overdischarge Detector/Released Voltage from Overdischarge vs. R1 (CELL1)



CELL balance detector / Released Voltage from CELL balance vs. R1 (CELL1)



Ver. A

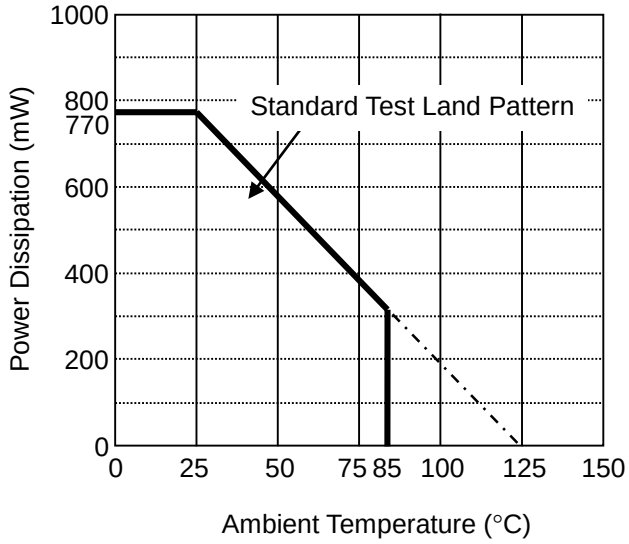
The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following conditions are used in this measurement.

Measurement Conditions

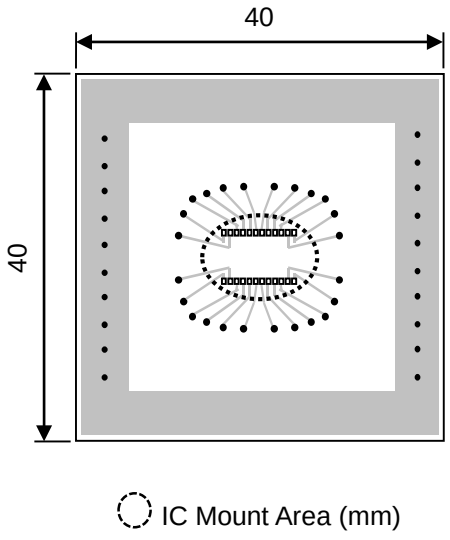
	Standard Test Land Pattern
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Double-Sided Board)
Board Dimensions	40 mm × 40 mm × 1.6 mm
Copper Ratio	Top Side: Approx. 50% Bottom Side: Approx. 50%
Through-holes	f 0.5 mm × 44 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

	Standard Test Land Pattern
Power Dissipation	770 mW
Thermal Resistance	qja = (125 − 25°C) / 0.770 W = 130°C/W

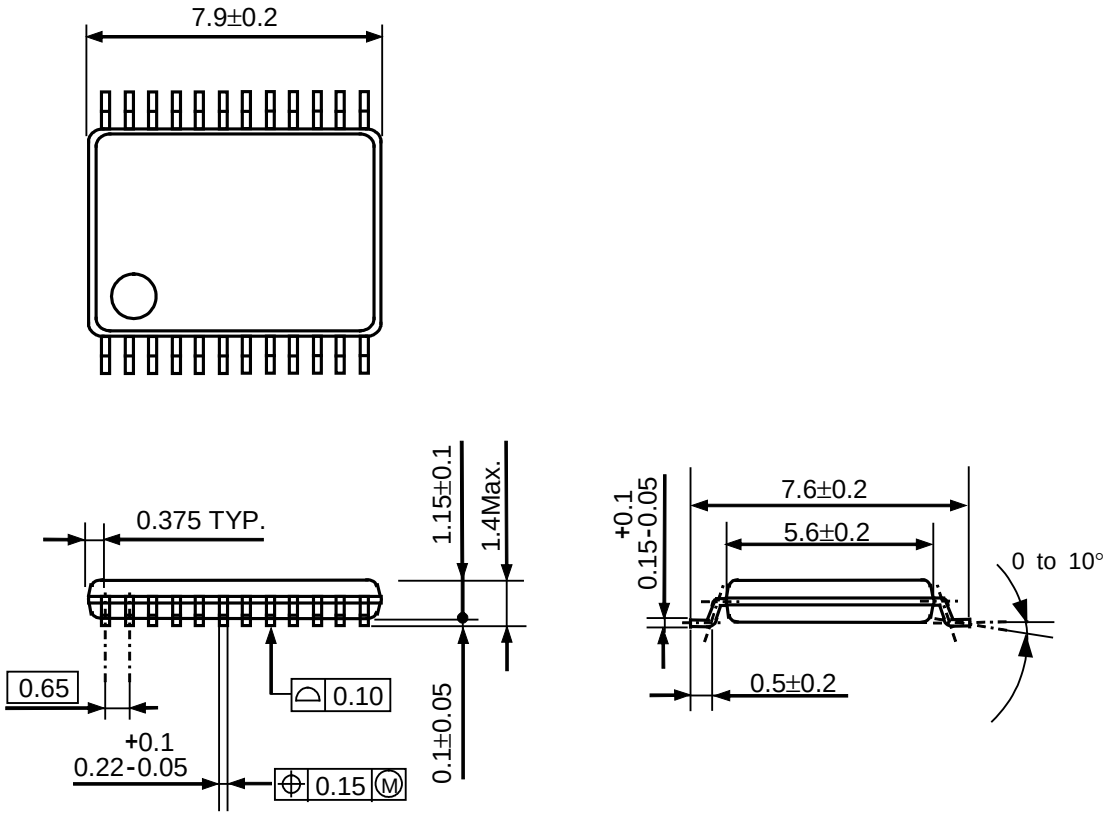


Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

RICOH



SSOP-24 Package Dimensions (Unit: mm)

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