

# DATA SHEET

Datasheet.Live

## **NE5517/NE5517A/AU5517**

Dual operational transconductance  
amplifier

Product data  
Replaces NE5517/NE5517A dated 2001 Aug 03

2002 Dec 06

## Dual operational transconductance amplifier

NE5517/NE5517A/  
AU5517

## DESCRIPTION

The AU5517 and NE5517 contain two current-controlled transconductance amplifiers, each with a differential input and push-pull output. The AU5517/NE5517 offers significant design and performance advantages over similar devices for all types of programmable gain applications. Circuit performance is enhanced through the use of linearizing diodes at the inputs which enable a 10 dB signal-to-noise improvement referenced to 0.5% THD. The AU5517/NE5517 is suited for a wide variety of industrial and consumer applications.

Constant impedance buffers on the chip allow general use of the AU5517/NE5517. These buffers are made of Darlington transistors and a biasing network that virtually eliminate the change of offset voltage due to a burst in the bias current  $I_{ABC}$ , hence eliminating the audible noise that could otherwise be heard in high quality audio applications.

## FEATURES

- Constant impedance buffers
- $\Delta V_{BE}$  of buffer is constant with amplifier  $I_{BIAS}$  change
- Excellent matching between amplifiers
- Linearizing diodes
- High output signal-to-noise ratio

## APPLICATIONS

- Multiplexers
- Timers
- Electronic music synthesizers
- Dolby™ HX Systems
- Current-controlled amplifiers, filters
- Current-controlled oscillators, impedances

## PIN CONFIGURATION

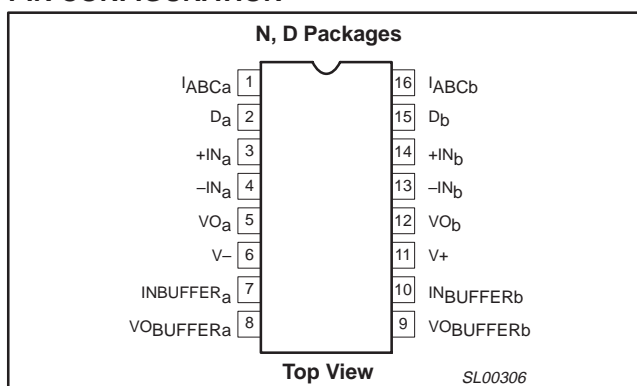


Figure 1. Pin Configuration

## PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$I_{ABCa}$	Amplifier bias input A
2	$D_a$	Diode bias A
3	$+IN_a$	Non-inverting input A
4	$-IN_a$	Inverting input A
5	$V_{Oa}$	Output A
6	$V-$	Negative supply
7	$IN_{BUFFERa}$	Buffer input A
8	$VO_{BUFFERa}$	Buffer output A
9	$VO_{BUFFERb}$	Buffer output B
10	$IN_{BUFFERb}$	Buffer input B
11	$V+$	Positive supply
12	$V_{Ob}$	Output B
13	$-IN_b$	Inverting input B
14	$+IN_b$	Non-inverting input B
15	$D_b$	Diode bias B
16	$I_{ABCb}$	Amplifier bias input B

## ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70 °C	NE5517N	SOT38-4
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70 °C	NE5517AN	SOT38-4
16-Pin Small Outline (SO) Package	0 to +70 °C	NE5517D	SOT109-1
16-Pin Small Outline (SO) Package	-40 to +125 °C	AU5517D	SOT109-1

# Dual operational transconductance amplifier

NE5517/NE5517A/  
AU5517

## CIRCUIT SCHEMATIC

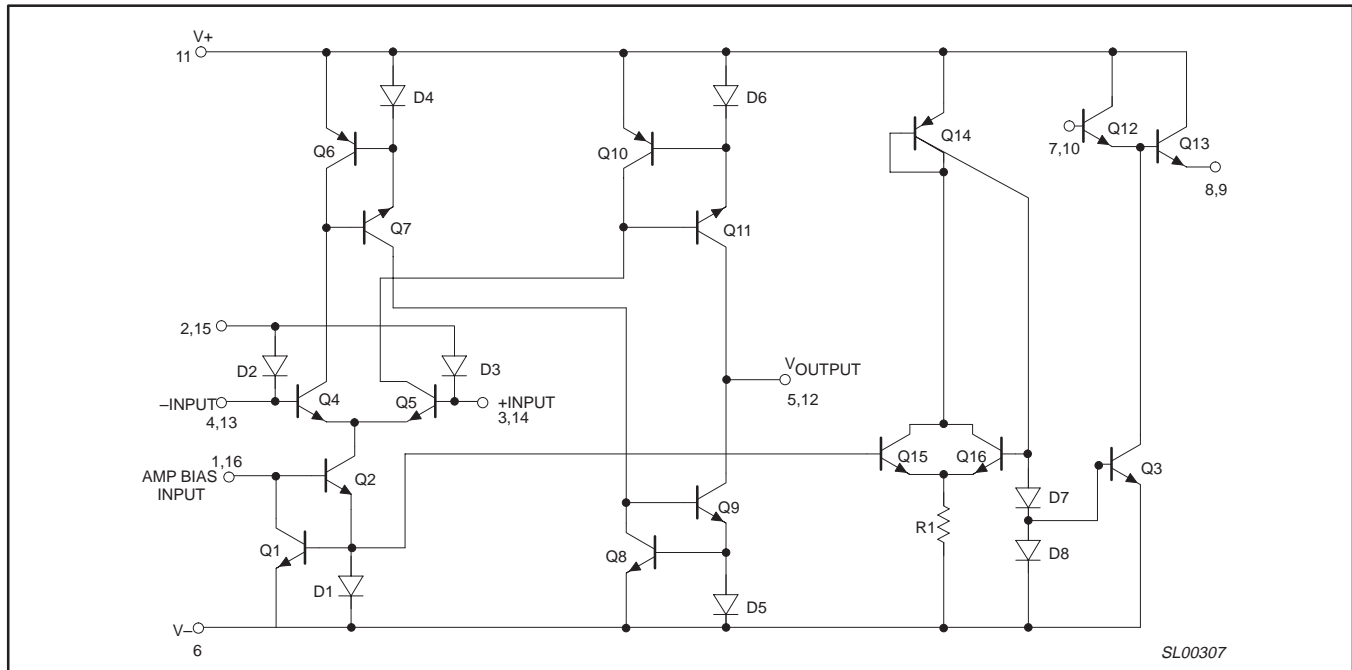


Figure 2. Circuit Schematic

## CONNECTION DIAGRAM

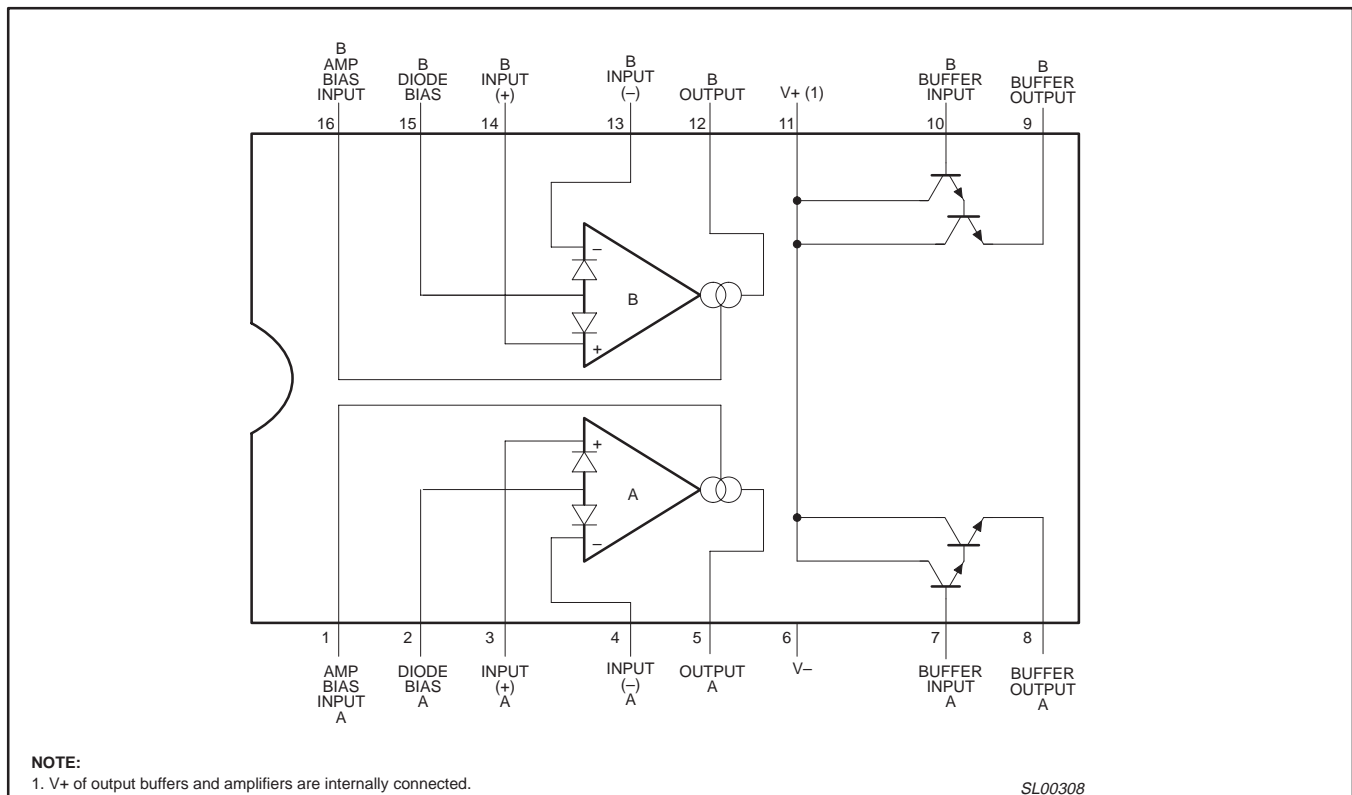


Figure 3. Connection Diagram

## Dual operational transconductance amplifier

NE5517/NE5517A/  
AU5517**ABSOLUTE MAXIMUM RATINGS**

SYMBOL	PARAMETER	RATING	UNIT
$V_S$	Supply voltage <sup>1</sup>	44 $V_{DC}$ or $\pm 22$	V
$P_D$	Power dissipation, $T_{amb} = 25\text{ }^\circ\text{C}$ (still air) <sup>2</sup>		
	NE5517N, NE5517AN	1500	mW
	NE5517D, AU5517D	1125	mW
$V_{IN}$	Differential input voltage	$\pm 5$	V
$I_D$	Diode bias current	2	mA
$I_{ABC}$	Amplifier bias current	2	mA
$I_{SC}$	Output short-circuit duration	Indefinite	
$I_{OUT}$	Buffer output current <sup>3</sup>	20	mA
$T_{amb}$	Operating temperature range		
	NE5517N, NE5517AN	0 $^\circ\text{C}$ to +70 $^\circ\text{C}$	$^\circ\text{C}$
	AU5517D	-40 $^\circ\text{C}$ to +125 $^\circ\text{C}$	$^\circ\text{C}$
$V_{DC}$	DC input voltage	$+V_S$ to $-V_S$	
$T_{stg}$	Storage temperature range	-65 $^\circ\text{C}$ to +150 $^\circ\text{C}$	$^\circ\text{C}$
$T_{sld}$	Lead soldering temperature (10 sec max)	230	$^\circ\text{C}$

**NOTES:**

- For selections to a supply voltage above  $\pm 22$  V, contact factory
- The following derating factors should be applied above 25  $^\circ\text{C}$   
N package at 12.0 mW/ $^\circ\text{C}$   
D package at 9.0 mW/ $^\circ\text{C}$
- Buffer output current should be limited so as to not exceed package dissipation.

## Dual operational transconductance amplifier

NE5517/NE5517A/  
AU5517DC ELECTRICAL CHARACTERISTICS<sup>1</sup>

SYMBOL	PARAMETER	TEST CONDITIONS	AU5517/NE5517			NE5517A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V <sub>OS</sub>	Input offset voltage	Over temperature range I <sub>ABC</sub> 5 μA		0.4	5		0.4	2	mV
				0.3	5		0.3	5	mV
								2	mV
	ΔV <sub>OS</sub> /ΔT	Avg. TC of input offset voltage		7			7		μV/°C
	V <sub>OS</sub> including diodes	Diode bias current (I <sub>D</sub> ) = 500 μA		0.5	5		0.5	2	mV
V <sub>OS</sub>	Input offset change	5 μA ≤ I <sub>ABC</sub> ≤ 500 μA		0.1			0.1	3	mV
I <sub>OS</sub>	Input offset current			0.1	0.6		0.1	0.6	μA
	ΔI <sub>OS</sub> /ΔT	Avg. TC of input offset current		0.001			0.001		μA/°C
I <sub>BIAS</sub>	Input bias current	Over temperature range		0.4	5		0.4	5	μA
				1	8		1	7	μA
	ΔI <sub>B</sub> /ΔT	Avg. TC of input current		0.01			0.01		μA/°C
g <sub>M</sub>	Forward transconductance	Over temperature range	6700	9600	1300	7700	9600	1200	μmho
			5400			4000			
	g <sub>M</sub> tracking			0.3			0.3		dB
I <sub>OUT</sub>	Peak output current	R <sub>L</sub> = 0, I <sub>ABC</sub> = 5 μA		5		3	5	7	μA
		R <sub>L</sub> = 0, I <sub>ABC</sub> = 500 μA	350	500	650	350	500	650	μA
		R <sub>L</sub> = 0	300			300			μA
V <sub>OUT</sub>	Peak output voltage	Positive							V
		Negative							V
		R <sub>L</sub> = ∞, 5 μA ≤ I <sub>ABC</sub> ≤ 500 μA	+12	+14.2		+12	+14.2		V
		R <sub>L</sub> = ∞, 5 μA ≤ I <sub>ABC</sub> ≤ 500 μA	-12	-14.4		-12	-14.4		V
I <sub>CC</sub>	Supply current	I <sub>ABC</sub> = 500 μA, both channels		2.6	4		2.6	4	mA
	V <sub>OS</sub> sensitivity								
			Positive	ΔV <sub>OS</sub> /ΔV+		20	150		20
	Negative	ΔV <sub>OS</sub> /ΔV-		20	150		20	150	μV/V
CMRR	Common-mode rejection ration		80	110		80	110		dB
	Common-mode range		±12	±13.5		±12	±13.5		V
	Crosstalk	Referred to input <sup>2</sup> 20 Hz < f < 20 kHz		100			100		dB
I <sub>IN</sub>	Differential input current	I <sub>ABC</sub> = 0, input = ±4 V		0.02	100		0.02	10	nA
	Leakage current	I <sub>ABC</sub> = 0 (Refer to test circuit)		0.2	100		0.2	5	nA
R <sub>IN</sub>	Input resistance		10	26		10	26		kΩ
B <sub>W</sub>	Open-loop bandwidth			2			2		MHz
SR	Slew rate	Unity gain compensated		50			50		V/μs
I <sub>NBUFFER</sub>	Buffer input current	5		0.4	5		0.4	5	μA
V <sub>OBUFFER</sub>	Peak buffer output voltage	5	10			10			V
	ΔV <sub>BE</sub> of buffer	Refer to Buffer V <sub>BE</sub> test circuit <sup>3</sup>		0.5	5		0.5	5	mV

## NOTES:

- These specifications apply for V<sub>S</sub> = ±15 V, T<sub>amb</sub> = 25 °C, amplifier bias current (I<sub>ABC</sub>) = 500 μA, Pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.
- These specifications apply for V<sub>S</sub> = ±15 V, I<sub>ABC</sub> = 500 μA, R<sub>OUT</sub> = 5 kΩ connected from the buffer output to -V<sub>S</sub> and the input of the buffer is connected to the transconductance amplifier output.
- V<sub>S</sub> = ±15, R<sub>OUT</sub> = 5 kΩ connected from Buffer output to -V<sub>S</sub> and 5 μA ≤ I<sub>ABC</sub> ≤ 500 μA.

# Dual operational transconductance amplifier

NE5517/NE5517A/  
AU5517

## TYPICAL PERFORMANCE CHARACTERISTICS

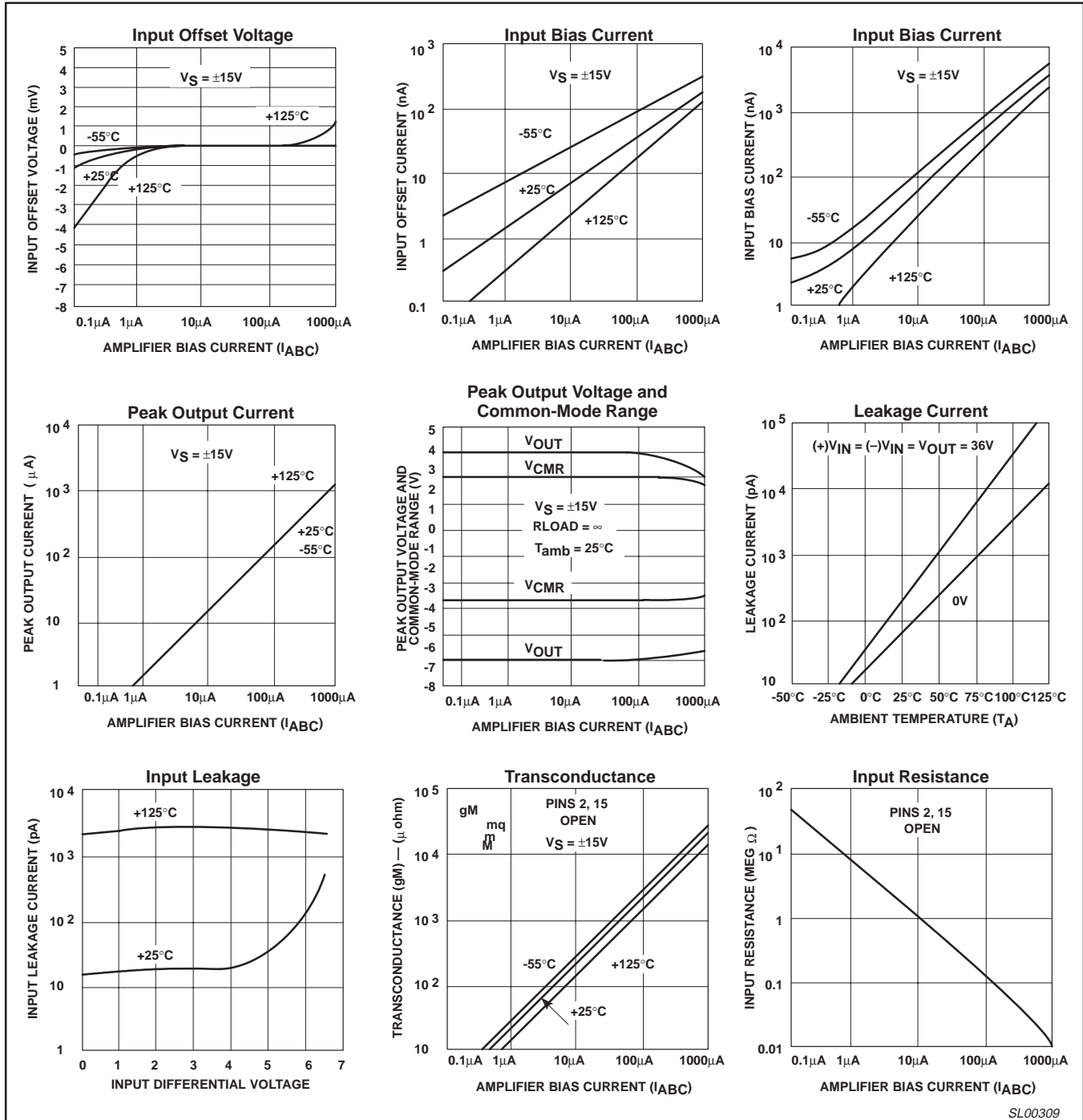
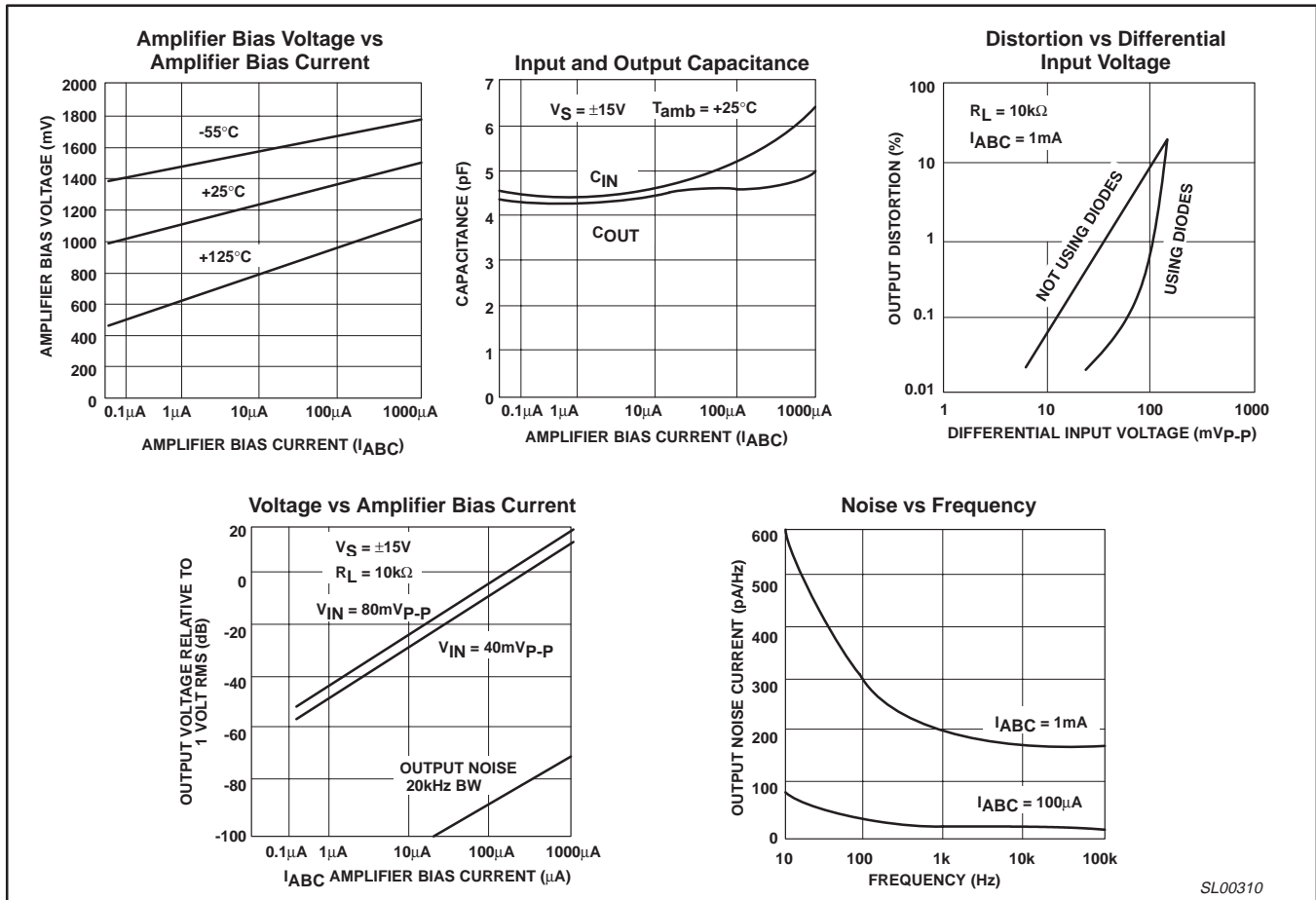


Figure 4. Typical Performance Characteristics

# Dual operational transconductance amplifier

NE5517/NE5517A/  
AU5517

## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



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Figure 5. Typical Performance Characteristics (cont.)

# Dual operational transconductance amplifier

## NE5517/NE5517A/ AU5517

### TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

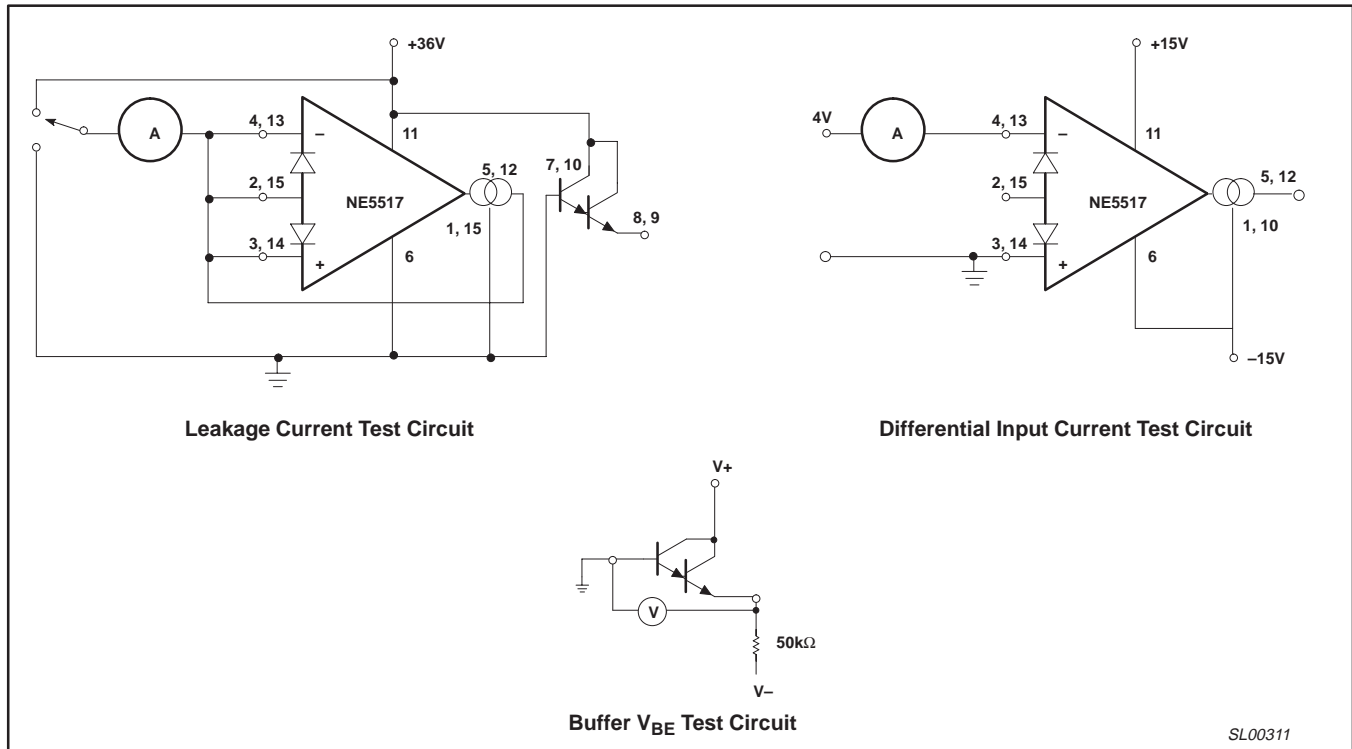


Figure 6. Typical Performance Characteristics (cont.)

### APPLICATIONS

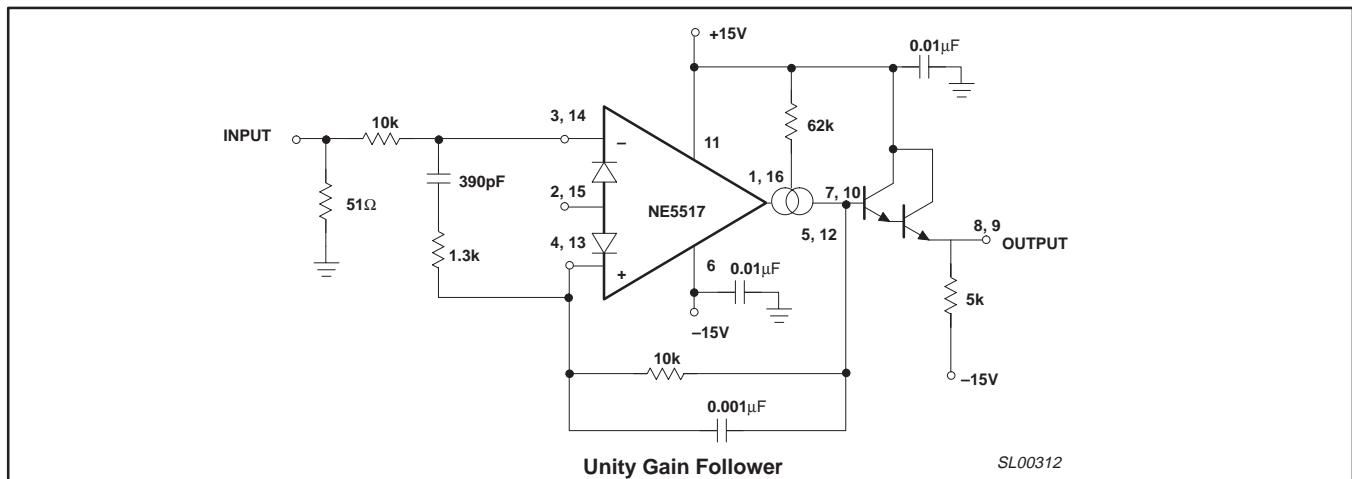


Figure 7. Applications



## Dual operational transconductance amplifier

NE5517/NE5517A/  
AU5517**CIRCUIT DESCRIPTION**

The circuit schematic diagram of one-half of the AU5517/NE5517, a dual operational transconductance amplifier with linearizing diodes and impedance buffers, is shown in Figure 8.

**1. Transconductance Amplifier**

The transistor pair, Q<sub>4</sub> and Q<sub>5</sub>, forms a transconductance stage. The ratio of their collector currents (I<sub>4</sub> and I<sub>5</sub>, respectively) is defined by the differential input voltage, V<sub>IN</sub>, which is shown in equation 1.

$$V_{IN} = \frac{KT}{q} \ln \frac{I_5}{I_4} \quad (1)$$

Where V<sub>IN</sub> is the difference of the two input voltages

$$KT \approx 26 \text{ mV at room temperature (300 °K).}$$

Transistors Q<sub>1</sub>, Q<sub>2</sub> and diode D<sub>1</sub> form a current mirror which focuses the sum of current I<sub>4</sub> and I<sub>5</sub> to be equal to amplifier bias current I<sub>B</sub>:

$$I_4 + I_5 = I_B \quad (2)$$

If V<sub>IN</sub> is small, the ratio of I<sub>5</sub> and I<sub>4</sub> will approach unity and the Taylor series of ln function can be approximated as

$$\frac{KT}{q} \ln \frac{I_5}{I_4} \approx \frac{KT}{q} \frac{I_5 - I_4}{I_4} \quad (3)$$

and I<sub>4</sub> ≈ I<sub>5</sub> ≈ I<sub>B</sub>

$$\frac{KT}{q} \ln \frac{I_5}{I_4} \approx \frac{KT}{q} \frac{I_5 - I_4}{1/2 I_B} = \frac{2KT}{q} \frac{I_5 - I_4}{I_B} = V_{IN} \quad (4)$$

$$I_5 - I_4 = V_{IN} \frac{(I_B)^q}{2KT}$$

The remaining transistors (Q<sub>6</sub> to Q<sub>11</sub>) and diodes (D<sub>4</sub> to D<sub>6</sub>) form three current mirrors that produce an output current equal to I<sub>5</sub> minus I<sub>4</sub>. Thus:

$$V_{IN} \left( I_B \frac{q}{2KT} \right) = I_O \quad (5)$$

The term  $\frac{(I_B)^q}{2KT}$  is then the transconductance of the amplifier and is proportional to I<sub>B</sub>.

**2. Linearizing Diodes**

For V<sub>IN</sub> greater than a few millivolts, equation 3 becomes invalid and the transconductance increases non-linearly. Figure 9 shows how the internal diodes can linearize the transfer function of the operational amplifier. Assume D<sub>2</sub> and D<sub>3</sub> are biased with current sources and the input signal current is I<sub>S</sub>. Since

I<sub>4</sub> + I<sub>5</sub> = I<sub>B</sub> and I<sub>5</sub> - I<sub>4</sub> = I<sub>O</sub>, that is:

$$I_4 = (I_B - I_O), I_5 = (I_B + I_O)$$

For the diodes and the input transistors that have identical geometries and are subject to similar voltages and temperatures, the following equation is true:

$$\frac{I}{q} \ln \frac{I_D + I_S}{I_D - I_S} = \frac{KT}{q} \ln \frac{1/2(I_B + I_O)}{1/2(I_B - I_O)} \quad (6)$$

$$I_O = I_S \frac{2I_B}{I_D} \text{ for } |I_S| < \frac{I_D}{2}$$

The only limitation is that the signal current should not exceed I<sub>D</sub>.

**3. Impedance Buffer**

The upper limit of transconductance is defined by the maximum value of I<sub>B</sub> (2 mA). The lowest value of I<sub>B</sub> for which the amplifier will function therefore determines the overall dynamic range. At low values of I<sub>B</sub>, a buffer with very low input bias current is desired. A Darlington amplifier with constant-current source (Q<sub>14</sub>, Q<sub>15</sub>, Q<sub>16</sub>, D<sub>7</sub>, D<sub>8</sub>, and R<sub>1</sub>) suits the need.

**APPLICATIONS****Voltage-Controlled Amplifier**

In Figure 10, the voltage divider R<sub>2</sub>, R<sub>3</sub> divides the input-voltage into small values (mV range) so the amplifier operates in a linear manner.

It is:

$$I_{OUT} = -V_{IN} \cdot \frac{R_3}{R_2 + R_3} \cdot g_M;$$

$$V_{OUT} = I_{OUT} \cdot R_L;$$

$$A = \frac{V_{OUT}}{V_{IN}} = \frac{R_3}{R_2 + R_3} \cdot g_M \cdot R_L$$

$$(3) g_M = 19.2 I_{ABC}$$

(g<sub>M</sub> in μmhos for I<sub>ABC</sub> in mA)

Since g<sub>M</sub> is directly proportional to I<sub>ABC</sub>, the amplification is controlled by the voltage V<sub>C</sub> in a simple way.

When V<sub>C</sub> is taken relative to -V<sub>CC</sub> the following formula is valid:

$$I_{ABC} = \frac{(V_C - 1.2V)}{R_1}$$

The 1.2 V is the voltage across two base-emitter baths in the current mirrors. This circuit is the base for many applications of the AU5517/NE5517.

# Dual operational transconductance amplifier

# NE5517/NE5517A/ AU5517

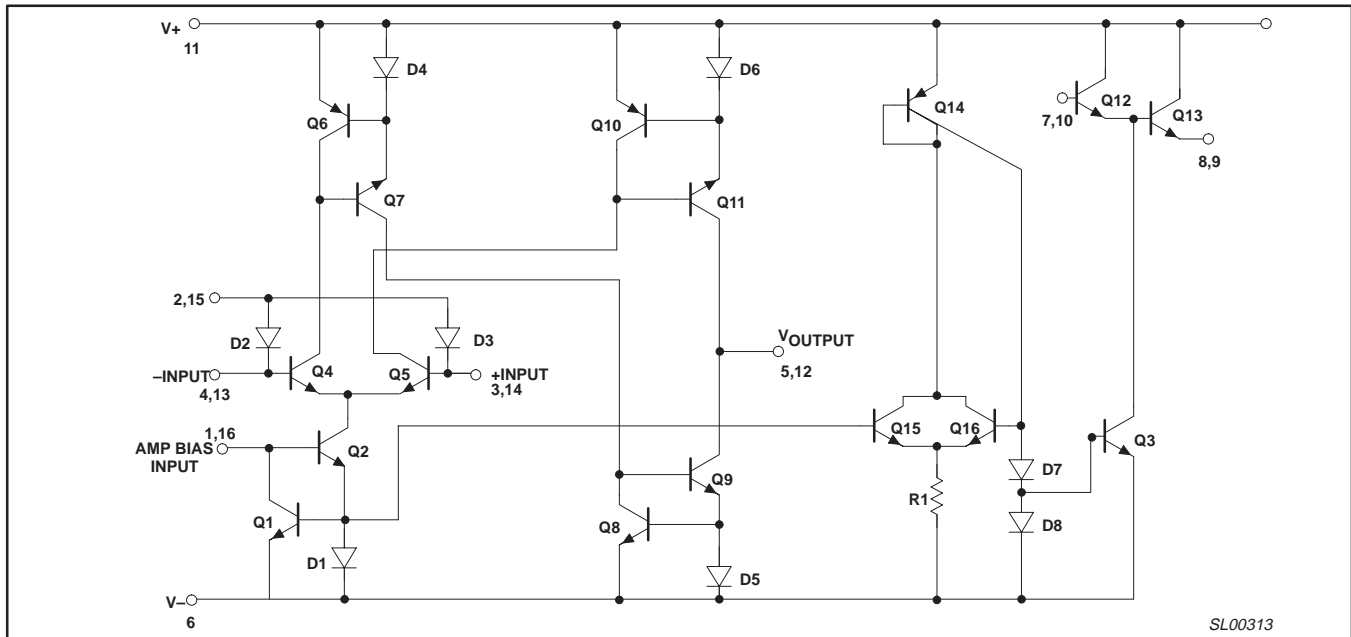


Figure 8. Circuit Diagram of NE5517

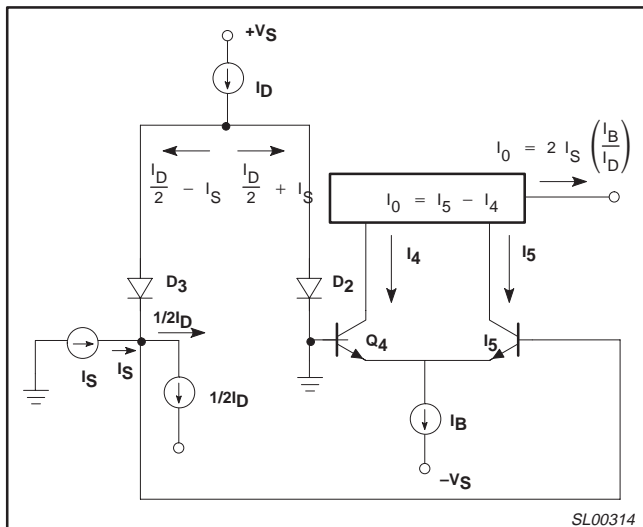


Figure 9. Linearizing Diode

### Stereo Amplifier With Gain Control

Figure 11 shows a stereo amplifier with variable gain via a control input. Excellent tracking of typical 0.3 dB is easy to achieve. With the potentiometer,  $R_P$ , the offset can be adjusted. For AC-coupled amplifiers, the potentiometer may be replaced with two 510  $\Omega$  resistors.

### Modulators

Because the transconductance of an OTA (Operational Transconductance Amplifier) is directly proportional to  $I_{ABC}$ , the amplification of a signal can be controlled easily. The output current is the product from transconductance  $\times$  input voltage. The circuit is effective up to approximately 200 kHz. Modulation of 99% is easy to achieve.

### Voltage-Controlled Resistor (VCR)

Because an OTA is capable of producing an output current proportional to the input voltage, a voltage variable resistor can be made. Figure 13 shows how this is done. A voltage presented at the  $R_X$  terminals forces a voltage at the input. This voltage is multiplied by  $g_M$  and thereby forces a current through the  $R_X$  terminals:

$$R_X = \frac{R + R_A}{g_M + R_A}$$

where  $g_M$  is approximately 19.21  $\mu$ MHOs at room temperature. Figure 14 shows a Voltage Controlled Resistor using linearizing diodes. This improves the noise performance of the resistor.

### Voltage-Controlled Filters

Figure 15 shows a Voltage Controlled Low-Pass Filter. The circuit is a unity gain buffer until  $X_C/g_M$  is equal to  $R/R_A$ . Then, the frequency response rolls off at a 6dB per octave with the -3 dB point being defined by the given equations. Operating in the same manner, a Voltage Controlled High-Pass Filter is shown in Figure 16. Higher order filters can be made using additional amplifiers as shown in Figures 17 and 18.

### Voltage-Controlled Oscillators

Figure 19 shows a voltage-controlled triangle-square wave generator. With the indicated values a range from 2 Hz to 200 kHz is possible by varying  $I_{ABC}$  from 1 mA to 10  $\mu$ A.

The output amplitude is determined by  $I_{OUT} \times R_{OUT}$ .

Please notice the differential input voltage is not allowed to be above 5 V.

With a slight modification of this circuit you can get the sawtooth pulse generator, as shown in Figure 20.

# Dual operational transconductance amplifier

## NE5517/NE5517A/ AU5517

### APPLICATION HINTS

To hold the transconductance  $g_M$  within the linear range,  $I_{ABC}$  should be chosen not greater than 1 mA. The current mirror ratio should be as accurate as possible over the entire current range. A current mirror with only two transistors is not recommended. A suitable current mirror can be built with a PNP transistor array which causes excellent matching and thermal coupling among the

transistors. The output current range of the DAC normally reaches from 0 to -2 mA. In this application, however, the current range is set through  $R_{REF}$  (10 k $\Omega$ ) to 0 to -1 mA.

$$I_{DACMAX} = 2 \cdot \frac{V_{REF}}{R_{REF}} = 2 \cdot \frac{-5V}{10k\Omega} = 1mA$$

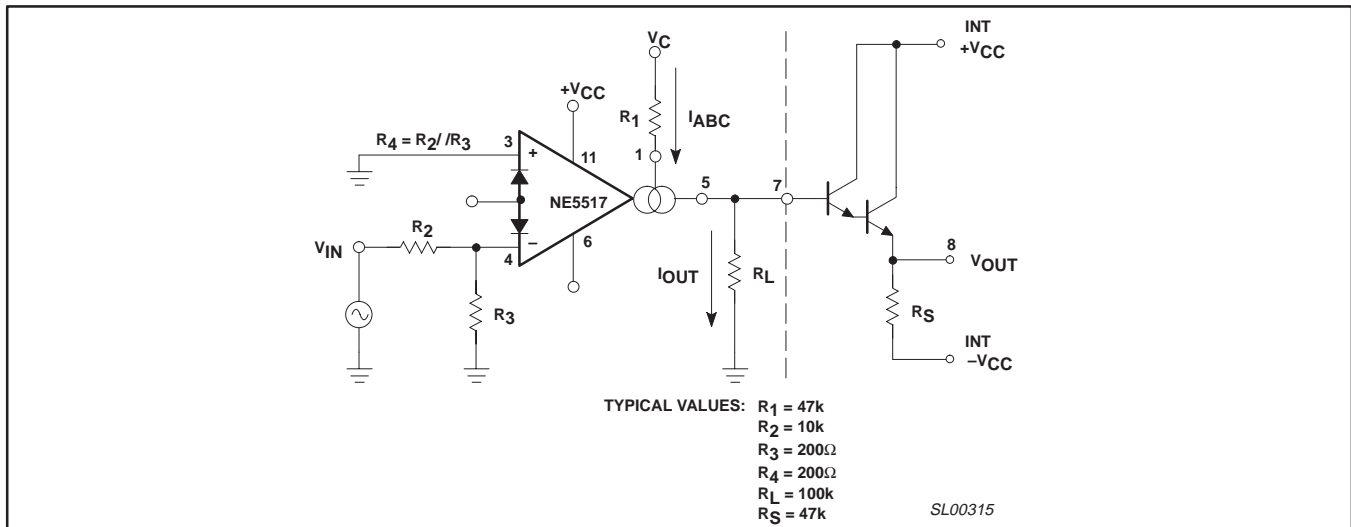


Figure 10.

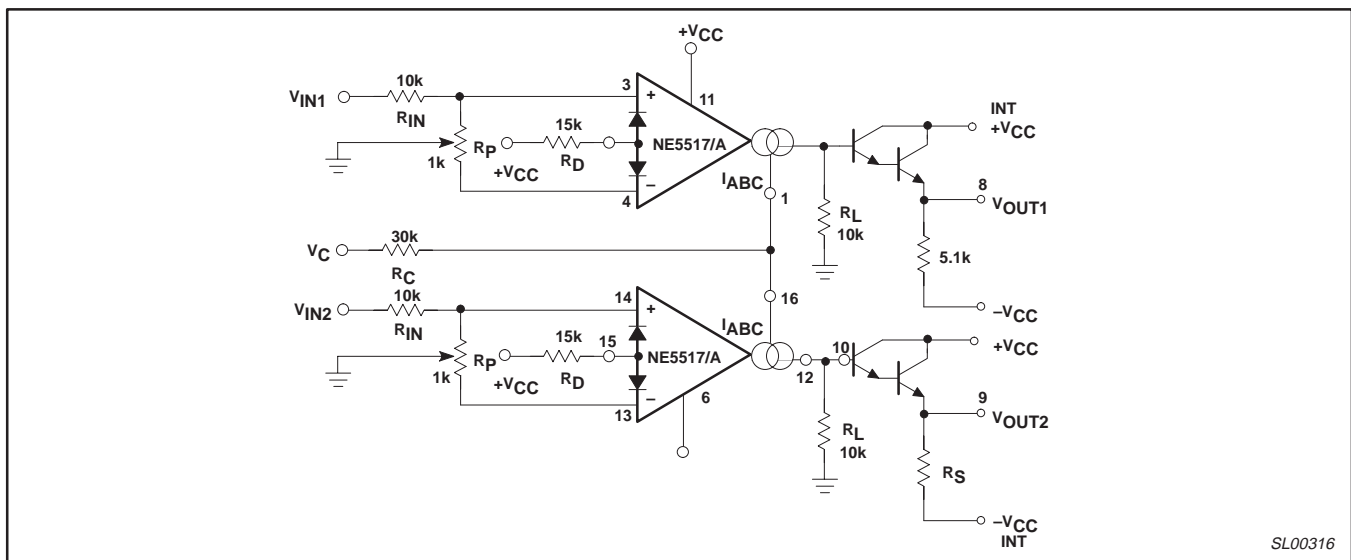


Figure 11. Gain-Controlled Stereo Amplifier

# Dual operational transconductance amplifier

NE5517/NE5517A/  
AU5517

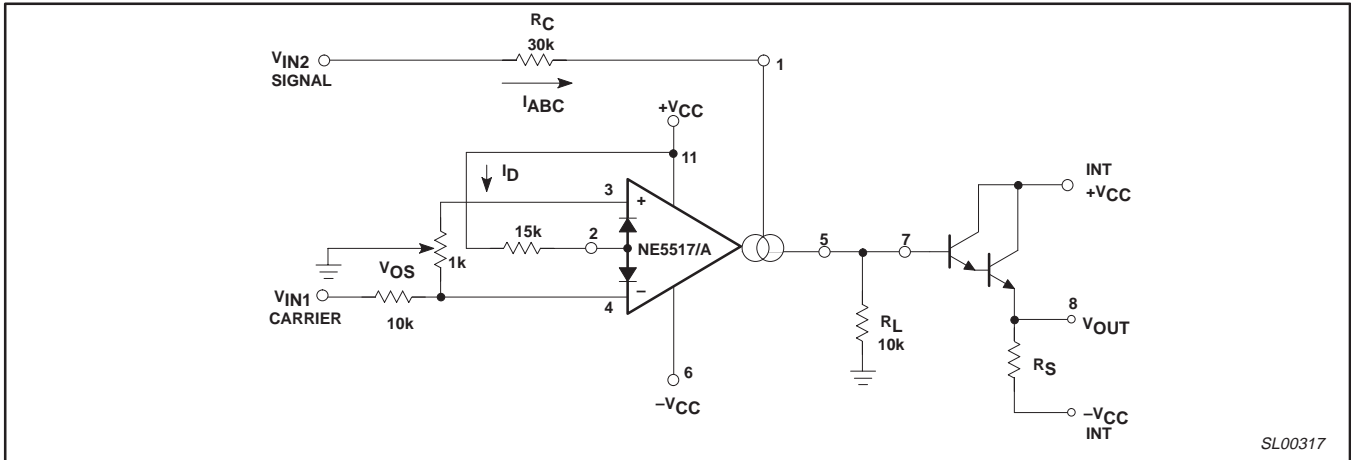
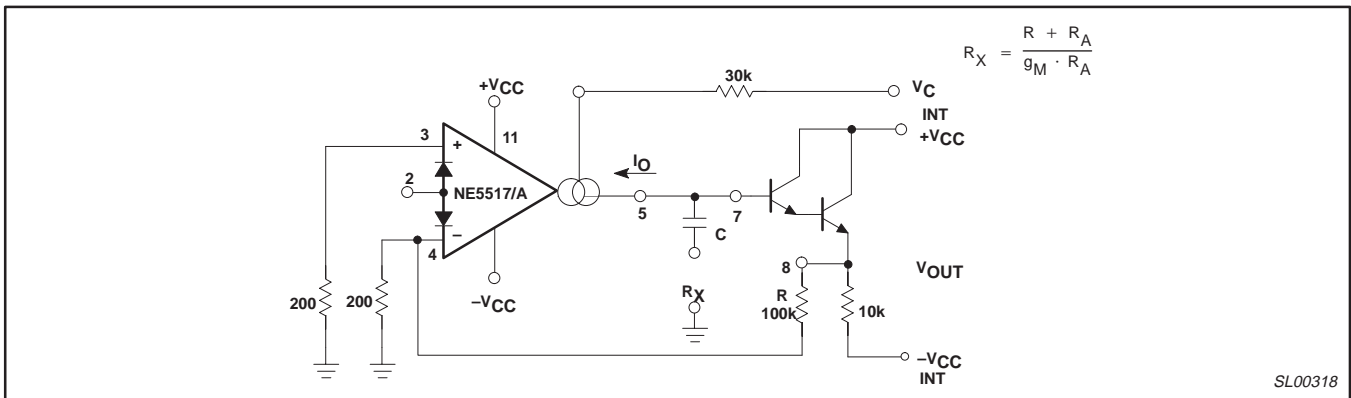


Figure 12. Amplitude Modulator



$$R_X = \frac{R + R_A}{g_M \cdot R_A}$$

Figure 13. VCR

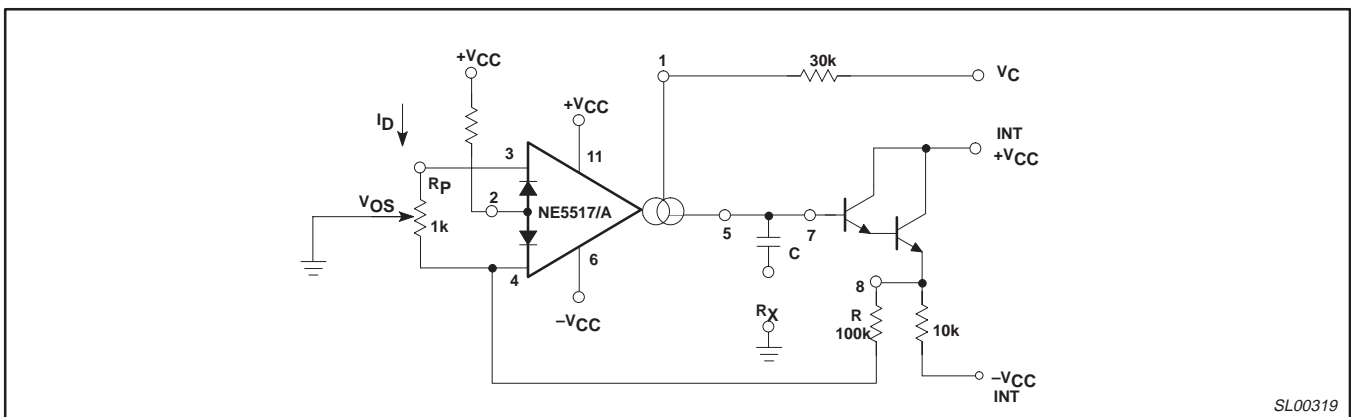


Figure 14. VCR with Linearizing Diodes

# Dual operational transconductance amplifier

## NE5517/NE5517A/ AU5517

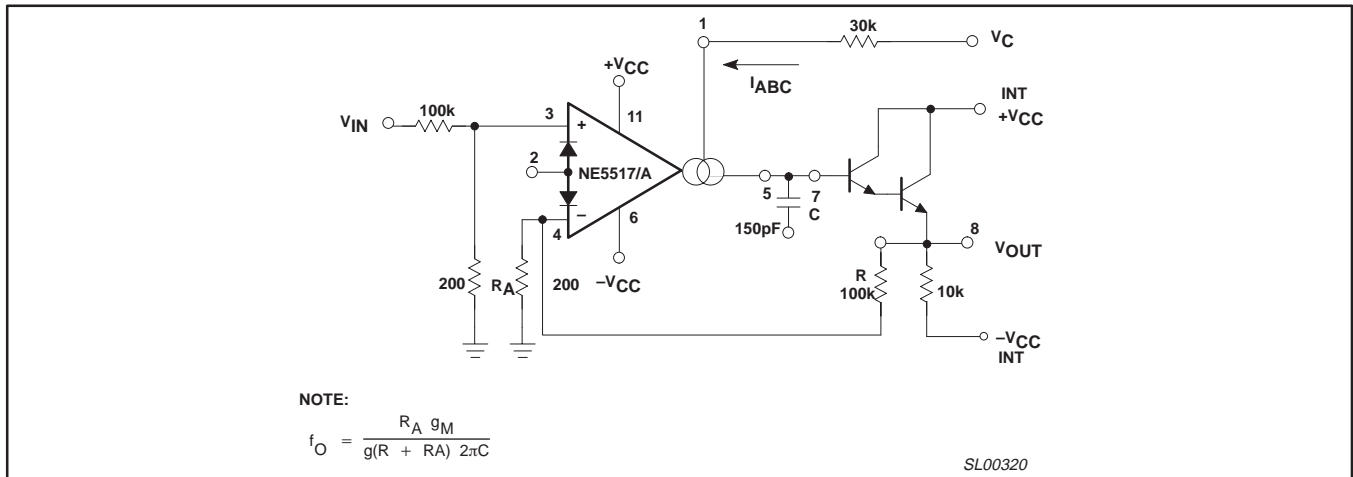


Figure 15. Voltage-Controlled Low-Pass Filter

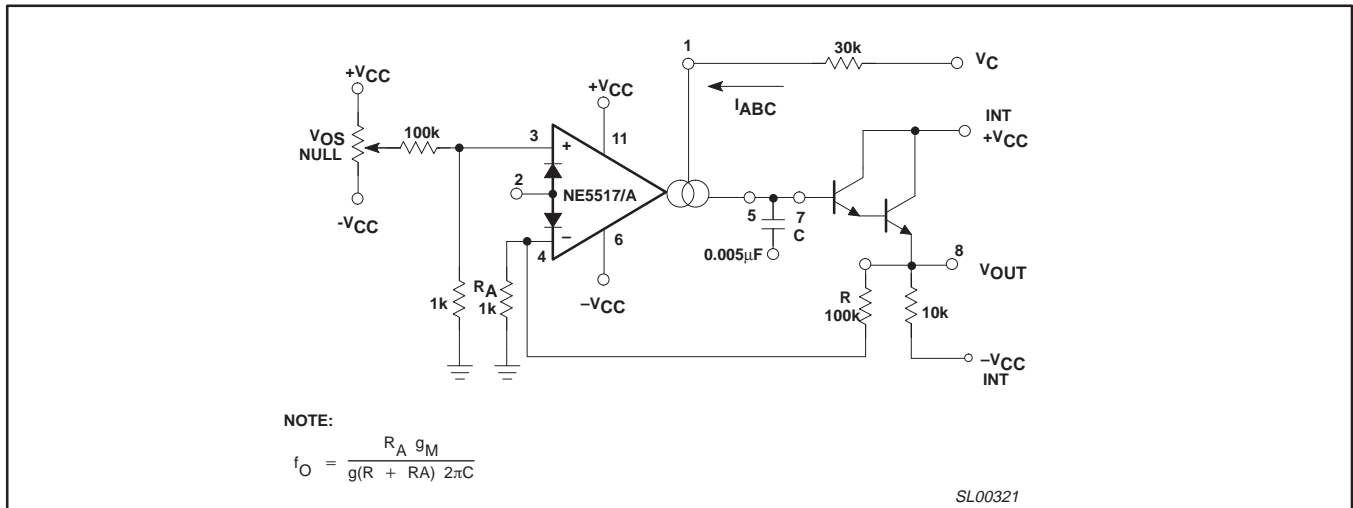


Figure 16. Voltage-Controlled High-Pass Filter

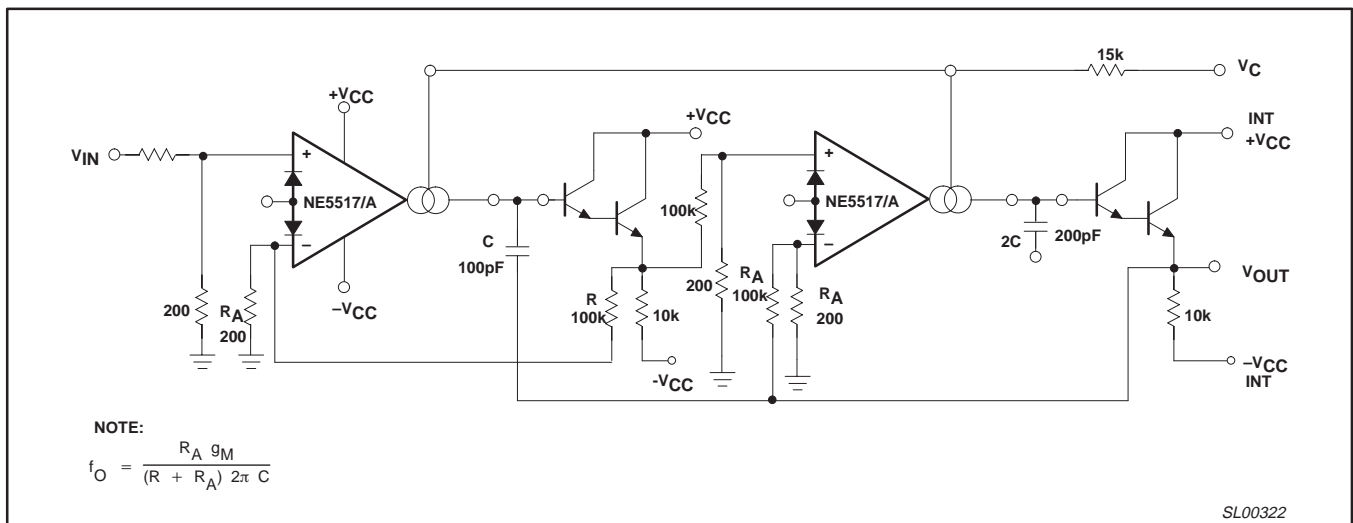


Figure 17. Butterworth Filter - 2nd Order

# Dual operational transconductance amplifier

# NE5517/NE5517A/ AU5517

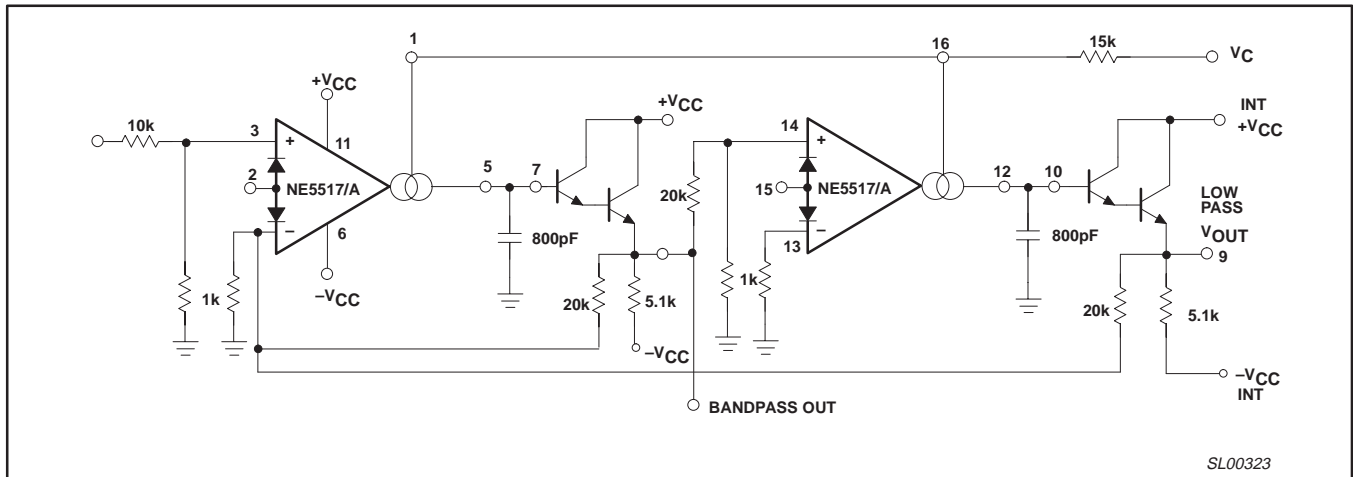


Figure 18. State Variable Filter

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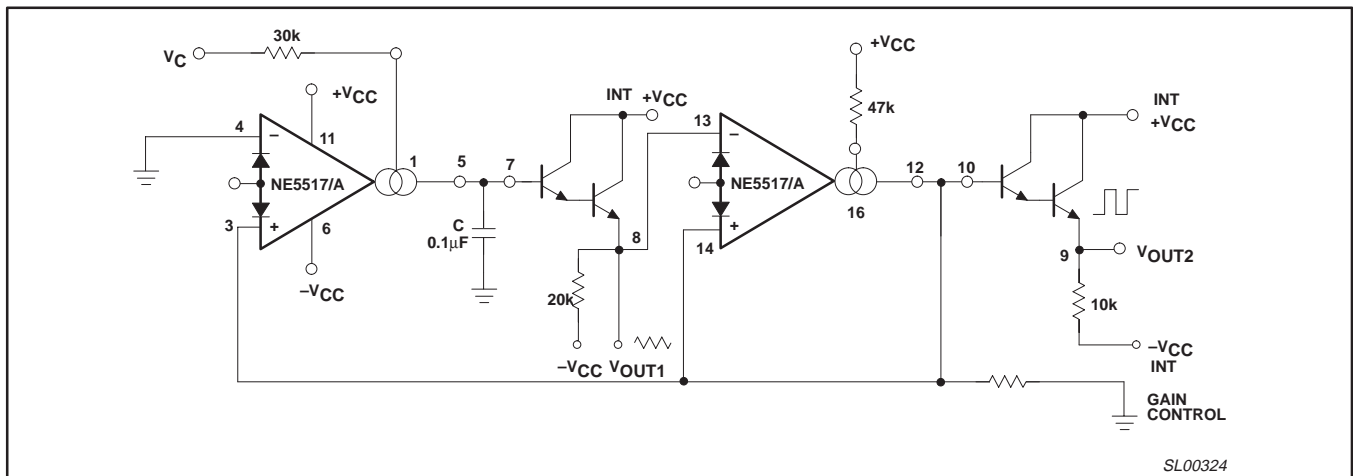


Figure 19. Triangle-Square Wave Generator (VCO)

SL00324

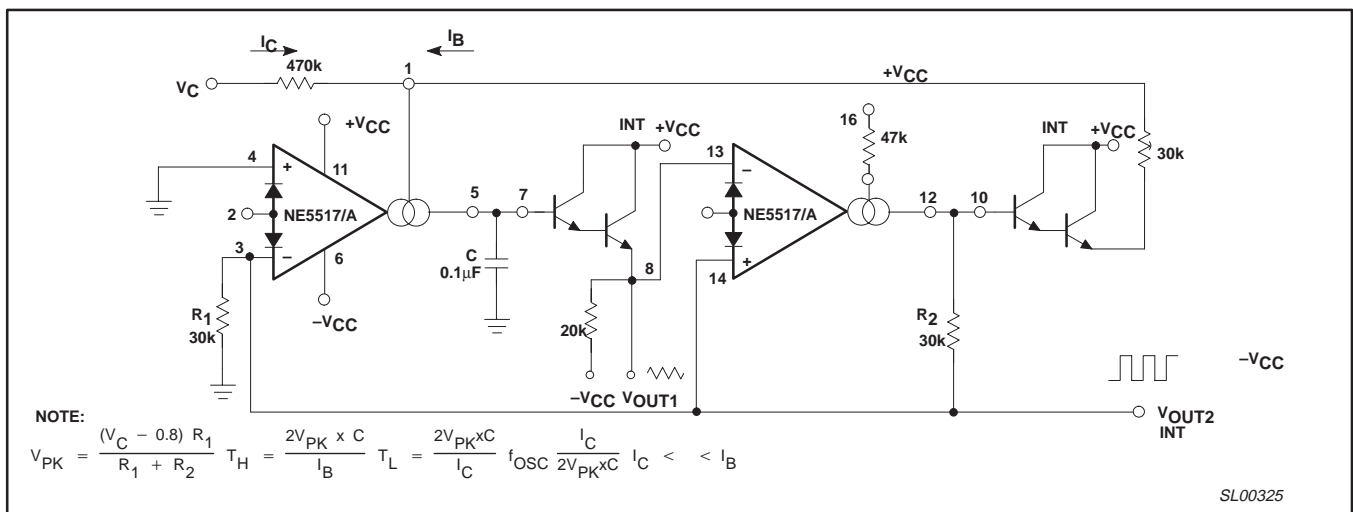


Figure 20. Sawtooth Pulse VCO

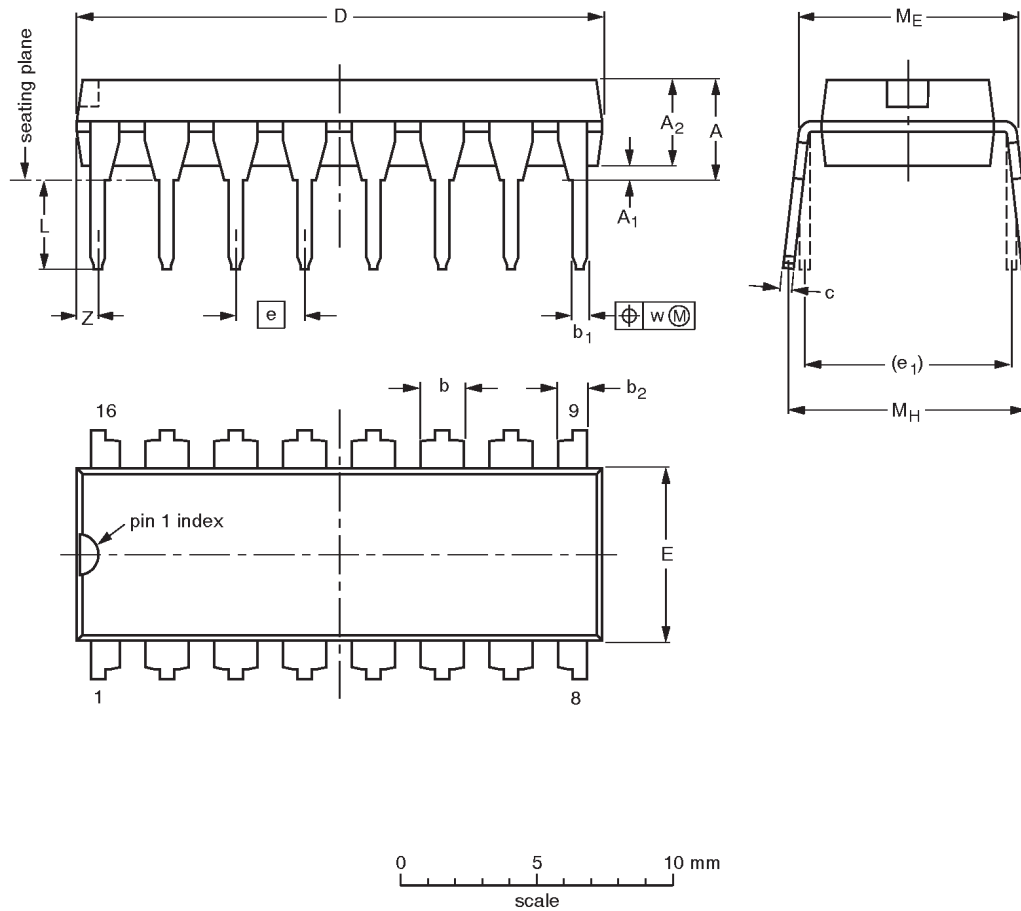
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# Dual operational transconductance amplifier

NE5517/NE5517A/  
AU5517

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

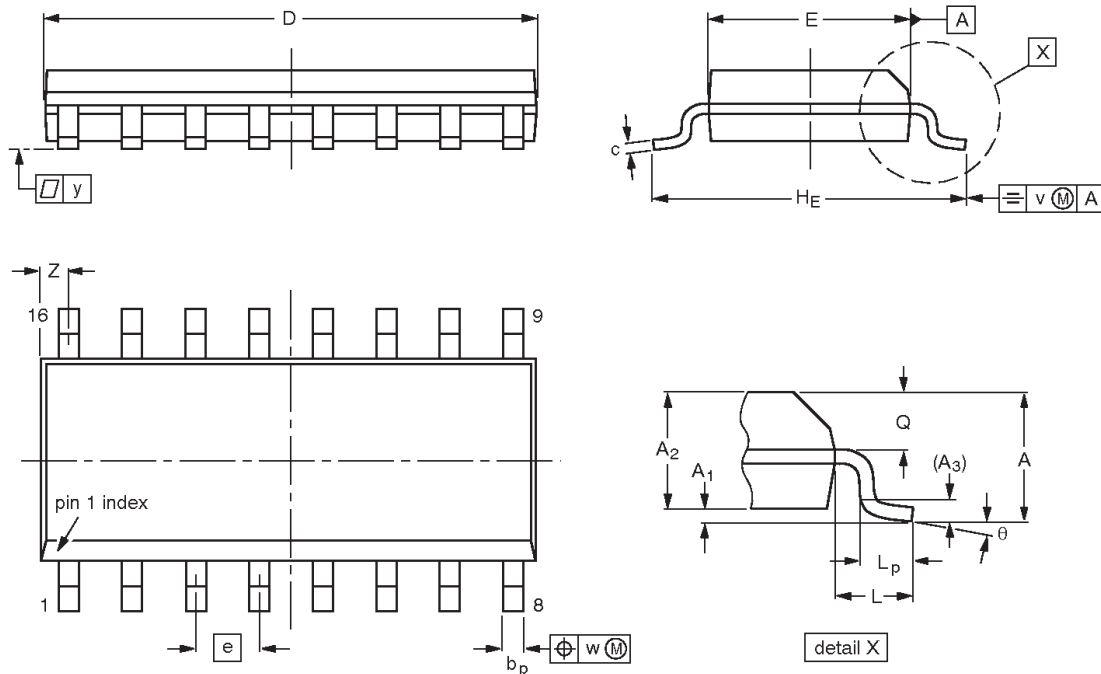
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	IEC	JEDEC	EIAJ			
SOT38-4						92-11-17 95-01-14

# Dual operational transconductance amplifier

NE5517/NE5517A/  
AU5517

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07	MS-012				97-05-22- 99-12-27



## Dual operational transconductance amplifier

NE5517/NE5517A/  
AU5517

## REVISION HISTORY

Rev	Date	Description
_3	20021206	<b>Product data (9397 750 10796); type number AU5517 added. ECN 853-0887 29176 of 08 November 2002; supersedes Product data NE5517_NE5517A version 2 of 03 August 2001.</b> Modifications: <ul style="list-style-type: none"><li>• Type number AU5517 added.</li><li>• "Description" section edited.</li></ul>
_2	20010803	<b>Product data (9397 750 09175); NE5517/NE5517A only; ECN 853-0887 26833 of 2001 Aug 03 .</b>

## Dual operational transconductance amplifier

NE5517/NE5517A/  
AU5517

## Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2] [3]</sup>	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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## Contact information

For additional information please visit  
<http://www.semiconductors.philips.com>. Fax: +31 40 27 24825

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For sales offices addresses send e-mail to:  
[sales.addresses@www.semiconductors.philips.com](mailto:sales.addresses@www.semiconductors.philips.com)

Document order number:

9397 750 10796

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