

# SN54ALS112A, SN74ALS112A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

SDAS199A – APRIL 1982 – REVISED DECEMBER 1994

- Fully Buffered to Offer Maximum Isolation From External Disturbance
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

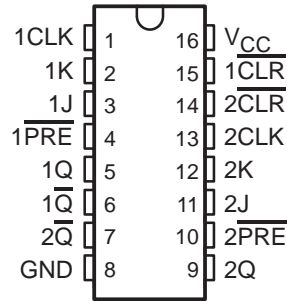
TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY (MHz)	TYPICAL POWER DISSIPATION PER FLIP-FLOP (mW)
'ALS112A	50	6

## description

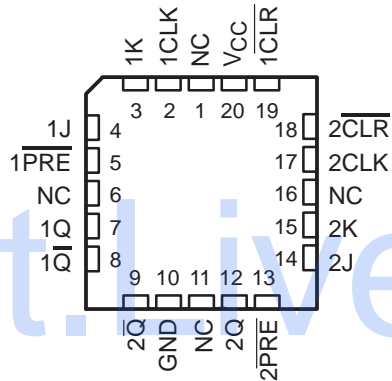
These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset ( $\overline{PRE}$ ) or clear ( $\overline{CLR}$ ) inputs sets or resets the outputs, regardless of the levels of the other inputs. When  $\overline{PRE}$  and  $\overline{CLR}$  are inactive (high), data at the J and K inputs meeting the setup-time requirements is transferred to the outputs on the negative-going edge of the clock pulse (CLK). Clock triggering occurs at a voltage level and is not directly related to the fall time of the clock pulse. Following the hold-time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54ALS112A is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS112A is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54ALS112A . . . J PACKAGE  
SN74ALS112A . . . D OR N PACKAGE  
(TOP VIEW)



SN54ALS112A . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE  
(each flip-flop)

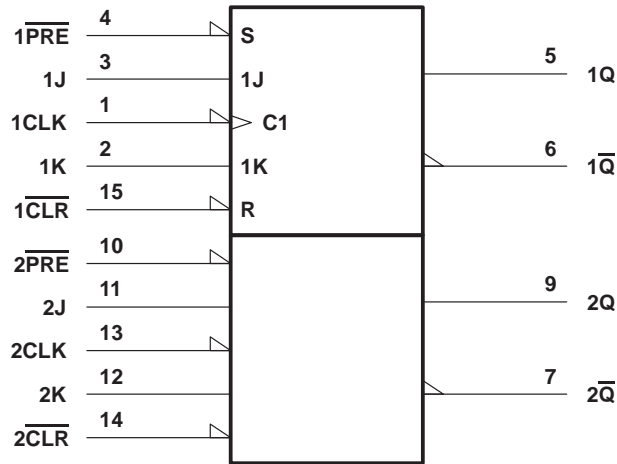
INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H <sup>†</sup>	H <sup>†</sup>
H	H	↓	L	L	Q <sub>0</sub>	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q <sub>0</sub>	$\overline{Q}_0$

<sup>†</sup> The output levels in this configuration may not meet the minimum levels for  $V_{OH}$ . Furthermore, this configuration is nonstable; that is, it does not persist when either  $\overline{PRE}$  or  $\overline{CLR}$  returns to its inactive (high) level.

# SN54ALS112A, SN74ALS112A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

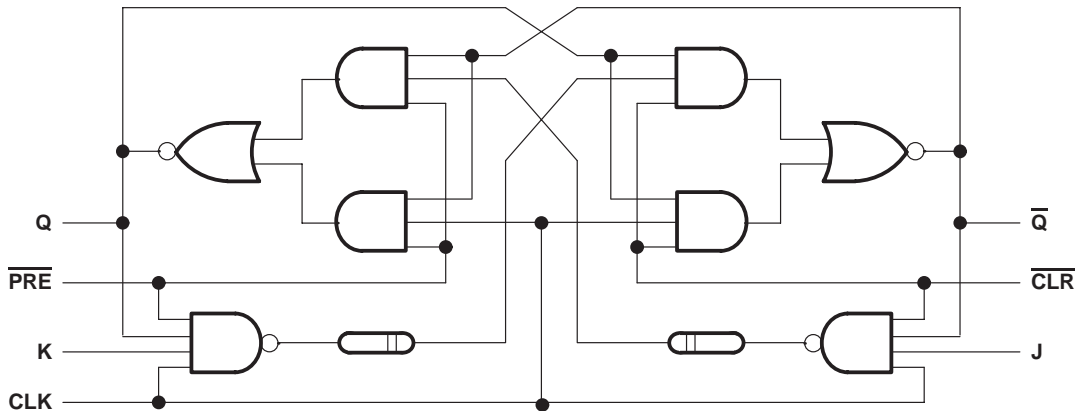
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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, and N packages.

## logic diagram (positive logic)‡



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Operating free-air temperature range, $T_A$ : SN54ALS112A	-55°C to 125°C
SN74ALS112A	0°C to 70°C
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

# SN54ALS112A, SN74ALS112A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

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## recommended operating conditions

		SN54ALS112A			SN74ALS112A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.7			0.8	V
$I_{OH}$	High-level output current			-0.4			-0.4	mA
$I_{OL}$	Low-level output current			4			8	mA
$f_{clock}$	Clock frequency	0		25	0		30	MHz
$t_w$	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low		15	10		ns	
		CLK high		20	16.5			
		CLK low		20	16.5			
$t_{su}$	Setup time before CLK↓	Data		25	22		ns	
		$\overline{PRE}$ or $\overline{CLR}$ inactive		22	20			
$t_h$	Hold time after CLK↓	Data		0	0		ns	
$T_A$	Operating free-air temperature	-55		125	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS112A		SN74ALS112A		UNIT
				MIN	TYP†	MAX	MIN	
$V_{IK}$		$V_{CC} = 4.5\text{ V}$ ,	$I_I = -18\text{ mA}$		-1.5		-1.5	V
$V_{OH}$		$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$ ,	$I_{OH} = -0.4\text{ mA}$	$V_{CC}-2$		$V_{CC}-2$		V
$V_{OL}$		$V_{CC} = 4.5\text{ V}$	$I_{OL} = 4\text{ mA}$	0.25	0.4	0.25	0.4	V
			$I_{OL} = 8\text{ mA}$			0.35	0.5	
$I_I$	J, K, or CLK	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 7\text{ V}$		0.1		0.1	mA
	$\overline{PRE}$ or $\overline{CLR}$				0.2		0.2	
$I_{IH}$	J, K, or CLK	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 2.7\text{ V}$		20		20	$\mu\text{A}$
	$\overline{PRE}$ or $\overline{CLR}$				40		40	
$I_{IL}$	J, K, or CLK	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 0.4\text{ V}$		-0.2		-0.2	mA
	$\overline{PRE}$ or $\overline{CLR}$				-0.4		-0.4	
$I_{O\ddagger}$		$V_{CC} = 5.5\text{ V}$ ,	$V_O = 2.25\text{ V}$	-20	-112	-30	-112	mA
$I_{CC}$		$V_{CC} = 5.5\text{ V}$ ,	See Note 1	2.5	4.5	2.5	4.5	mA

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

NOTE 1:  $I_{CC}$  is measured with J, K, CLK, and  $\overline{PRE}$  grounded, then with J, K, CLK, and  $\overline{CLR}$  grounded.



**SN54ALS112A, SN74ALS112A**  
**DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS**  
**WITH CLEAR AND PRESET**

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**switching characteristics (see Figure 1)**

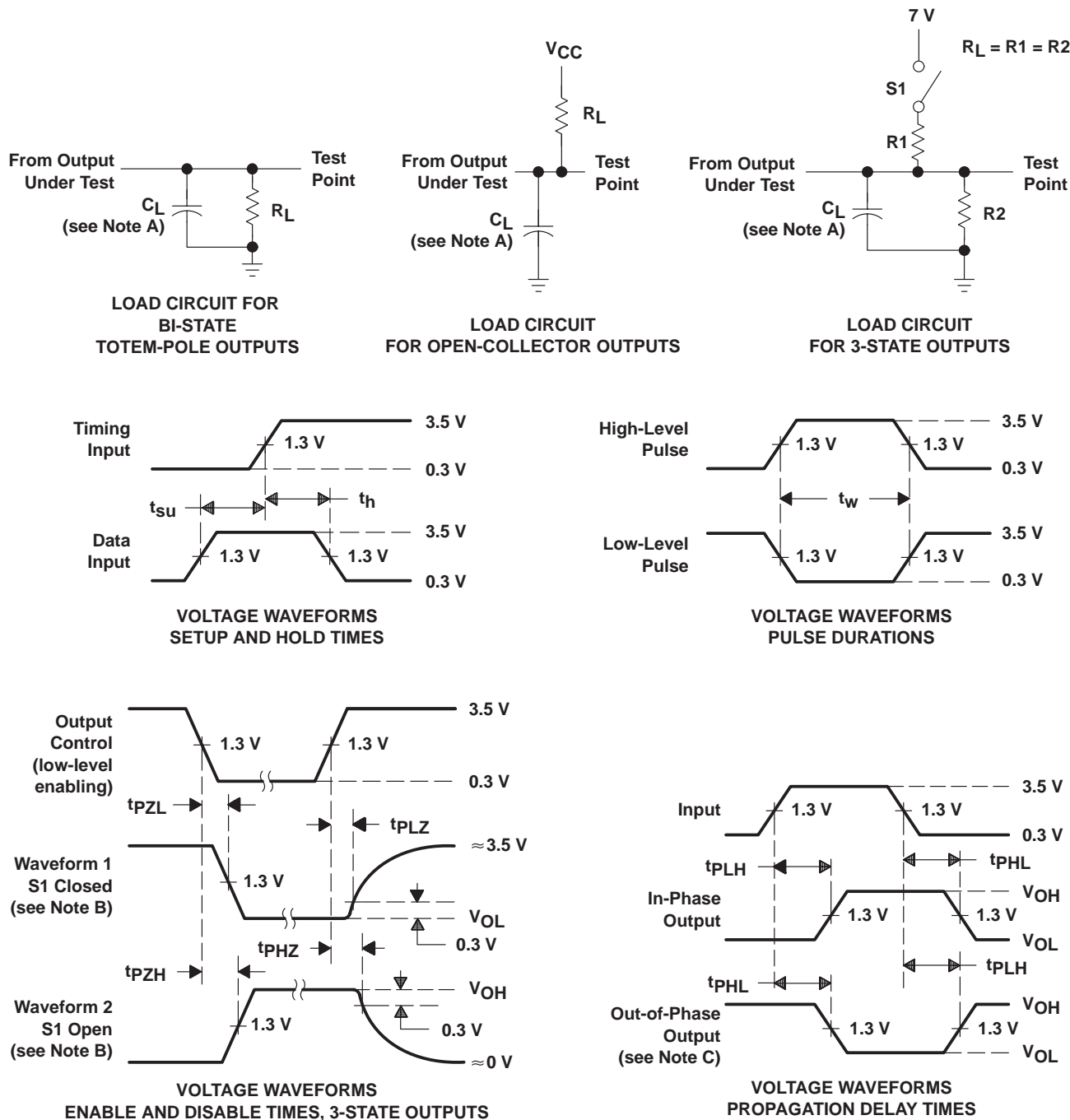
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = \text{MIN to MAX}^\dagger$				UNIT
			SN54ALS112A		SN74ALS112A		
			MIN	MAX	MIN	MAX	
$f_{\max}$			25		30		MHz
$t_{PLH}$	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{Q}$	3	26	3	15	ns
$t_{PHL}$			4	23	4	18	
$t_{PLH}$	CLK	Q or $\overline{Q}$	3	23	3	15	ns
$t_{PHL}$			5	24	5	19	

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

# SN54ALS112A, SN74ALS112A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

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## PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
84000022A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
8400002EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
8400002FA	OBSOLETE	CFP	W	16		TBD	Call TI	Call TI
JM38510/37103B2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
JM38510/37103BEA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SN54ALS112AJ	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SN74ALS112AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS112ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS112ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS112ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS112AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74ALS112AN3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74ALS112ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74ALS112ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS112ANSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54ALS112AFK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54ALS112AJ	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



4040180-3/D 07/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



4040140/D 10/96

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

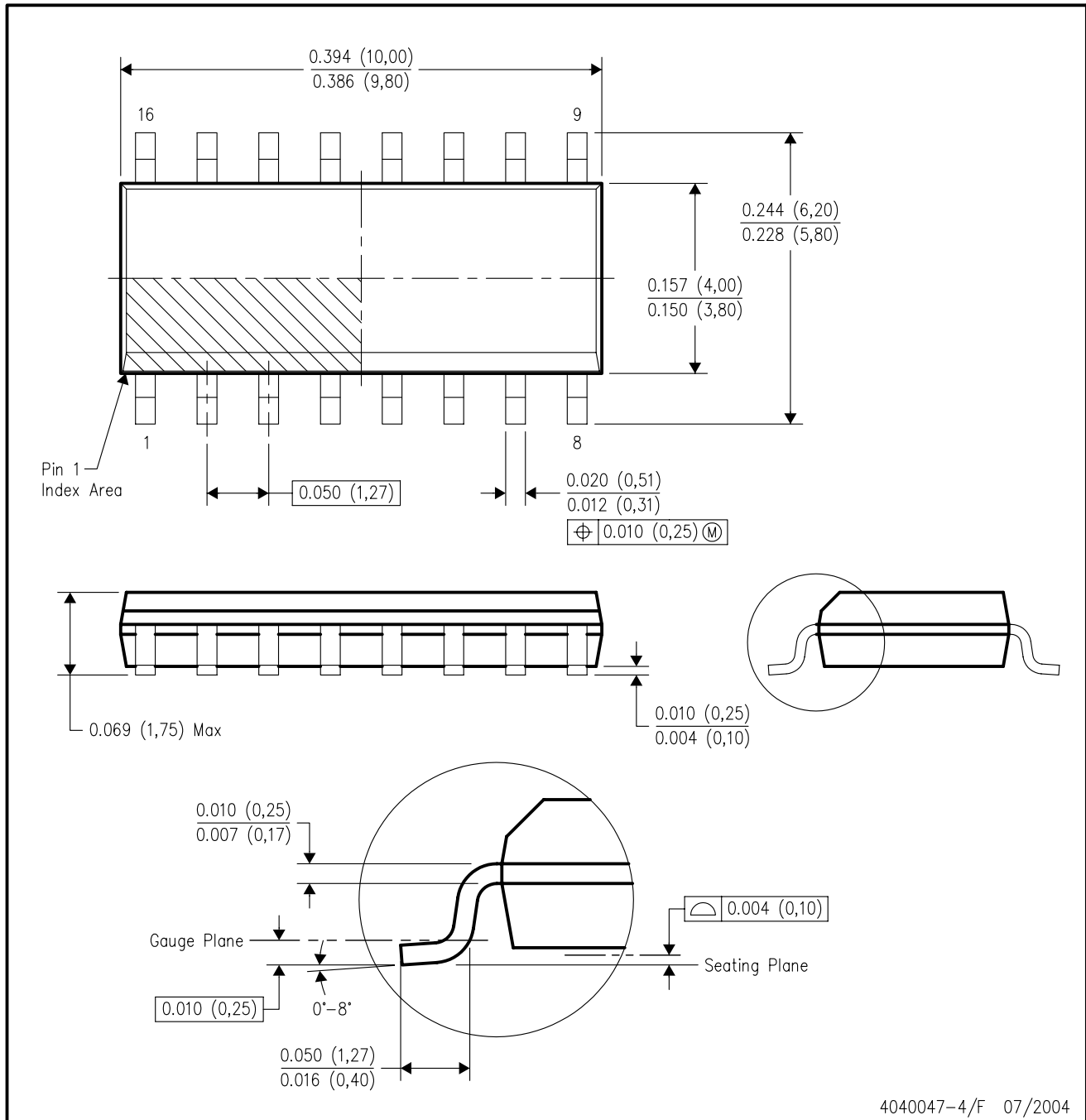


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-012 variation AC.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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clear gif

**SN74ALS112A**, Status: ACTIVE

View RoHS Compliant Devices

Dual J-K Negative-Edge-Triggered Flip-Flops With Clear and Preset



clear gif

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<input type="checkbox"/> Quality & Pb-Free Data	<input type="checkbox"/> Pricing/Packaging	<input type="checkbox"/> Applications Notes
<input type="checkbox"/> Related Products	<input type="checkbox"/> Inventory	<input type="checkbox"/> Simulation Models
<input type="checkbox"/> Tools & Software	<input type="checkbox"/> Symbols/Footprints	<input type="checkbox"/> Reference Designs



**Refine Your Selection**

- Logic: J-K Flip-Flops

**Support**

- KnowledgeBase
- Contact Technical Support
- TI Cross Reference
- Training
- Part Marking Lookup
- Part Number Nomenclature

**Datasheet**



**Dual J-K Negative-Edge-Triggered Flip-Flops With Clear And Preset (Rev. A)** (sn74als112a.pdf, 498 KB)  
01 Dec 1994 [Download](#)

Download Datasheet



	SN54ALS112A	SN74ALS112A
Voltage Nodes(V)	5	5
Vcc range(V)	4.5 to 5.5	4.5 to 5.5
Input Level	TTL	TTL
Output Level	TTL	TTL
Output Drive(mA)		-0.4/8
Output	2S	2S
No. of Bits	2	2
th(ns)		0
tpd max(ns)		19
tsu(ns)		22
	<a href="#">Samples</a>	<a href="#">Samples</a>
	<a href="#">Inventory</a>	<a href="#">Inventory</a>

**Product Information**

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Fully Buffered to Offer Maximum Isolation From External Disturbance  
Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

**Description**

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset ( $\overline{PRE}$ ) or clear ( $\overline{CLR}$ ) inputs sets or resets the outputs, regardless of the levels of the other inputs.

When  $\overline{PRE}$  and  $\overline{CLR}$  are inactive (high), data at the J and K inputs meeting the setup-time requirements is transferred to the outputs on the negative-going edge of the clock pulse (CLK). Clock triggering occurs at a voltage level and is not directly related to the fall time of the clock pulse. Following the hold-time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54ALS112A is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS112A is characterized for operation from 0°C to 70°C.

**Pricing/Packaging/CAD Design Tools/Samples**

			Price	Packaging			CAD Design Tools	Samples
Device	Status	Temp (°C)	Budget Price (\$US)   QTY	Industry Standard (TI Pkg)   Pins	Top Side Marking	Standard Pack Quantity	Footprints	Samples
SN74ALS112AD	ACTIVE	0 to 70	0.51   1KU	SOIC (D)   16	View	40	<input type="checkbox"/>	Purchase Samples
SN74ALS112ADE4	ACTIVE	0 to 70	0.51   1KU	SOIC (D)   16	View	40	<input type="checkbox"/>	Purchase Samples
SN74ALS112ADR	ACTIVE	0 to 70	0.51   1KU	SOIC (D)   16	View	2500	<input type="checkbox"/>	Purchase Samples
SN74ALS112ADRE4	ACTIVE	0 to 70	0.51   1KU	SOIC (D)   16	View	2500	<input type="checkbox"/>	Purchase Samples
SN74ALS112AN	ACTIVE	0 to 70	0.51   1KU	PDIP (N)   16	View	25	<input type="checkbox"/>	Purchase Samples
SN74ALS112AN3	OBSOLETE	0 to 70		PDIP (N)   16	View		<input type="checkbox"/>	Not Available
SN74ALS112ANE4	ACTIVE	0 to 70	0.51   1KU	PDIP (N)   16	View	25	<input type="checkbox"/>	Request Free Samples
SN74ALS112ANSR	ACTIVE	0 to 70	0.51   1KU	SO (NS)   16	View	2000	<input type="checkbox"/>	Purchase Samples
SN74ALS112ANSRE4	ACTIVE	0 to 70	0.51   1KU	SO (NS)   16	View	2000	<input type="checkbox"/>	Purchase Samples

**Inventory**

		TI Inventory Status			Reported Distributor Inventory			
SN74ALS112AD		As of 9:19 AM GMT, 29 Nov 2005			As of 9:19 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY   Date	Lead Time	Region	Company	In Stock	Purchase	
	4662*	3065   13 Dec	10 Weeks	Americas	Avnet	>1k	<input type="text"/>	
		3266   21 Dec		Europe	EBV Elektronik	120	<input type="text"/>	
		>10k   31 Jan			Spoerle	692	<input type="text"/>	
SN74ALS112ADE4		As of 9:19 AM GMT, 29 Nov 2005			As of 9:19 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY   Date	Lead Time	Region	Company	In Stock	Purchase	
	4662*	3065   13 Dec	10 Weeks	None Reported <a href="#">View Distributors</a>				
		3266   21 Dec						
		>10k   31 Jan						
SN74ALS112ADR		As of 9:19 AM GMT, 29 Nov 2005			As of 9:19 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY   Date	Lead Time	Region	Company	In Stock	Purchase	
	0*	4528   30 Nov	10 Weeks	None Reported <a href="#">View Distributors</a>				
		1652   14 Dec						
		3304   22 Dec						
		>10k   1 Feb						
SN74ALS112ADRE4		As of 9:19 AM GMT, 29 Nov 2005			As of 9:19 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY   Date	Lead Time	Region	Company	In Stock	Purchase	
	0*	4528   30 Nov	10 Weeks	None Reported <a href="#">View Distributors</a>				
		1652   14 Dec						
		3304   22 Dec						
		>10k   1 Feb						
SN74ALS112AN		As of 9:19 AM GMT, 29 Nov 2005			As of 9:19 AM GMT, 29 Nov 2005			

View all Distributors

Choose a Region





	In Stock	In Progress QTY   Date	Lead Time	Region	Company	In Stock	Purchase
	3631*	>10k   16 Jan	10 Weeks	Americas	Arrow	150	<input type="text"/>
					Avnet	>1k	<input type="text"/>
					DigiKey	894	<input type="text"/>
					Newark InOne	182	<input type="text"/>
<b>SN74ALS112ANE4</b>	As of 9:19 AM GMT, 29 Nov 2005			As of 9:19 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY   Date	Lead Time	Region	Company	In Stock	Purchase
	3631*	>10k   16 Jan	10 Weeks	None Reported	<a href="#">View Distributors</a>		
<b>SN74ALS112ANSR</b>	As of 9:19 AM GMT, 29 Nov 2005			As of 9:19 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY   Date	Lead Time	Region	Company	In Stock	Purchase
	2000*	>10k   16 Dec	10 Weeks	None Reported	<a href="#">View Distributors</a>		
<b>SN74ALS112ANSRE4</b>	As of 9:19 AM GMT, 29 Nov 2005			As of 9:19 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY   Date	Lead Time	Region	Company	In Stock	Purchase
	2000*	>10k   16 Dec	10 Weeks	None Reported	<a href="#">View Distributors</a>		

\* Our information is updated daily, so please check back with us soon if this does not meet your needs. You may also contact your [TI Authorized Distributor](#), including those [listed above](#), for real time stock information.

\*\* Lead time information is not available at this time. However, our information is updated daily so please check back with us soon. Please contact your preferred [TI Authorized Distributor](#) for additional information.

### Quality & Lead (Pb)-Free Data

<input type="checkbox"/>	Product Content				MTBF/FIT Rate	
Device	Eco Plan*	Lead/Ball Finish	MSL Rating/Peak Reflow	Details	Details	
SN74ALS112AD <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">View</a>	<a href="#">View</a>	
SN74ALS112ADE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">View</a>	<a href="#">View</a>	
SN74ALS112ADR <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">View</a>	<a href="#">View</a>	
SN74ALS112ADRE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">View</a>	<a href="#">View</a>	
SN74ALS112AN <input type="checkbox"/>	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC	<a href="#">View</a>	<a href="#">View</a>	
SN74ALS112ANE4 <input type="checkbox"/>	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC	<a href="#">View</a>	<a href="#">View</a>	
SN74ALS112ANSR <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">View</a>	<a href="#">View</a>	
SN74ALS112ANSRE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">View</a>	<a href="#">View</a>	

\* The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please click on the Product Content Details "View" link in the table above for the latest availability information and additional product content details.

If the information you are requesting is not available online at this time, contact one of our [Product Information Centers](#) regarding the availability of this information.

### Technical Documents

<input type="checkbox"/> <b>Datasheets</b>	<b>Keep track of what's new</b>
<b>Dual J-K Negative-Edge-Triggered Flip-Flops With Clear And Preset (Rev. A)</b> (sn74als112a.pdf, 498 KB)	
01 Dec 1994 <a href="#">Download</a>	
<input type="checkbox"/> <b>Application Notes</b>	

**Semiconductor Packing Material Electrostatic Discharge (ESD) Protection** (szza047.htm, 9 KB)

08 Jul 2004 [Abstract](#)

**Shelf-Life Evaluation of Lead-Free Component Finishes** (szza046.htm, 9 KB)

24 May 2004 [Abstract](#)

**Understanding and Interpreting Standard-Logic Data Sheets (Rev. B)** (szza036b.htm, 8 KB)

28 May 2003 [Abstract](#)

**TI IBIS File Creation, Validation, and Distribution Processes** (szza034.htm, 9 KB)

29 Aug 2002 [Abstract](#)

**Bus-Interface Devices With Output-Damping Resistors Or Reduced-Drive Outputs (Rev. A)** (scba012a.htm, 9 KB)

01 Aug 1997 [Abstract](#)

**Designing With Logic (Rev. C)** (sdya009c.htm, 9 KB)

01 Jun 1997 [Abstract](#)

**Live Insertion** (sdya012.htm, 9 KB)

01 Oct 1996 [Abstract](#)

**Input and Output Characteristics of Digital Integrated Circuits** (sdya010.htm, 9 KB)

01 Oct 1996 [Abstract](#)

**Advanced Schottky (ALS and AS) Logic Families** (sdaa010.htm, 9 KB)

01 Aug 1995 [Abstract](#)

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#### **User Guides**

**LOGIC Pocket Data Book** (scyd013.pdf, 4835 KB)

05 Dec 2002 [Download](#)

#### **More Literature**

**Logic Selection Guide 2005 (Rev. X)** (sdyu001x.pdf, 6909 KB)

15 Mar 2005 [Download](#)

**Military Semiconductors Selection Guide 2004-2005 (Rev. D)** (sgyc003d.pdf, 964 KB)

10 Aug 2004 [Download](#)

**Logic Cross-Reference (Rev. A)** (scyb017a.pdf, 2938 KB)

07 Oct 2003 [Download](#)

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