

QT6 BLOCK DIAGRAM

LAYER 1 : TOP
 LAYER 2 : SGND
 LAYER 3 : IN2
 LAYER 4 : SGND1
 LAYER 5 : SVCC
 LAYER 6 : IN2
 LAYER 7 : SGND2
 LAYER 8 : BOT

Cable Docking
 VGA
 RJ-45
 CIR/Pwr btn
 SPDIF Out
 Stereo MIC
 Headphone Jack
 USB Port
 VOL Cntr
 PAGE 40

SYSTEM CHARGER(ISL6251AHAZ-T)
 PAGE 41

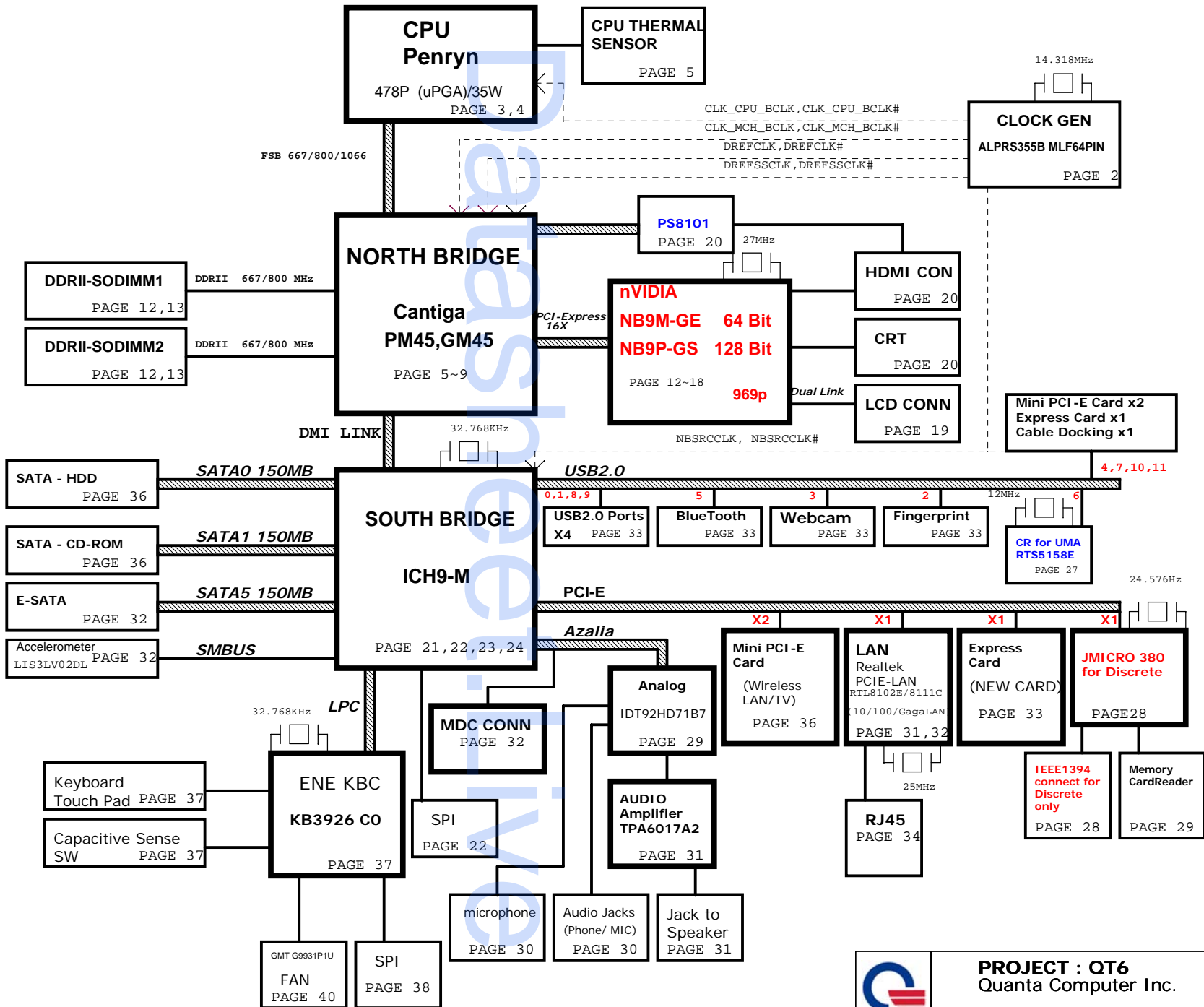
SYSTEM POWER ISL6237IRZ-T
 PAGE 42

DDR II SMDR_VTERM
 1.8V/1.8VSUS(TPSS51116REGR)
 PAGE 46

VCCP +1.5V AND GMCH
 1.05V(RT8204)
 PAGE 43

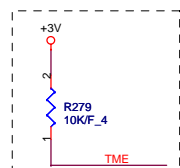
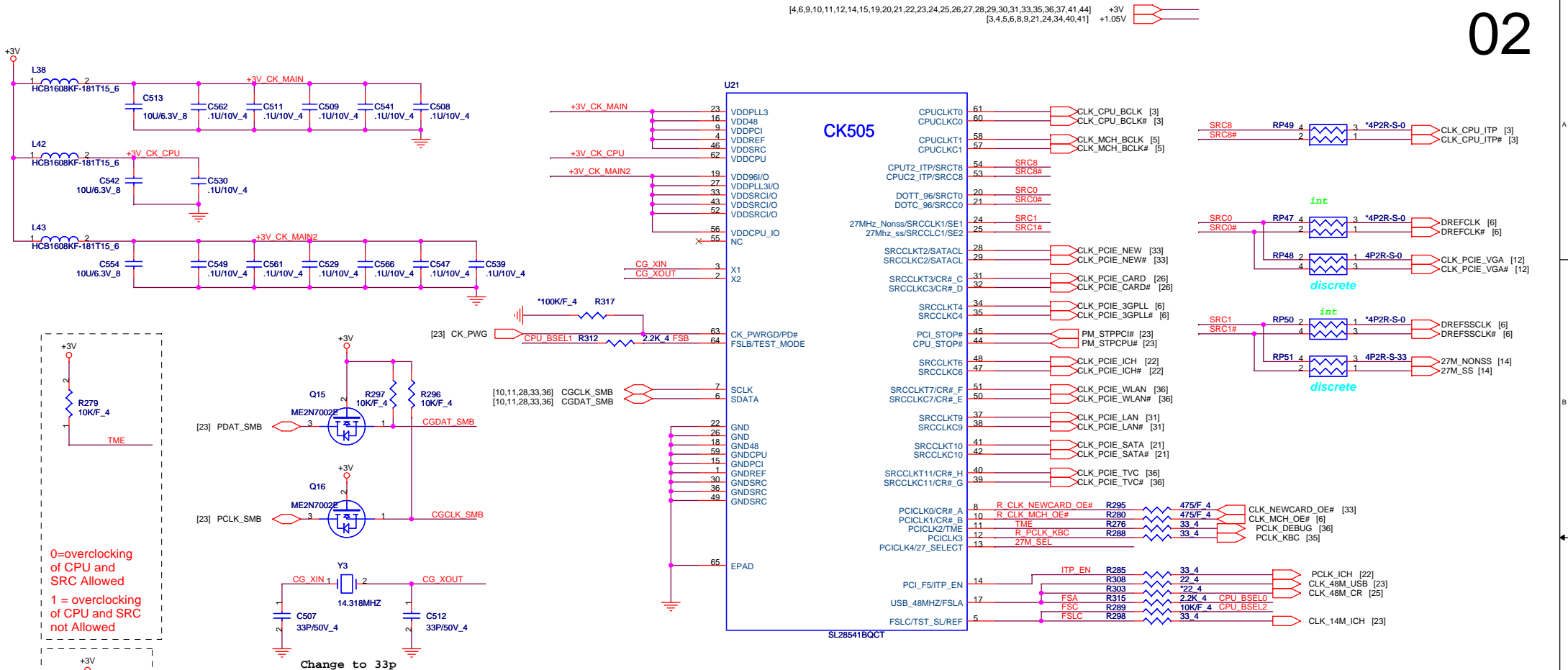
VGACORE(1.025V)Oz8118
 PAGE 45

CPU CORE ISL6266A
 PAGE 44

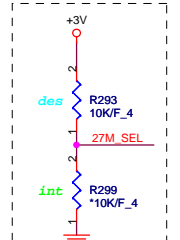


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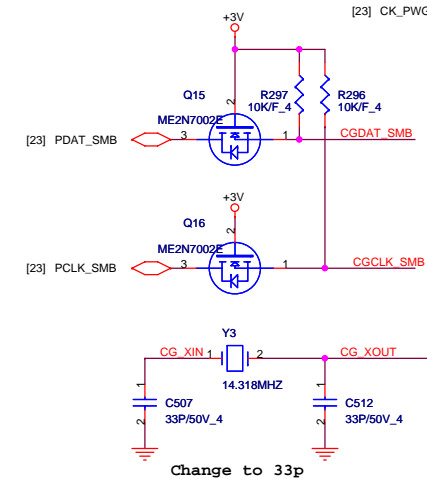
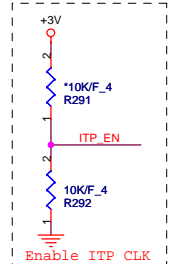
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Block Diagram		
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0=overclocking of CPU and SRC Allowed
1 = overclocking of CPU and SRC not Allowed



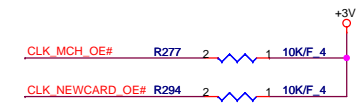
0=UMA
1 = External VGA



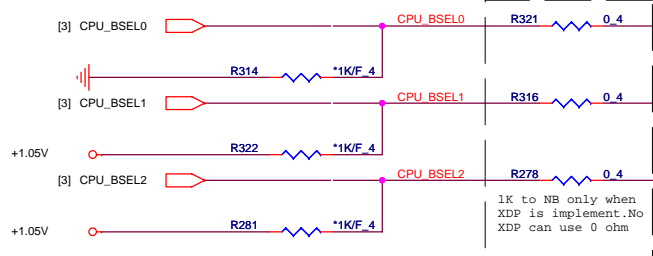
27M_SEL PIN13	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

CK505 QFN64

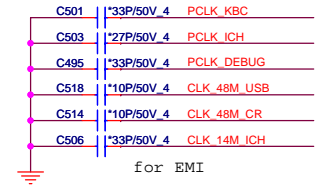
- ICS ICS9LPRS355BKLF ALPRS355000
- Silego SLG8SP513VTR AL8SP513000
- Realtek RTM875N-606-VD-GR AL000875000



CPU Clock select

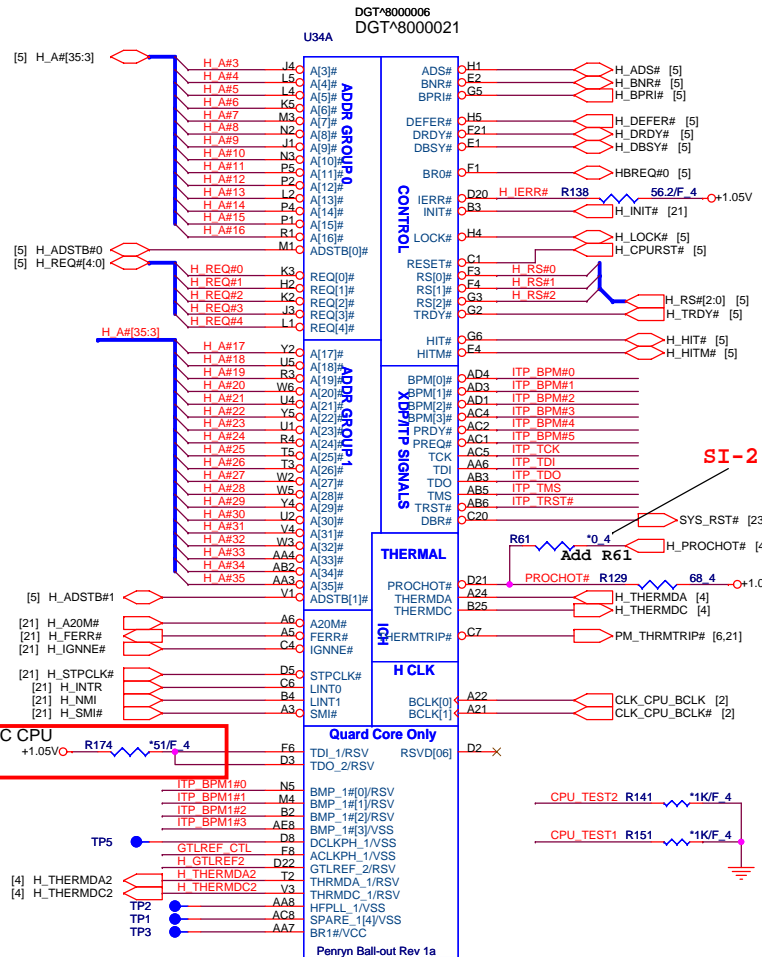


FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33



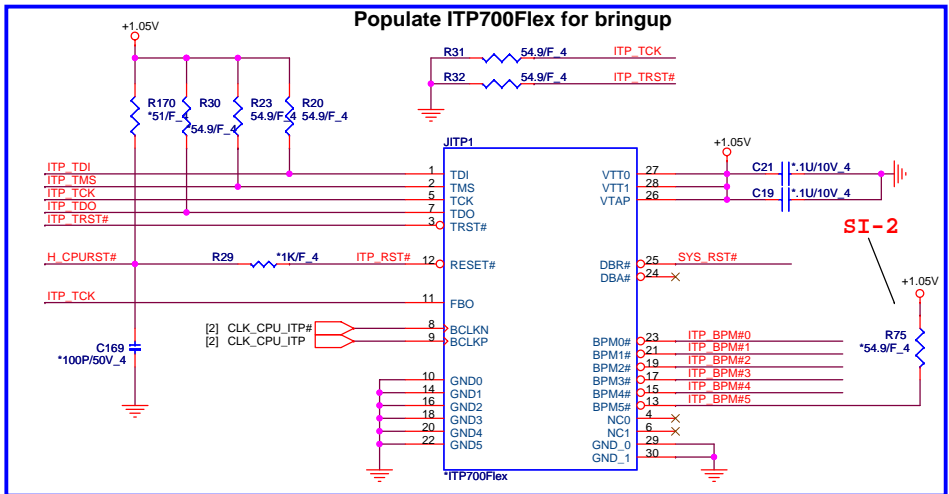
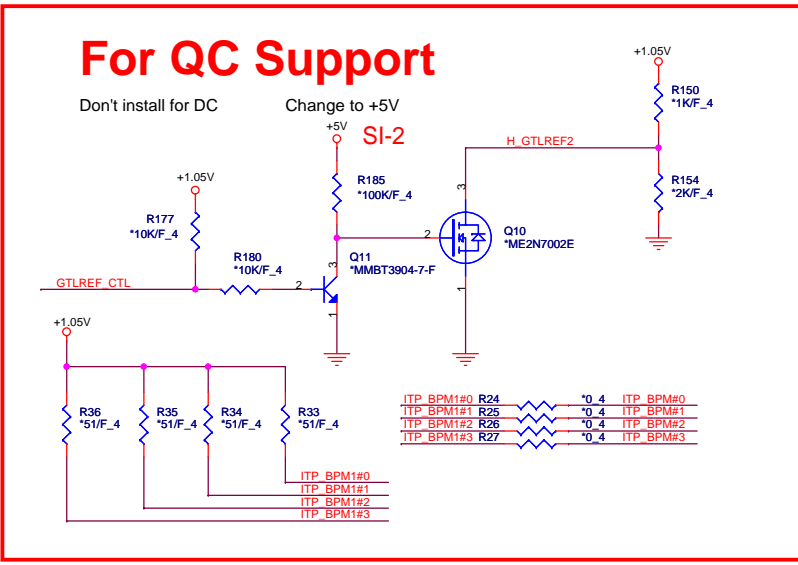
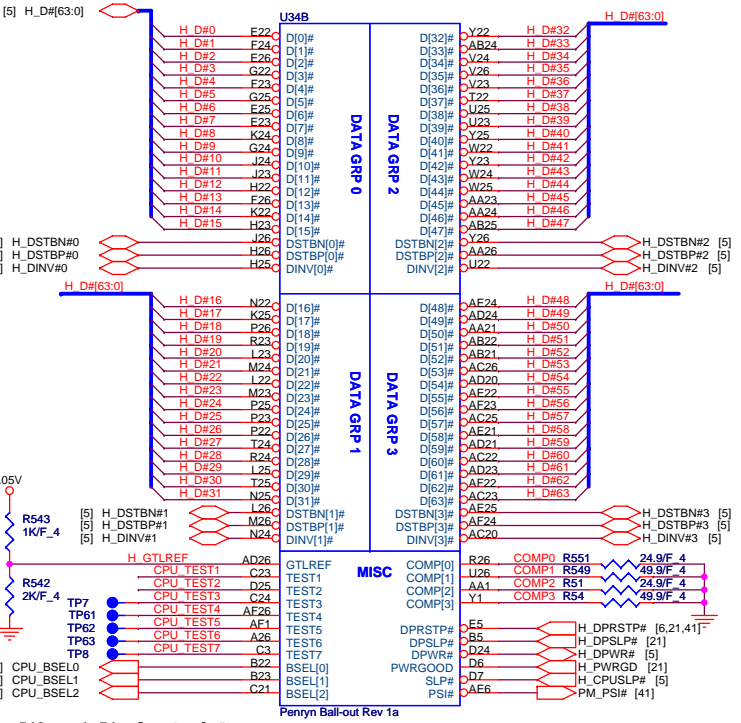
PROJECT : QT6
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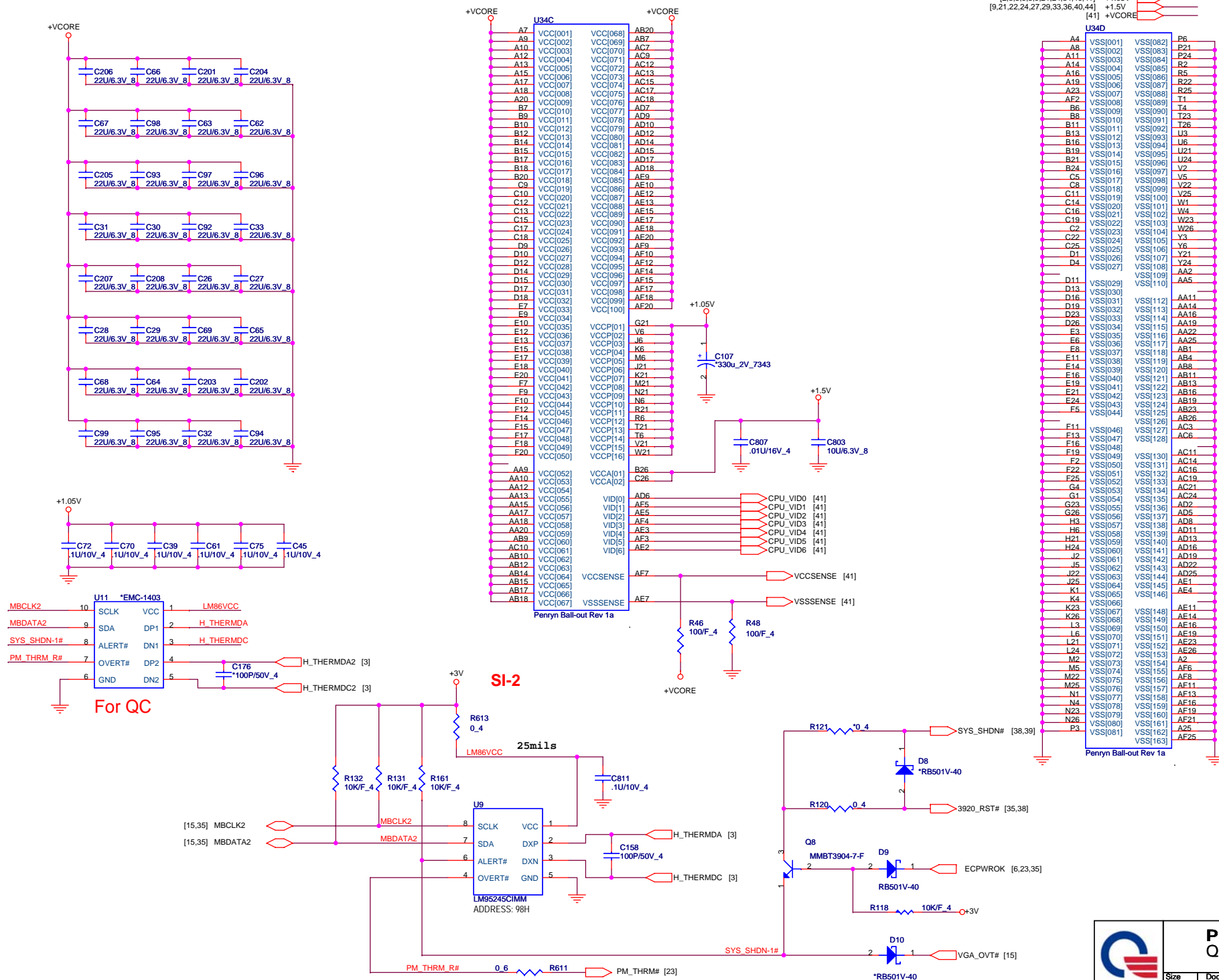
Size Custom	Document Number	Rev 1A
Clock Generator		
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For QC CPU
+1.05V R174 *51/F_4

CPU TEST2 R141 *1K/F_4
CPU TEST1 R151 *1K/F_4





MCH_CFG_5 DMIx2 selection
Low = DMI X2
High = DMI X4 (Default)
MCH_CFG_16 FSB Dynamic ODT
Low = Dynamic ODT disabled
High = Dynamic ODT enabled (default)

MCH_CFG_9 PCI Express Graphic Lane
Low = Reverse Lane
High = Normal operation(Default)
MCH_CFG_19 DMI Lane Reversal
Low = Normal operation (Default)
High = Reverse Lanes

MCH_CFG_6 ITPM Host Interface
Low = The ITPM Host Interface is enabled2
High = The ITPM Host Interface is disabled (default)

MCH_CFG_7 Intel(R) Management Engine Crypto
Low = Intel(R) Management Engine Crypto
High = Intel(R) Management Engine Crypto

MCH_CFG_10 PCIe Lookback Enable
Low = Enabled3
High = Disabled (Default)

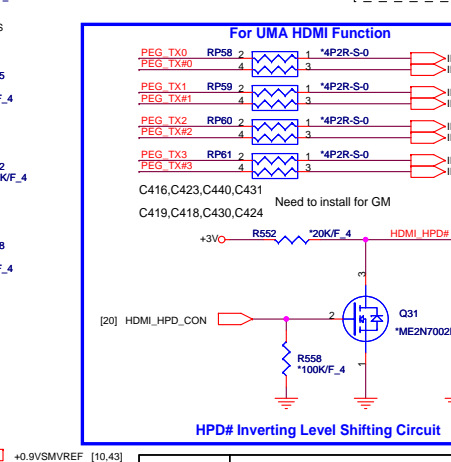
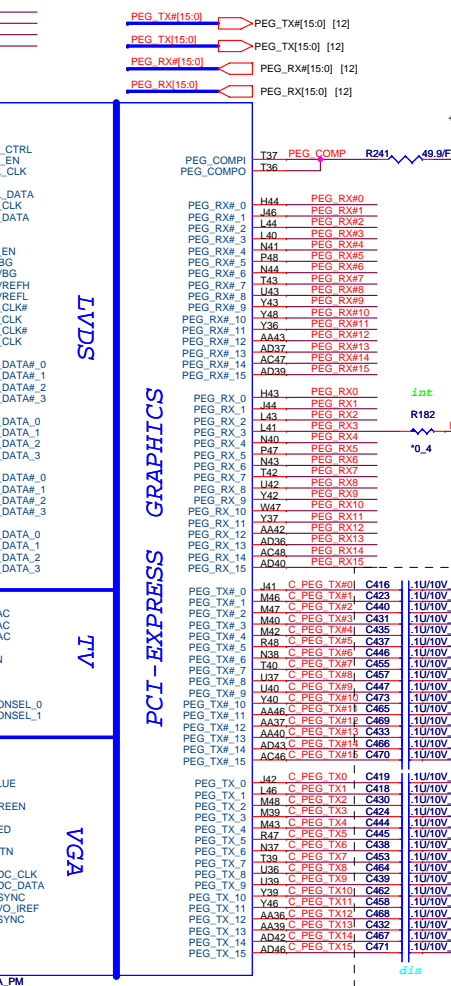
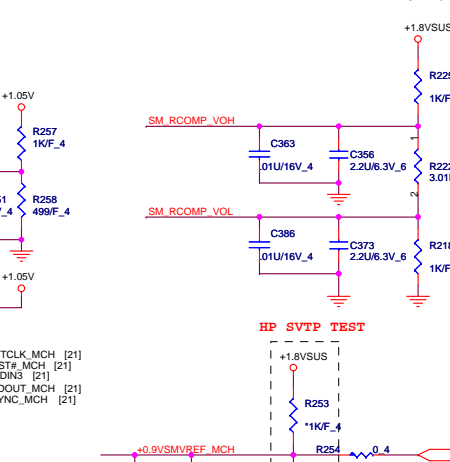
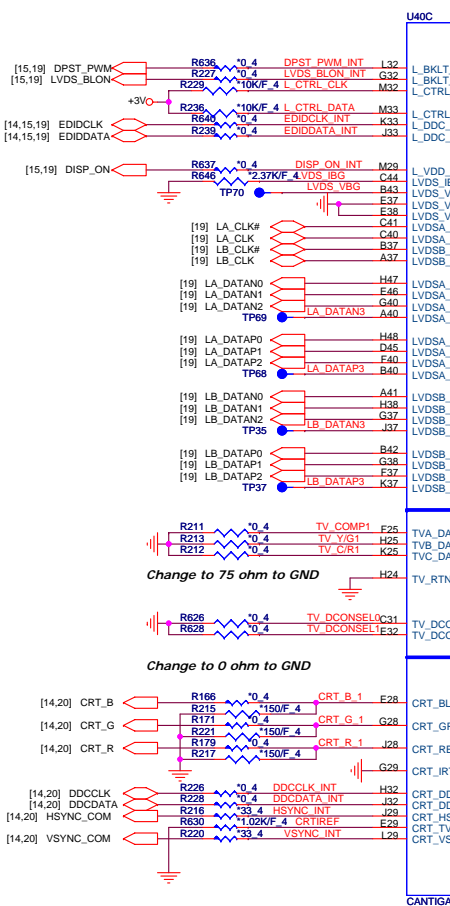
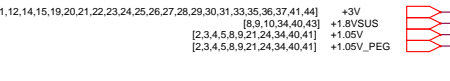
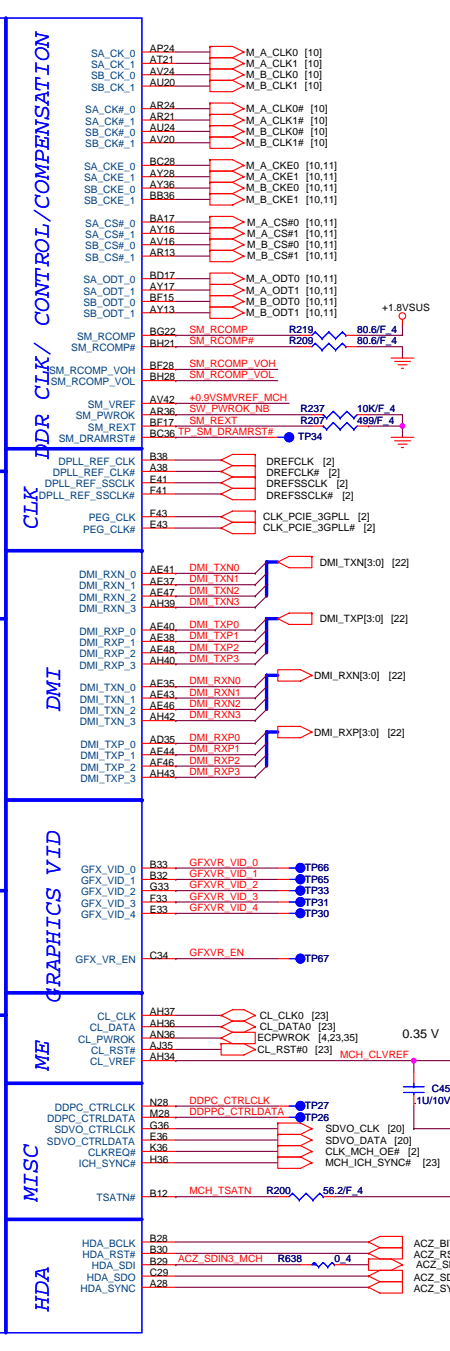
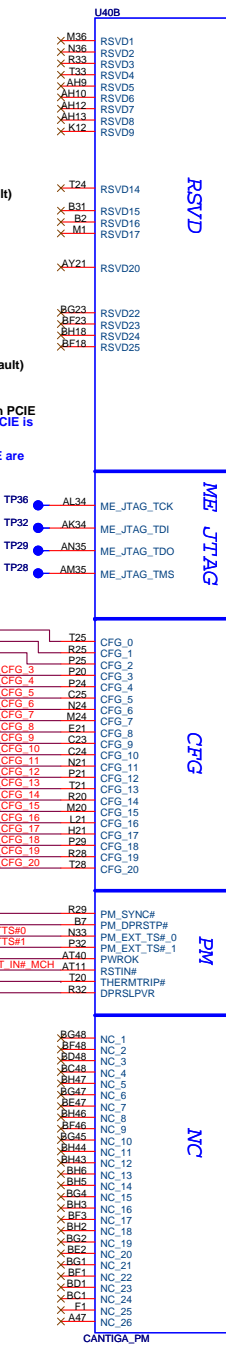
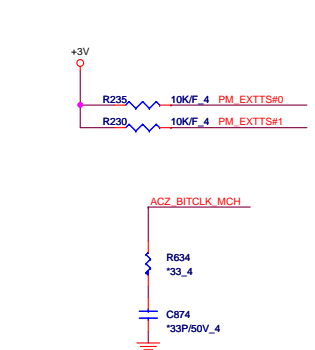
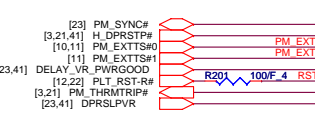
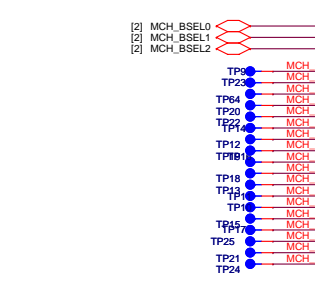
MCH_CFG_12/13 XOR/ALLZ/CLOCK Un-gating

Table with 2 columns: MCH_CFG_12, MCH_CFG_13. Rows include Reserved, XOR Mode enabled, All-Z Mode enabled, Normal operation (Default).

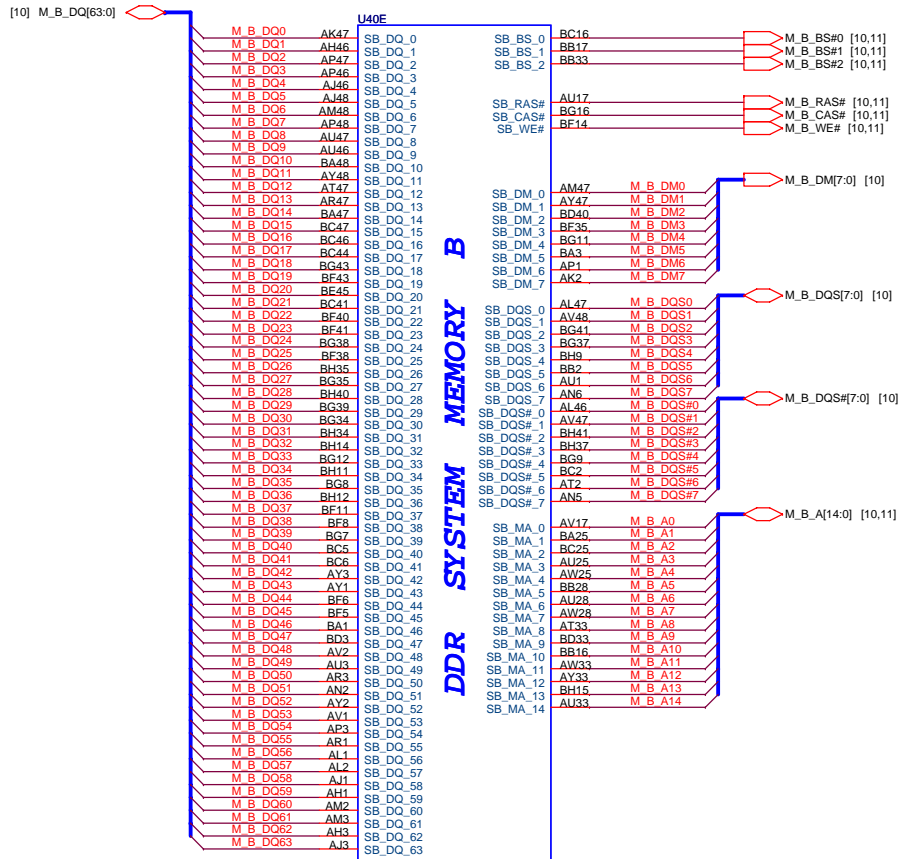
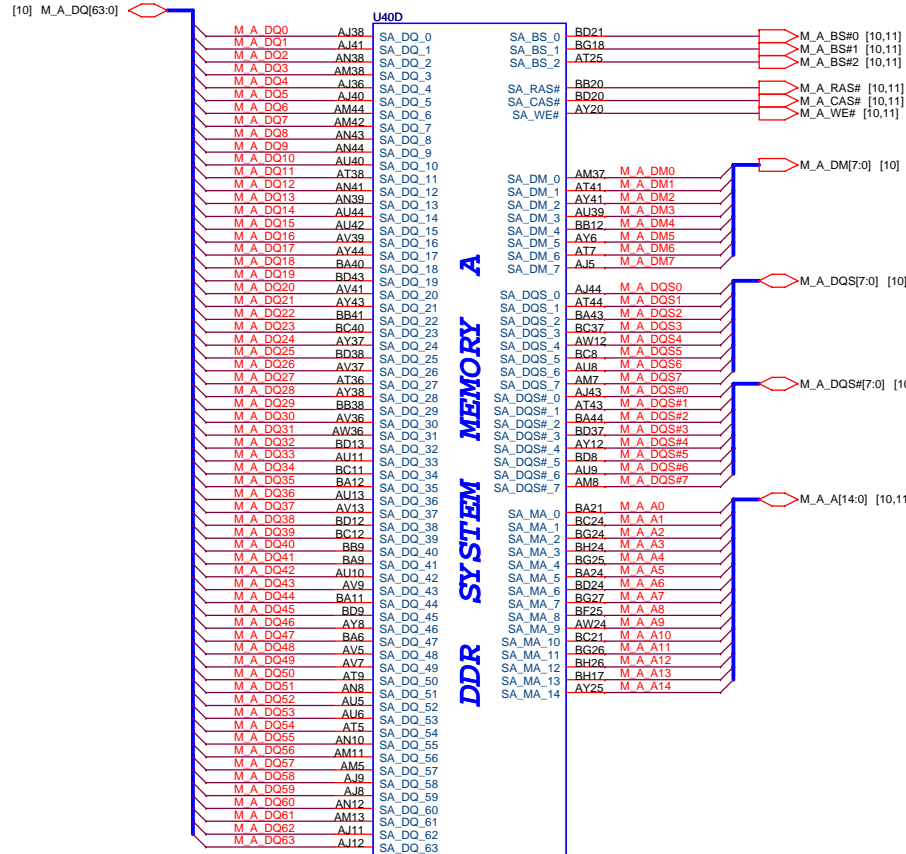
Digital Display Port (SDVO/DP/HDMI) Concurrent with PCIE
Low = Only digital display port (SDVO/DP/HDMI) or PCIE is operational (default)
High = Digital display port (SDVO/DP/HDMI) and PCIE are operating simultaneously with the DP port

MCH_CFG:0
000 = FSB1066
010 = FSB800
011 = FSB667
Others = Reserved

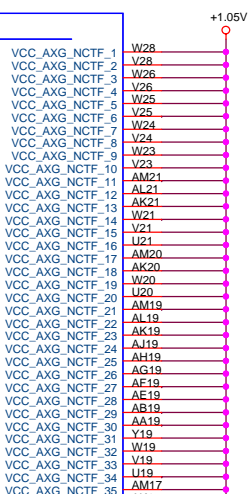
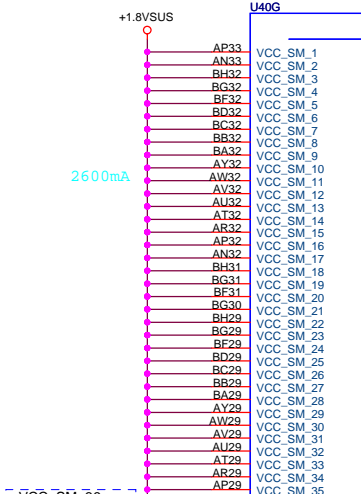
MCH_CFG_3 MCH_CFG_4 MCH_CFG_5 MCH_CFG_6 MCH_CFG_7 MCH_CFG_8 MCH_CFG_9 MCH_CFG_10 MCH_CFG_11 MCH_CFG_12 MCH_CFG_13 MCH_CFG_14 MCH_CFG_15 MCH_CFG_16 MCH_CFG_17 MCH_CFG_18 MCH_CFG_19 MCH_CFG_20



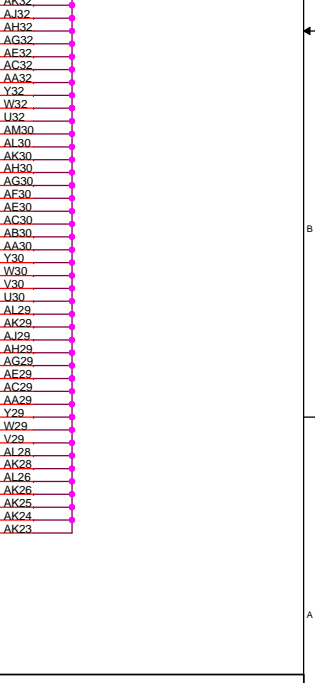
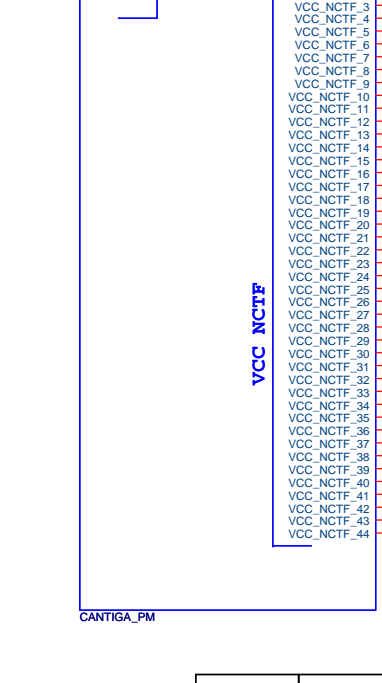
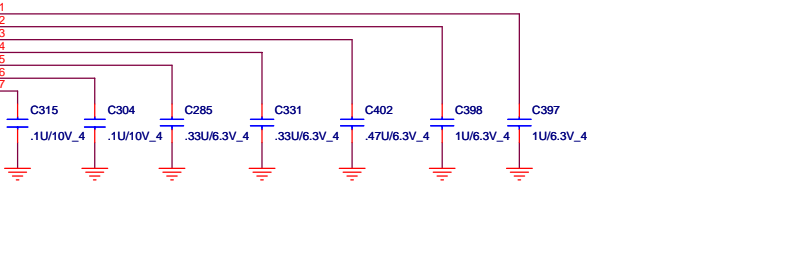
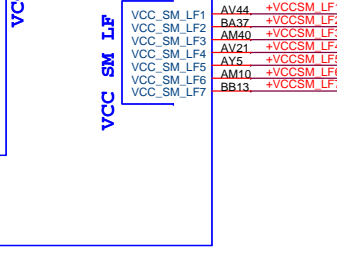
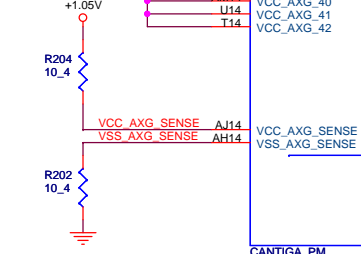
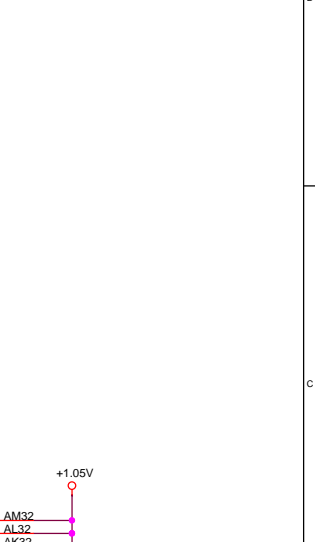
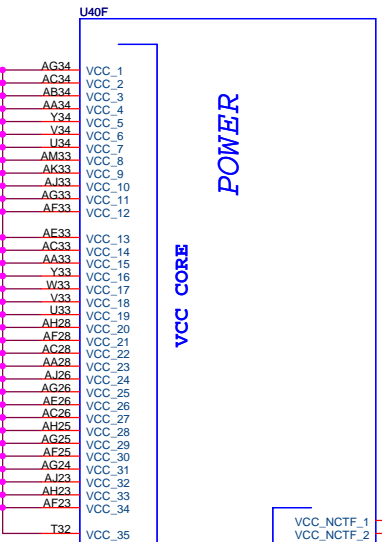
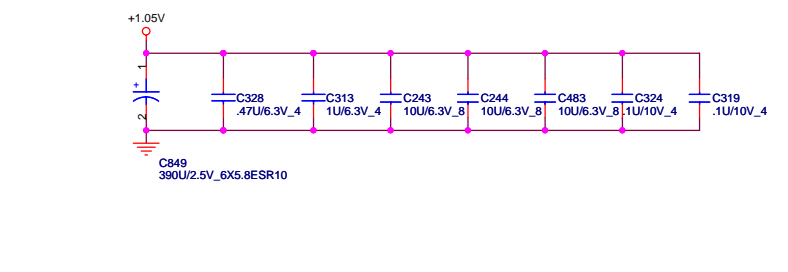
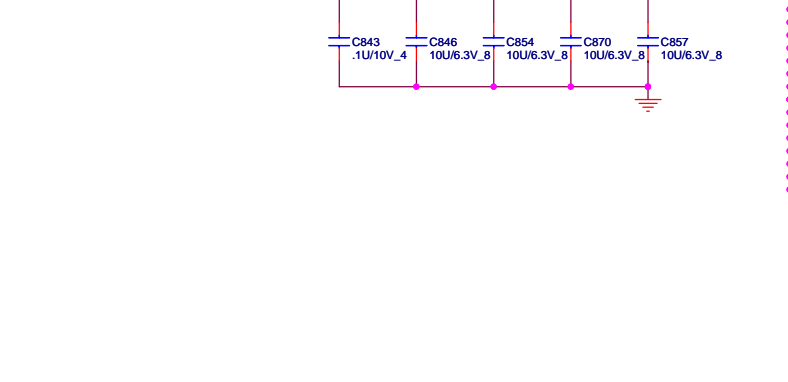
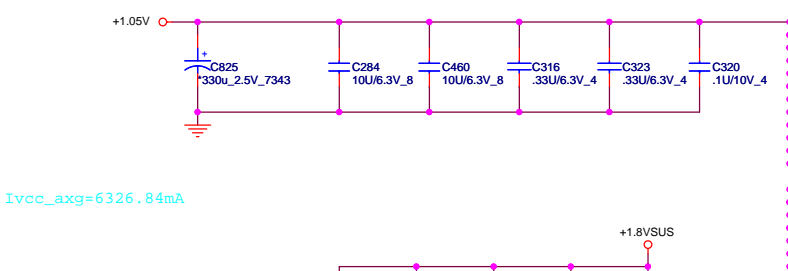
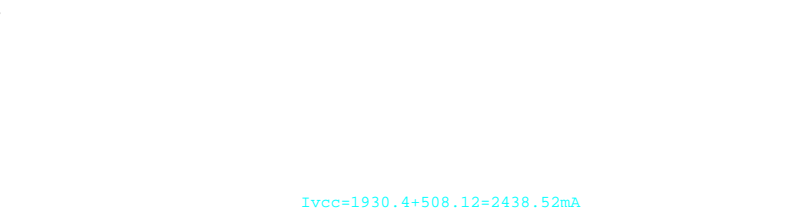
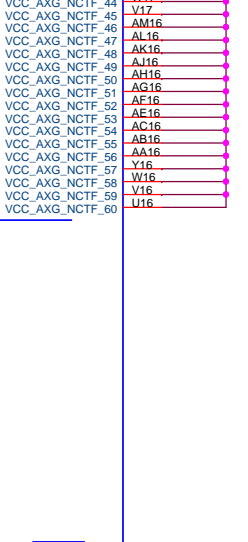
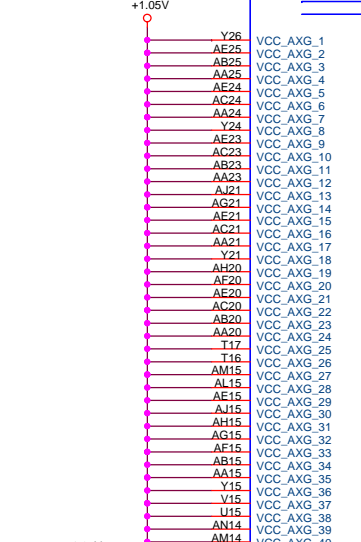
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Size Custom Document Number Cantiga DMI/DISP 2/5 Rev 1A
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[6,9,10,34,40,43] +1.8VSUS
[2,3,4,5,6,9,21,24,34,40,41] +1.05V



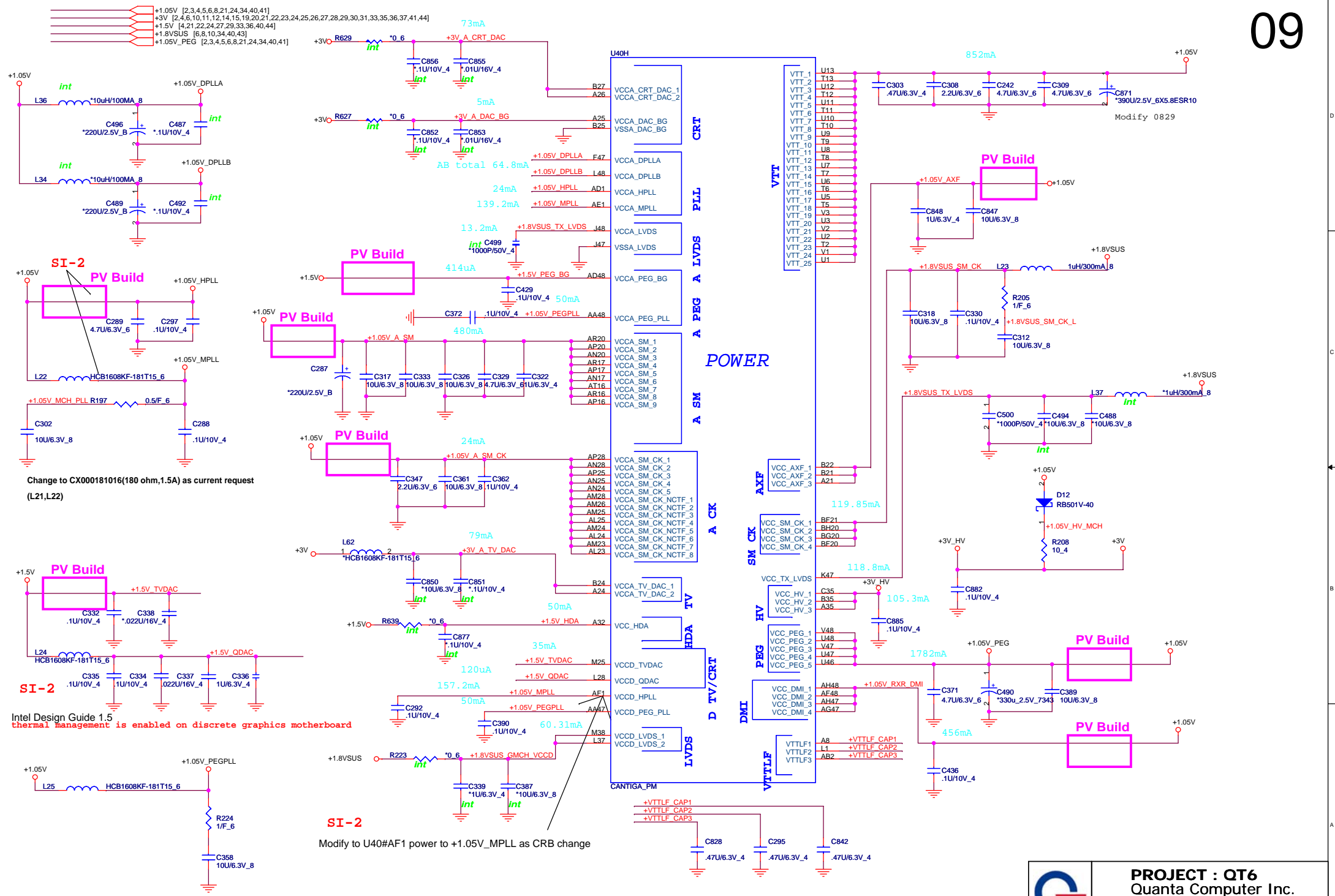
VCC_SM_36 through VCC_SM_42 can be left as NC for DDR2 desigs.



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Size Custom Document Number **Cantiga Vcc 4/5** Rev 1A


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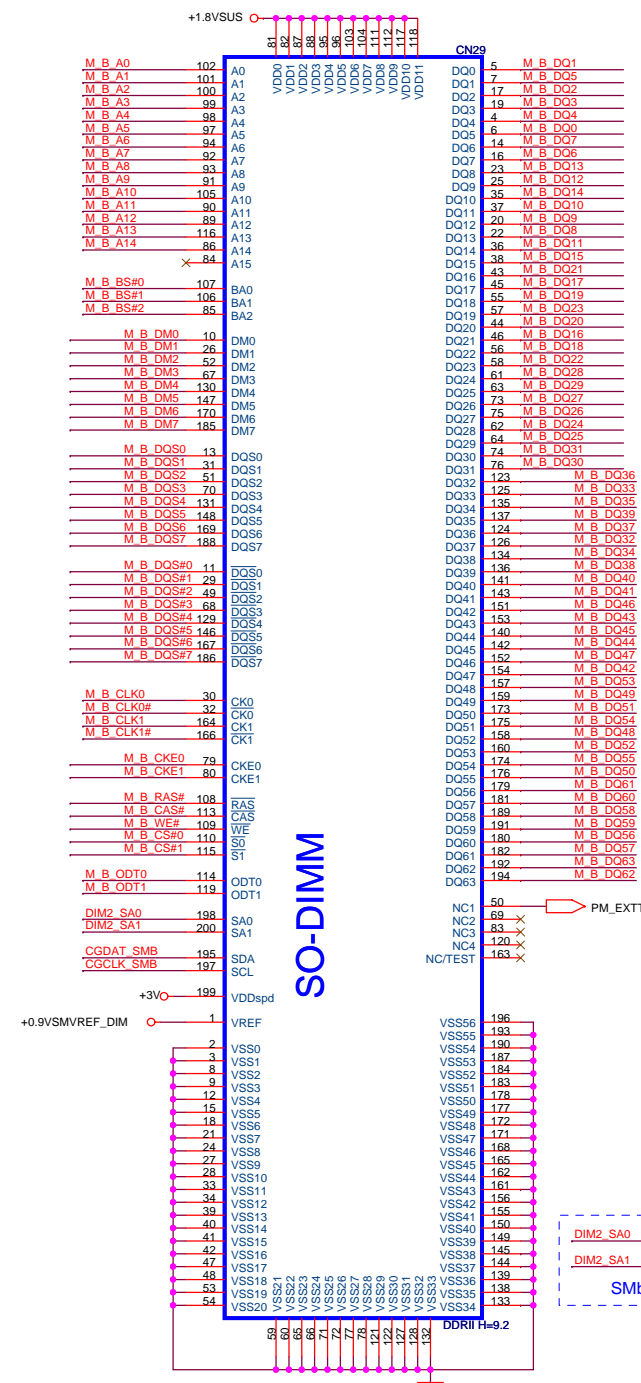


Change to CX000181016 (180 ohm, 1.5A) as current request (L21, L22)

Intel Design Guide 1.5 thermal management is enabled on discrete graphics motherboard

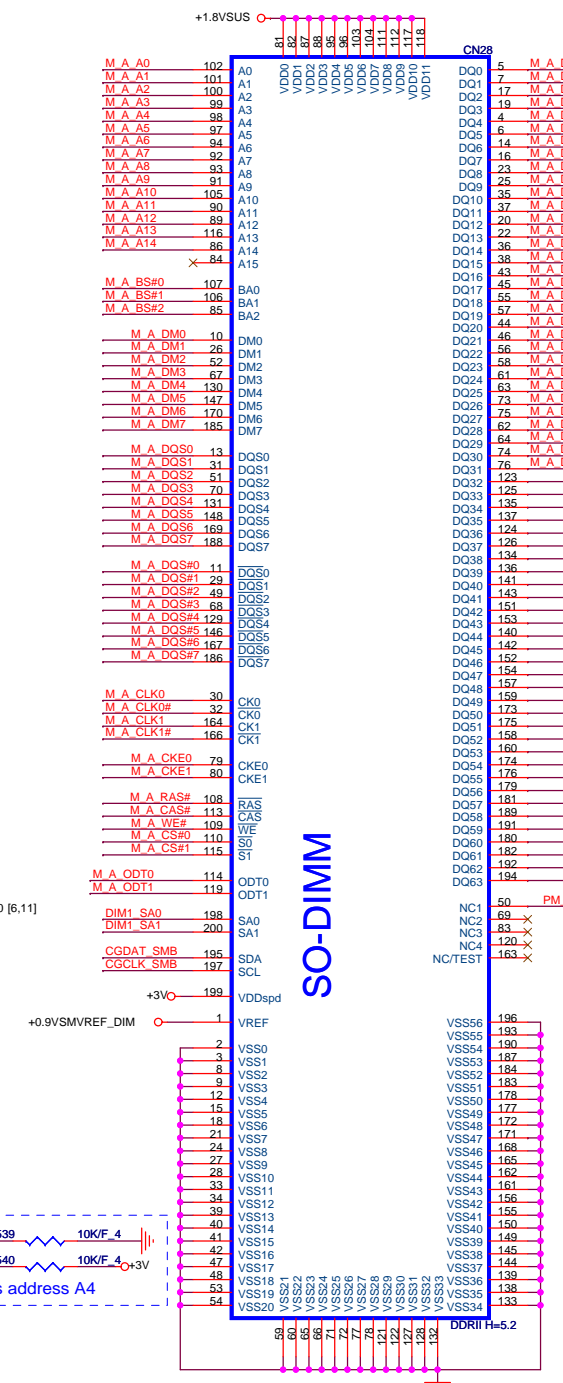
Modify to U40#AF1 power to +1.05V_MPLL as CRB change

	PROJECT : QT6 Quanta Computer Inc.	
	Size Custom Document Number Cantiga Power 5/5	Rev 3A Date: Tuesday, February 26, 2008 Sheet 9 of 44



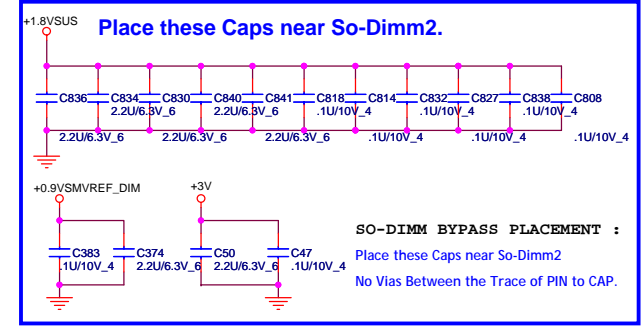
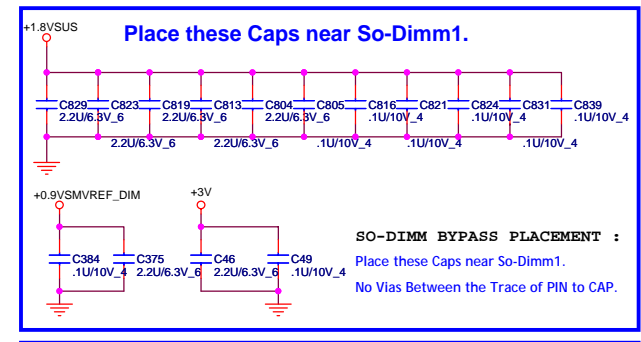
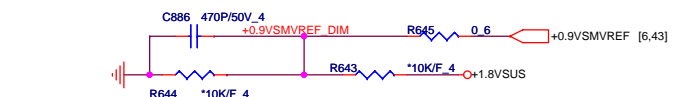
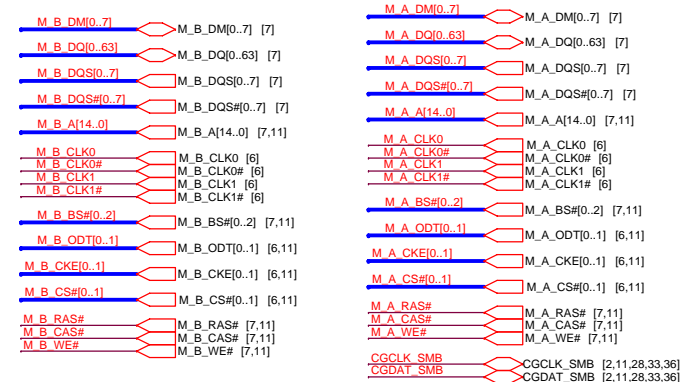
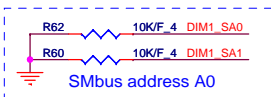
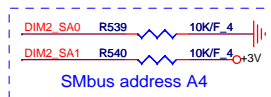
SO-DIMM

H 9.2
DGMK0000036



SO-DIMM

H 5.2
DGMK0000031



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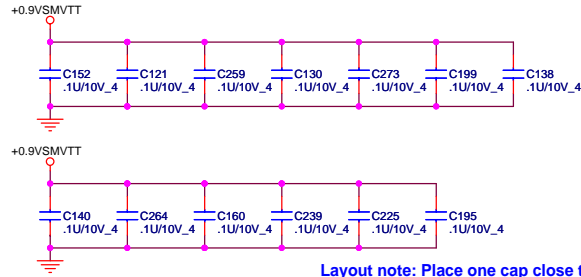
NB5

Size Custom Document Number **DDR2 DIMM** Rev 1A

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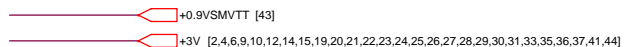
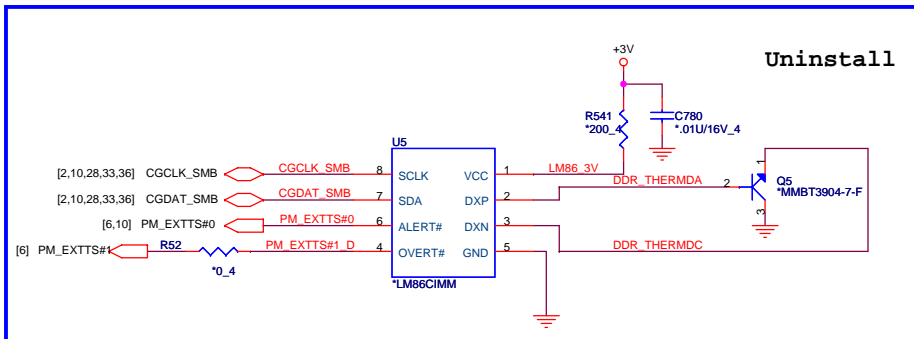
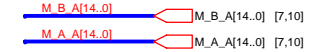
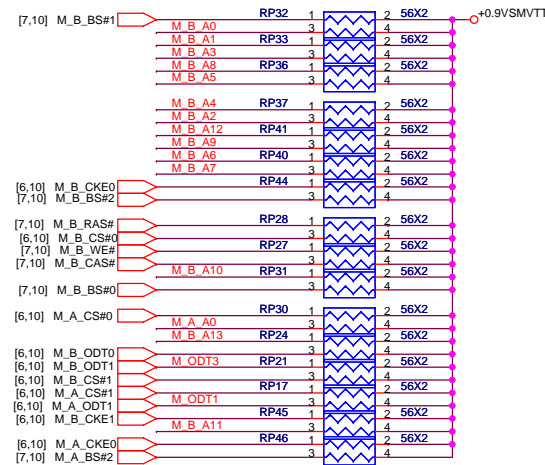
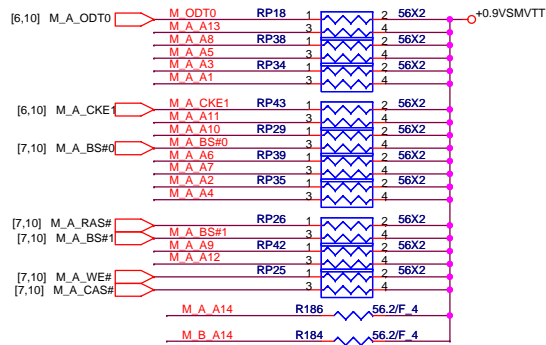
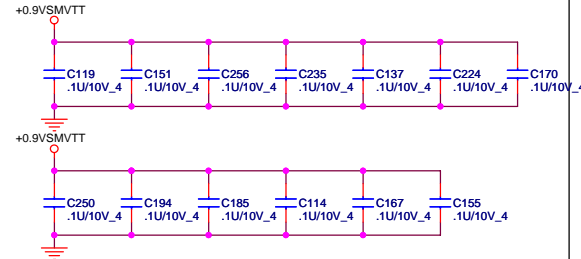
DDRII DUAL CHANNEL A,B.

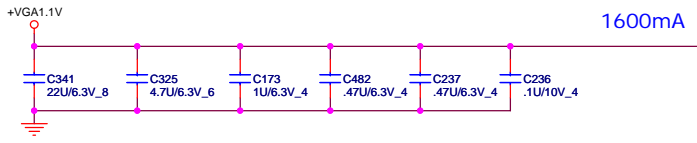
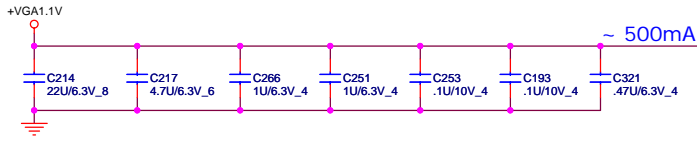
DDRII A CHANNEL



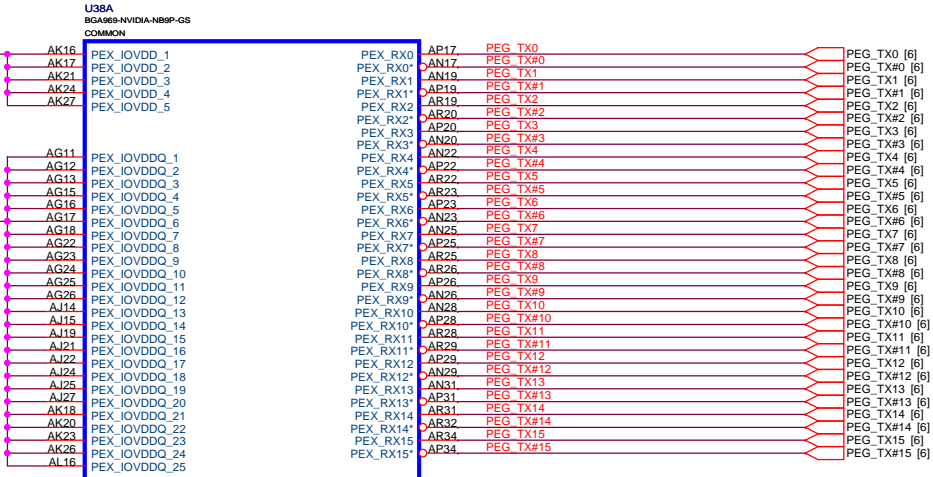
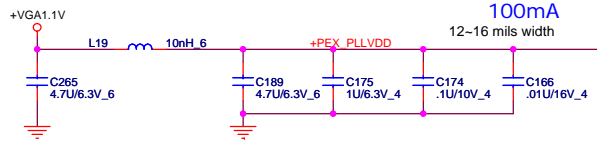
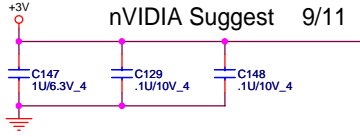
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

DDRII B CHANNEL

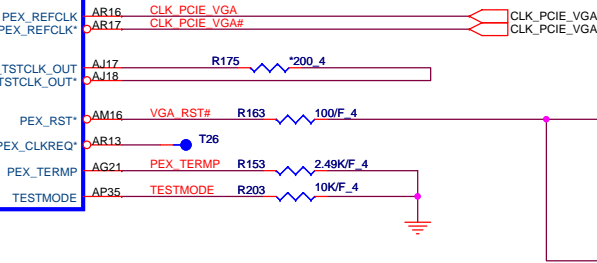
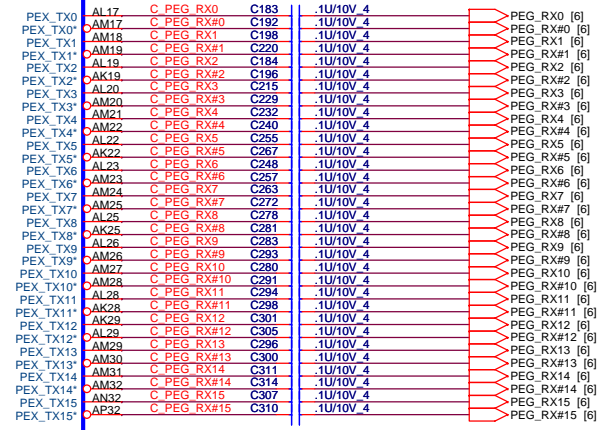




Near BGA



PCI EXPRESS



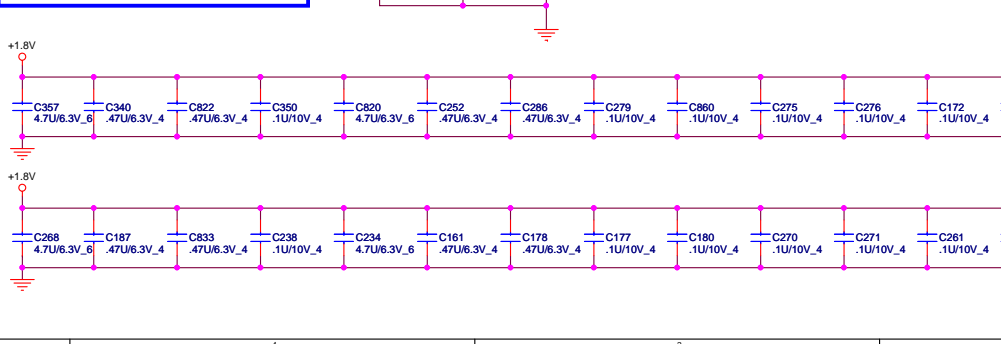
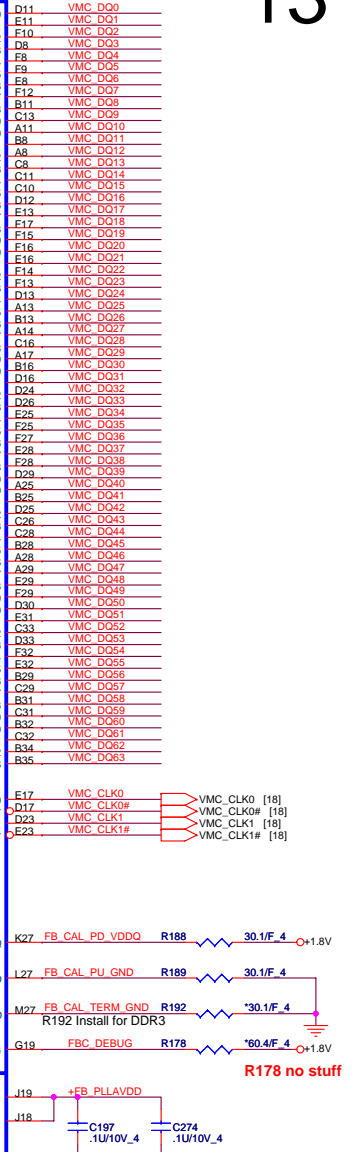
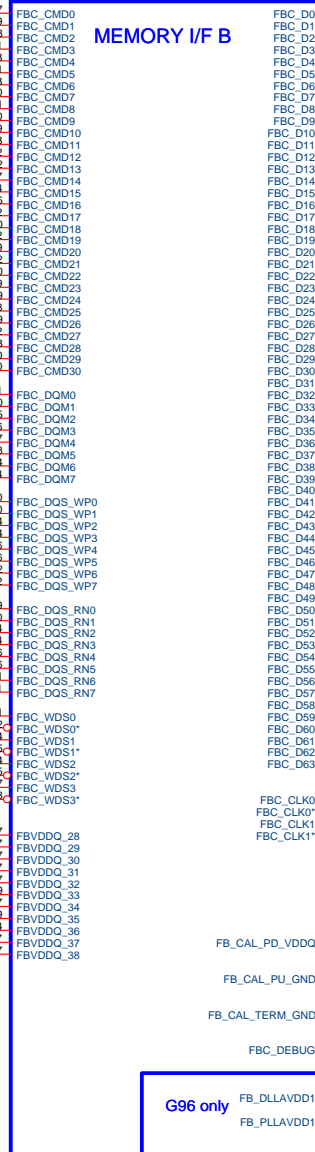
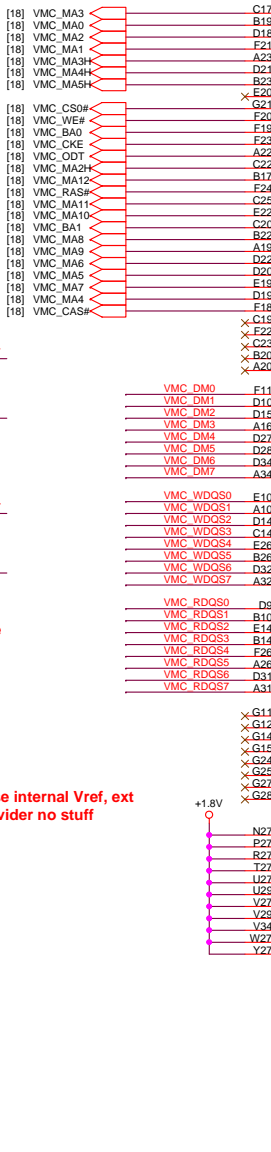
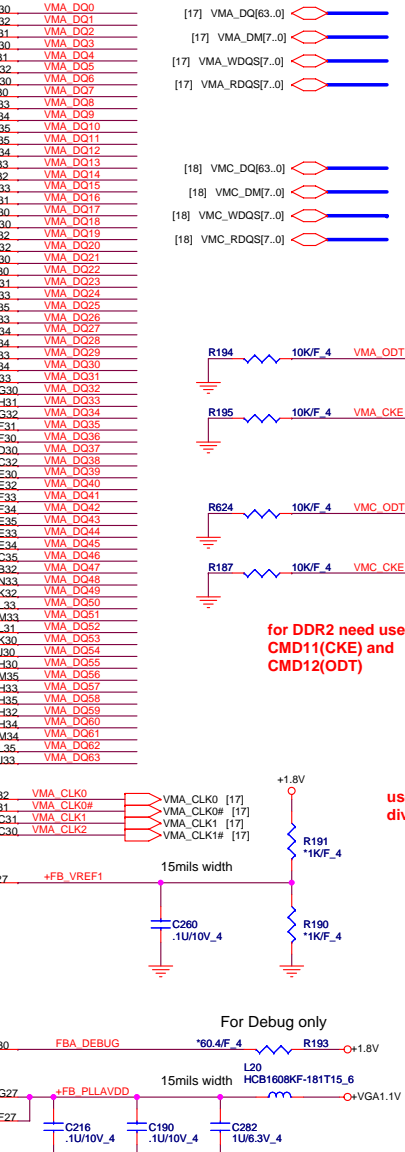
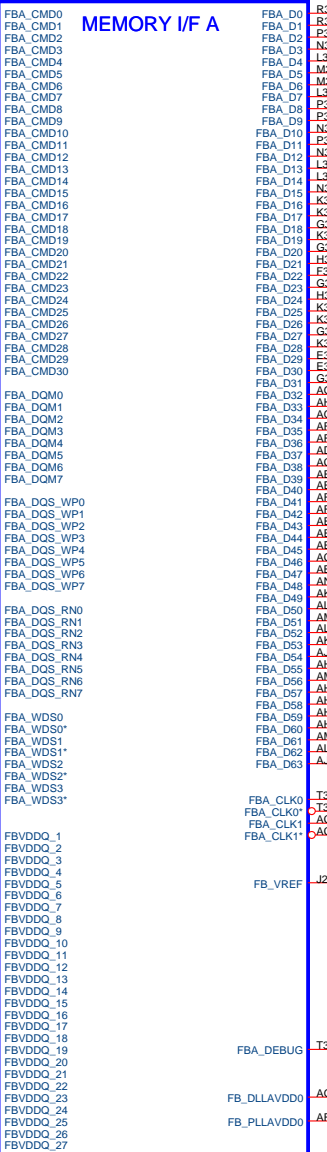
U38B
BGAR99-NVIDIA-NB9P-GS
COMMON

[17] VMA_MA3	Y32	FBA_CMD0
[17] VMA_MA0	W31	FBA_CMD1
[17] VMA_MA2	U31	FBA_CMD2
[17] VMA_MA1	Y32	FBA_CMD3
[17] VMA_MA3H	AB35	FBA_CMD4
[17] VMA_MA4H	AB34	FBA_CMD5
[17] VMA_MASH	W35	FBA_CMD6
	W33	FBA_CMD7
	W30	FBA_CMD8
[17] VMA_CS0#	T34	FBA_CMD9
[17] VMA_WE#	T35	FBA_CMD10
[17] VMA_CKE	AB31	FBA_CMD11
	X30	FBA_CMD12
[17] VMA_ODT	Y34	FBA_CMD13
[17] VMA_MA2H	W32	FBA_CMD14
[17] VMA_MA12	W32	FBA_CMD14
[17] VMA_RAS#	AA30	FBA_CMD15
[17] VMA_MA11	AA32	FBA_CMD16
[17] VMA_MA10	Y33	FBA_CMD17
[17] VMA_BA1	U32	FBA_CMD18
[17] VMA_MA8	Y31	FBA_CMD19
[17] VMA_MA5	U34	FBA_CMD20
[17] VMA_MA6	Y35	FBA_CMD21
[17] VMA_MA9	W34	FBA_CMD22
[17] VMA_MA7	Y30	FBA_CMD23
[17] VMA_MA4	U35	FBA_CMD24
[17] VMA_CAS#	U30	FBA_CMD25
	X33	FBA_CMD26
	AB30	FBA_CMD27
	X33	FBA_CMD28
	T33	FBA_CMD29
	W29	FBA_CMD30

VMA_DM0	P30	FBA_DM0#
VMA_DM1	P32	FBA_DM1#
VMA_DM2	J30	FBA_DM2#
VMA_DM3	H34	FBA_DM3#
VMA_DM4	AF34	FBA_DM4#
VMA_DM5	AF35	FBA_DM5#
VMA_DM6	AL32	FBA_DM6#
VMA_DM7	AL34	FBA_DM7#

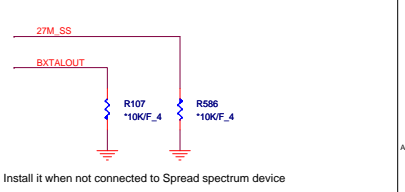
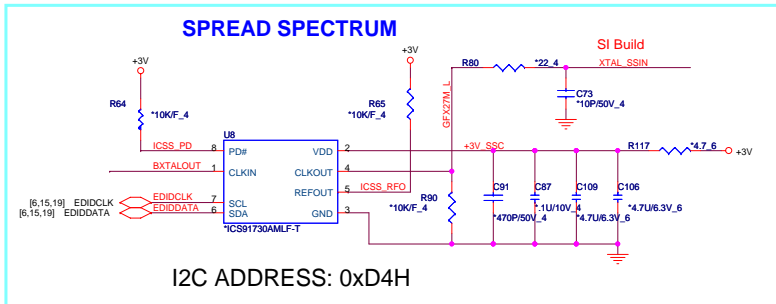
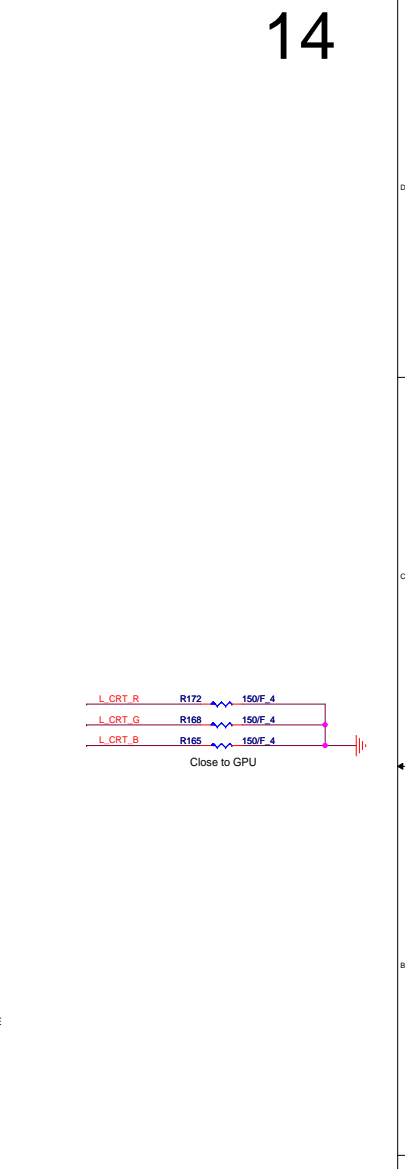
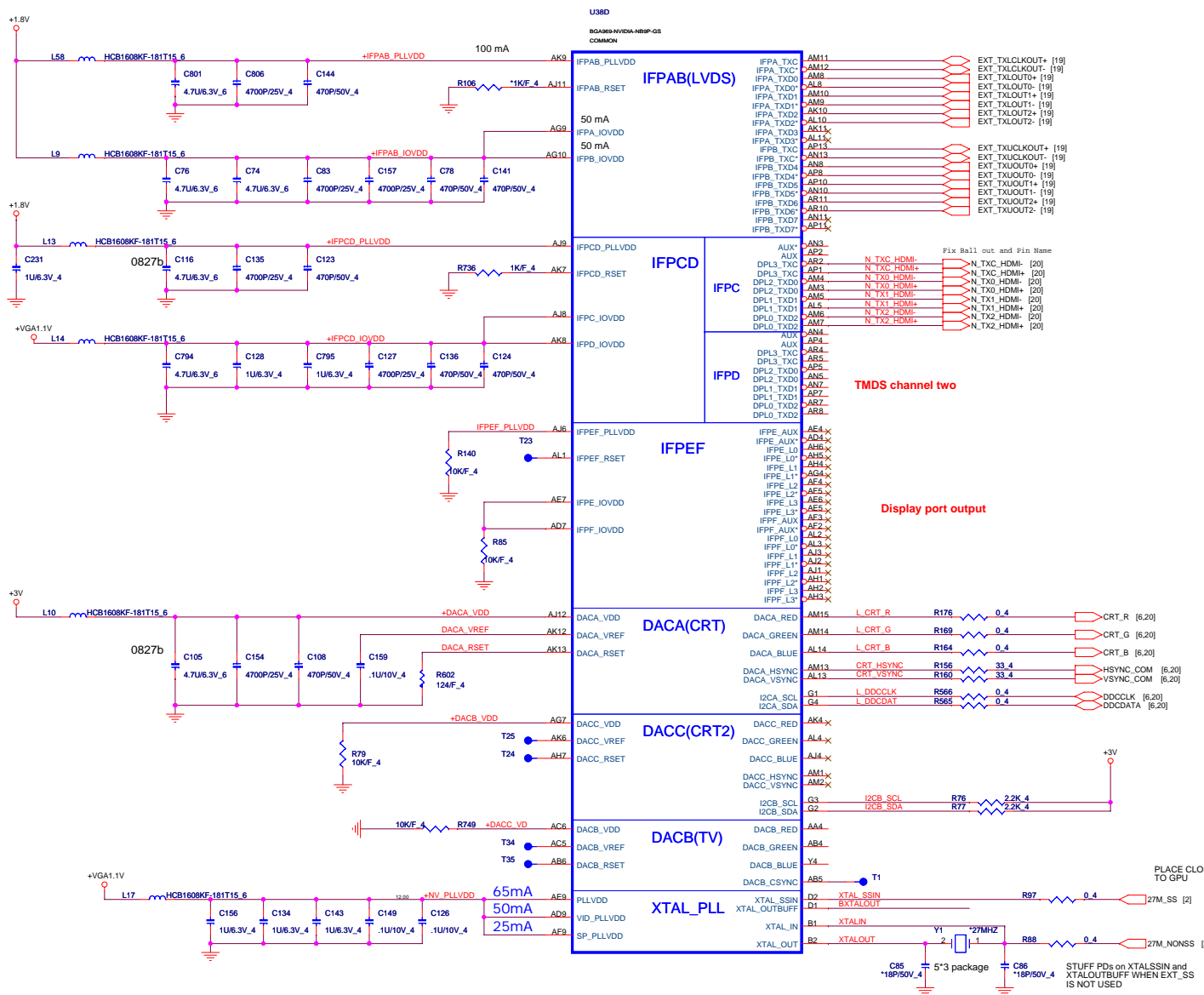
VMA_WDQ50	N31	FBA_DQS_WP0
VMA_WDQ51	L34	FBA_DQS_WP1
VMA_WDQ52	J32	FBA_DQS_WP2
VMA_WDQ53	H35	FBA_DQS_WP3
VMA_WDQ54	AE31	FBA_DQS_WP4
VMA_WDQ55	AC33	FBA_DQS_WP5
VMA_WDQ56	AJ32	FBA_DQS_WP6
VMA_WDQ57	AJ34	FBA_DQS_WP7

VMA_RDQ50	N32	FBA_DQS_RN0
VMA_RDQ51	L35	FBA_DQS_RN1
VMA_RDQ52	H31	FBA_DQS_RN2
VMA_RDQ53	G35	FBA_DQS_RN3
VMA_RDQ54	AD32	FBA_DQS_RN4
VMA_RDQ55	AC34	FBA_DQS_RN5
VMA_RDQ56	AJ31	FBA_DQS_RN6
VMA_RDQ57	AJ35	FBA_DQS_RN7



PROJECT : QT6
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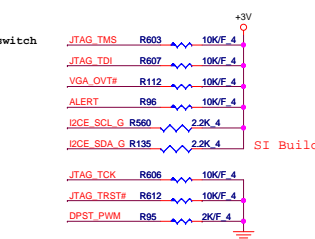
Size Custom	Document Number	Rev 1A
	NV9X (MEMORY I/F) 2/5	
Date: Tuesday, February 26, 2008	Sheet 13	of 44



NB9P-GS (G96) Straps NB9M-GE (G98) Straps GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NV_VDD VID0
6	OUT	N/A	NV_VDD VID1
7	OUT	N/A	FB_VDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL

SEE Datasheet for details on G9x Straps!



Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

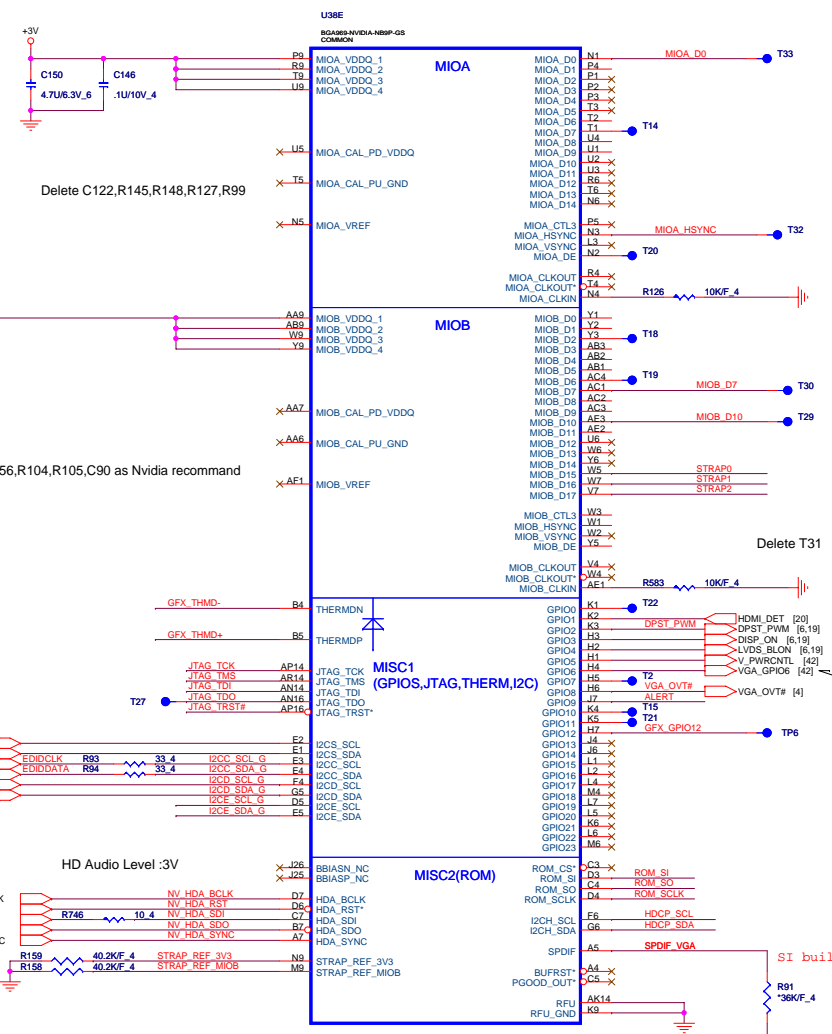
	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_277	TVMODE[2]	TVMODE[1]	TVMODE[0]	1000
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM100	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

PCI_DEVID: **STRAP2 R554**
 NB9M-GE 0x06E 8 1000 PU 5K
 NB9M-GS 0x06E 9 1001 PU 10K
 NB9P-GE2 0x064 8 1000 PU 5K
 NB9P-GS 0x064 9 1001 PU 10K

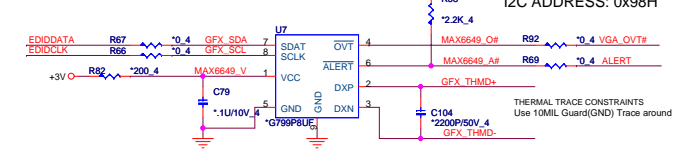
CS33572FB13 RES CHIP 35.7K 1/16W +-1% (0402)
 CS34532FB18 RES CHIP 45.3K 1/16W +-1% (0402)
RAM ID: ROM_SI R585
 SAM 0101 PD 30.1K
 QIM 0110 PD 35.7K
 HYN 0111 PD 45.3K

NB9X VRAM Configuration Table

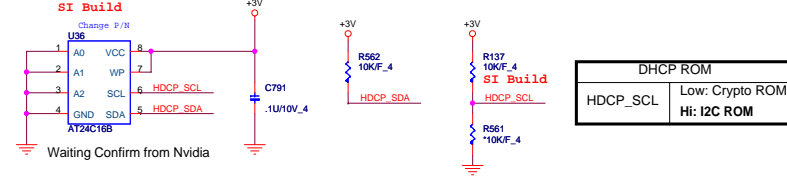
RAM_CFG[3:0]	DESCRIPTION	Vendor
0111	DDR2 32Mx16x8, 128bit, 512MB	Hynix
0110	DDR2 32Mx16x8, 128bit, 512MB	Gilmonda
0101	DDR2 32Mx16x8, 128bit, 512MB	Samsung
other	Reserved	



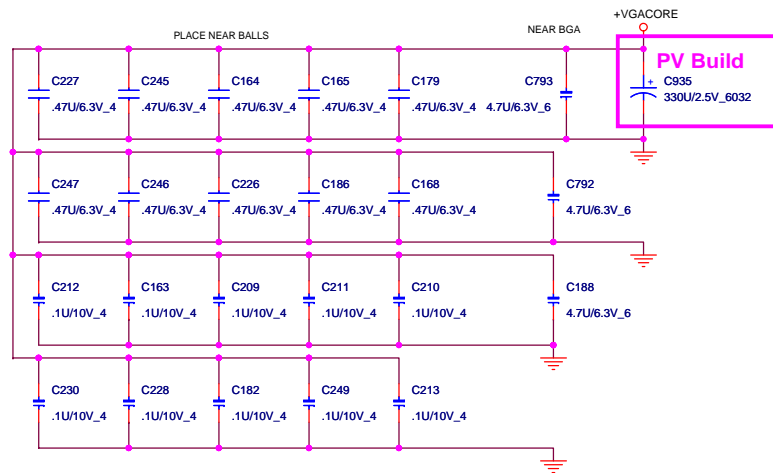
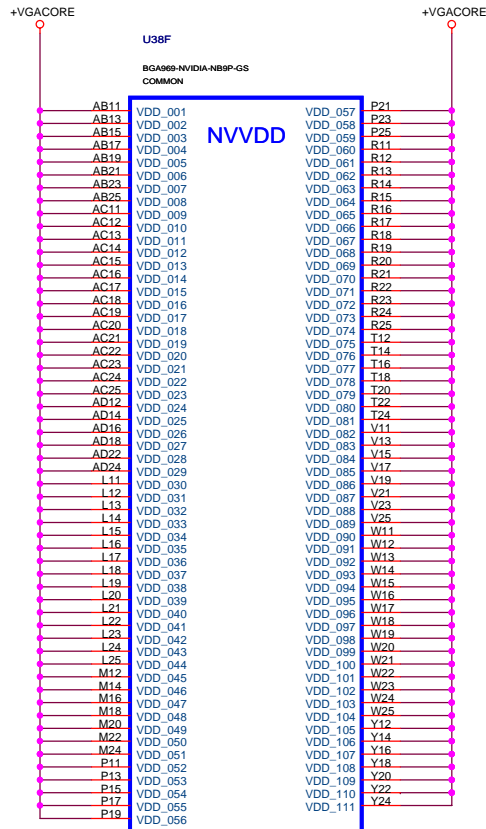
VGA THERMAL CIRCUIT



HDPCP ROM

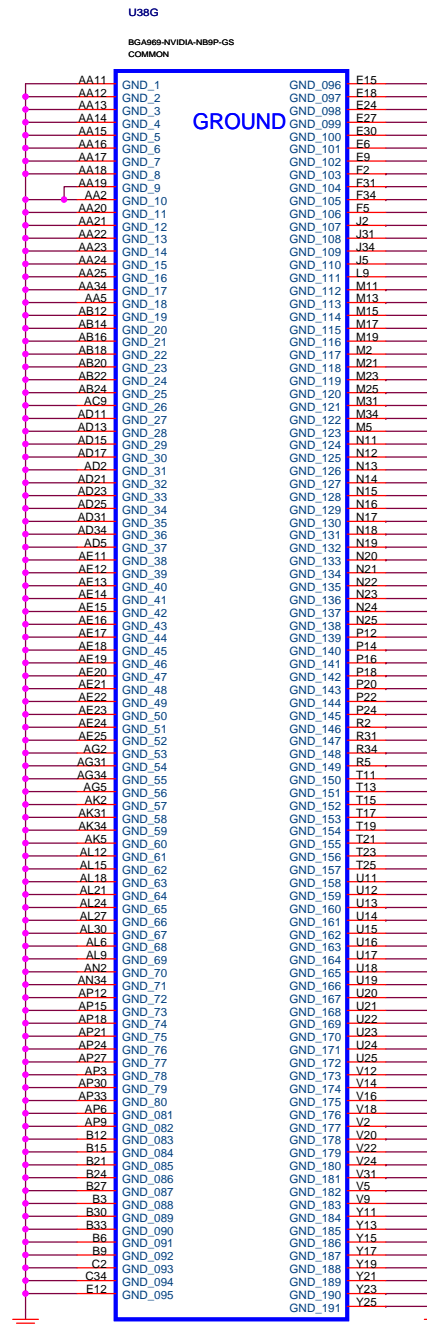
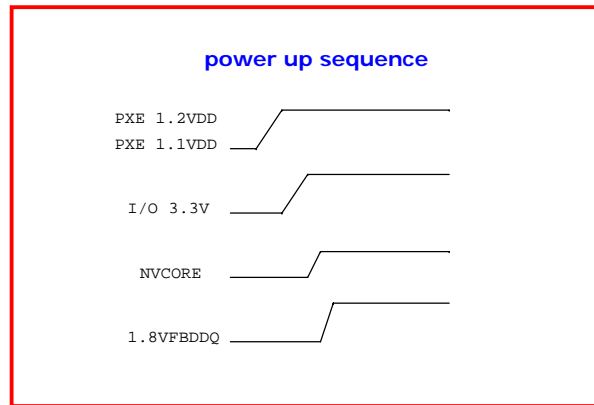


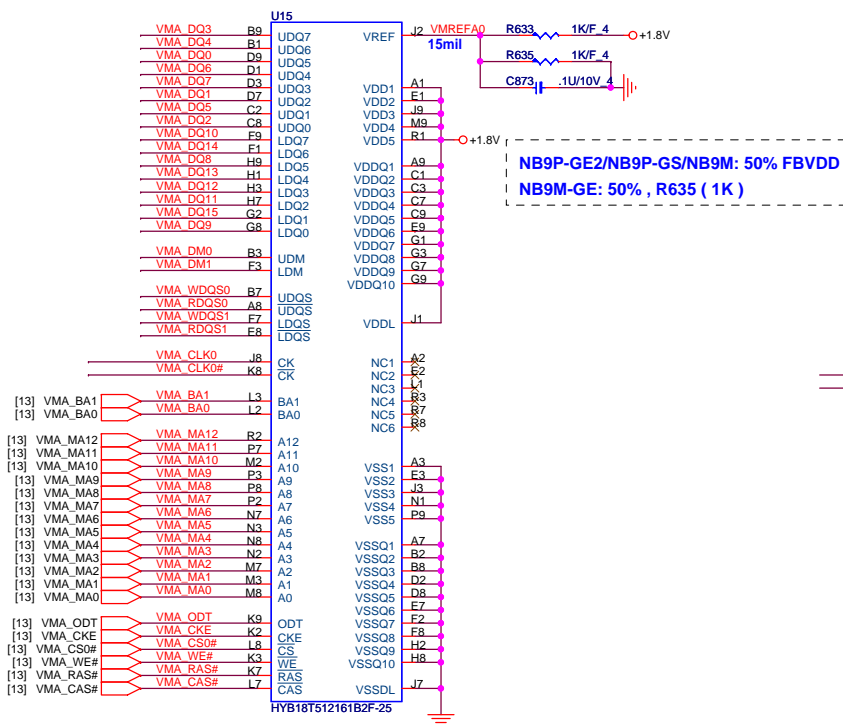
NVVDD Decoupling



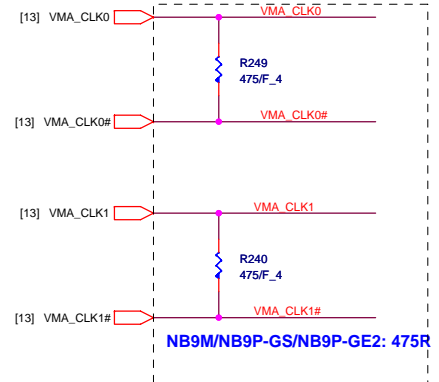
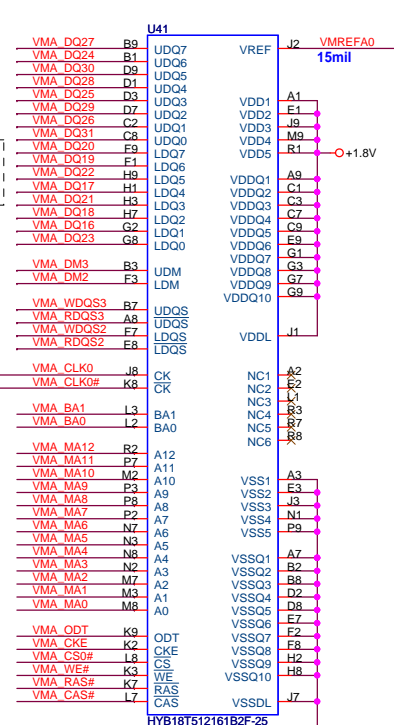
Follow Design Guide DG-03276-001 4.7uF x3 and 0.47x10 uF instead of 0.1uF x10

NB9M: VGACORE +0.90V (Normal) , +1.09V

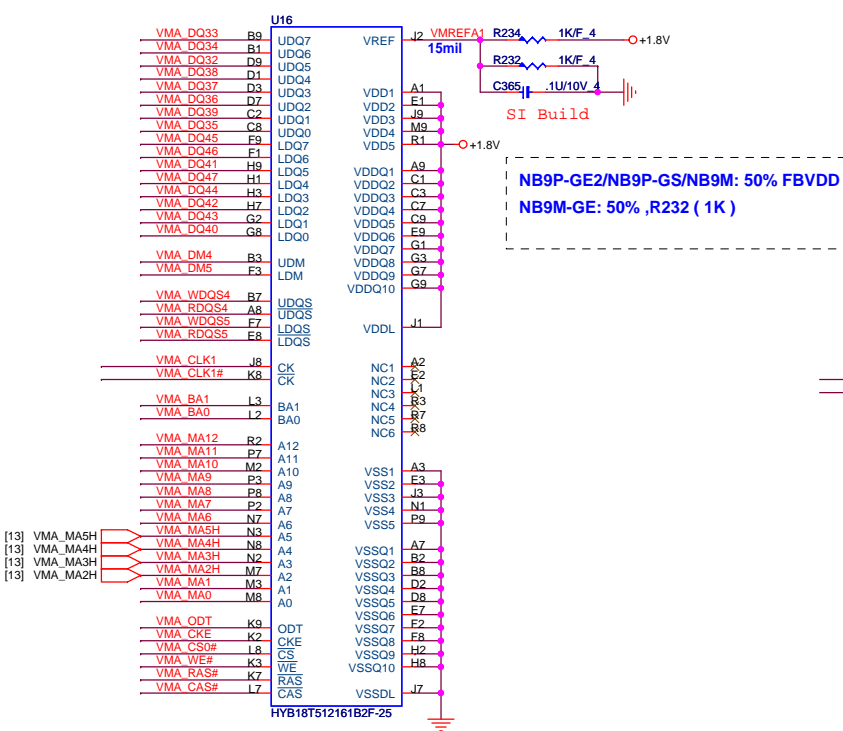




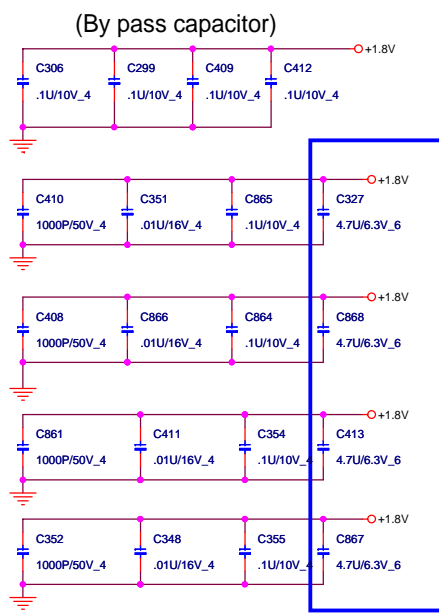
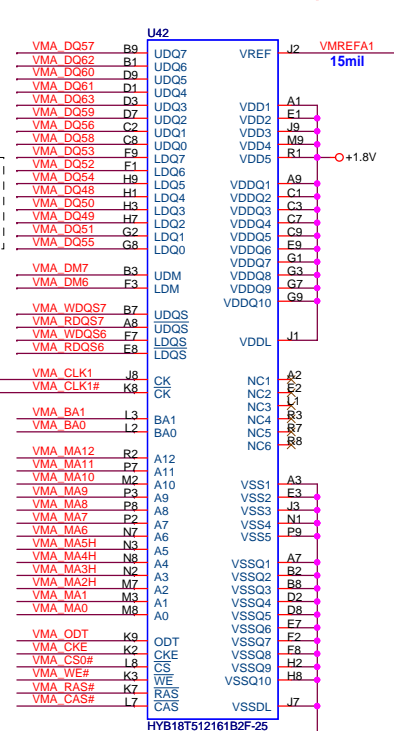
NB9P-GE2/NB9P-GS/NB9M: 50% FBVDD
 NB9M-GE: 50%, R635 (1K)



CS14752FB11 RES CHIP 475 1/16W +-1%(0402)



NB9P-GE2/NB9P-GS/NB9M: 50% FBVDD
 NB9M-GE: 50%, R232 (1K)



(By pass capacitor)

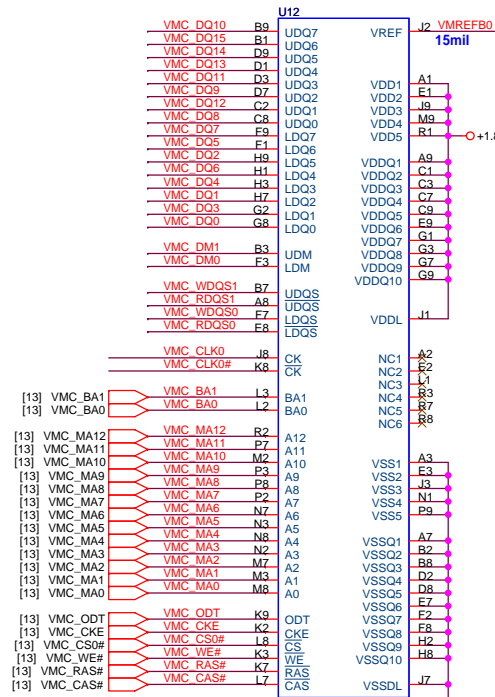
For DB:
 NB9P : AKD59G-T502(Samsung,32M*16)
 NB9M : AKD5FG-TW31(Hynix,32M*16)
 AKD5FG-T*03(Qimonda 32M*16)

- [13] VMA_DQ[63..0]
- [13] VMA_DM[7..0]
- [13] VMA_WDQS[7..0]
- [13] VMA_RDQS[7..0]

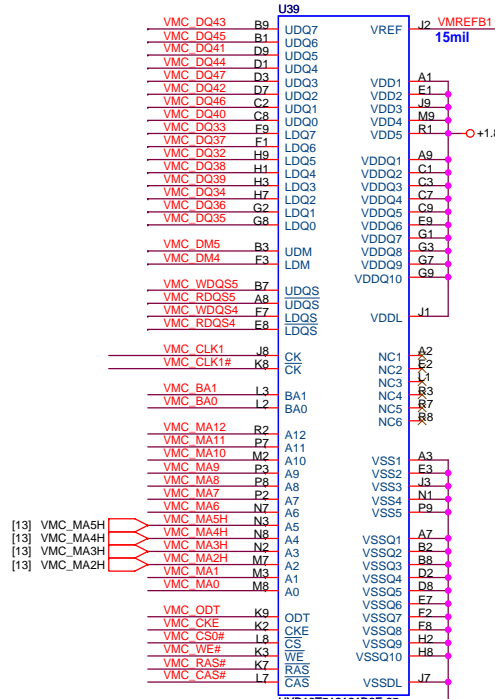
256Mb : AKD5JGAT*05
 512Mb : AKD59G-T*01

PROJECT : QT6
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Size Custom	Document Number NV9X VRAM-1(GDDR2 BGA84)	Rev 1A
Date: Tuesday, February 26, 2008		Sheet 17 of 44



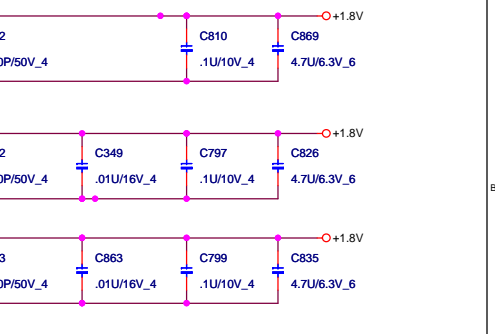
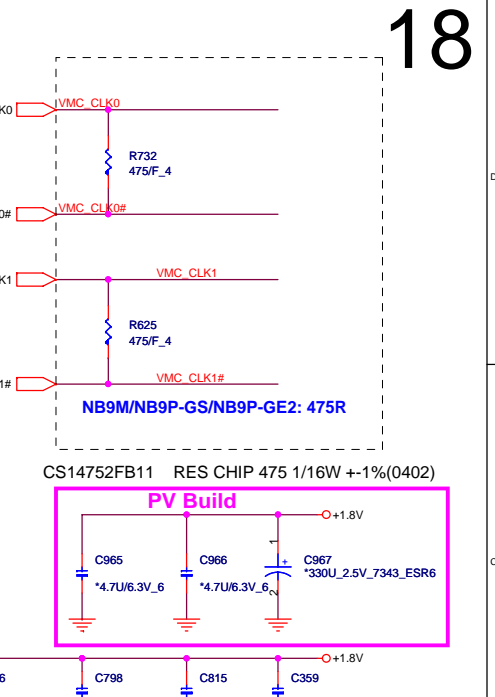
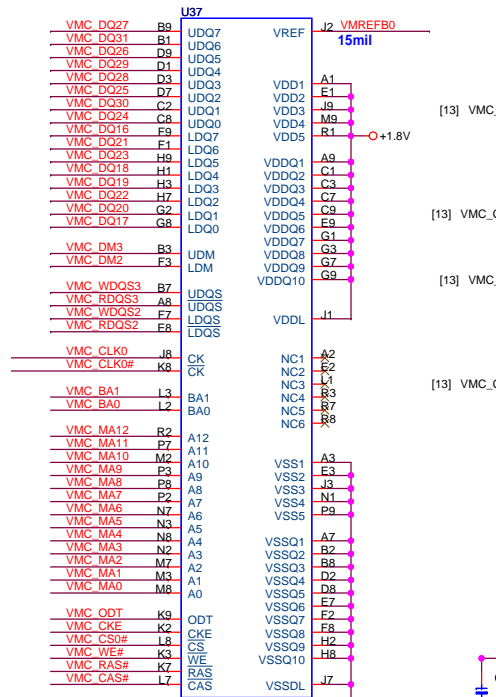
**NB9P-GE2/NB9P-GS/NB9M: 50% FBVDD
NB9M-GE:50% , R133(1K)**



**NB9P-GE2/NB9P-GS/NB9M: 50% FBVDD
NB9M-GE: 50% ,R632 (1K)**

VRAM Vendor

NB9M-GE	1	3
NB9P-GS	2	



- [13] VMC_DQ[63..0]
- [13] VMC_DM[7..0]
- [13] VMC_WDQS[7..0]
- [13] VMC_RDQS[7..0]

SI-2

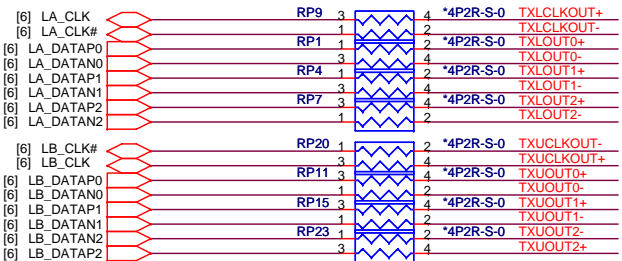
- | | | | |
|---|-------------|---------------------------------------|---------|
| 3 | AKD5FG-T501 | IC SDRAM(84P) K4N51163QG-HC25(FBGA) | Samsung |
| 2 | AKD5FG-T*03 | IC SDRAM(84P)HYB18T512161B2F-25(FBGA) | Qimonda |
| 1 | AKD5FG-TW31 | IC SDRAM(84P) HY5PS121621CFP-25(FBGA) | Hynix |

PROJECT : QT6
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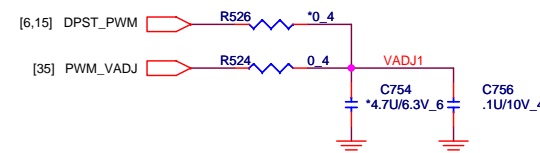
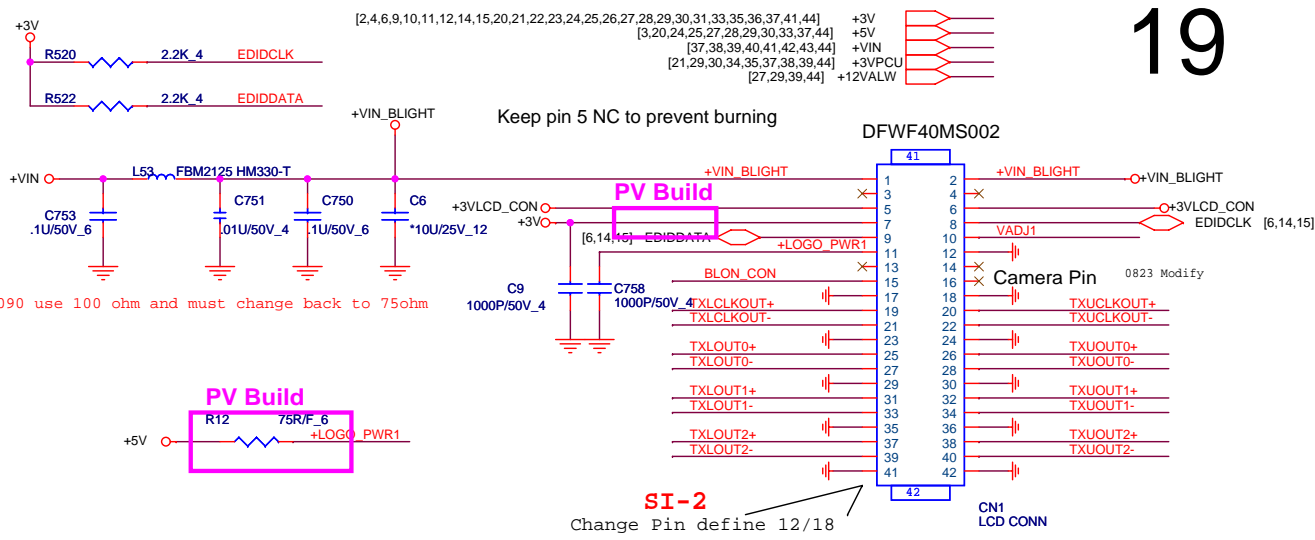
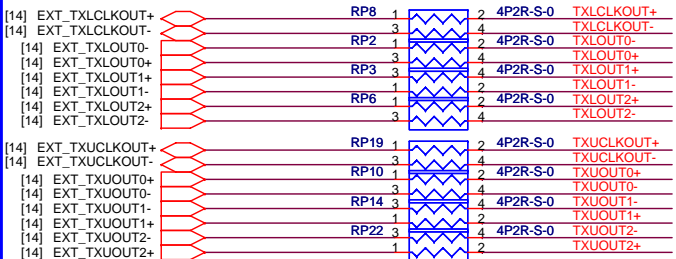
Size Custom	Document Number NV9X VRAM-2(GDDR2 BGA84)	Rev 1A
Date: Tuesday, February 26, 2008		Sheet 18 of 44

- 1. If LCD connector near GPU, then place these series Resistors near GPU
- 2. If LCD connector near N/B, then place these series Resistors near N/B

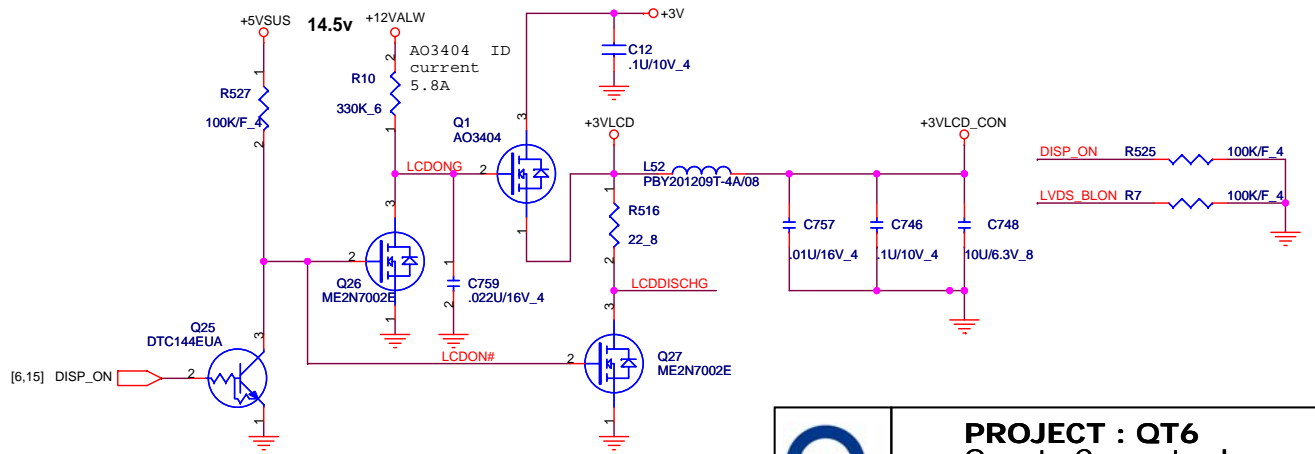
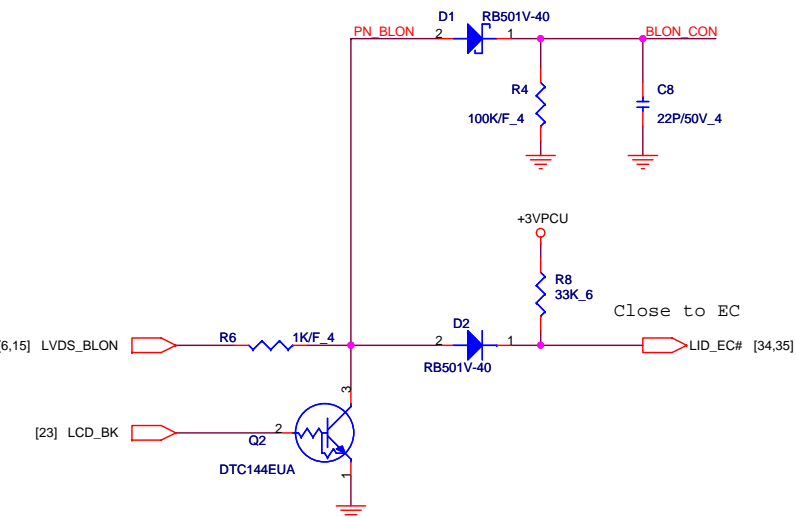
OPTION SIGNAL FROM NB FOR UMA VGA



OPTION SIGNAL FROM Nvidia to VGA

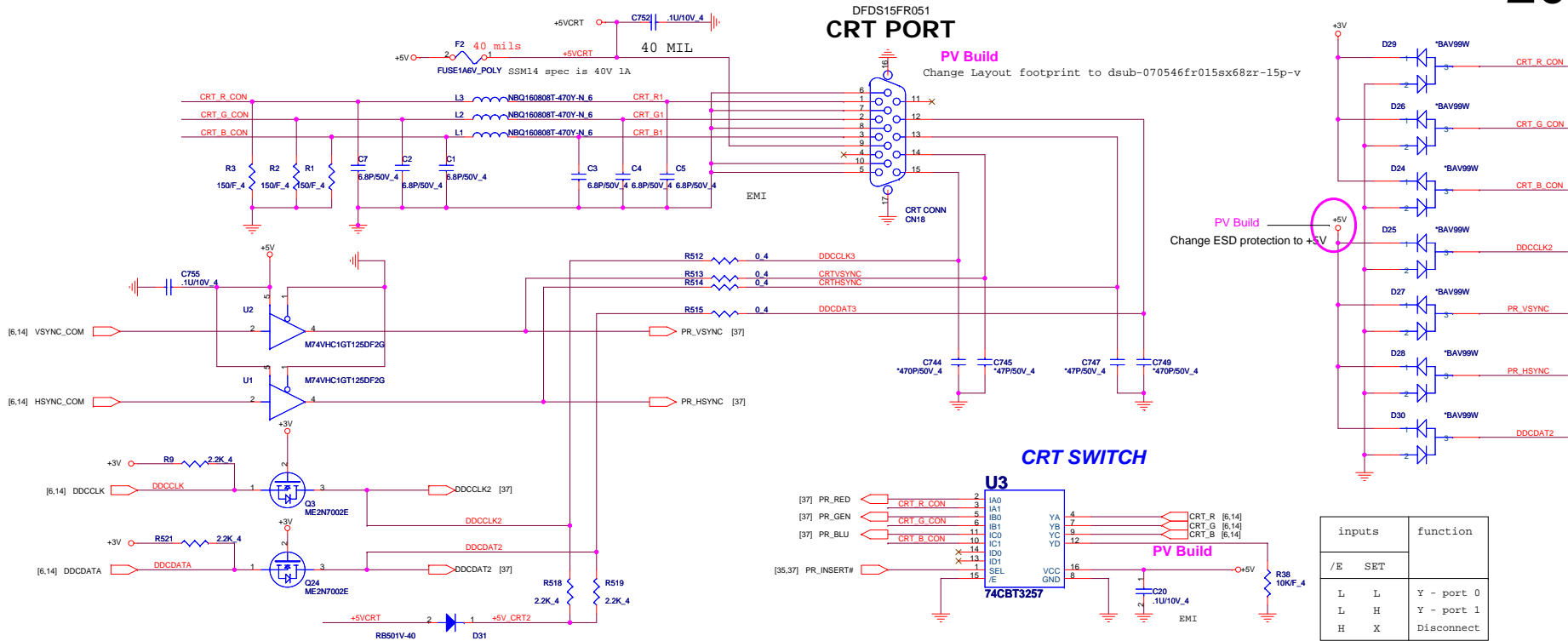


PV Build
Delete CN20,R63,C761(Remove Logo light2)

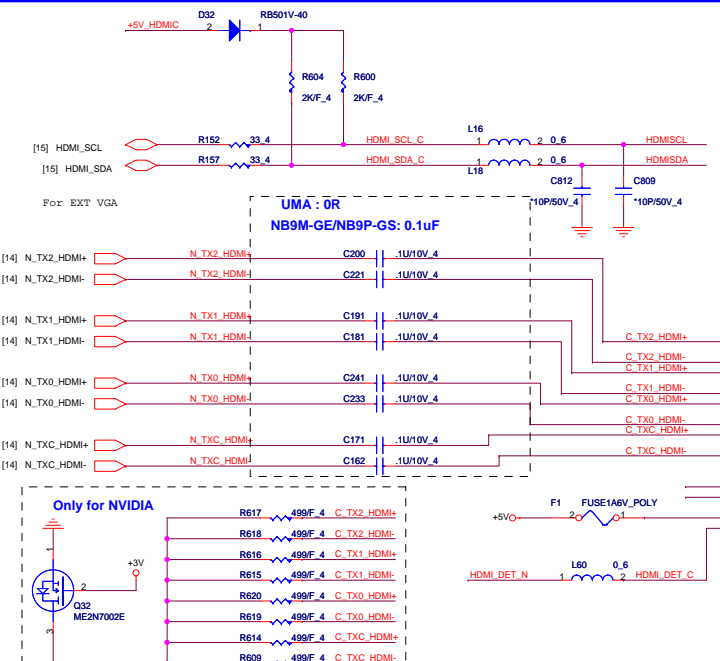
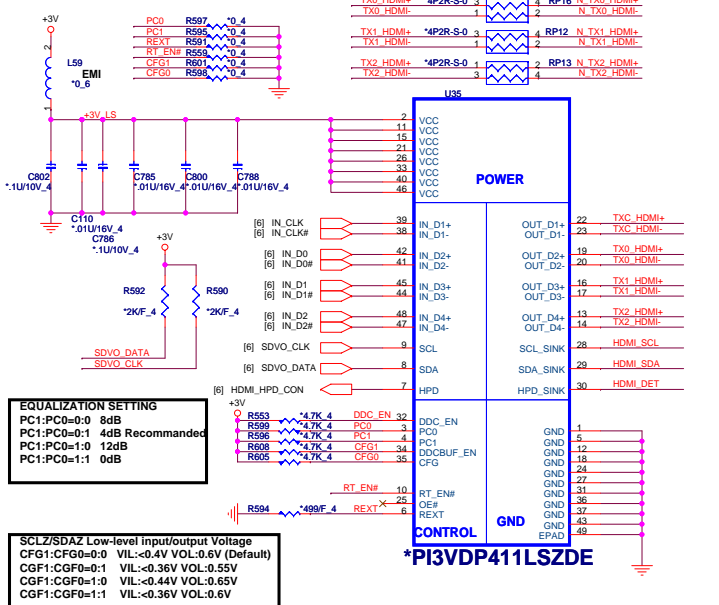


PROJECT : QT6
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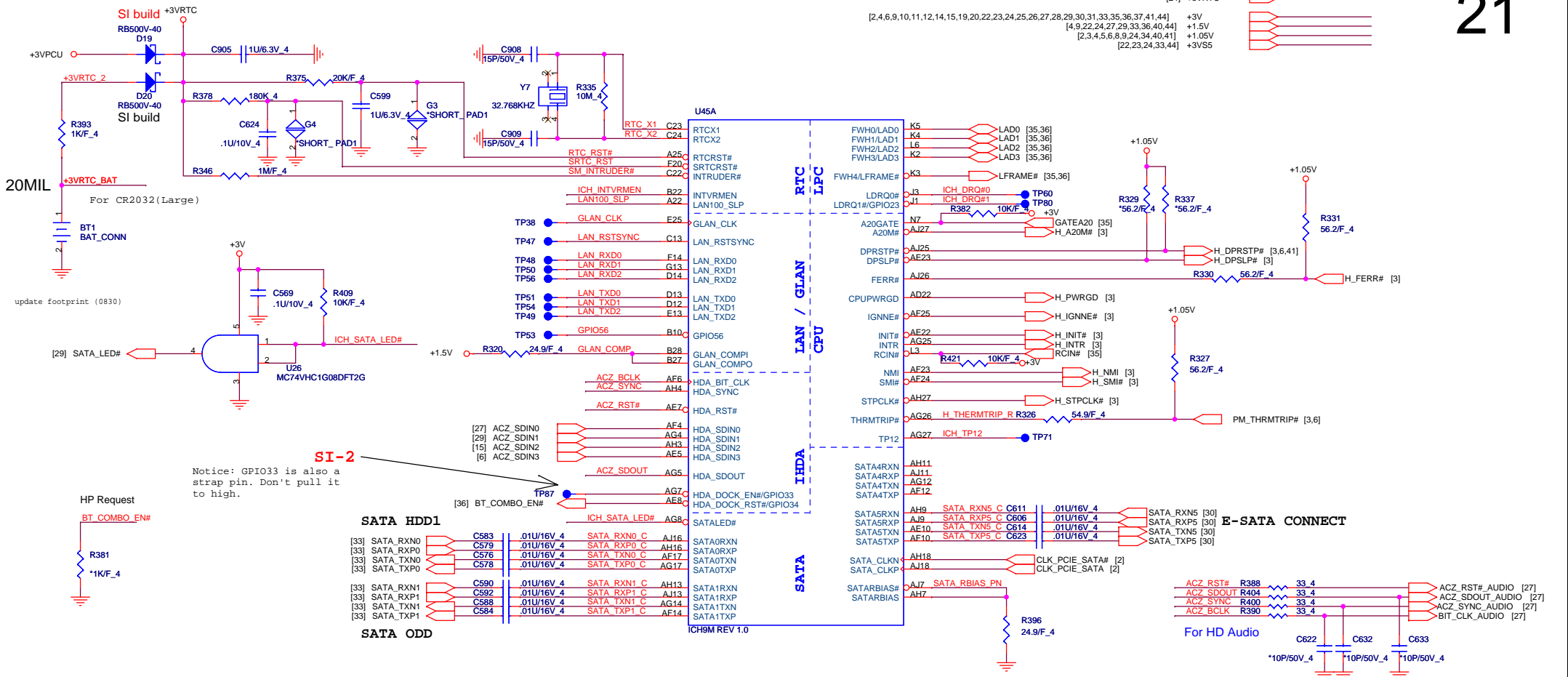
Size B	Document Number LCD CONN/Lid function	Rev 3A
Date: Tuesday, February 26, 2008 Sheet 19 of 44		



For UMA HDMI function



HDMI PORT



20MIL
For CR2032(Large)

update footprint (0830)

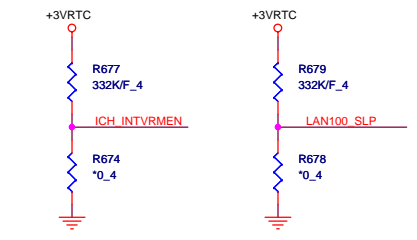
Notice: GPIO33 is also a strap pin. Don't pull it to high.

SB Strap

ICH9-M Internal VR Enable strap
(Internal VR for VccSus1_05, VccSus1_5 and VccCL1_5)

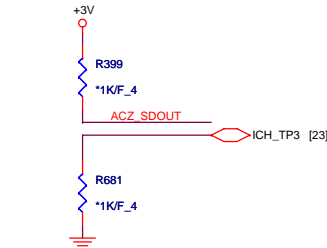
ICH9-M LAN100_SLP Strap
(Internal VR for VccLAN1_05 and VccCL1_05)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)
LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)



XOR Chain Entrance Strap

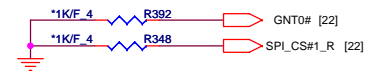
ICH_TP3	HDA_SDOOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIe port config bit 1



ICH9 Boot BIOS select

STRAP	PCI_GNT0#	SPL_CS#1
SPI	0	1
PCI	1	0
LPC	1	1

(default)



A16 swap override strap

PCI_GNT#3	Low = A16 swap override enabled Hi = Default
-----------	---



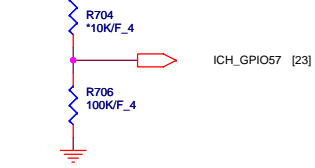
No Reboot Strap

ACZ_SPKR	Low: Default Hi: No reboot
----------	-------------------------------

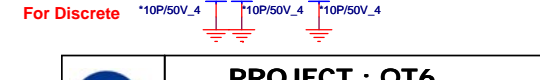
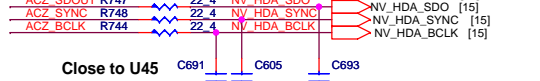
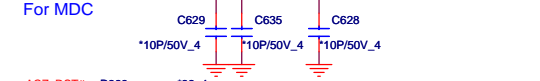
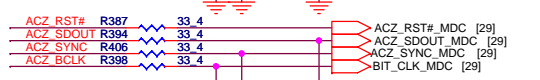


TPM physical presence

ICH_GPIO57	Low: Default
------------	--------------



E-SATA CONNECT



PROJECT : QT6
Quanta Computer Inc.

Size Custom Document Number ICH9-M Host 1/4 Rev 2B

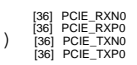
Date: Tuesday, February 26, 2008 Sheet 21 of 44

SWAP PCIE PORT6 TO PORT2 (Lan and New card swap) -->Rename the port name by function and port

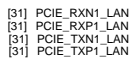
[4,9,21,24,27,29,33,36,40,44] +1.5V
 [2,4,6,9,10,11,12,14,15,19,20,21,23,24,25,26,27,28,29,30,31,33,35,36,37,41,44] +3V
 [23,25,30,36,40,41,42,44] +3VSUS



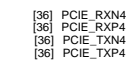
MINI CARD PCI-E(WLAN)



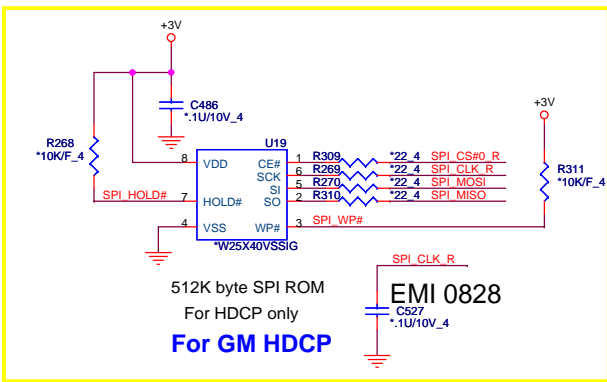
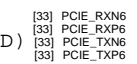
SI-2
PCIE-LAN



TV CARD PCI-E



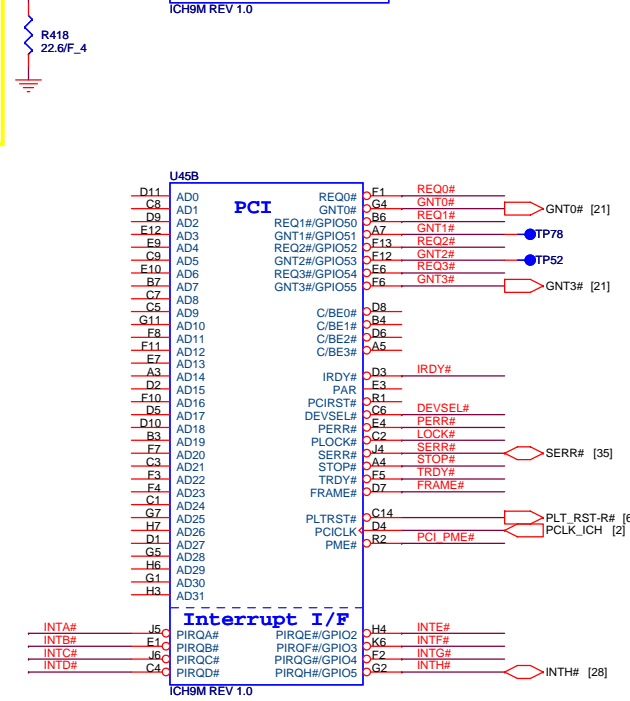
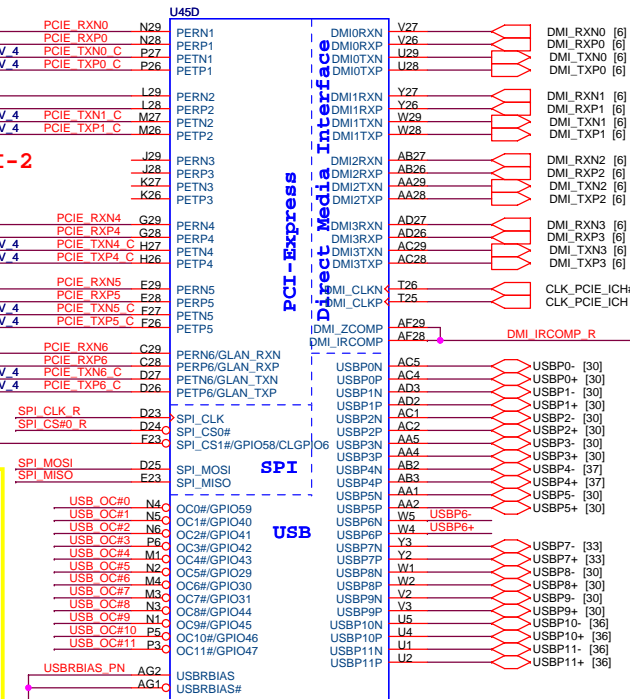
SI-2
EXPRESS CARD (NEW CARD)



512K byte SPI ROM
For HDCP only
For GM HDCP

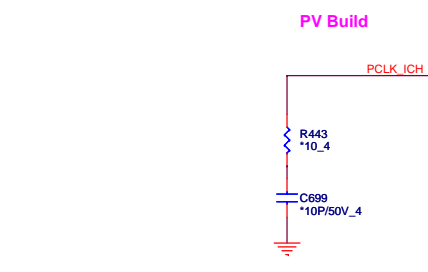
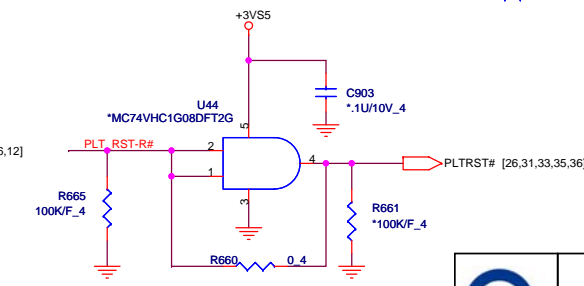
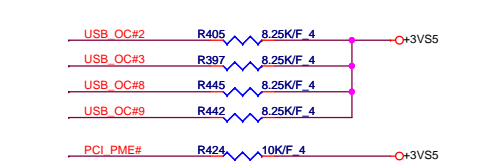
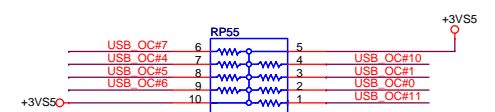
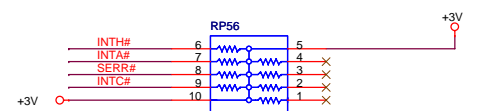
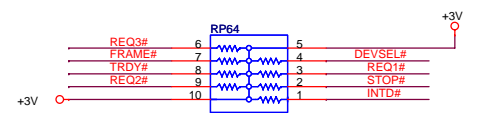
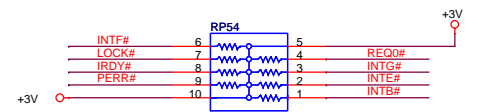
EMI 0828
C527
.1U/10V_4

SPI CLK_R
C527
.1U/10V_4



- USB Connector
- E-SATA and USB Connector
- FINGERPRINT
- Carama USB
- Docking
- BLUETOOTH
- NEW CARD
- USB Connector
- USB Connector
- Robson Min-Card
- TV Min-Card

SI-2
SI-2 Delete
Delete RP53,RP57 and tied from SB to CR(USB6)

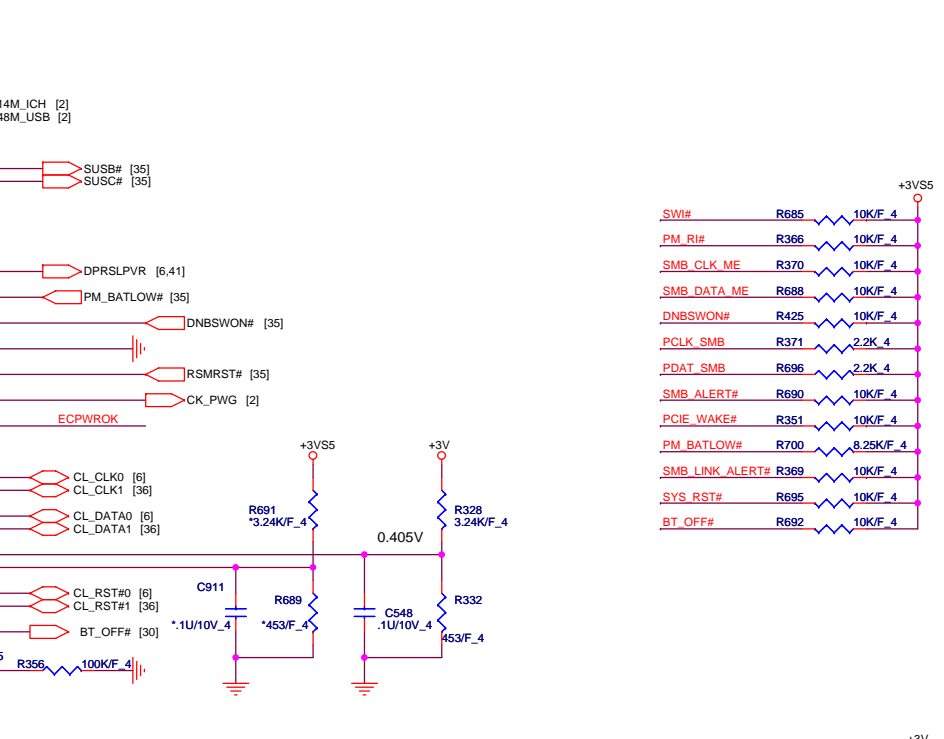
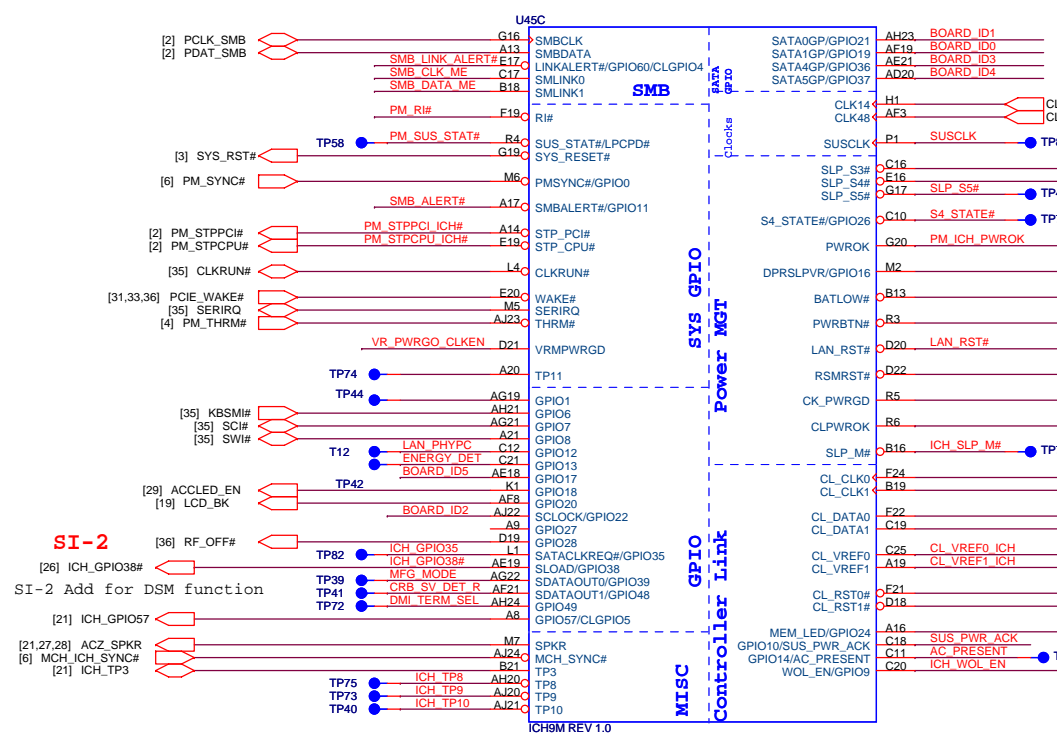


PROJECT : QT6
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Size Custom Document Number ICH9-M PCIE 2/4 Rev 2B

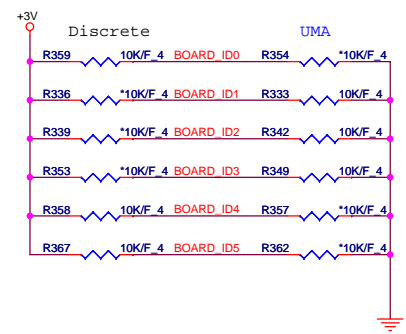
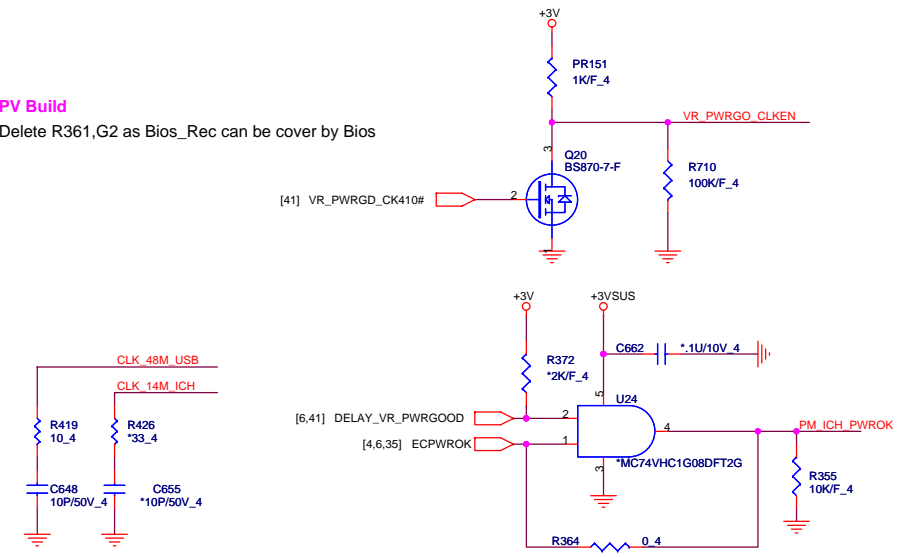
Date: Tuesday, February 26, 2008 Sheet 22 of 44

[4,9,21,22,24,27,29,33,36,40,44] +1.5V
 [2,4,6,9,10,11,12,14,15,19,20,21,22,24,25,26,27,28,29,30,31,33,35,36,37,41,44] +3V
 [21,22,24,33,44] +3VS5
 [25,30,36,40,41,42,44] +3VSUS



PV Build

Delete R361,G2 as Bios_Rec can be cover by Bios

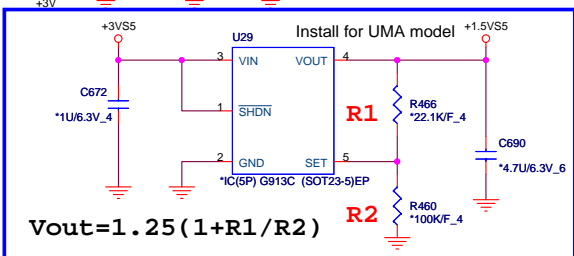
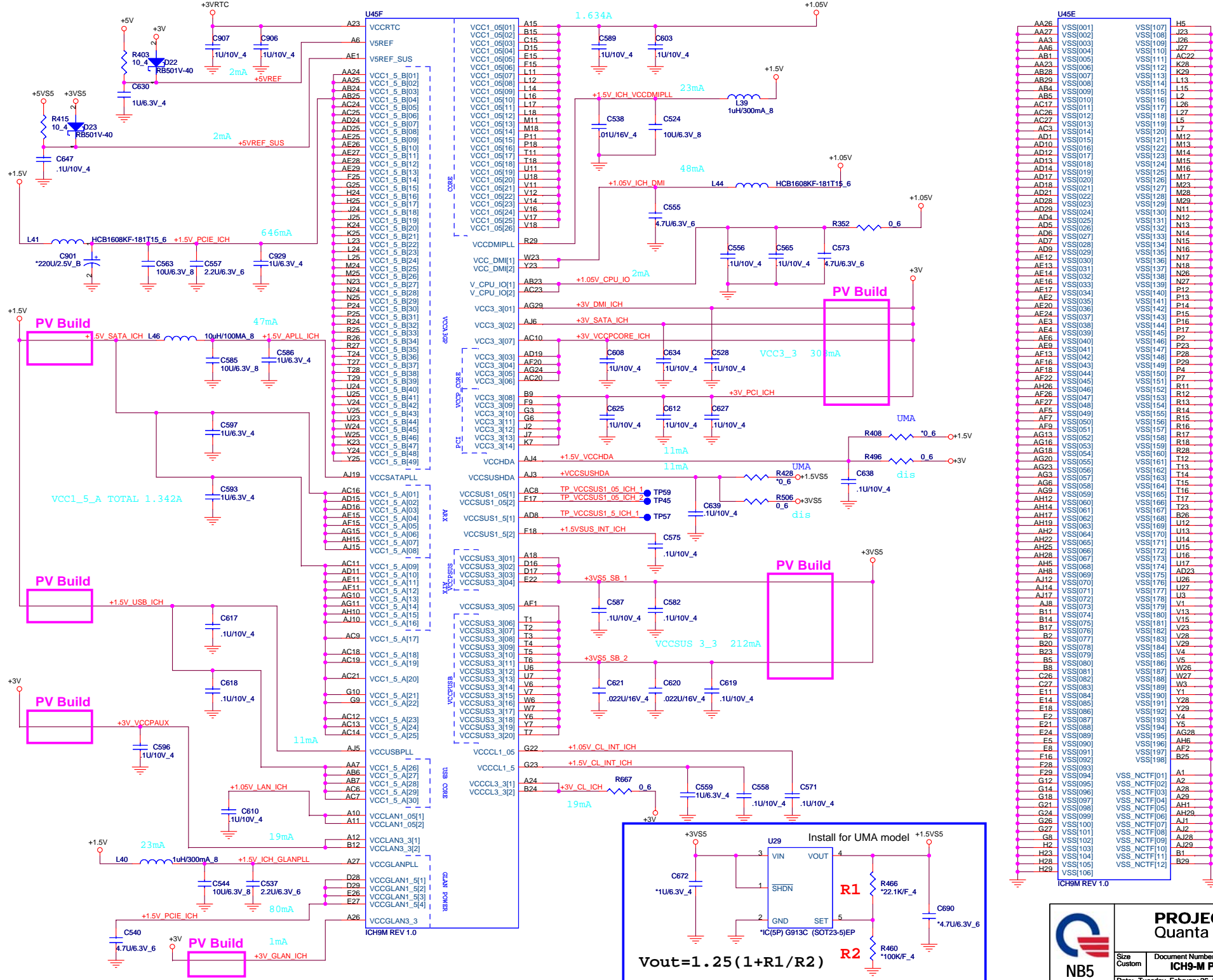


Board ID 0: 1-->Discrete , 0-->UMA
 Board ID 1
 Board ID 2
 Board ID 3
 Board ID 4
 Board ID 5

PROJECT : QT6

Quanta Computer Inc.

Size Custom	Document Number ICH9-M GPIO 3/4	Rev 1A
Date: Tuesday, February 26, 2008 Sheet 23 of 44		



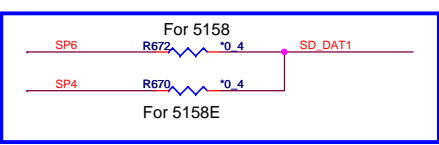
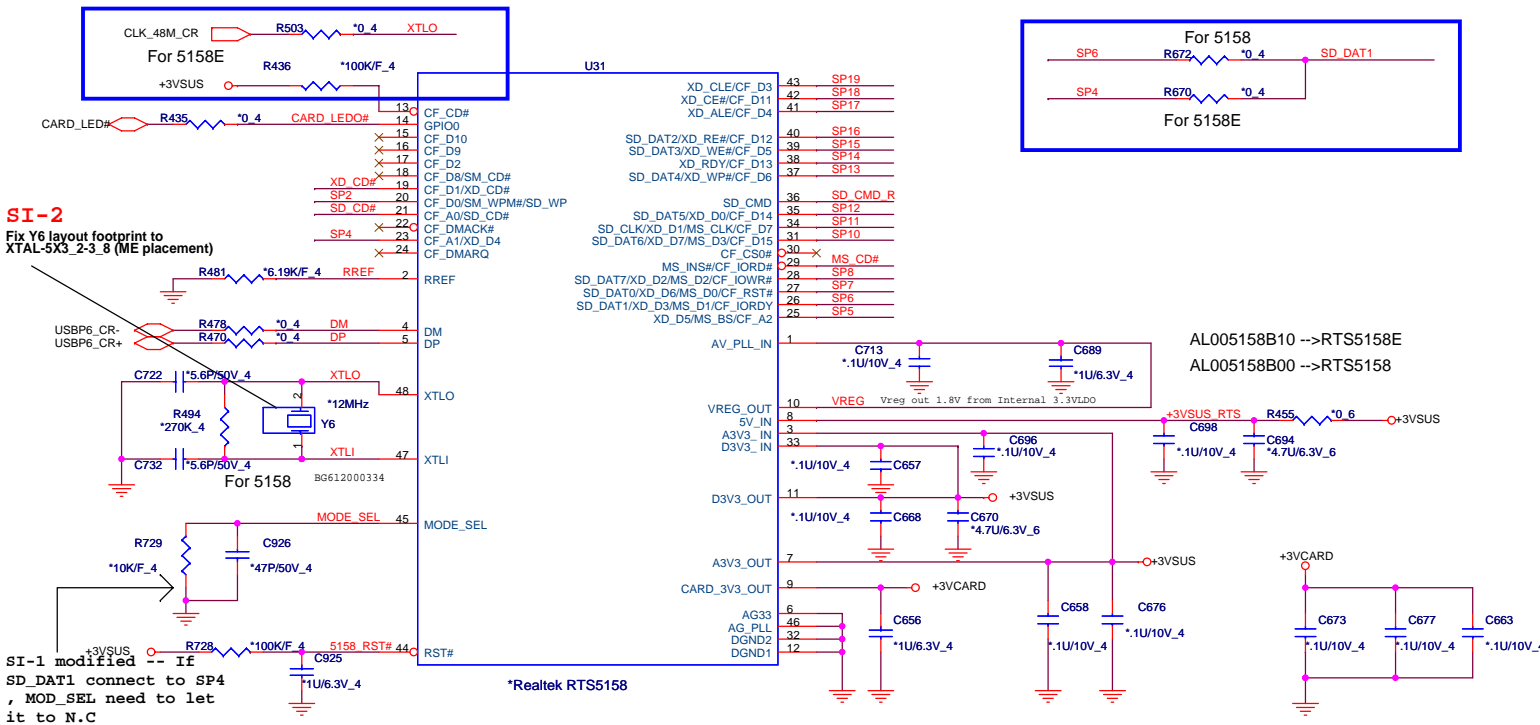
U45E

AA26	VSS1001	VSS107	H5
AA27	VSS1002	VSS108	J23
AA3	VSS1003	VSS109	J26
AA6	VSS1004	VSS110	K22
AB1	VSS1005	VSS111	K28
AA23	VSS1006	VSS112	L12
AB28	VSS1007	VSS113	L13
AB29	VSS1008	VSS114	L15
AB4	VSS1009	VSS115	L2
AC17	VSS1010	VSS116	L26
AC26	VSS1011	VSS117	L27
AC27	VSS1012	VSS118	L5
AC3	VSS1013	VSS119	L7
AD1	VSS1014	VSS120	L12
AD10	VSS1015	VSS121	M12
AD11	VSS1016	VSS122	M13
AD12	VSS1017	VSS123	M14
AD13	VSS1018	VSS124	M15
AD14	VSS1019	VSS125	M16
AD17	VSS1020	VSS126	M17
AD18	VSS1021	VSS127	M23
AD21	VSS1022	VSS128	M28
AD28	VSS1023	VSS129	M29
AD29	VSS1024	VSS130	N11
AD6	VSS1025	VSS131	N12
AD5	VSS1026	VSS132	N13
AD6	VSS1027	VSS133	N14
AD7	VSS1028	VSS134	N15
AD9	VSS1029	VSS135	N16
AE12	VSS1030	VSS136	N17
AE13	VSS1031	VSS137	N18
AE14	VSS1032	VSS138	N26
AE16	VSS1033	VSS139	N27
AE17	VSS1034	VSS140	P12
AE2	VSS1035	VSS141	P13
AE7	VSS1036	VSS142	P14
AE24	VSS1037	VSS143	P15
AE3	VSS1038	VSS144	P16
AE4	VSS1039	VSS145	P17
AE6	VSS1040	VSS146	P2
AE9	VSS1041	VSS147	P23
AF13	VSS1042	VSS148	P28
AF16	VSS1043	VSS149	P29
AF18	VSS1044	VSS150	P7
AF22	VSS1045	VSS151	R11
AH26	VSS1046	VSS152	R12
AF26	VSS1047	VSS153	R13
AF27	VSS1048	VSS154	R14
AF3	VSS1049	VSS155	R15
AF7	VSS1050	VSS156	R16
AF9	VSS1051	VSS157	R17
AG13	VSS1052	VSS158	R18
AG16	VSS1053	VSS159	R28
AG18	VSS1054	VSS160	R29
AG23	VSS1055	VSS161	T13
AG3	VSS1056	VSS162	T14
AG6	VSS1057	VSS163	T15
AG9	VSS1058	VSS164	T16
AH12	VSS1059	VSS165	T17
AH14	VSS1060	VSS166	T23
AH14	VSS1061	VSS167	T27
AH17	VSS1062	VSS168	U1
AH19	VSS1063	VSS169	U2
AH2	VSS1064	VSS170	U14
AH25	VSS1065	VSS171	U15
AH28	VSS1066	VSS172	U16
AH5	VSS1067	VSS173	U17
AH8	VSS1068	VSS174	AD23
AH12	VSS1069	VSS175	U26
AH14	VSS1070	VSS176	U27
AH17	VSS1071	VSS177	U3
AH17	VSS1072	VSS178	U1
AH8	VSS1073	VSS179	V13
B1	VSS1074	VSS180	V15
B17	VSS1075	VSS181	V23
B2	VSS1076	VSS182	V28
B2	VSS1077	VSS183	V29
B23	VSS1078	VSS184	V4
B5	VSS1079	VSS185	V5
B8	VSS1080	VSS186	W26
C26	VSS1081	VSS187	W27
C27	VSS1082	VSS188	W3
E11	VSS1083	VSS189	Y1
E14	VSS1084	VSS190	Y28
E18	VSS1085	VSS191	Y6
E24	VSS1086	VSS192	AC28
E2	VSS1087	VSS193	Y4
E21	VSS1088	VSS194	Y5
E5	VSS1089	VSS195	AH6
E8	VSS1090	VSS196	AF2
F16	VSS1091	VSS197	B25
F28	VSS1092	VSS198	
F29	VSS1093		
G12	VSS1094	VSS_NCTF[01]	A1
G14	VSS1095	VSS_NCTF[02]	A2
G18	VSS1096	VSS_NCTF[03]	A28
G21	VSS1097	VSS_NCTF[04]	A29
G24	VSS1098	VSS_NCTF[05]	AH1
G26	VSS1099	VSS_NCTF[06]	AH29
G27	VSS1100	VSS_NCTF[07]	A1
H2	VSS1101	VSS_NCTF[08]	AJ2
H23	VSS1102	VSS_NCTF[09]	AJ28
H28	VSS1103	VSS_NCTF[10]	AJ29
H29	VSS1104	VSS_NCTF[11]	B1
	VSS1105	VSS_NCTF[12]	B29

IC93M REV 1.0

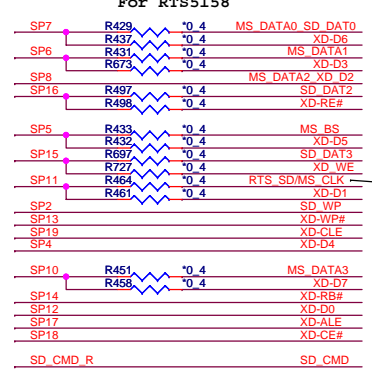


PROJECT : QT6
Quanta Computer Inc.

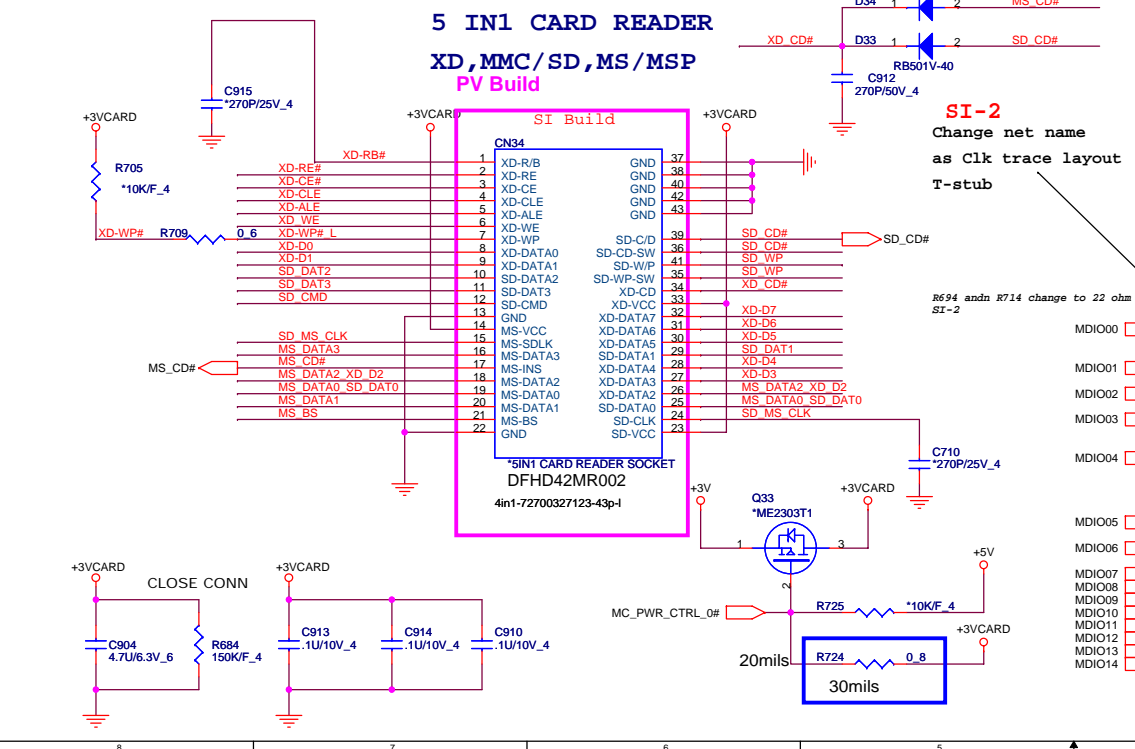


Note:

SD/MMMC	MS	XD
SP0		XD CD#
SP1		XD CD#
SP2	SD_WP	XD CD#
SP3	SD_CD#	
SP4	SD_DAT1	XD D4
SP5	MS_BS	XD D5
SP6	SD_DAT1	MS D1
SP7	SD_DAT0	MS D0
SP8	SD_DAT7	MS D2
SP9	MS_INS#	
SP10	SD_DAT6	MS D3
SP11	SD_CLK	MS SCLK
SP12	SD_DAT5	XD D0
SP13	SD_DAT4	XD WP#
SP14	SD_DAT4	XD R/#
SP15	SD_DAT3	XD WE#
SP16	SD_DAT2	XD RE#
SP17		XD ALE
SP18		XD CE#
SP19		XD CLE



SI-2
Change net name as Clk trace layout T-stub



JMB 380 Note:

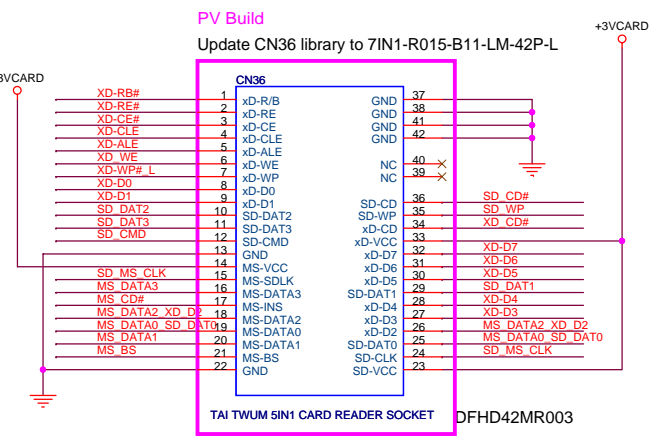
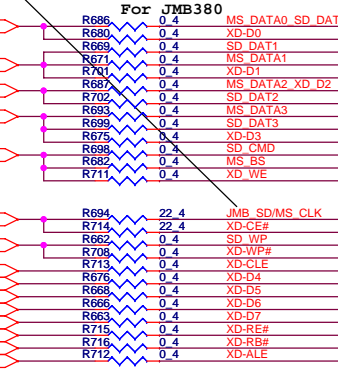
SD/MMMC	MS	XD
MDID0	SD DAT0	MS D0
MDID1	SD DAT1	MS D1
MDID2	SD DAT2	MS D2
MDID3	SD DAT3	MS D3
MDID4	SD CMD	MS BS
MDID5	SD CLK	MS SCLK
MDID6	SD_WP	XD_WP#
MDID7		XD_CLE
MDID8	SD DAT4	XD D4
MDID9	SD DAT5	XD D5
MDID10	SD DAT6	XD D6
MDID11	SD DAT7	XD D7
MDID12		XD RE#
MDID13		XD R/#
MDID14		XD ALE

CR1 LEDV SD1 LED# MS1 LED# XD LED#

CR1 PCTLN SD1 PCTLN# MS1 PCTLN# XD PCTLN#

CR1 CD0 SD1 CD# MS1 CD# XD CD#

CR1 CD1 MS1 CD# XD CD#



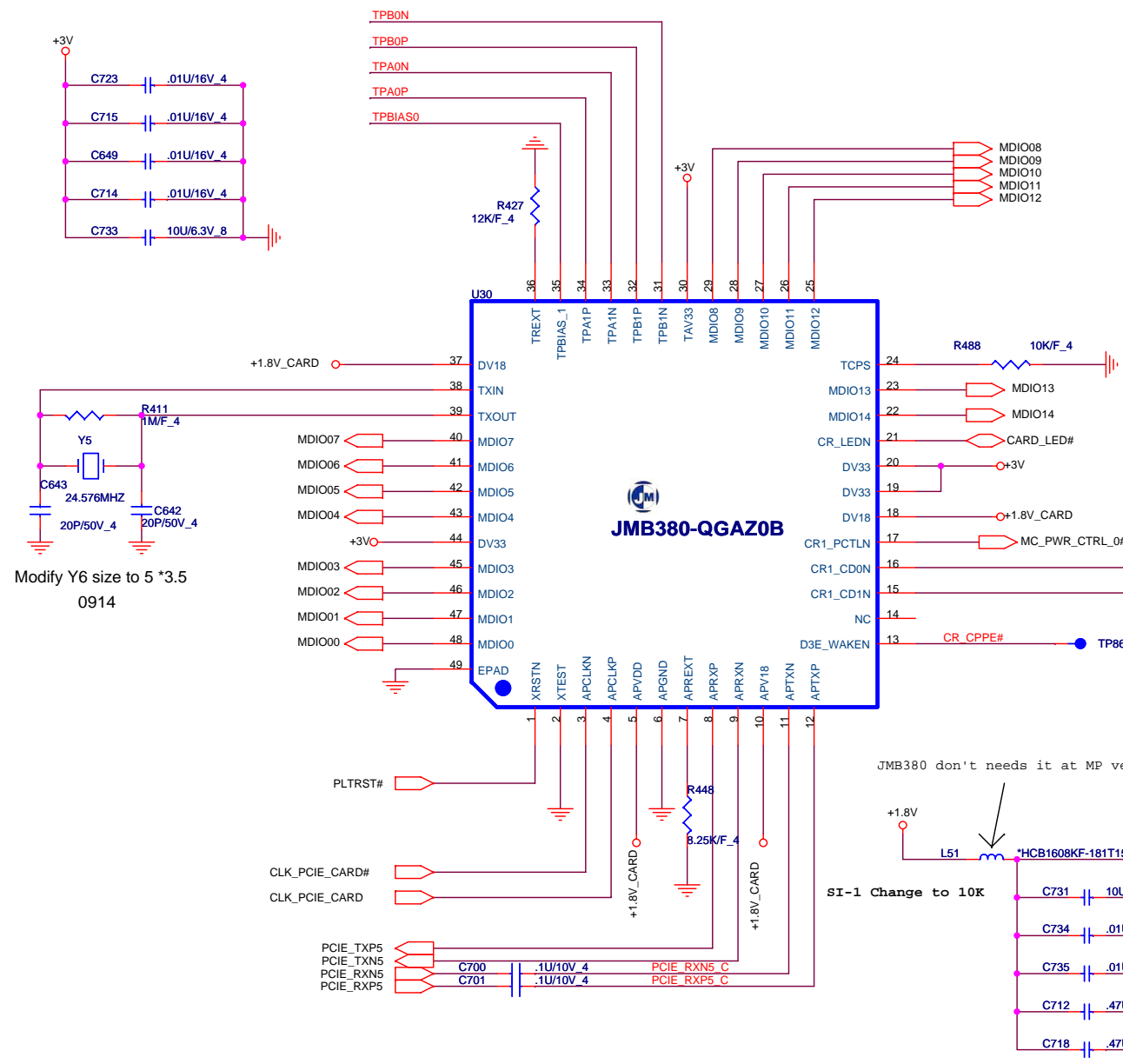
Close to CN34

From JMB380 JMB SD/MS_CLK R707 *0.4 SD MS_CLK

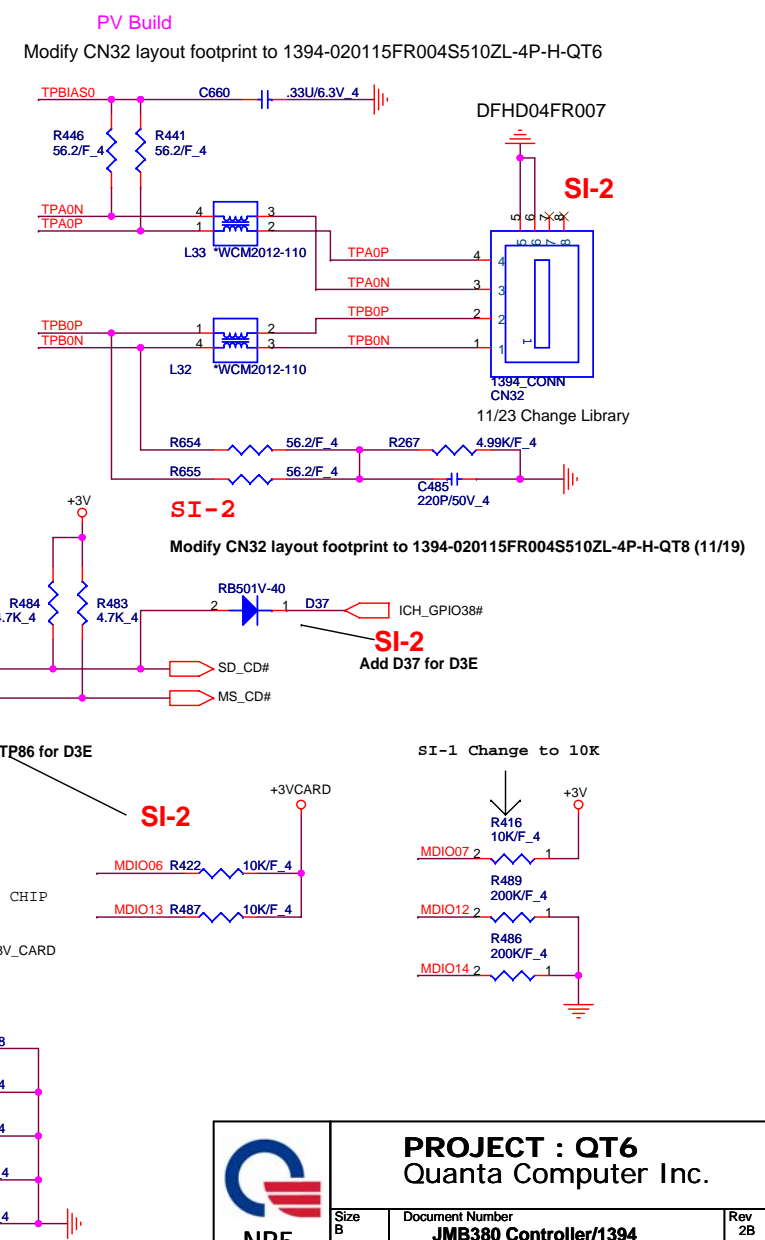
From RTS5158E RTS SD/MS_CLK R717 *0.4 SD MS_CLK

New add R707, R717 for SD/MS CLK trace layout





Modify Y6 size to 5 * 3.5
0914



PV Build
Modify CN32 layout footprint to 1394-020115FR004S510ZL-4P-H-QT8

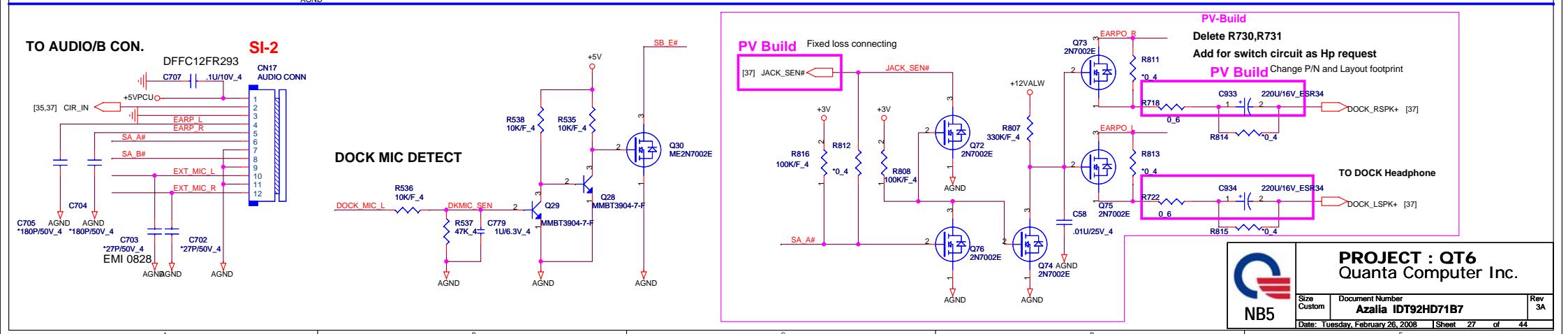
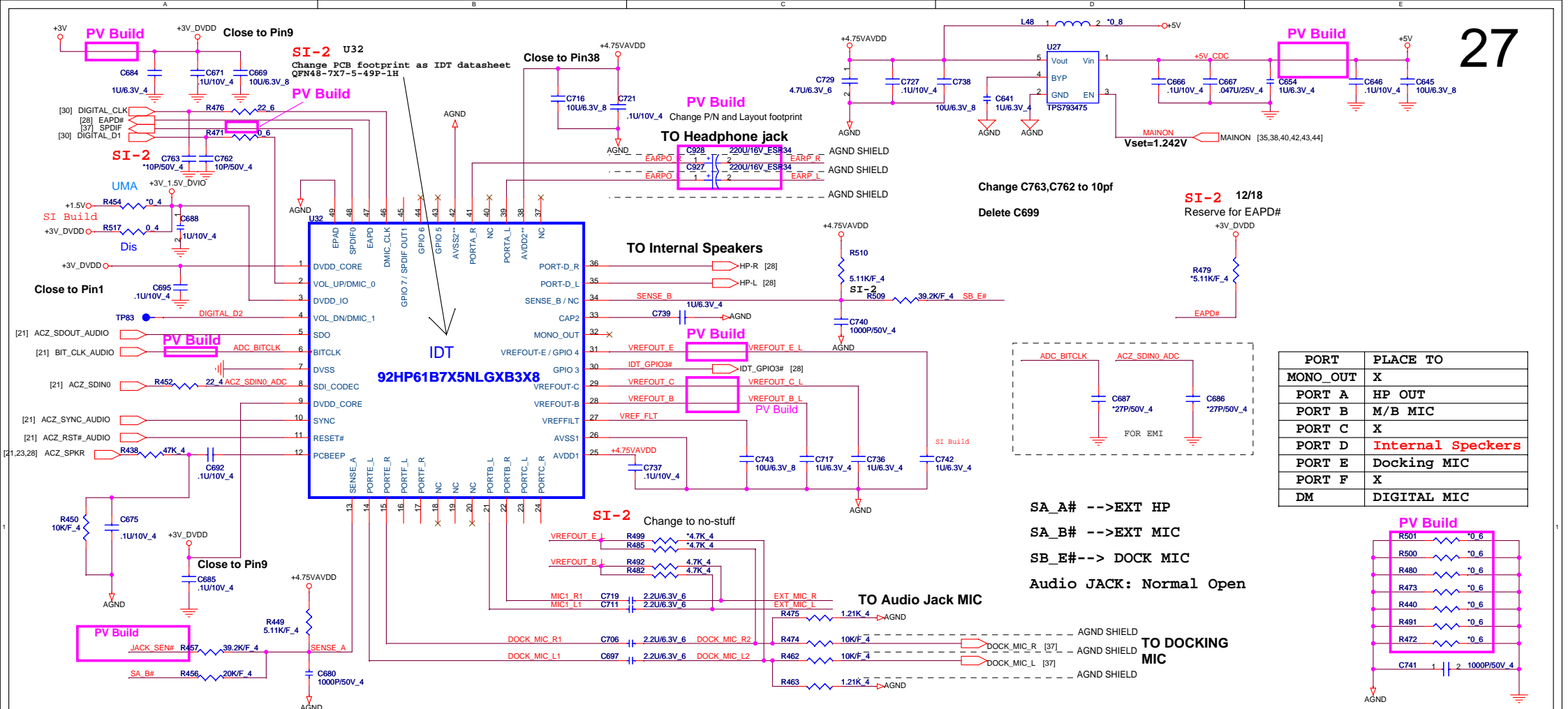
SI-2
Modify CN32 layout footprint to 1394-020115FR004S510ZL-4P-H-QT8 (11/19)

SI-2

SI-1 Change to 10K



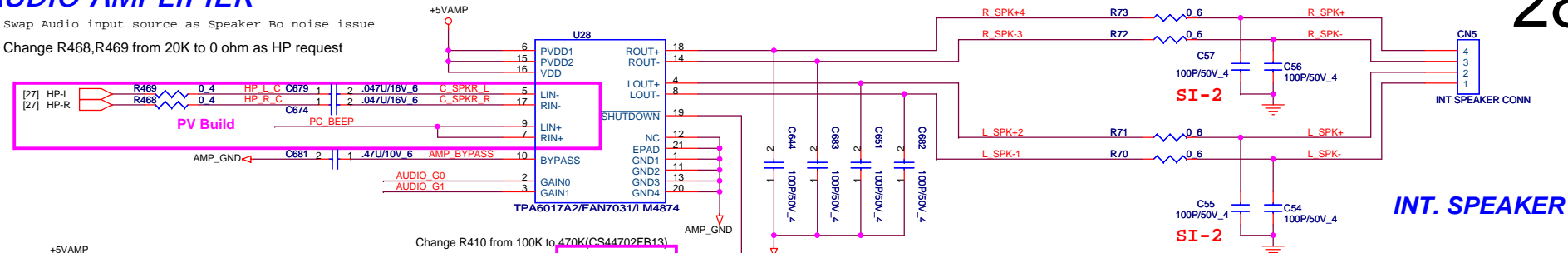
PROJECT : QT6 Quanta Computer Inc.		
Size B	Document Number JMB380 Controller/1394	Rev 2B
Date: Tuesday, February 26, 2008	Sheet 26	of 44



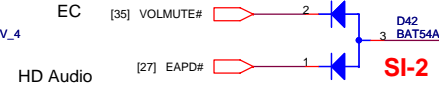
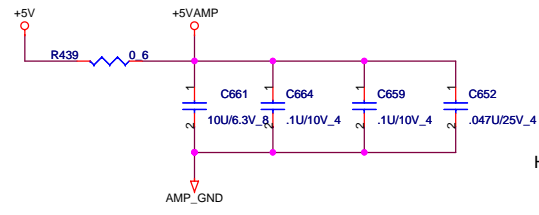
AUDIO AMPLIFIER

Swap Audio input source as Speaker Bo noise issue

Change R468,R469 from 20K to 0 ohm as HP request



Change R410 from 100K to 470K(CS44702ER13)



- AL001431K04
- AL6017A2K12
- APA2031 ,AL002031K00

6017A2 Gain Table

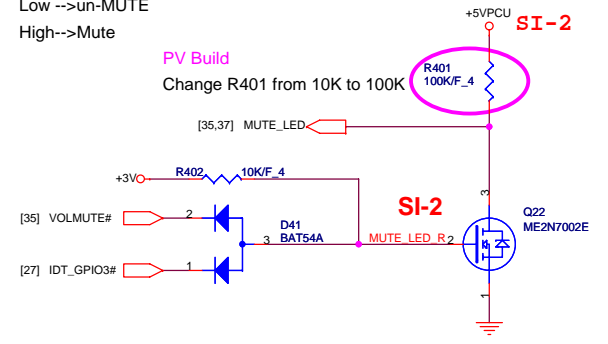
GAIN0	GAIN1	AV	RIN
0	0	6dB	90K
0	1	10dB	70K
1	0	15.6dB	45K
1	1	21.6dB	25K

MUTE_LED

Low --> un-MUTE

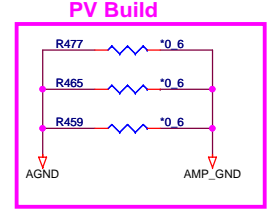
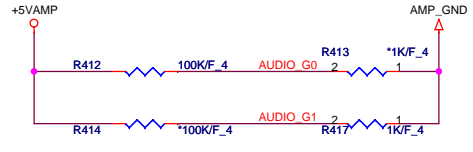
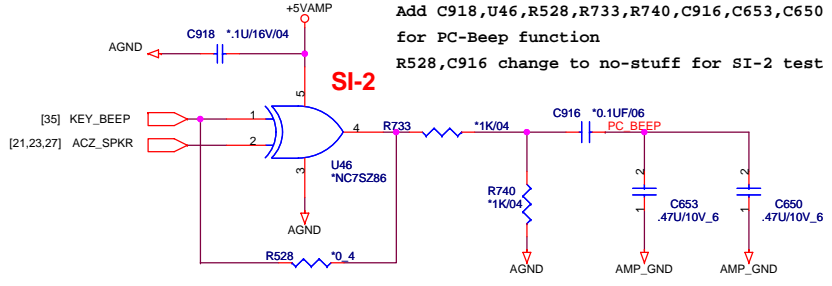
High --> Mute

Change Power source to +5VPCU as power situation

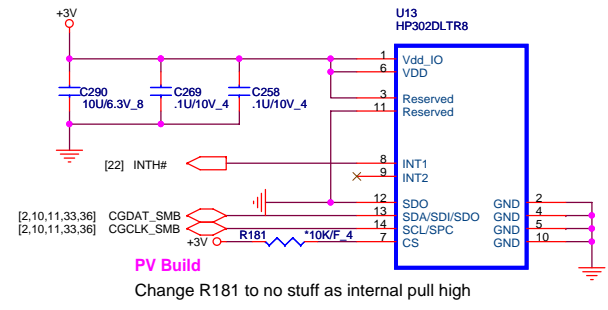


Add in SI-2

Add C918,U46,R528,R733,R740,C916,C653,C650 for PC-BEEP function
R528,C916 change to no-stuff for SI-2 test -->12/6

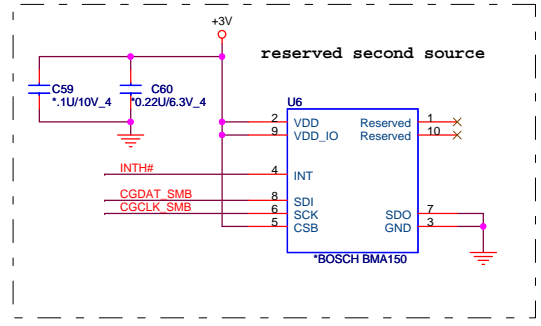


Accelerometer Sensor



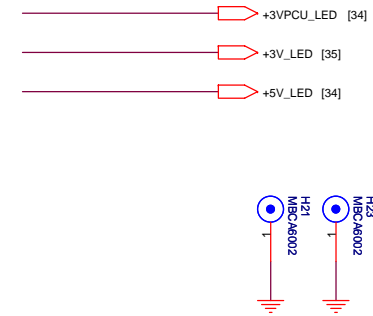
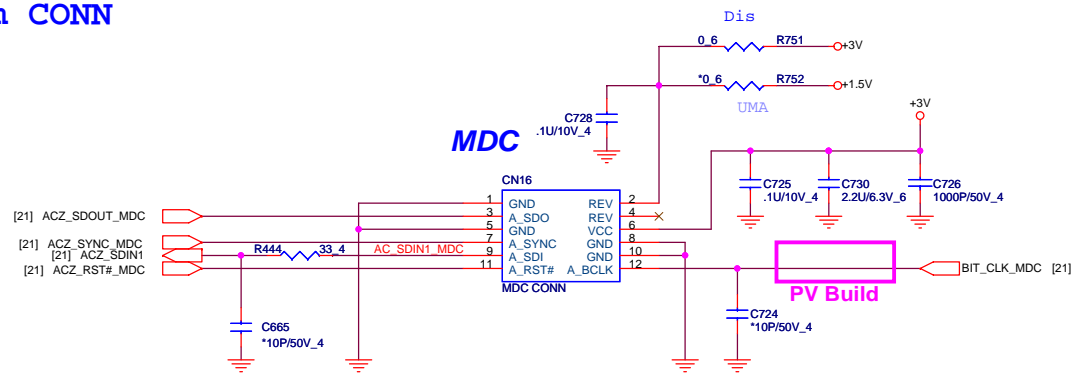
Change R181 to no stuff as internal pull high

Pin 12: Low 38hex
Pin 12: unconnected/floating 3Ahex



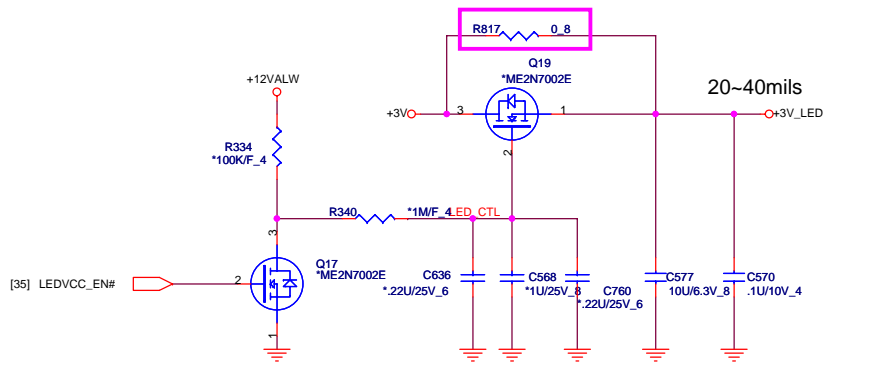
PROJECT : QT6
Quanta Computer Inc.

Size Custom	Document Number AMP_TPA6017/Accelerometer	Rev 3A
Date: Tuesday, February 26, 2008		Sheet 28 of 44

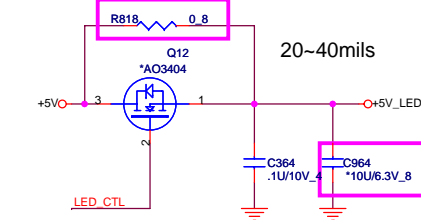


Needs to change Library as ME request

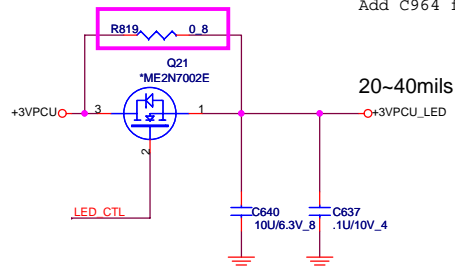
LED PWR CONTROL



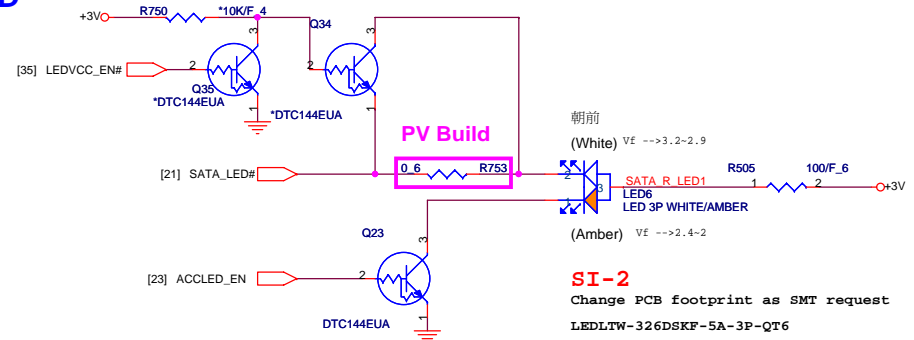
Change Q12 to AO3404 as LED current limited



PV Build
Add R817,R818,R819 as HP LED spec change
Add C964 for reserve



LED

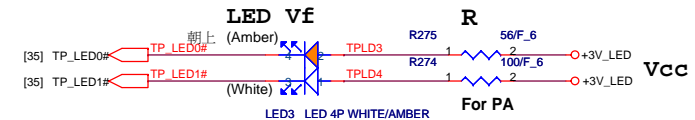
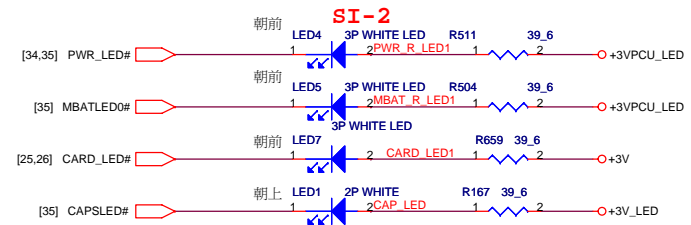


朝前 (White) Vf -->3.2~2.9
朝前 (Amber) Vf -->2.4~2

SI-2

Change PCB footprint as SMT request
LEDLTW-326DSKF-5A-3P-QT6
Swap pin , Pin 2 and Pin as Library pin

Modify LED4,LED5,LED7 layout footprint to ledl-s110kgct-3p-qt6 (11/19)



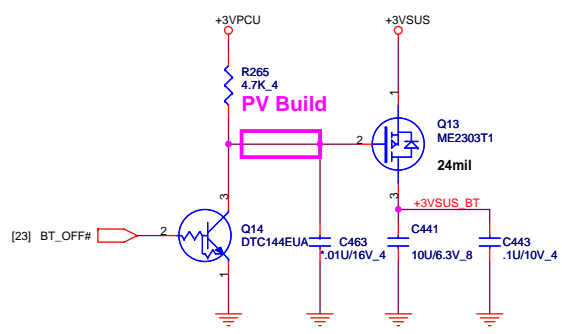
$$I = \frac{V_{cc} - V_f}{R}$$



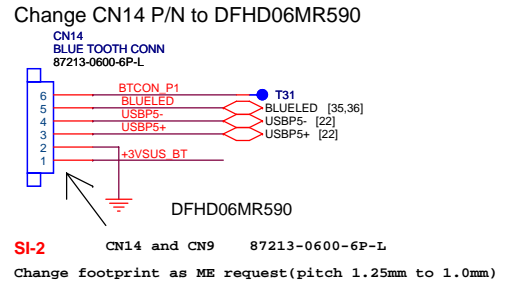
PROJECT : QT6
Quanta Computer Inc.

Size Custom	Document Number MDC/LED	Rev 3A
Date: Tuesday, February 26, 2008 Sheet 29 of 44		

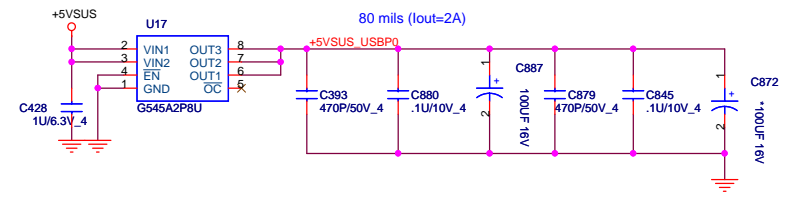
BLUETOOTH



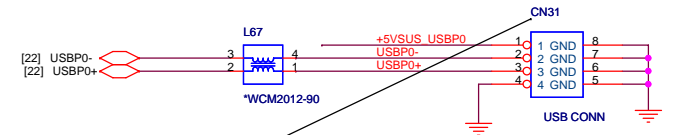
PV Build



LEFT SIDE USBX1 and E-SATA/USB COMBO 30

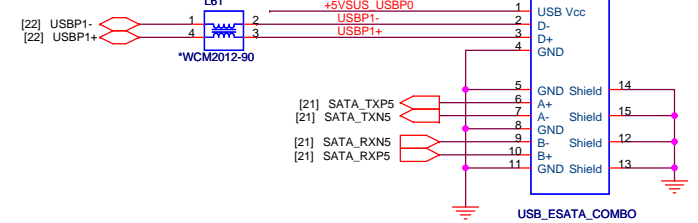


USB 0



SI-2 CN30, CN31
Change Connector layout type from SMD_PAD to Dip as SMT request

USB & ESATA

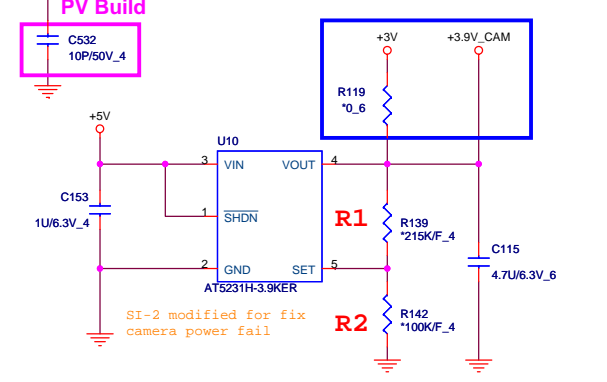
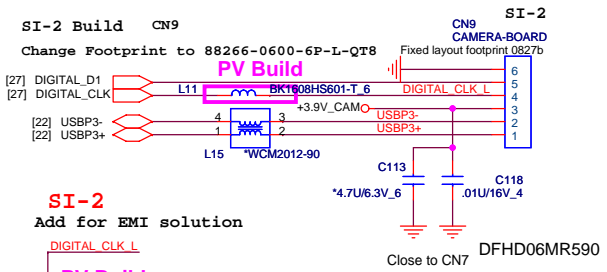


USB-C-2006102-11P-H-QT6

Touch Screen

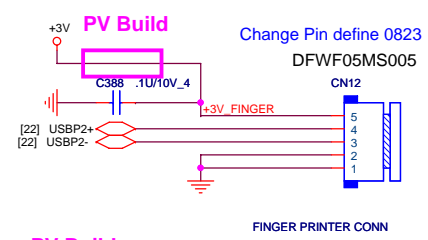
Delete Touch-Screen in SI-2
CN2, C10, L4
SI-2 Build

USB CAMERA /DIGITAL MIC CONNECT



$$V_{out} = 1.25(1 + R1/R2)$$

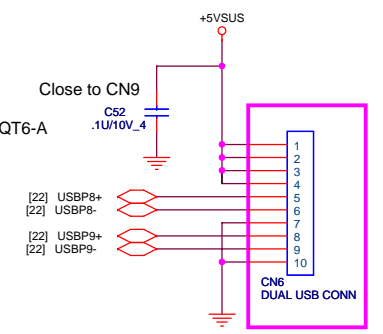
USB fingerprint CON



PV Build
Change CN12 to BL123-05R-5P-L-QT6-A

1. ESD GND
2. SYSTEM GND
3. USB-
4. USB+
5. USB PWR(+3V)

RIGHT SIDE USBX2

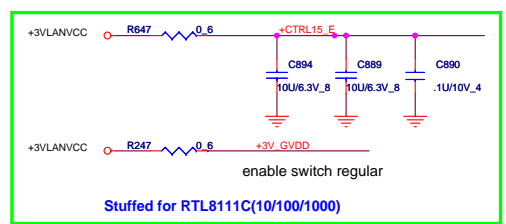
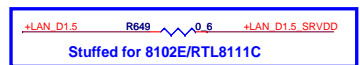


	PROJECT : QT6 Quanta Computer Inc.	
	Size Custom	Document Number BTWC/FT/TS/ESATA/USB
Date: Tuesday, February 26, 2008 Sheet 30 of 44		

T : Stuffed for RTL8111C(10/100/1000)

E : Stuffed for 8101E/8102E(10/100)

For 8102E/8111C



31

SI-2 8102E No Mount
8111C No Mount ,R247 mount

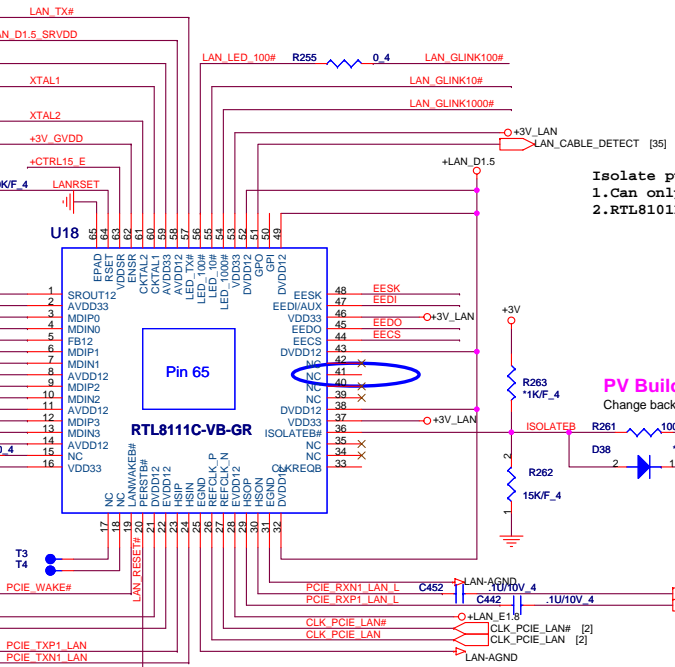
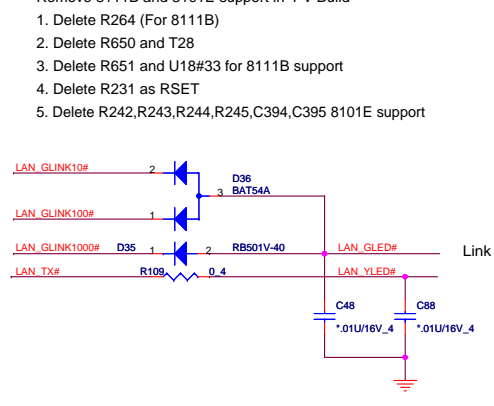
U18#63 wider than 40 mils
U18#1 wider than 60 mils

C531 SI-2
New add and Close to Pin 5
From Vendor EMI suggest

SI-2 R434
8111C = No Mount
8102E = Mount

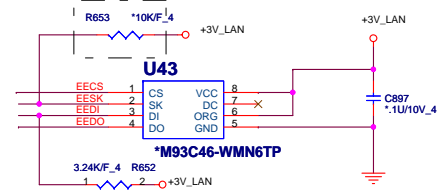
SI-2
Swap PCIE from Port 6 to PCIE Port 2

- PV Build**
- Remove 8111B and 8101E support in PV Build
 - Delete R264 (For 8111B)
 - Delete R650 and T28
 - Delete R651 and U18#33 for 8111B support
 - Delete R231 as RSET
 - Delete R242,R243,R244,R245,C394,C395 8101E support



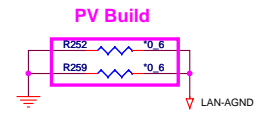
Isolate pull low:
1.Can only disable RTL8111C.
2.RTL8101E can't disable

for 93C56 used. NC if 93C46 is used.



PV Build
Change back to R261 at 1/24

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

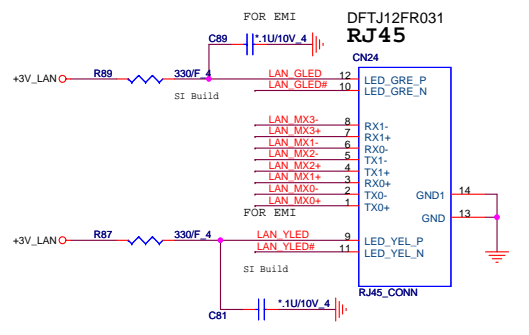
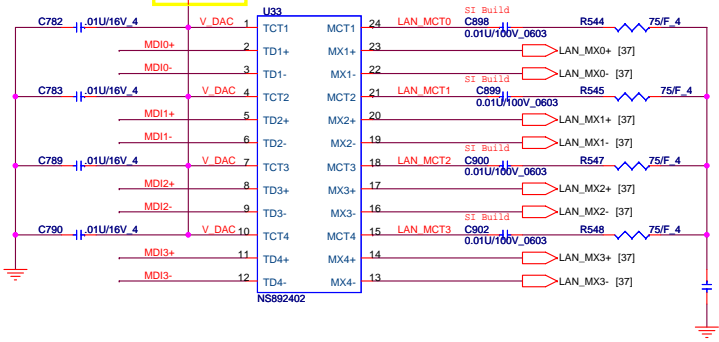


SI-2
Swap PCIE from Port 6 to PCIE Port 1

AL08111C001 IC CTRL(64P) RTL8111C-VB-GR(QFN)
AL08102E001 IC CTRL(64P) RTL8102E-VB-GR(QFN)

Stuffed for RTL8101E

Add C898,C899,C900,C902 as HP request



NS892402:GIGABIT DB0AT9LAN05
NS892405:10/100 DB0ZB1LAN04

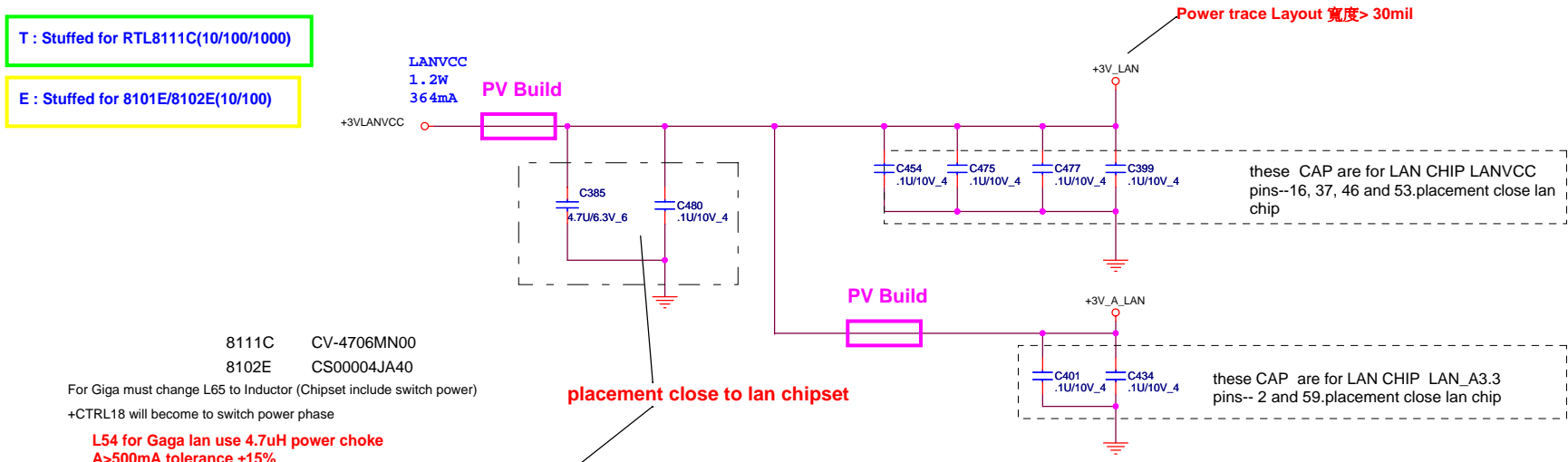
PROJECT : QT6
Quanta Computer Inc.

Size Custom Document Number **RTL8111C/8101E/RJ45** Rev 2B

Date: Tuesday, February 26, 2008 Sheet 31 of 44

T : Stuffed for RTL8111C(10/100/1000)

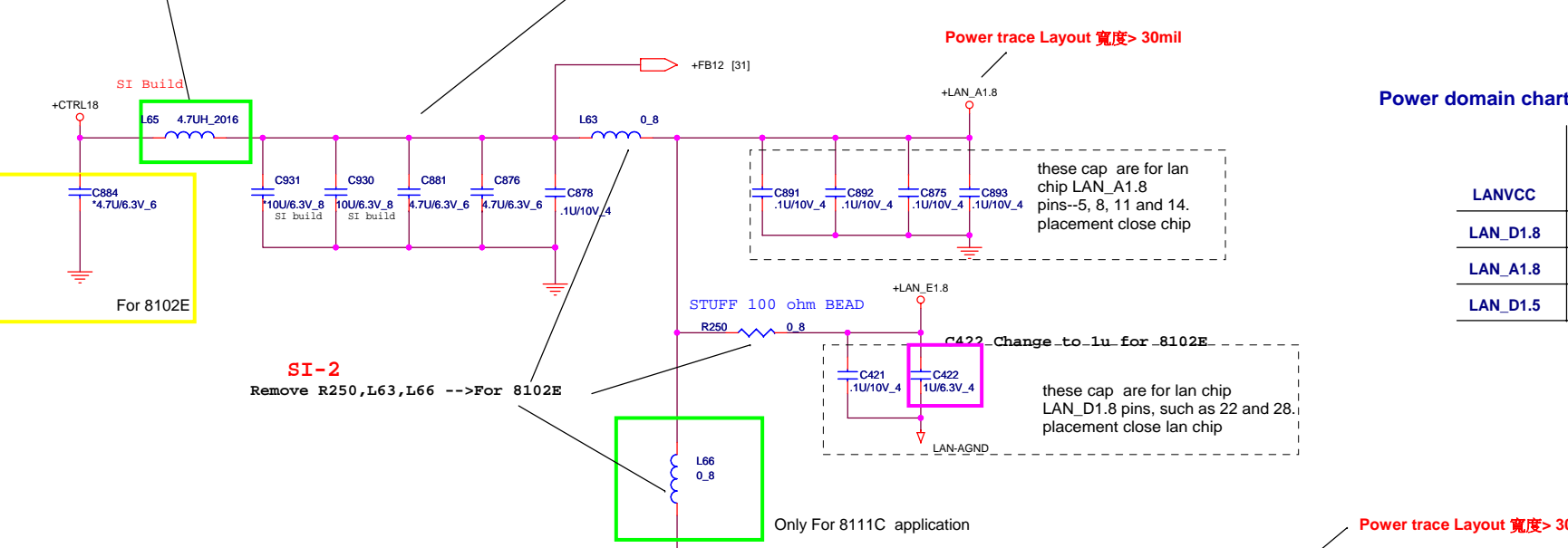
E : Stuffed for 8101E/8102E(10/100)



8111C CV-4706MN00
8102E CS00004JA40

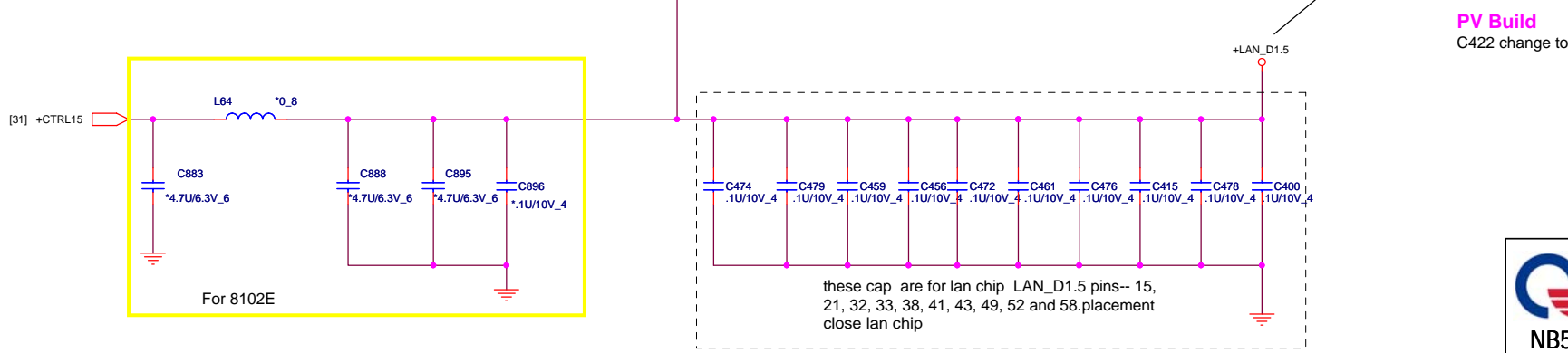
For Giga must change L65 to Inductor (Chipset include switch power)
+CTRL18 will become to switch power phase

**L54 for Giga lan use 4.7uH power choke
A>500mA tolerance ±15%**



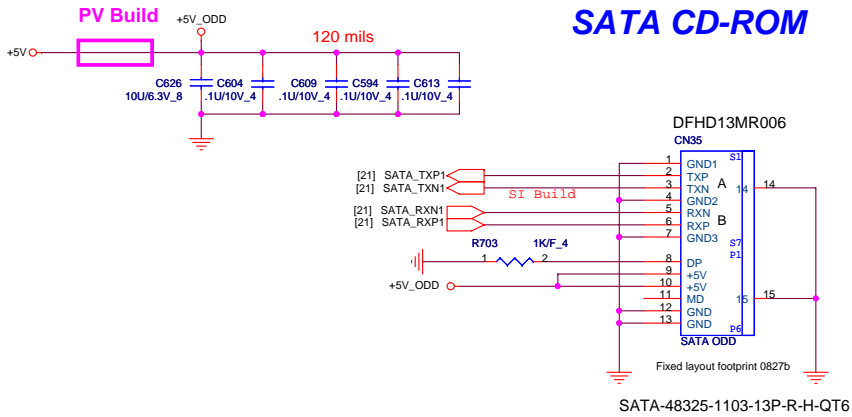
Power domain chart

	RTL8111C(P) RTL8102E
LANVCC	3.3V
LAN_D1.8	1.2V
LAN_A1.8	1.2V
LAN_D1.5	1.2V

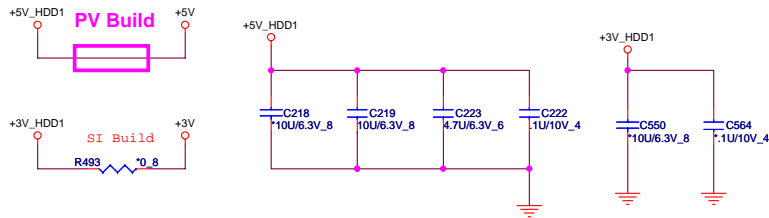
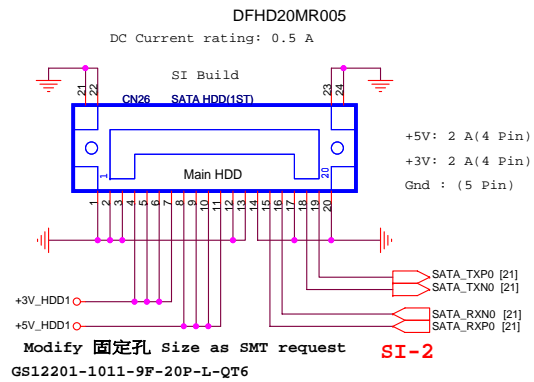


PROJECT : QT6
Quanta Computer Inc.

Size A3	Document Number LAN Power	Rev 1A
Date: Tuesday, February 26, 2008	Sheet 32 of 44	

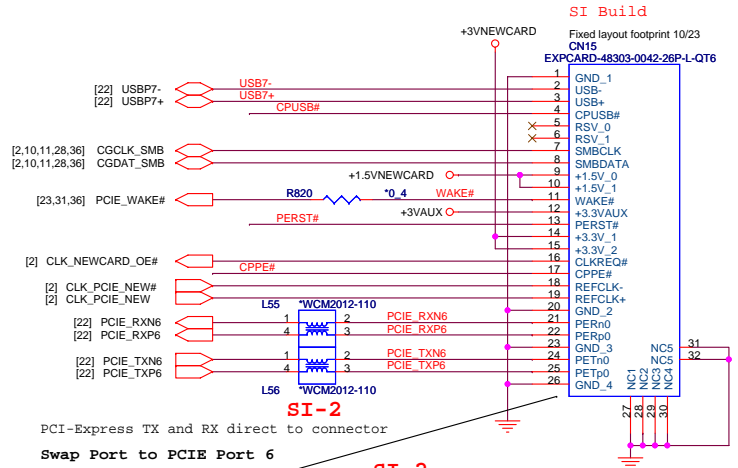


SATA HDD CONNECTOR

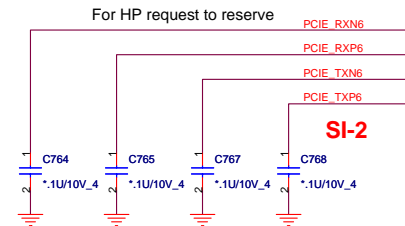
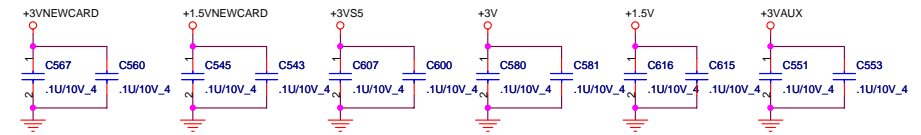
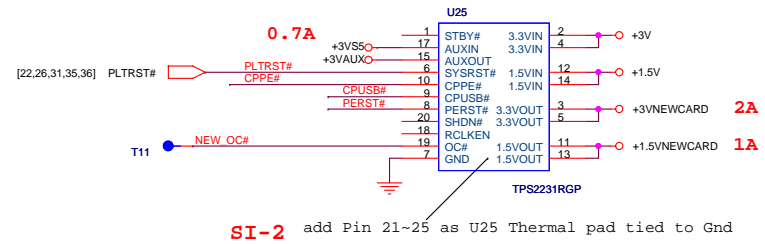


NEWCARD

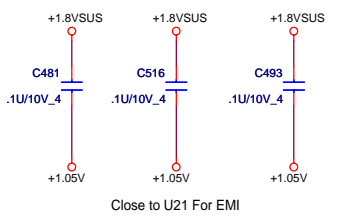
NEWCARD (PCIEXPRESS*1 + USB*1)



Change CN15#31,32 as ME request for Hole pad
 expcard-48303-0042-26p-l-qt6 as ME modify Pad size(pin31,32)
 Move CN15#29,30 Pin as ME request(Molex confirm drawing)



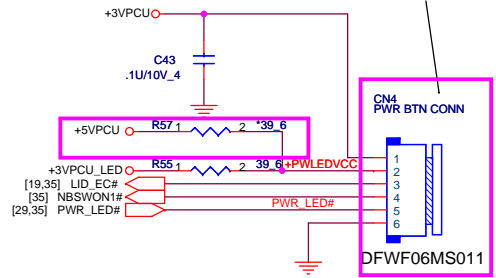
	PROJECT : QT6		Rev 2B
	Quanta Computer Inc.		
Size Custom	Document Number	Rev 2B	
ODD/HDD/NEW CARD			
Date: Tuesday, February 26, 2008 Sheet 33 of 44			



Close to U21 For EMI

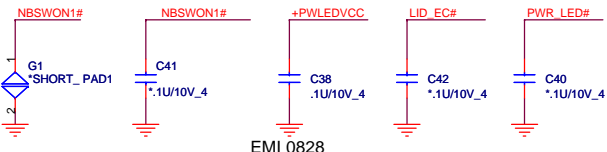
PV Build

Change CN4 to BL123-06R-6P-L-QT6-A



1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

POWER BOTTON CONNECT



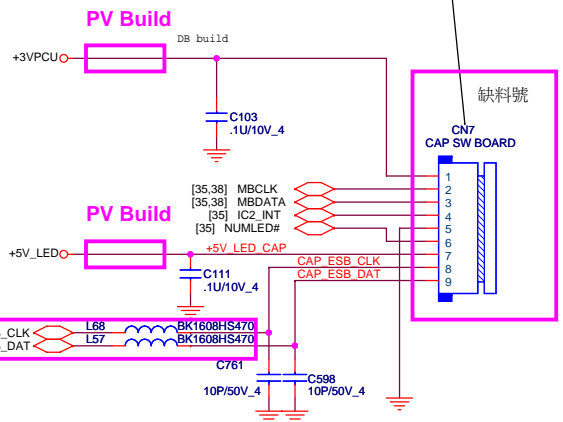
EMI 0828

POWER SW CONNECT

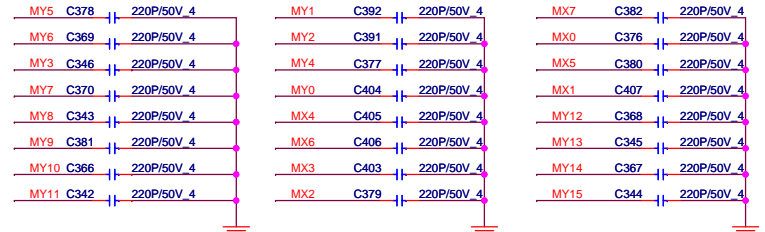
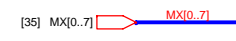
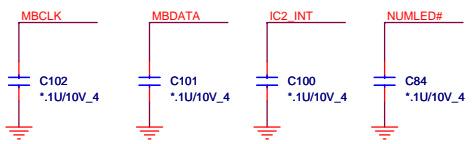
CAP SW CONNECT

PV Build

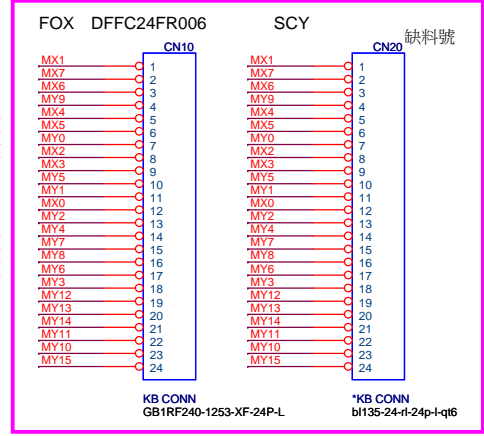
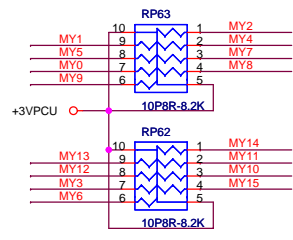
Change CN7 to BL123-09R-9P-L-QT6-A



1. +3VPCU
2. MBCLK
3. MBDATA
4. CAP_INT
5. GND
6. NUM LOCK LED
7. +5V_LED
8. ESB_CLK
9. ESB_DAT

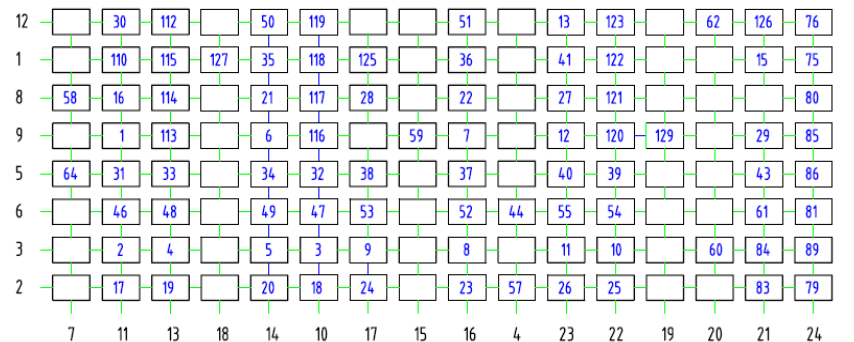
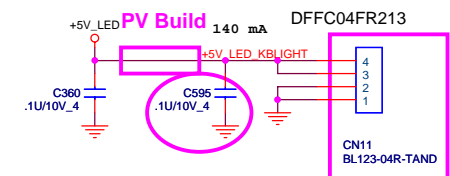


KEYBOARD PULL-UP



PV Build

Add C595 and close to CN11
Change CN11 to BL123-04R-4P-L-QT6-A
Change CN10 to GB1RF240-1253-XF-24P-L as Foxconn drawing

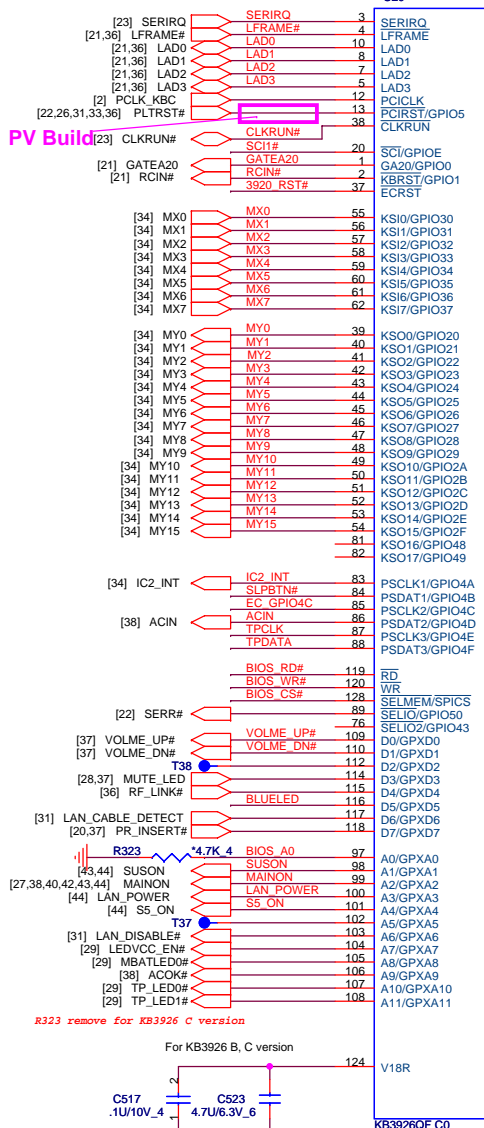


PROJECT : QT6
Quanta Computer Inc.

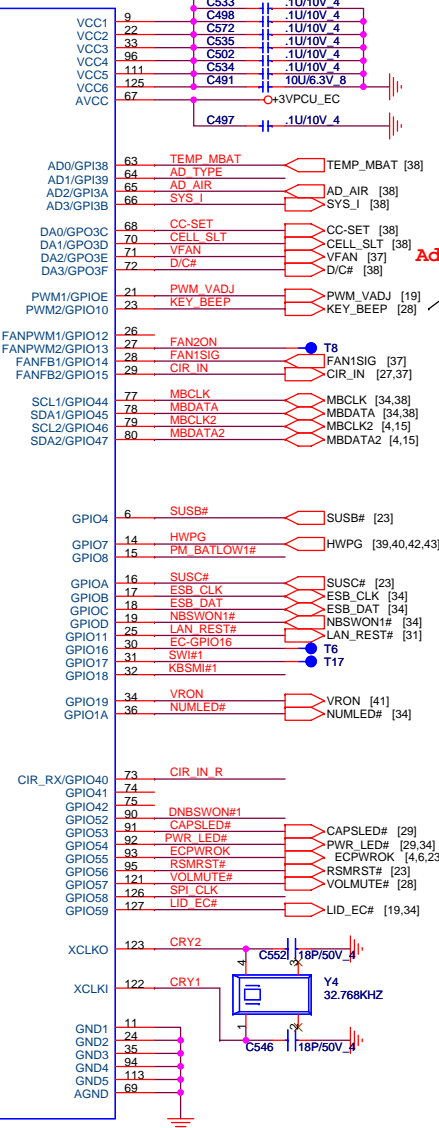
Size Custom Document Number
KB/CAP/POWER CONN

Date: Tuesday, February 26, 2008 Sheet 34 of 44

Change U20 layout footprint to LQFP128-16X16-4-AA1

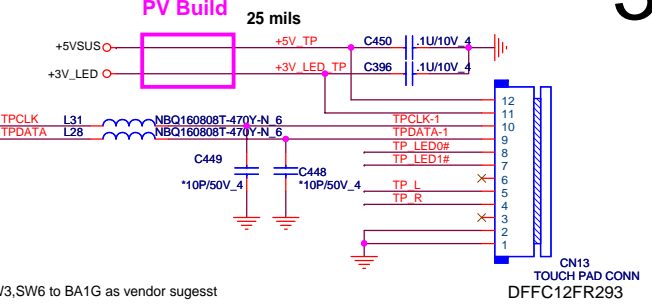


SI-2



Add in SI-2

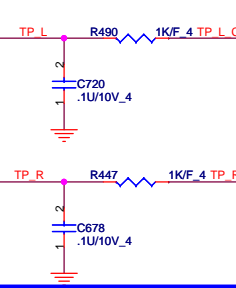
TOUCH PAD CONNECTOR PV Build



PV Build

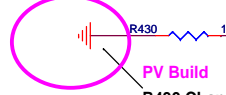
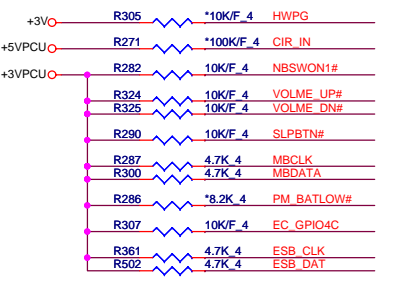
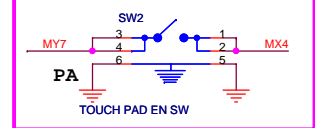
Change to SW2,SW3,SW6 to BA1G as vendor suggesst

TOUCH PAD L/R



PV Build

TOUCH PAD ON/OFF



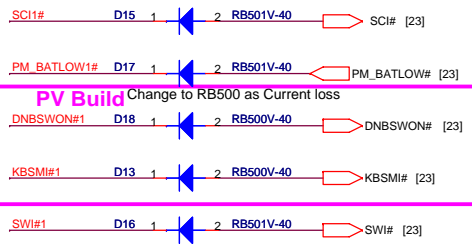
SI-2
 Add R430 and tied to U20 Pin 115 and change Q18 footprint to SOT23
 Delete Q18 and tied to U20#116 direction

Socket: DG008000031

- MXIC AKE5GFK0Z09
- WINBOND AKE3GFP0N08
- PME AKE3GZP0500
- EON AKE3GZP0Q00
- AIT AKE3GZP0801

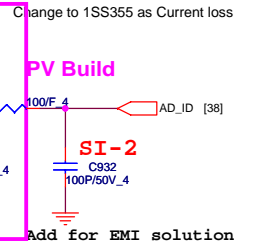
SI-2

Add Pin 117,103 for DSM,116 for Bluetooth,Pin 23 for Key Beep to Amplifier
 Add T37,T38,T39 for EC
 Delete T10 and tie pin 117 from Lan for DSM



R273

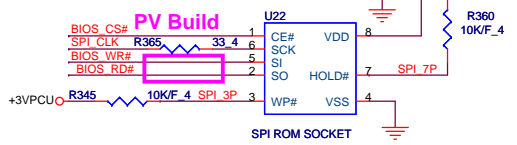
64.9K -->65W CS36492FB17
 33.2K -->90W CS33322FB13



Add for EMI solution

SI-2 Add for Power request

1M byte SPI BIOS



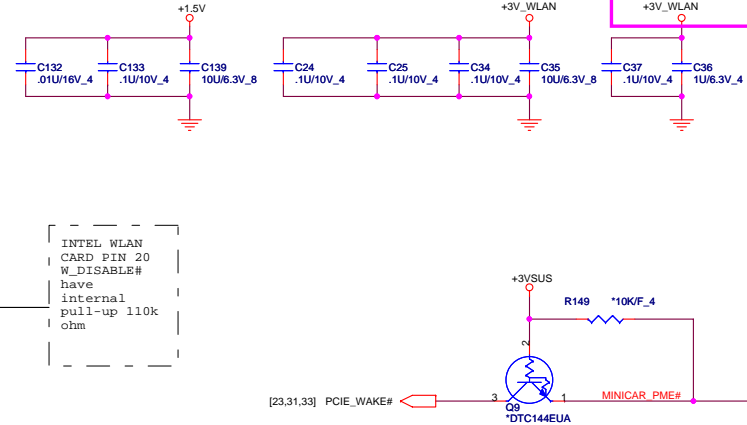
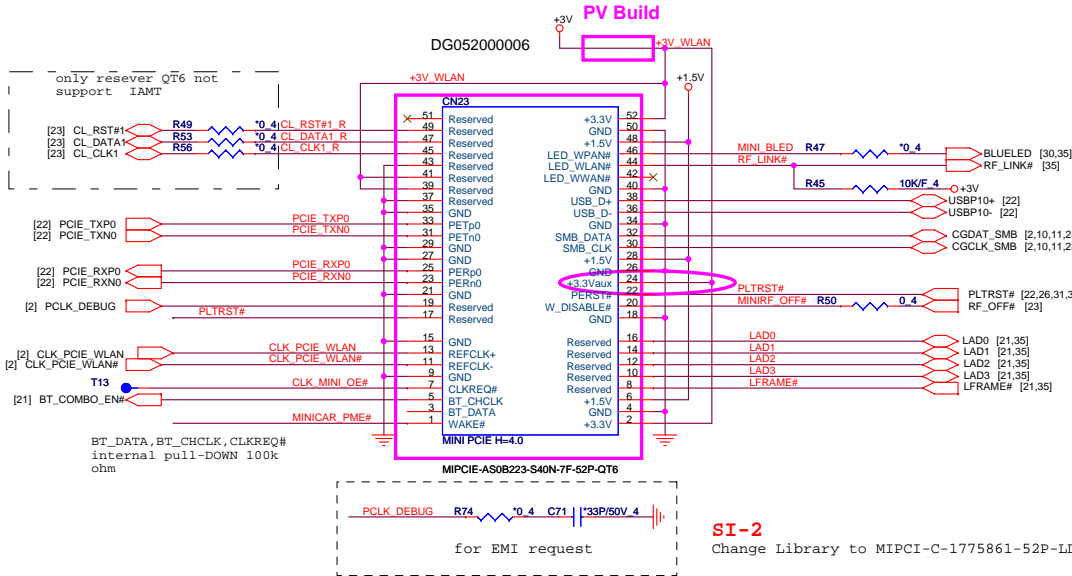
SI-2
 Change Layout footprint to X6179-10XXXX-8P-SOCKET(Socket)

PROJECT : QT6
Quanta Computer Inc.

Size Custom Document Number **KB3926/ROM/TP** Rev 3A
 Date: Tuesday, February 26, 2008 Sheet 35 of 44

Mini PCI-E Card 1 WLAN

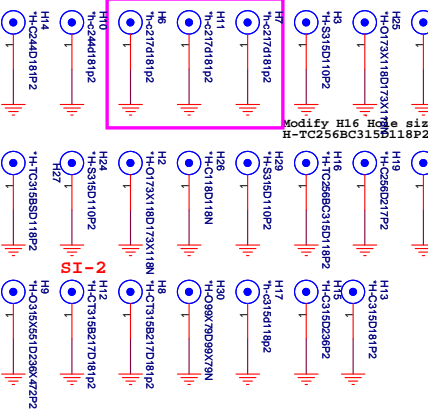
PV Build Delete R78 and tied the CN23#24 to R110 direction
Change CN23 layout footprint to MIPCI-E-AS0B223-S40N-7F-52P-QT6 as ME drawing



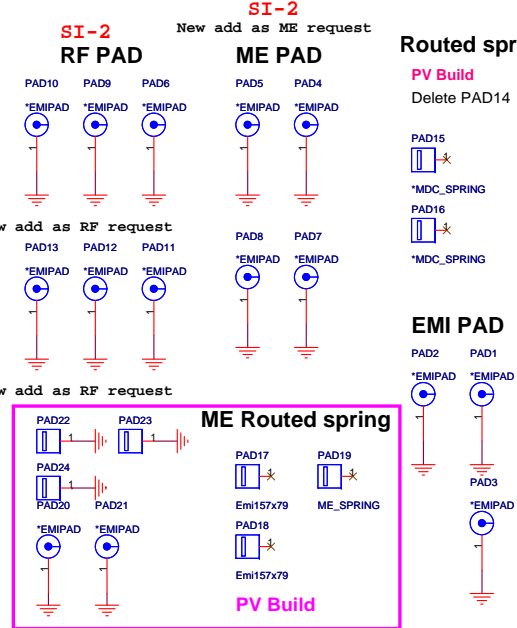
INTEL WLAN CARD PIN 20 W_DISABLE# have internal pull-up 110k ohm

M/B Screw Hole

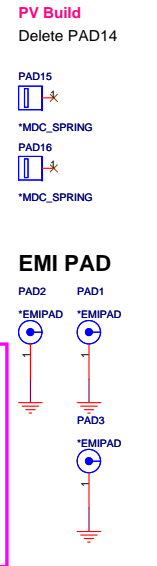
SI-2, h-e276x315d118p2



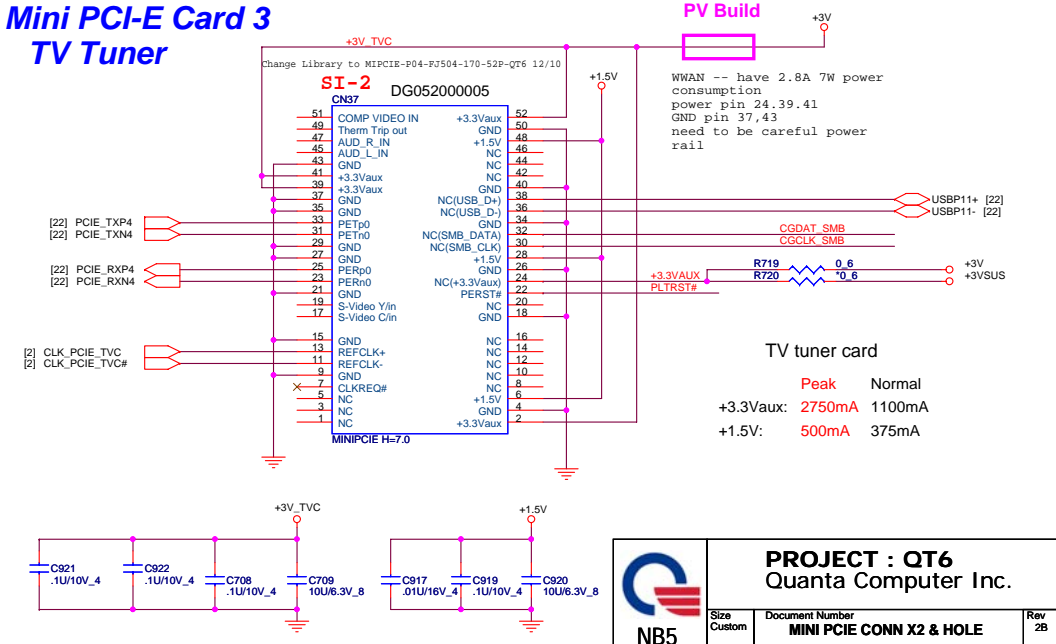
- PV Build**
- Change H1 to h-ctsbds118p2
 - Add PAD17 (Emi157x79)
 - Add PAD18 (Emi157x79)
 - Add PAD19 (Emi236x59)
 - Delete H4,H5 and modify battery connector
 - Change H6,H7,H11 to h-c217d181p2 as ME drawing update



Routed spring



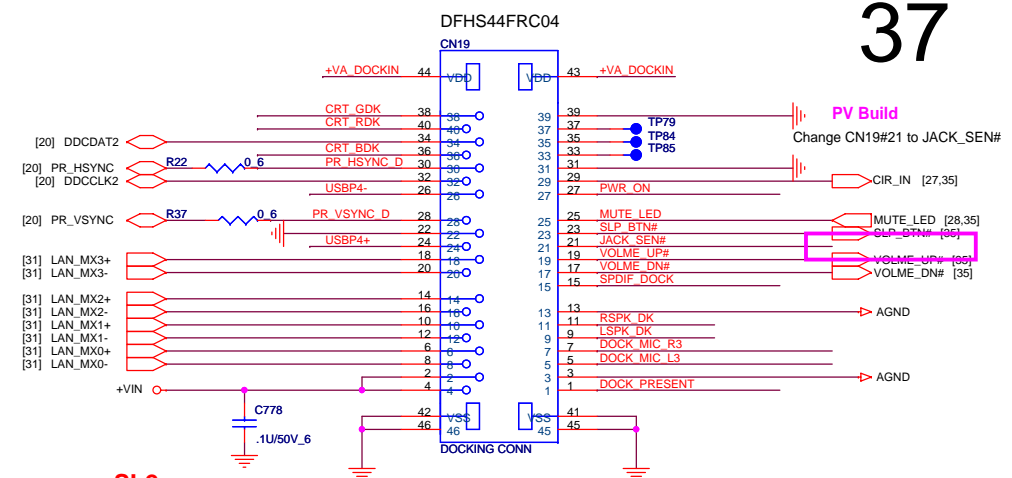
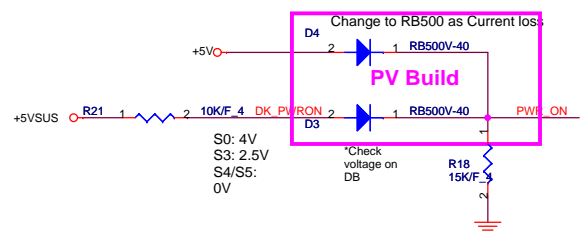
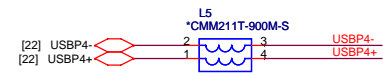
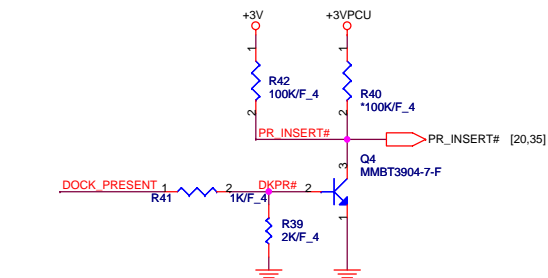
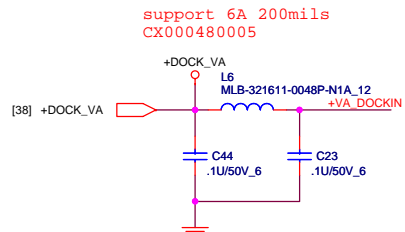
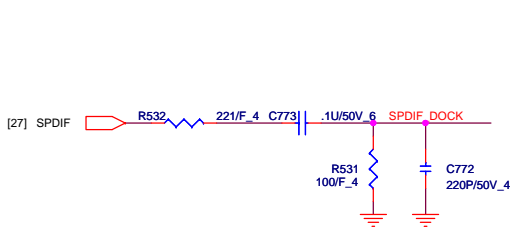
Mini PCI-E Card 3 TV Tuner



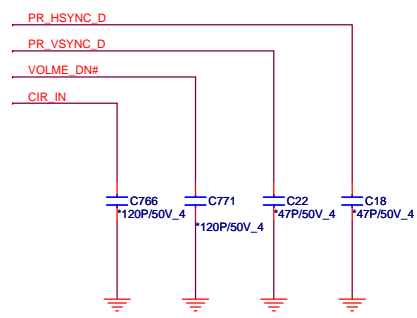
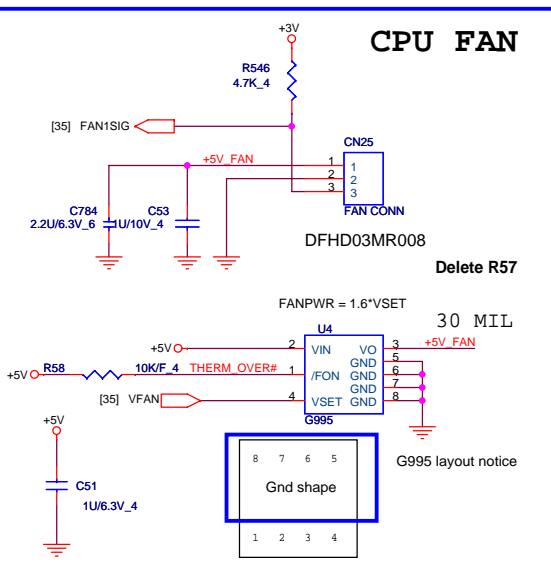
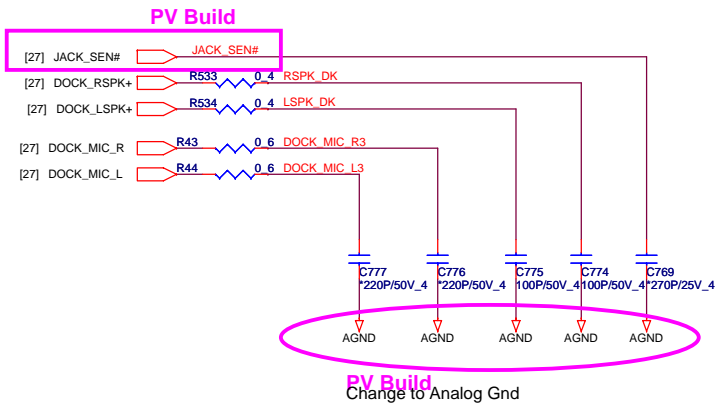
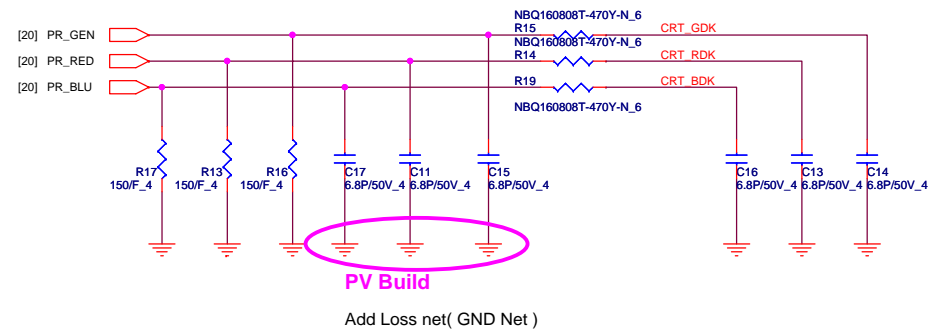
PROJECT : QT6
Quanta Computer Inc.

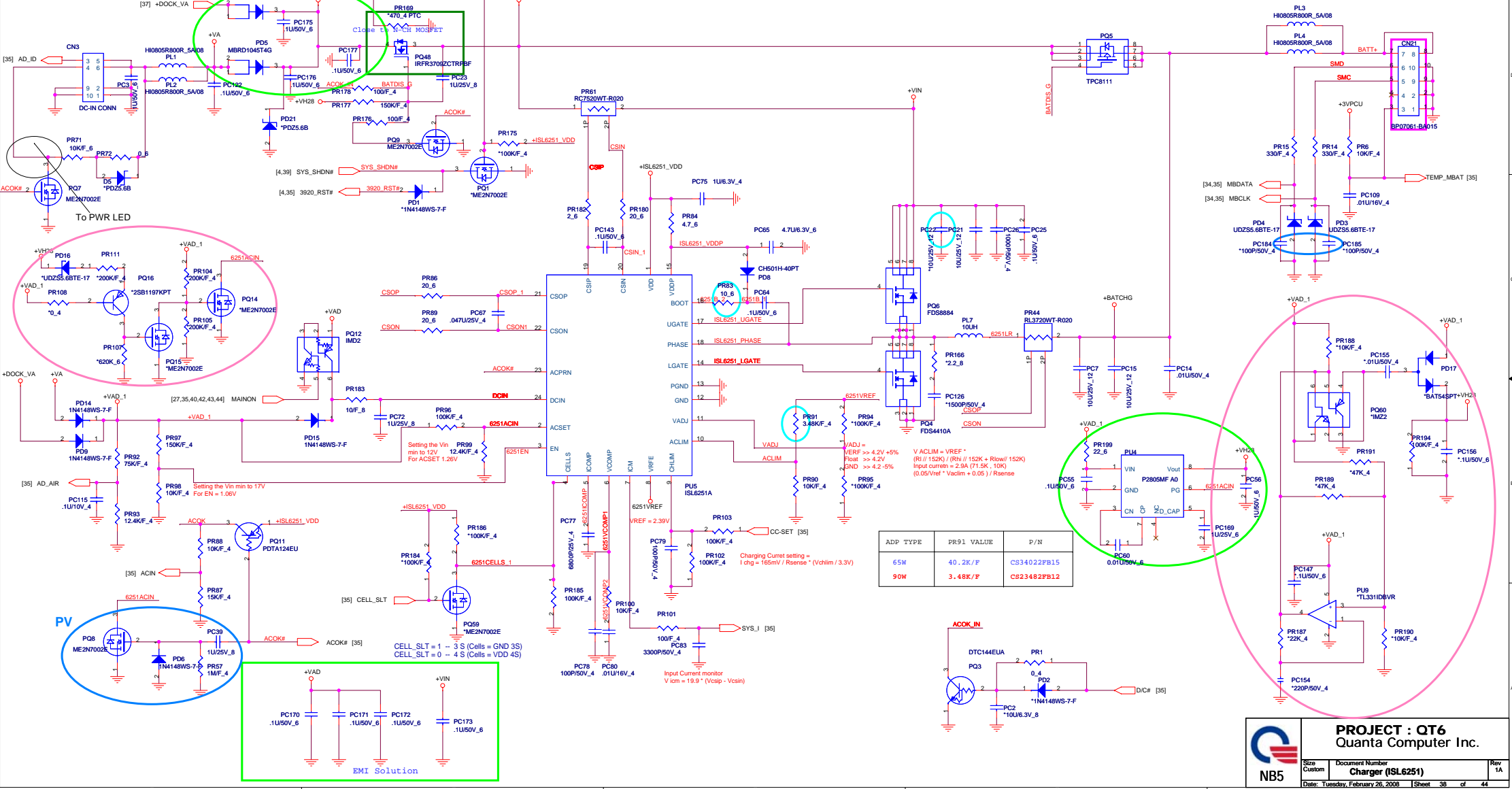
NBS

Size Custom	Document Number MINI PCIE CONN X2 & HOLE	Rev 2B
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SI-2
R13,R16,R17 Change to install





ADP TYPE	PR91 VALUE	P/N
65W	40.2K/F	CS34022FB15
90W	3.48K/F	CS23482FB12

PROJECT : QT6
Quanta Computer Inc.

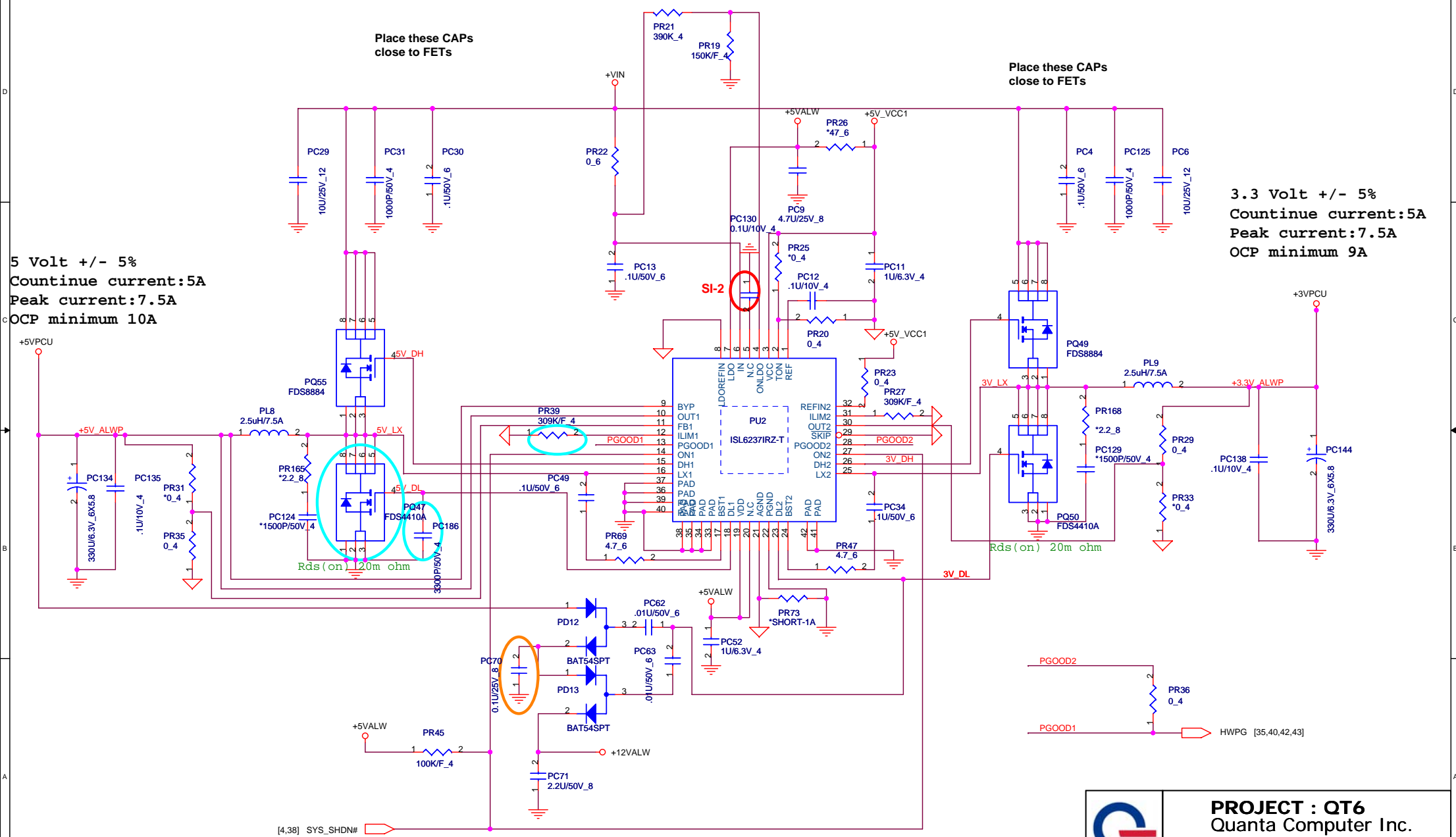
Size: Custom | Document Number: **Charger (ISL6251)** | Rev: 1A

Date: Tuesday, February 26, 2008 | Sheet: 38 of 44

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+12V_ALW

5 Volt +/- 5%
 Countinue current:5A
 Peak current:7.5A
 OCP minimum 10A

3.3 Volt +/- 5%
 Countinue current:5A
 Peak current:7.5A
 OCP minimum 9A



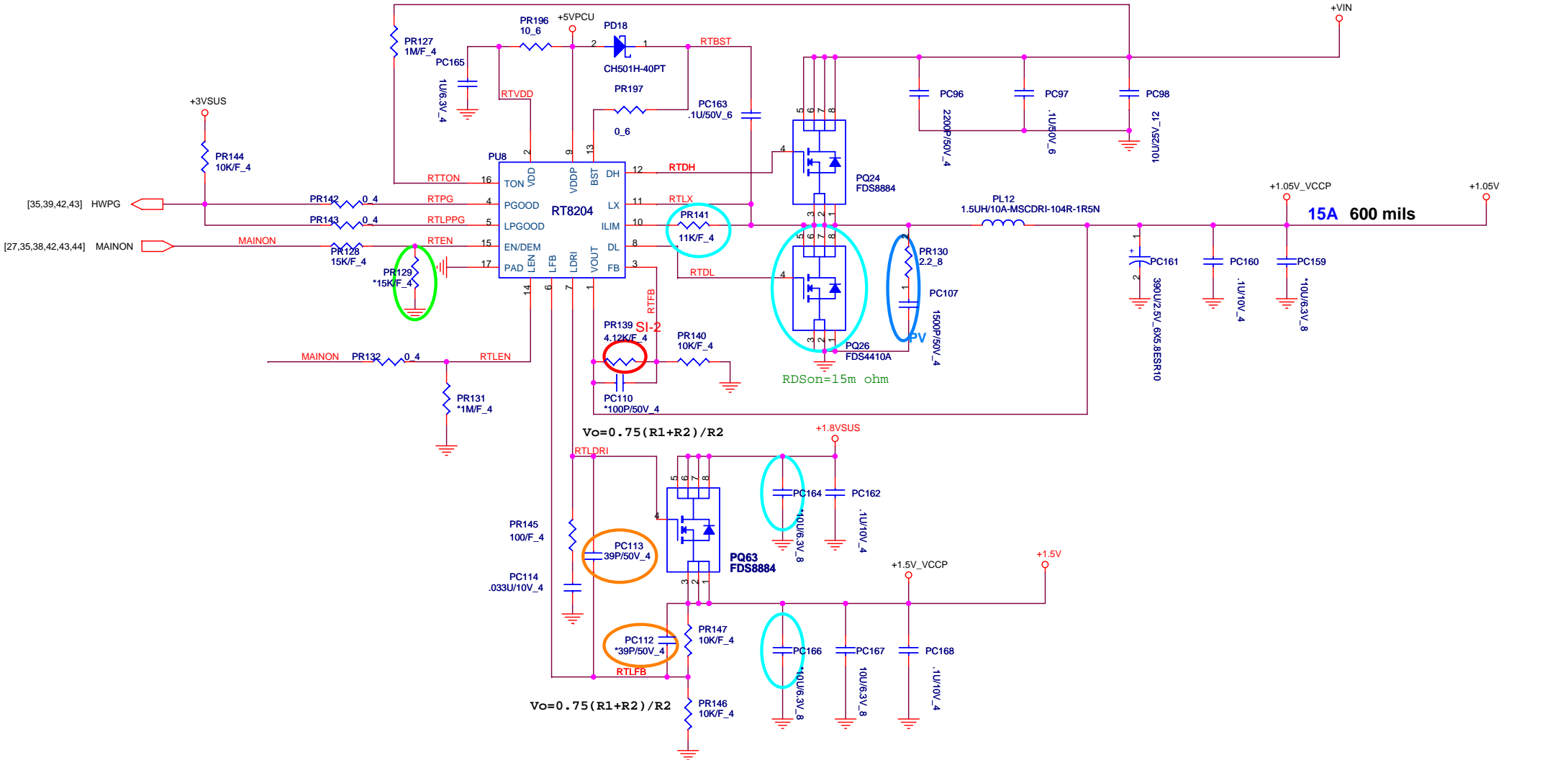
[4,38] SYS_SHDN#



PROJECT : QT6 Quanta Computer Inc.		
Size B	Document Number +5V/+3V (ISL6237)	Rev 1A
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VCCP1.05V & +1.5V

+1.05V Volt +/- 5%
 Countinue current:7.5A
 Peak current:10A
 OCP minimum 15A

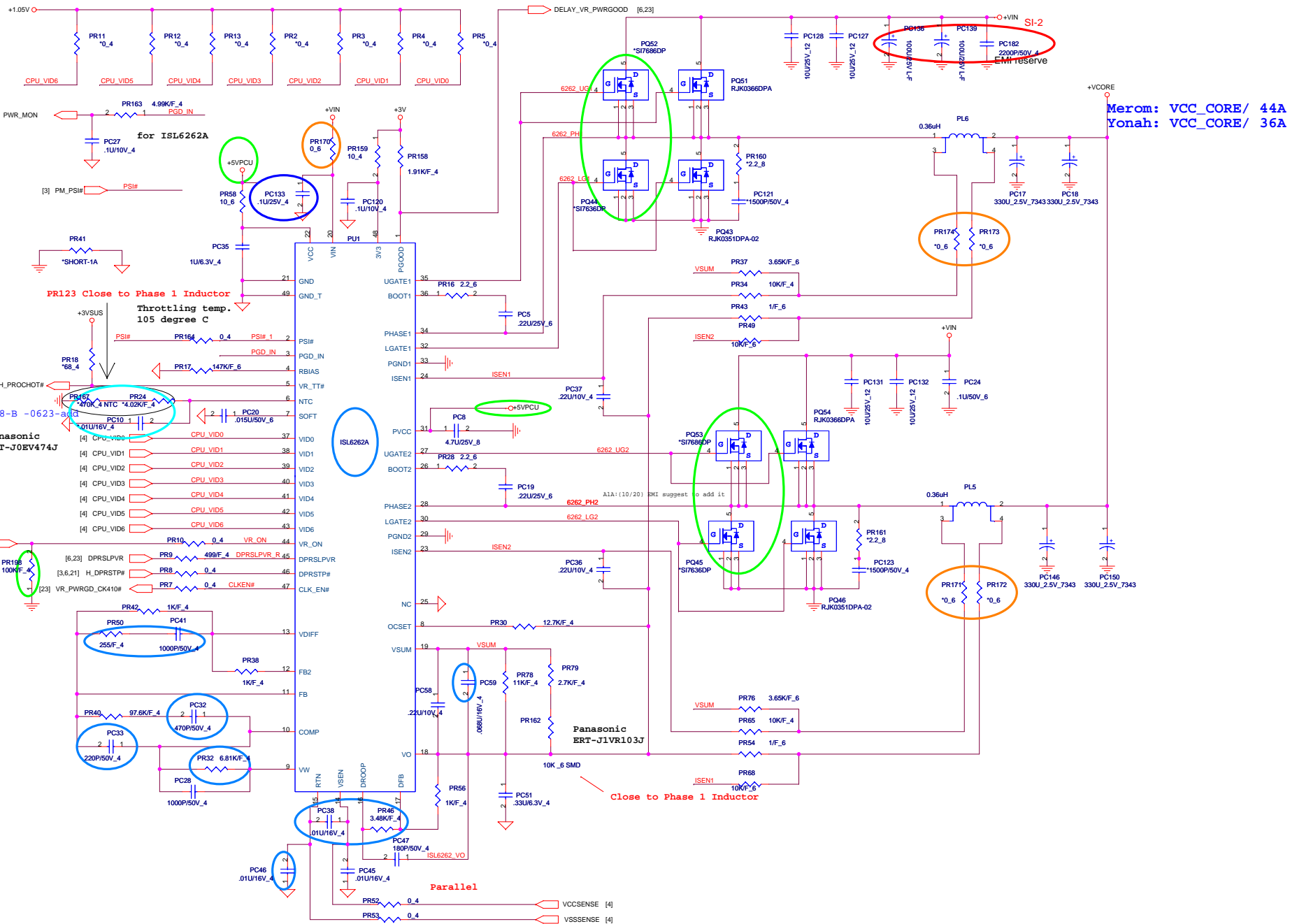


$$V_o = 0.75 \cdot (R1 + R2) / R2$$

$$V_o = 0.75 \cdot (R1 + R2) / R2$$



PROJECT : QT6 Quanta Computer Inc.		
Size B	Document Number +1.05V/+1.5V (RT8204)	Rev 1A
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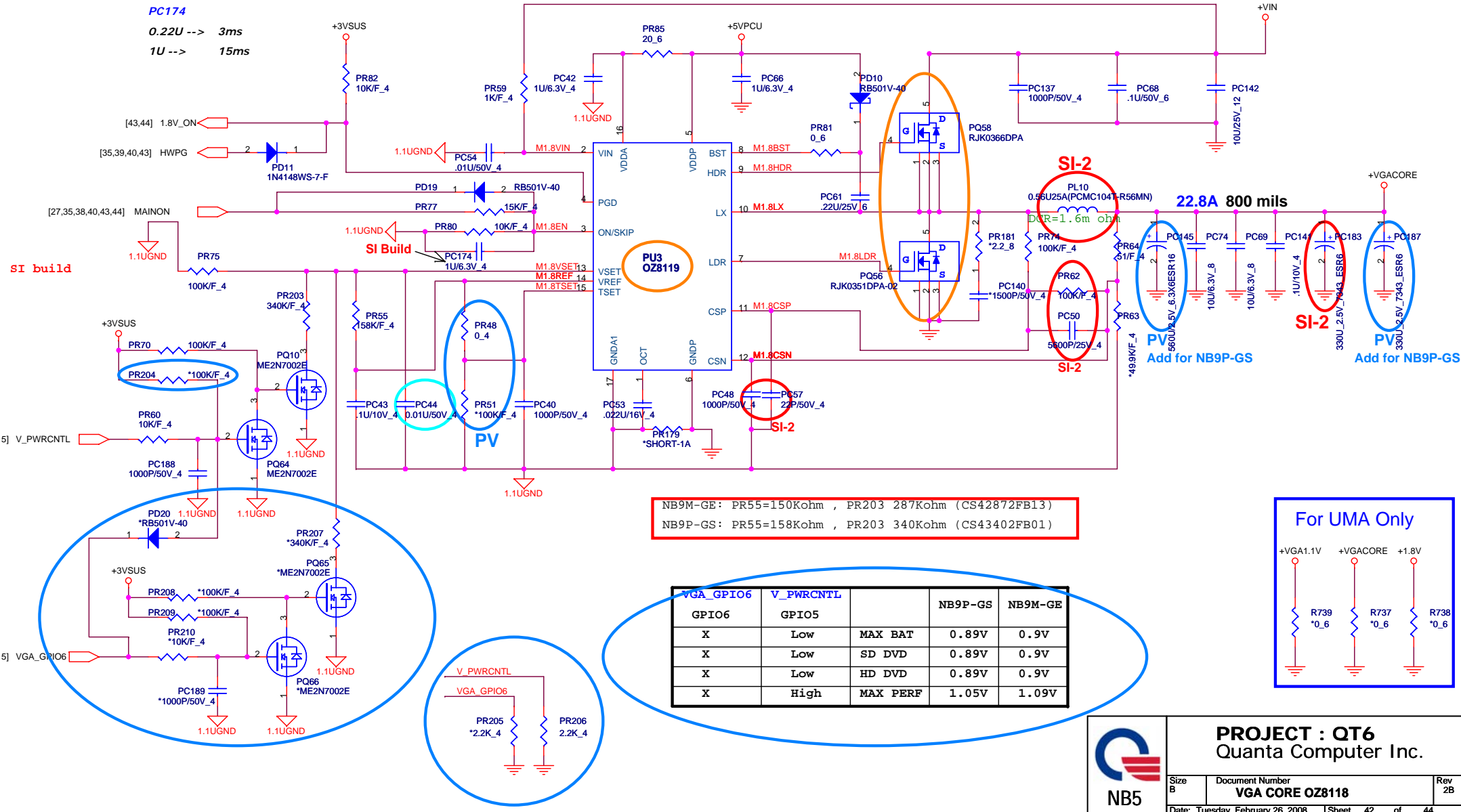
Merom: VCC_CORE/ 44A
 Yonah: VCC_CORE/ 36A

VGA Core & VCC1.1

+1.1Volt +/- 5%
 Countinue current:17.54A
 Peak current:22.8A
 OCP minimum 23A

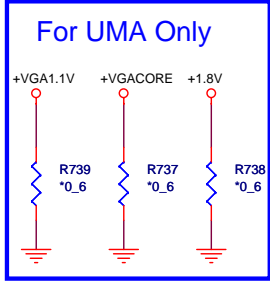
PC174

0.22U --> 3ms
 1U --> 15ms



NB9M-GE: PR55=150Kohm , PR203 287Kohm (CS42872FB13)
 NB9P-GS: PR55=158Kohm , PR203 340Kohm (CS43402FB01)

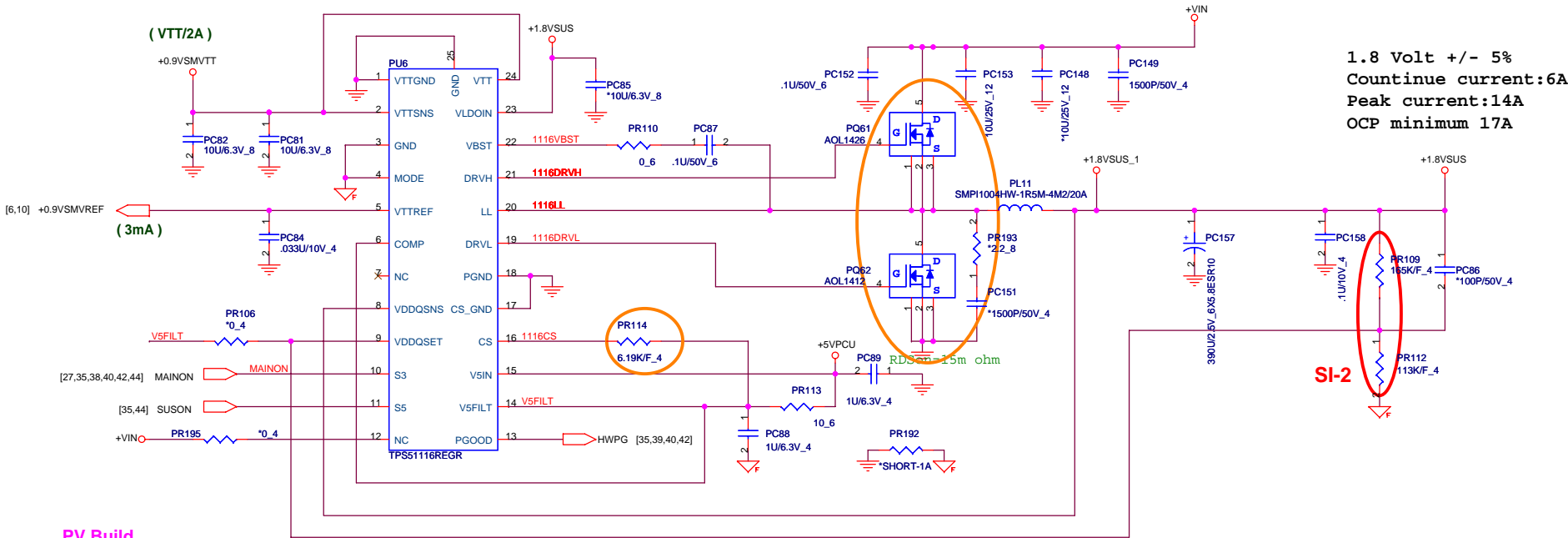
VGA_GPIO6	V_PWRCTRL		NB9P-GS	NB9M-GE
X	Low	MAX BAT	0.89V	0.9V
X	Low	SD DVD	0.89V	0.9V
X	Low	HD DVD	0.89V	0.9V
X	High	MAX PERF	1.05V	1.09V



PROJECT : QT6

Quanta Computer Inc.

Size B	Document Number VGA CORE OZ8118	Rev 2B
Date: Tuesday, February 26, 2008 Sheet 42 of 44		

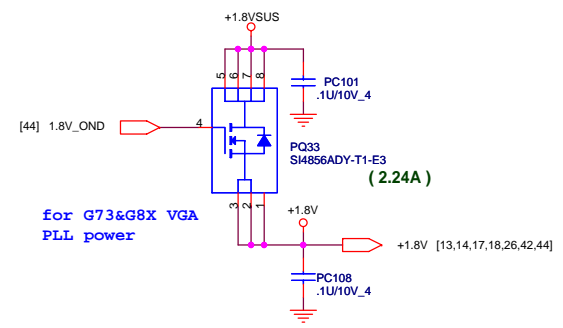
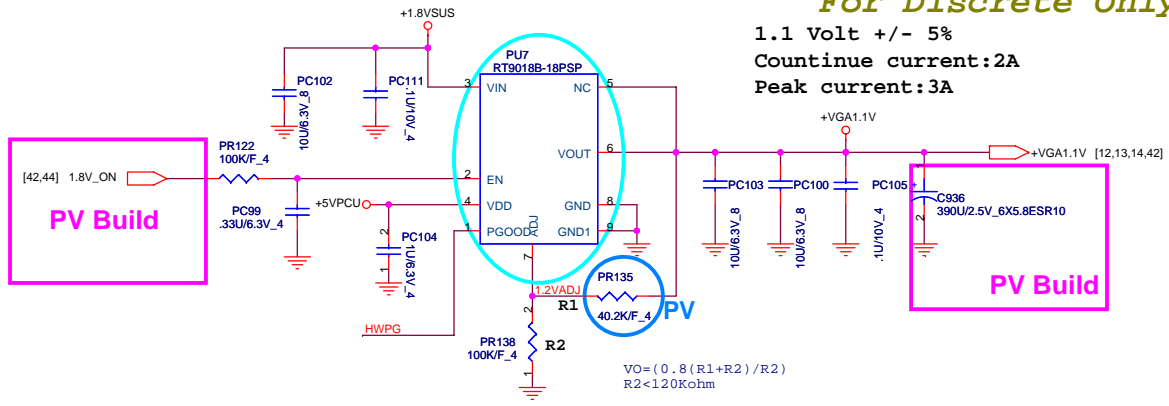


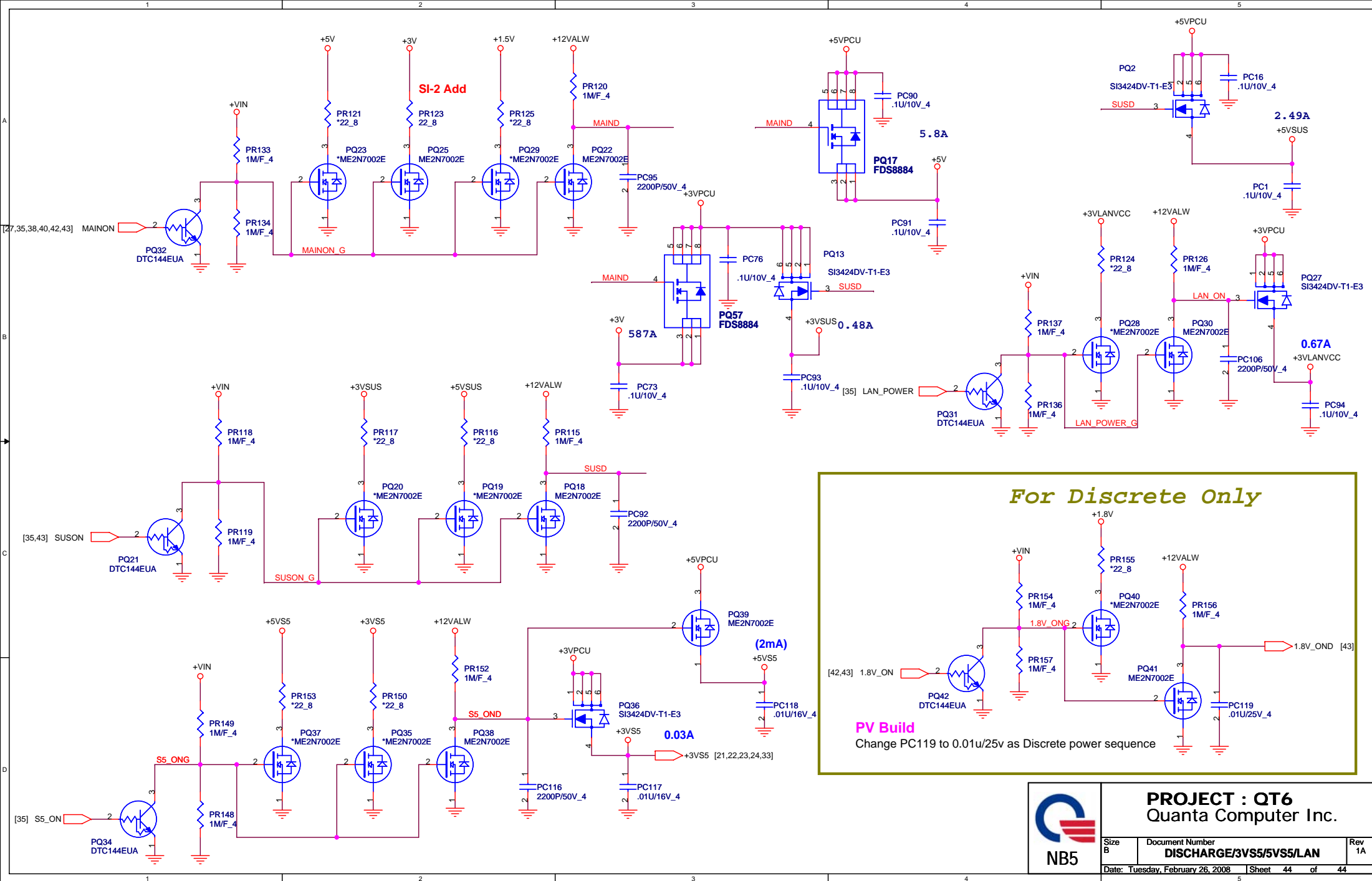
PV Build

Change PR122 tied to 1.8V_ON as power sequence request

For Discrete Only

1.1 Volt +/- 5%
Continue current:2A
Peak current:3A





SI-2 Add

For Discrete Only

PV Build
Change PC119 to 0.01u/25V as Discrete power sequence



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Quanta Computer Inc.

Size B	Document Number DISCHARGE/3VS5/5VS5/LAN	Rev 1A
Date: Tuesday, February 26, 2008 Sheet 44 of 44		