MOTOROLA

MMH0026
MMH0026C

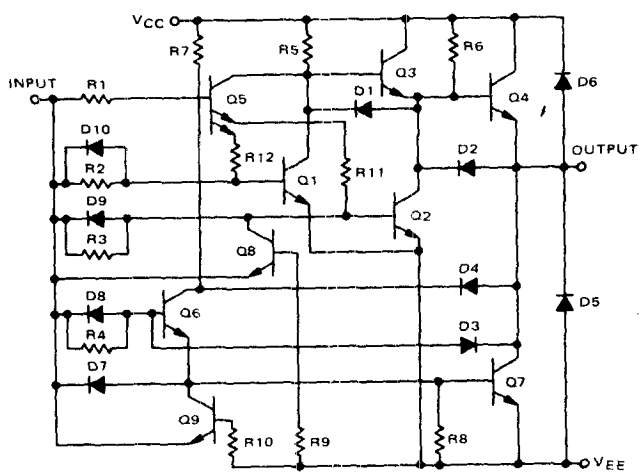
Specifications and Applications Information

DUAL MOS CLOCK DRIVER

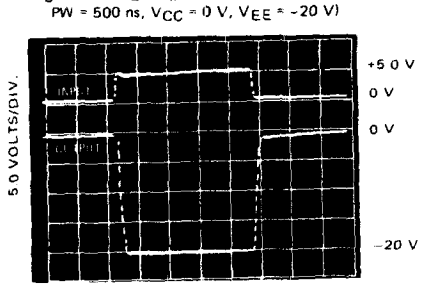
. . . designed for high-speed driving of highly capacitive loads in a MOS system.

- Fast Transition Times – 20 ns with 1000 pF Load
- High Output Swing – 20 Volts
- High Output Current Drive – ±1.5 Amperes
- High Repetition Rate – 5.0 to 10 MHz Depending on Load
- MTTL and MDTL Compatible Inputs
- Low Power Consumption when in MOS "0" State – 2.0 mW
- +5.0-Volt Operation for N-Channel MOS Compatibility

FIGURE 1 – CIRCUIT SCHEMATIC
(1/2 CIRCUIT SHOWN)



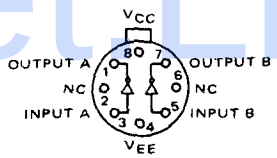
TYPICAL OPERATION
(R_S = 10 Ω, C_L = C_{in} = 1000 pF, f = 1.0 MHz,
PW = 500 ns, V_{CC} = 0 V, V_{EE} = -20 V)



DUAL MOS CLOCK DRIVER

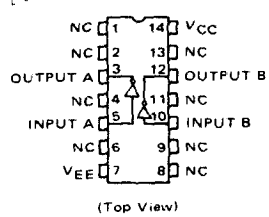
SILICON MONOLITHIC INTEGRATED CIRCUIT

G SUFFIX
METAL PACKAGE
CASE 601-02
TO-99



(Top View)

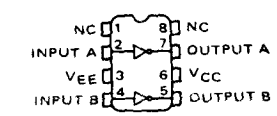
L SUFFIX
CERAMIC PACKAGE
CASE 632-02
TO-116



(Top View)

P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MMH0026C Only)

U SUFFIX
CERAMIC PACKAGE
CASE 693



(Top View)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating		Symbol	Value			Unit
Differential Supply Voltage		V_{CC}-V_{EE}	+22			Vdc
Input Current		I_I	+100			mA
Input Voltage		V_I	V_{EE} + 5.5			Vdc
Peak Output Current		I_{Opk}	±1.5			A
Junction Temperature		T_J	+175	+175	+150	°C
Operating Ambient Temperature Range		T_A	G	U,L	P1	°C
	MMH0026		-55 to +125	-55 to +125	–	
	MMH0026C		0 to +70	0 to +70	0 to +70	
Storage Temperature Range		T_{stg}	-65 to +150	-65 to +150	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC}-V_{EE} = 10 V to 20 V, C_L = 1000 pF, T_A = -55 to +125°C for MMH0026 and 0 to +70°C for MMH0026C for min and max values; T_A = +25°C for all typical values unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Logic "1" Level Input Voltage V_O = V_{EE} + 1.0 Vdc		V_{IH}	V_{EE} + 2.0	V_{EE} + 1.5	–	Vdc
Logic "1" Level Input Current V_I -V_{EE} = 2.4 Vdc, V_O = V_{EE} + 1.0 Vdc		I_{IH}	–	10	15	mA
Logic "0" Level Input Voltage V_O = V_{CC} -1.0 Vdc		V_{IL}	–	V_{EE} + 0.6	V_{EE} + 0.4	Vdc
Logic "0" Level Input Current V_I -V_{EE} = 0 Vdc, V_O = V_{CC} -1.0 Vdc		I_{IL}	–	-0.005	-10	μA
Logic "0" Level Output Voltage V_{CC} = +5.0 Vdc, V_{EE} = -12 Vdc, V_I = -11.6 Vdc V_I -V_{EE} = 0.4 Vdc		V_{OH}	 4.0 V_{CC} -1.0	 4.3 V_{CC} -0.7	 – –	Vdc
Logic "1" Level Output Voltage V_{CC} = +5.0 Vdc, V_{EE} = -12 Vdc, V_I = -9.6 Vdc V_I -V_{EE} = 2.4 Vdc		V_{OL}	 – –	 -11.5 V_{EE} + 0.5	 -11 V_{EE} + 1.0	Vdc
"On" Supply Current V_{CC}-V_{EE} = 20 Vdc, V_I -V_{EE} = 2.4 Vdc		I_{CCL}	–	30	40	mA
"Off" Supply Current V_{CC}-V_{EE} = 20 Vdc, V_I -V_{EE} = 0 V	MMH0026C MMH0026	I_{CCH}	– –	10 –	100 500	μA

SWITCHING CHARACTERISTICS (V_{CC}-V_{EE} = 10 V to 20 V, C_L = 1000 pF, T_A = 25°C)

Propagation Time						
High to Low	(Figure 2)	t_{PHL}	5.0	7.5	12	ns
	(Figure 3)		–	11	–	
Low to High	(Figure 2)	t_{PLH}	5.0	12	15	
	(Figure 3)		–	13	–	
Transition Time (High to Low)		t_{THL}				ns
V_{CC}-V_{EE} = 20 Vdc, C_L = 250 pF	(Figure 2)		–	12	–	
V_{CC}-V_{EE} = 20 Vdc, C_L = 500 pF	(Figure 2)		–	15	18	
	(Figure 3)		–	30	40	
V_{CC}-V_{EE} = 20 Vdc, C_L = 1000 pF	(Figure 2)		–	20	35	
	(Figure 3)		–	36	50	
Transition Time (Low to High)		t_{TLH}				ns
V_{CC}-V_{EE} = 20 Vdc, C_L = 250 pF	(Figure 2)		–	10	–	
V_{CC}-V_{EE} = 20 Vdc, C_L = 500 pF	(Figure 2)		–	12	16	
	(Figure 3)		–	28	35	
V_{CC} -V_{EE} = 20 Vdc, C_L = 1000 pF	(Figure 2)		–	17	25	
	(Figure 3)		–	31	40	

TEST CIRCUIT

FIGURE 2 – AC TEST CIRCUIT AND WAVEFORMS

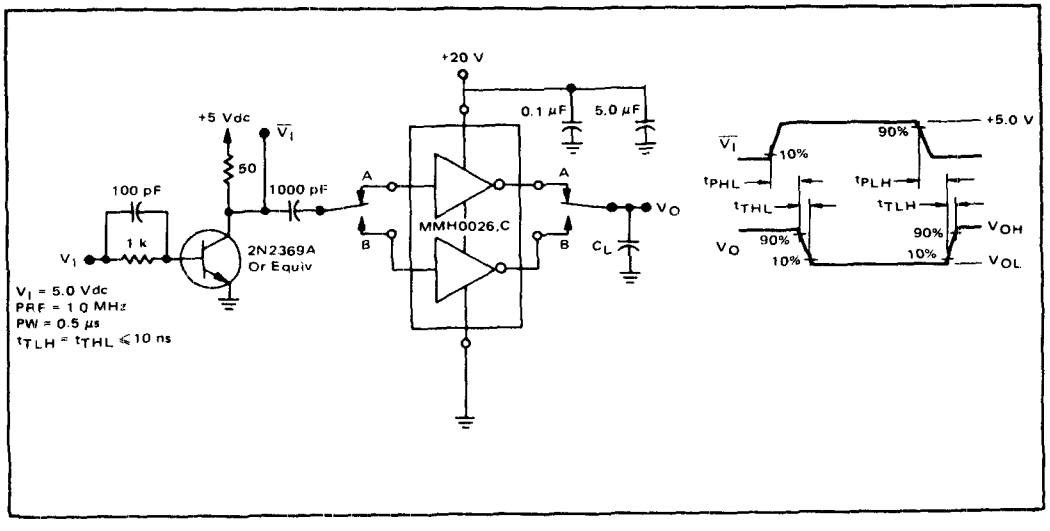
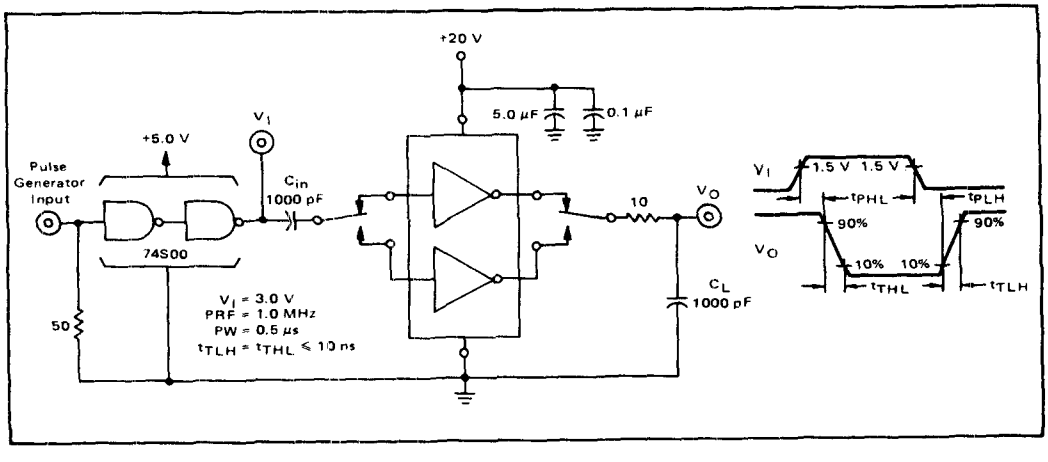


FIGURE 3 – AC TEST CIRCUIT AND WAVEFORMS



TYPICAL CHARACTERISTICS

(V_{CC} = + 20 V, V_{EE} = 0 V, T_A = +25°C unless otherwise noted.)

FIGURE 4 – INPUT CURRENT versus INPUT VOLTAGE

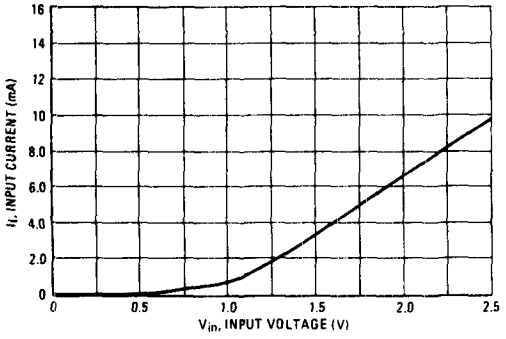


FIGURE 5 – SUPPLY CURRENT versus TEMPERATURE

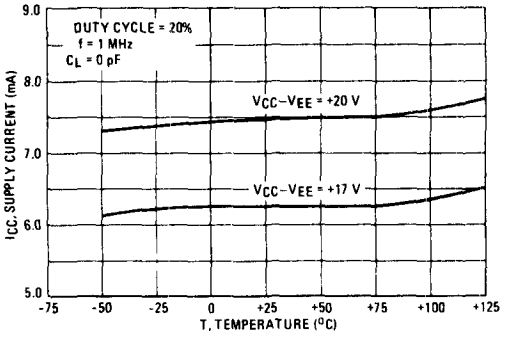


FIGURE 6 – OPTIMUM INPUT CAPACITANCE versus OUTPUT PULSE WIDTH

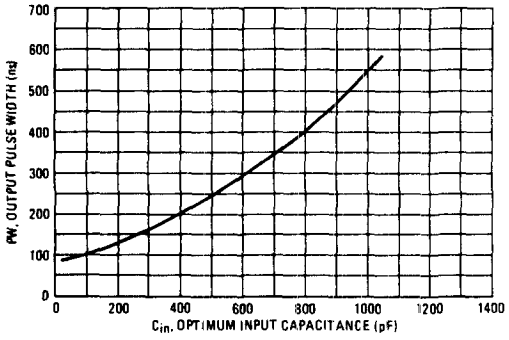


FIGURE 7 – TRANSITION TIMES versus LOAD CAPACITANCE

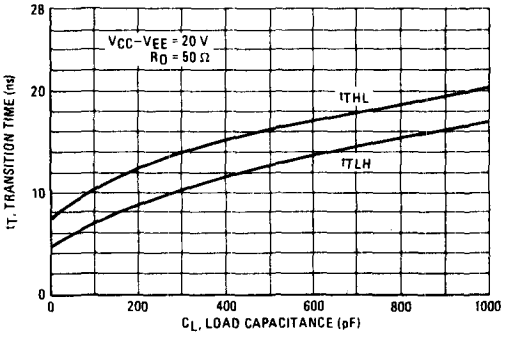


FIGURE 8 – PROPAGATION DELAY TIMES versus TEMPERATURE

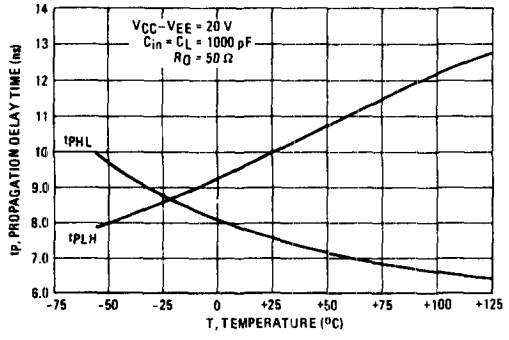
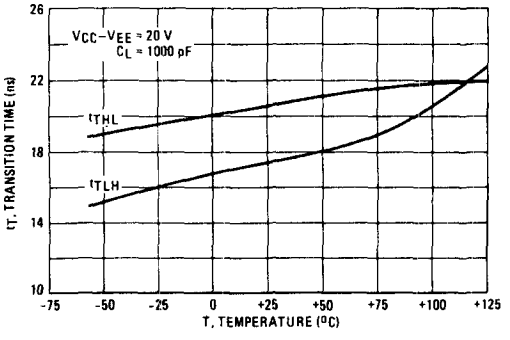


FIGURE 9 – TRANSITION TIMES versus TEMPERATURE



TYPICAL CHARACTISTICS (continued)

(V_{CC} = + 20 V, V_{EE} = 0 V, T_A = +25°C unless otherwise noted.)

FIGURE 10 – TRANSITION TIME versus TEMPERATURE FOR +5 VOLT DC-COUPLED OPERATION (See Figure 4.)

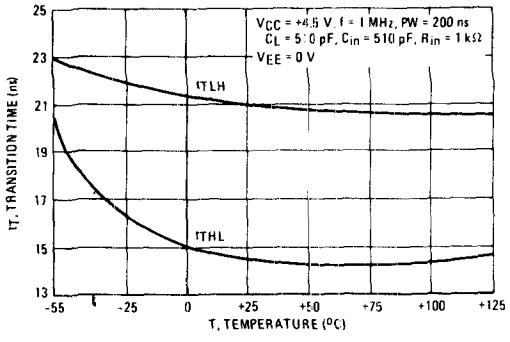


FIGURE 11 – PROPAGATION DELAY TIME versus TEMPERATURE FOR +5 VOLT DC-COUPLED OPERATION (See Figure 4.)

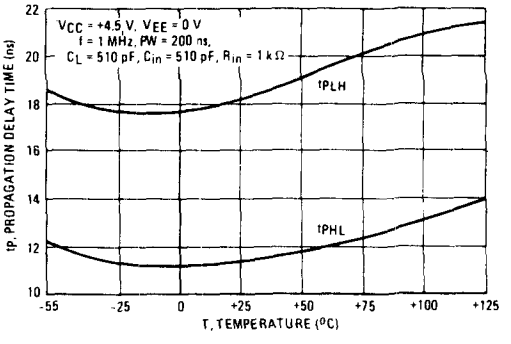


FIGURE 12 – DC-COUPLED SWITCHING RESPONSE versus R_{in} (See Figure 4.)

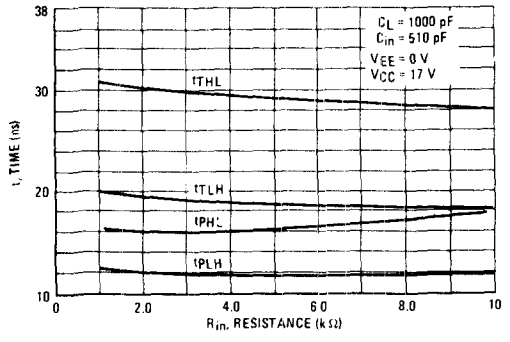


FIGURE 13 – DC-COUPLED SWITCHING versus C_{in} (See Figure 4.)

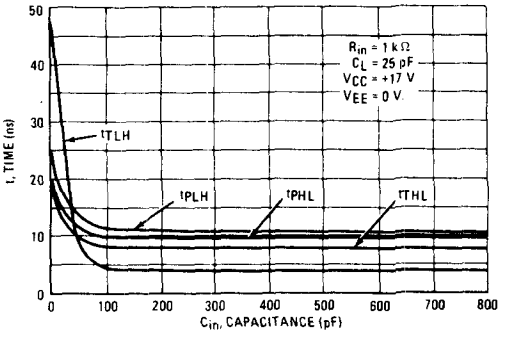


FIGURE 14 – MAXIMUM DC POWER DISSIPATION versus DUTY CYCLE (SINGLE DRIVER)

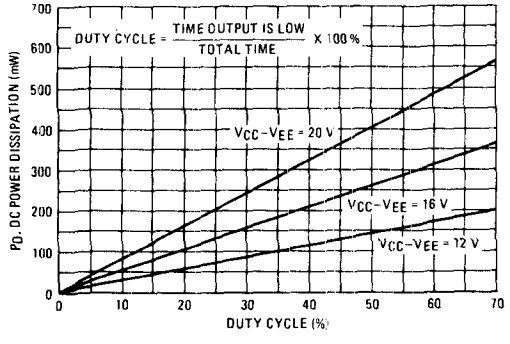
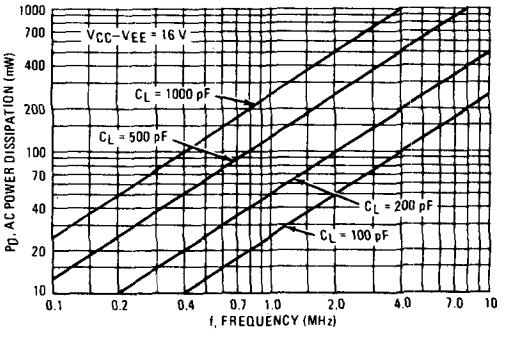


FIGURE 15 – AC POWER DISSIPATION versus FREQUENCY (SINGLE DRIVER)



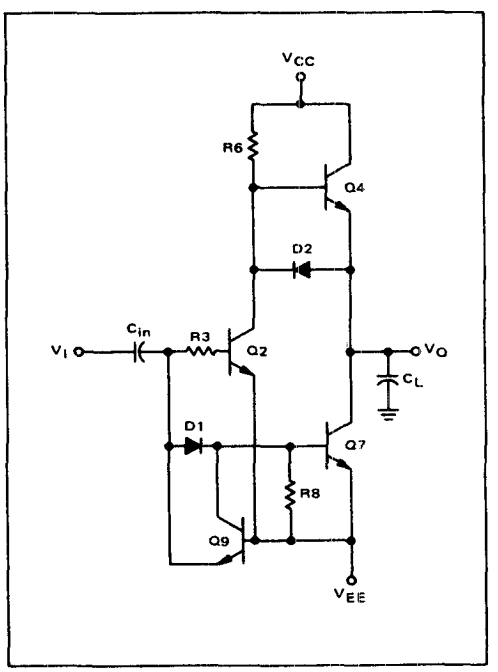
APPLICATIONS INFORMATION

OPERATION OF THE MMH0026

The simplified schematic diagram of MMH0026, shown in Figure 16, is useful in explaining the operation of the device. Figure 16 illustrates that as the input voltage level goes high, diode D1 provides an 0.7-volt "dead zone" thus ensuring that Q2 is turned "on" and Q4 is turned "off" before Q7 is turned "on". This prevents undesirable "current spiking" from the power supply, which would occur if Q7 and Q4 were allowed to be "on" simultaneously for an instant of time. Diode D2 prevents "zenering" of Q4 and provides an initial discharge path for the output capacitive load by way of Q2.

As the input voltage level goes low, the stored charge in Q2 is used advantageously to keep Q2 "on" and Q4 "off" until Q7 is "off". Again undesirable "current spiking" is prevented. Due to the external capacitor, the input side of C_{in} goes negative with respect to V_{EE} causing Q9 to conduct momentarily thus assuring rapid turn "off" of Q7.

FIGURE 16 – SIMPLIFIED SCHEMATIC DIAGRAM
(Ref.: Figure 1)



The complete circuit, Figure 1, basically creates Darlington devices of transistors Q7, Q4 and Q2 in the simplified circuit of Figure 16. Note in Figure 1 that when the input goes negative with respect to V_{EE}, diodes D7 through D10 turn "on" assuring faster turn "off" of transistors Q1, Q2, Q6 and Q7. Resistor R6 insures that the output will charge to within one V_{BE} voltage drop of the V_{CC} supply.

SYSTEM CONSIDERATIONS

Overshoot:

In most system applications the output waveform of the MMH0026 will "overshoot" to some degree. However, "overshoot" can be eliminated or reduced by placing a damping resistor in series with the output. The amount of resistance required is given by: $R_S = 2\sqrt{L/C_L}$ where L is the inductance of the line and C_L is the load capacitance. In most cases a series of damping resistor in the range of 10-to-50 ohms will be sufficient. The damping resistor also affects the transition times of the outputs. The speed reduction is given by the formula:

$t_{THL} \approx t_{TLH} = 2.2\ R_S\ C_L$ (R_S is the damping resistor).

Crosstalk:

The MMH0026 is sensitive to crosstalk when the output voltage level is high ($V_O \approx V_{CC}$). With the output in the high voltage level state, Q3 and Q4 are essentially turned "off". Therefore, negative-going crosstalk will pull the output down until Q4 turns "on" sufficiently to pull the output back towards V_{CC}. This problem can be minimized by placing a "bleeding" resistor from the output to ground. The "bleeding" resistor should be of sufficient size so that Q4 conducts only a few milliamperes. Thus, when noise is coupled, Q4 is already "on" and the line is quickly clamped by Q4. Also note that in Figure 1 D6 clamps the output one diode-voltage drop above V_{CC} for positive-going crosstalk.

Power Supply Decoupling:

The decoupling of V_{CC} and V_{EE} is essential in most systems. Sufficient capacitive decoupling is required to supply the peak surge currents during switching. At least a 0.1-μF to 1.0-μF low inductive capacitor should be placed as close to each driver package as the layout will permit.

Input Driving:

For those applications requiring split power supplies (V_{EE} < GND), ac coupling, as illustrated in Figure23, should be employed. Selection of the input capacitor size is determined by the desired output pulse width. Maximum performance is attained when the voltage at

APPLICATIONS INFORMATION (continued)

the input of the MMH0026 discharges to just above the device's threshold voltage (about 1.5 V). Figure 6 shows optimum values for C_{in} versus the desired output pulse width. The value for C_{in} may be roughly predicted by:

$$C_{in} = (2 \times 10^{-3})\ (PW_O). \quad (1)$$

For an output pulse width of 500 ns, the optimum value for C_{in} is:

$$C_{in} = (2 \times 10^{-3})\ (500 \times 10^{-9}) = 1000\ pF.$$

If single supply operation is required (V_{EE} = GND), then dc coupling as illustrated in Figure 24 can be employed. For maximum switching performance, a speed-up capacitor should be employed with dc coupling. Figures 12 and 13 show typical switching characteristics for various values of input resistance and capacitance.

POWER CONSIDERATIONS

Circuit performance and long-term circuit reliability are affected by die temperature. Normally, both are improved by keeping the integrated circuit junction temperatures low. Electrical power dissipated in the integrated circuit is the source of heat. This heat source increases the temperature of the die relative to some reference point, normally the ambient temperature. The temperature increase depends on the amount of power dissipated in the circuit and on the net thermal resistance between the heat source and the reference point. The basic formula for converting power dissipation into junction temperature is:

$$T_J = T_A + P_D\ (R_{\theta JC} + R_{\theta CA}) \quad (2)$$

or

$$T_J = T_A + P_D\ (R_{\theta JA}) \quad (3)$$

where

T_J = junction temperature
T_A = ambient temperature
P_D = power dissipation
$R_{\theta JC}$ = thermal resistance, junction to case
$R_{\theta CA}$ = thermal resistance, case to ambient
$R_{\theta JA}$ = thermal resistance, junction to ambient.

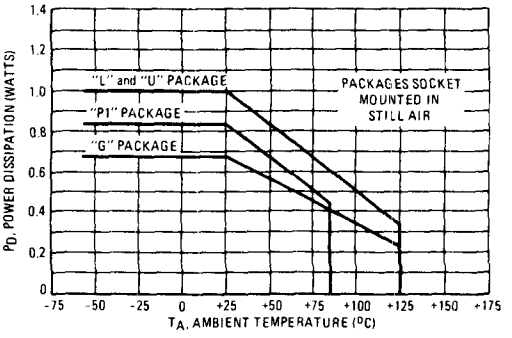
Power Dissipation for the MMH0026 MOS Clock Driver:

The power dissipation of the device (P_D) is dependent on the following system requirements: frequency of operation, capacitive loading, output voltage swing, and duty cycle. This power dissipation, when substituted into equation (3), should not yield a junction temperature, T_J, greater than T_J(max) at the maximum encountered ambient temperature. T_J(max) is specified for three integrated circuit packages in the maximum ratings section of this data sheet.

TABLE 1 – THERMAL CHARACTERISTICS OF "G", "L", "P1", AND "U" PACKAGES

PACKAGE TYPE (Mounted in Socket)	$R_{\theta JA}$ (°C/W) Still Air		$R_{\theta JC}$ (°C/W) Still Air	
	MAX	TYP	MAX	TYP
"G" (Metal Package)	220	175	70	40
"L" (Ceramic Package)	150	100	50	27
"P1" (Plastic Package)	150	100	70	40
"U" (Ceramic Package)	150	100	50	27

FIGURE 17 – MAXIMUM POWER DISSIPATION versus AMBIENT TEMPERATURE (As related to package)



With these maximum junction temperature values, the maximum permissible power dissipation at a given ambient temperature may be determined. This can be done with equations (2) or (3) and the maximum thermal resistance values given in Table 1 or alternately, by using the curves plotted in Figure 17. If, however, the power dissipation determined by a given system produces a calculated junction temperature in excess of the recommended maximum rating for a given package type, something must be done to reduce the junction temperature.

There are two methods of lowering the junction temperature without changing the system requirements. First, the ambient temperature may be reduced sufficiently to bring T_J to an acceptable value. Secondly, the $R_{\theta CA}$ term can be reduced. Lowering the $R_{\theta CA}$ term can be accomplished by increasing the surface area of the package with the addition of a heat sink or by blowing air across the package to promote improved heat dissipation.

APPLICATIONS INFORMATION (continued)

The following examples illustrate the thermal considerations necessary to increase the power capability of the MMH0026.

Assume that the ceramic package is to be used at a maximum ambient temperature (T_A) of +70°C. From Table 1: $R_{\theta JA(max)}$ = 150°C/watt, and from the maximum rating section of the data sheet: $T_J(max)$ = +175°C. Substituting the above values into equation (3) yields a maximum allowable power dissipation of 0.7 watts. Note that this same value may be read from Figure 17. Also note that this power dissipation value is for the device mounted in a socket.

Next, the maximum power consumed for a given system application must be determined. The power dissipation of the MOS clock driver is conveniently divided into dc and ac components. The dc power dissipation is given by:

$$P_{dc} = (V_{CC} - V_{EE}) \times (I_{CCL}) \times (\text{Duty Cycle}) \qquad (4)$$

$$\text{where } I_{CCL} = 40\ \text{mA} \left(\frac{V_{CC} - V_{EE}}{20\ \text{V}}\right).$$

Note that Figure 14 is a plot of equation (4) for three values of (V_{CC}–V_{EE}). For this example, suppose that the MOS clock driver is to be operated with V_{CC} = +16 V and V_{EE} = GND and with a 50% duty cycle. From equation (4) or Figure 14, the dc power dissipation (per driver) may be found to be 256 mW. If both drivers within the package are used in an identical way, the total dc power is 512 mW. Since the maximum total allowable power dissipation is 700 mW, the maximum ac power that can be dissipated for this example becomes:

$$P_{ac} = 0.7 - 0.512 = 188\ \text{mW}$$

The ac power for each driver is given by:

$$P_{ac} = (V_{CC} - V_{EE})^2 \times f \times C_L \qquad (5)$$

where f = frequency of operation

C_L = load capacitance (including all strays and wiring).

Figure 16 gives the maximum ac power dissipation versus switching frequency for various capacitive loads with V_{CC} = 16 V and V_{EE} = GND. Under the above conditions, and with the aid of Figure 15, the safe operating area beneath Curve A of Figure 18 can be generated.

Since both drivers have a maximum ac power dissipation of 188 mW, the maximum ac power per driver becomes 94 mW. A horizontal line intersecting all the capacitance load lines at the 94 mW level of Figure 15 will yield the maximum frequency of operation for each of the capacitive loads at the specified power level. By using the previous formulas and constants, a new safe operating area can be generated for any output voltage swing and duty cycle desired.

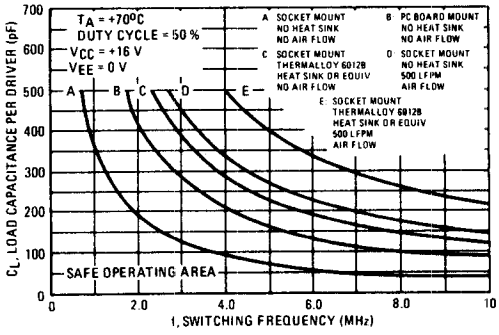
Note from Figure 18, that with highly capacitive loads, the maximum switching frequency is very low. The switching frequency can be increased by varying the following factors:

(a) decrease T_A
(b) decrease the duty cycle
(c) lower package thermal resistance ($R_{\theta JA}$)

In most cases conditions (a) and (b) are fixed due to system requirements. This leaves only the thermal resistance $R_{\theta JA}$ that can be varied.

Note from equation (2) that the thermal resistance is comprised of two parts. One is the junction-to-case thermal resistance ($R_{\theta JC}$) and the other is the case-to-ambient thermal resistance ($R_{\theta CA}$). Since the factor $R_{\theta JC}$ is a function of the die size and type of bonding employed, it cannot be varied. However, the $R_{\theta CA}$ term can be changed as previously discussed, see Page 7.

FIGURE 18 – LOAD CAPACITANCE versus FREQUENCY FOR "L" PACKAGE ONLY
(Both drivers used in identical way)



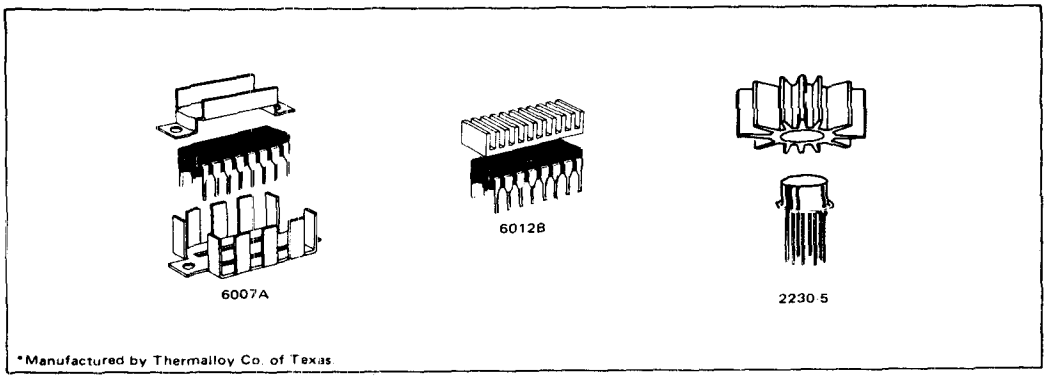
Heat Sink Considerations:

Heat sinks come in a wide variety of sizes and shapes that will accomodate almost any IC package made. Some of these heat sinks are illustrated in Figure 19. In the previous example, with the ceramic package, no heat sink and in a still air environment, $R_{\theta JA(max)}$ was 150°C/W.

For the following example the Thermalloy 6012B type heat sink, or equivalent, is chosen. With this heat sink, the $R_{\theta CA}$ for natural convection from Figure 20 is 44°C/W. From Table 1 $R_{\theta JC(max)}$ = 50°C/W for the ceramic

APPLICATIONS INFORMATION (continued)

FIGURE 19 – THERMALLOY* HEAT SINKS



*Manufactured by Thermalloy Co. of Texas

package. Therefore, the new $R_{\theta JA}$(max) with the 6012B heat sink added becomes:

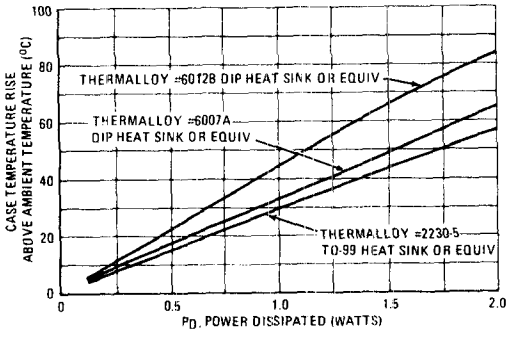
$$R_{\theta JA(max)} = 50^{o}C/W + 44^{o}C/W = 94^{o}C/W.$$

Thus the addition of the heat sink has reduced $R_{\theta JA}$(max) from 150°C/W down to 94°C/W. With the heat sink, the maximum power dissipation by equation (3) at T_A = +70°C is:

$$P_D = \frac{175^{o}C - 70^{o}C}{94^{o}C/W} = 1.11 \text{ watts.}$$

This gives approximately a 58% increase in maximum power dissipation. The safe operating area under Curve C of Figure 18 can now be generated as before with the aid of Figure 15 and equation (5).

FIGURE 20 – CASE TEMPERATURE RISE ABOVE AMBIENT versus POWER DISSIPATED USING NATURAL CONVECTION



Forced Air Considerations:

As illustrated in Figure 21, forced air can be employed to reduce the $R_{\theta JA}$ term. Note, however, that this curve is expressed in terms of typical $R_{\theta JA}$ rather than maximum $R_{\theta JA}$. Maximum $R_{\theta JA}$ can be determined in the following manner:

From Table 1 the following information is known:

(a) $R_{\theta JA(typ)} = 100^{o}$ C/W
(b) $R_{\theta JC(typ)} = 27^{o}$ C/W

Since:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad (6)$$

Then:

$$R_{\theta CA} = R_{\theta JA} - R_{\theta JC} \quad (7)$$

Therefore, in still air

$$R_{\theta CA(typ)} = 100^{o}C/W - 27^{o}C/W = 73^{o}C/W$$

From Curve 1 of Figure 21 at 500 LFPM and equation (7),

$$R_{\theta CA(typ)} = 53^{o}C/W - 27^{o}C/W = 26^{o}C/W.$$

Thus $R_{\theta CA}$(typ) has changed from 73°C/W (still air) to 26°C/W (500 LFPM), which is a decrease in typical $R_{\theta CA}$ by a ratio of 1:2.8. Since the typical value of $R_{\theta CA}$ was reduced by a ratio of 1:2.8, $R_{\theta CA}$(max) of 100°C/W should also decrease by a ratio of 1:2.8.

This yields an $R_{\theta CA(max)}$ at 500 LFPM of 36°C/W.

Therefore, from equation (6):

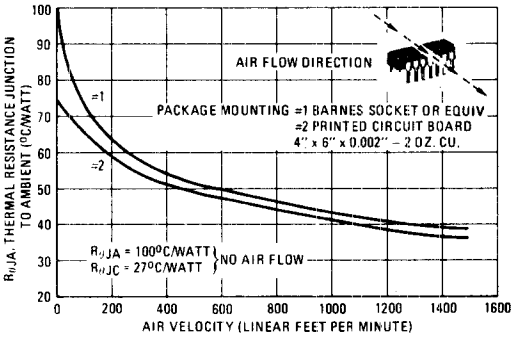
$$R_{\theta JA(max)} = 50^{o}C/W + 36^{o}C/W = 86^{o}C/W.$$

Therefore the maximum allowable power dissipation at 500 LFPM and T_A = +70°C is from equation (3):

$$P_D = \frac{175^{o}C - 70^{o}C}{+86^{o}C/W} = 1.2 \text{ watts.}$$

APPLICATIONS INFORMATION (continued)

FIGURE 21 – TYPICAL THERMAL RESISTANCE ($R_{\theta JA}$) OF "L" PACKAGE versus AIR VELOCITY



As with the previous examples, the dc power at 50% duty cycle is subtracted from the maximum allowable device dissipation (P_D) to obtain a maximum P_{ac}. The safe operating area under Curve D of Figure 18 can now be generated from Figure 15 and equation (5).

Heat Sink and Forced Air Combined:

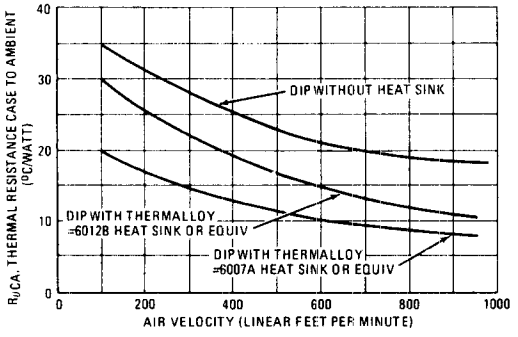
Some heat sink manufacturers provide data and curves of $R_{\theta CA}$ for still air and forced air such as illustrated in Figure 22. For example the 6012B heat sink has an $R_{\theta CA}$ = 17°C/W at 500 LFPM as noted in Figure 22. From equation (6):

$$\text{Max } R_{\theta JA} = 50^{\circ}C/W + 17^{\circ}C/W = 67^{\circ}C/W$$

From equation (3) at T_A = +70°C

$$P_D = \frac{175^{\circ}C - 70^{\circ}C}{67^{\circ}C/W} = 1.57 \text{ watts.}$$

FIGURE 22 – THERMAL RESISTANCE $R_{\theta CA}$ versus AIR VELOCITY



As before this yields a safe operating area under Curve E in Figure 18.

Note from Table 1 and Figure 21 that if the 14-pin ceramic package is mounted directly to the PC board (2 oz. cu. underneath), that typical $R_{\theta JA}$ is considerably less than for socket mount with still air and no heat sink. The following procedure can be employed to determine a safe operating area for this condition.

Given data from Table 1:

$$\text{typical } R_{\theta JA} = 100^{\circ}C/W$$
$$\text{typical } R_{\theta JC} = 27^{\circ}C/W$$

From Curve 2 of Figure 21, $R_{\theta JA}$(typ) is 75°C/W for a PC mount and no air flow. Then the typical $R_{\theta CA}$ is 75°C/W – 27°C/W = 48°C/W. From Table 1 the typical value of $R_{\theta CA}$ for socket mount is 100°C/W – 27°C/W = 73°C/W. This shows that the PC board mount results in a decrease in typical $R_{\theta CA}$ by a ratio of 1:1.5 below the typical value of $R_{\theta CA}$ in a socket mount. Therefore, the maximum value of socket mount $R_{\theta CA}$ of 100°C/W should also decrease by a ratio of 1:1.5 when the device is mounted in a PC board. The maximum $R_{\theta CA}$ becomes:

$$R_{\theta CA} = \frac{100^{\circ}C/W}{1.5} = 66^{\circ}C/W \text{ for PC board mount}$$

Therefore the maximum $R_{\theta JA}$ for a PC mount is from equation (6).

$$R_{\theta JA} = 50^{\circ}C/W + 66^{\circ}C/W = 116^{\circ}C/W.$$

With maximum $R_{\theta JA}$ known, the maximum power dissipation can be found and the safe operating area determined as before. See Curve B in Figure 18.

CONCLUSION

In most cases, heat sink manufacturer's publish only $R_{\theta CA}$ socket mount data. Although $R_{\theta CA}$ data for PC mounting is generally not available, this should present no problem. Note in Figure 21 that an air flow greater than 250 LFPM yields a socket mount $R_{\theta JA}$ approximately 6% greater than for a PC mount. Therefore, the socket mount data can be used for a PC mount with a slightly greater safety factor. Also it should be noted that thermal resistance measurements can vary widely. These measurement variations are due to the dependency of $R_{\theta CA}$ on the type environment and measurement techniques employed. For example, $R_{\theta CA}$ would be greater for an integrated circuit mounted on a PC board with little or no ground plane versus one with a substantial ground plane. Therefore, if the maximum calculated junction temperature is on the border line of being too high for a given system application, then thermal resistance measurements should be done on the system to be absolutely certain that the maximum junction temperature is not exceeded.

TYPICAL APPLICATIONS

FIGURE 23 – AC-COUPLED MOS CLOCK DRIVER

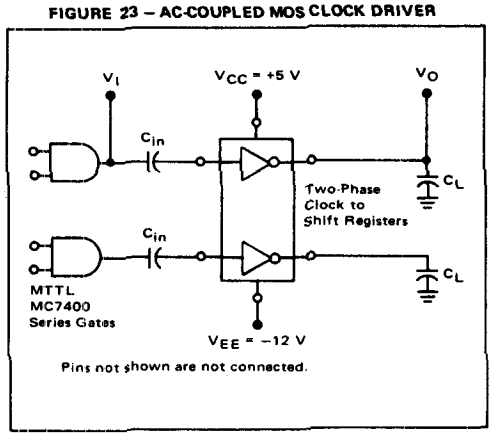


FIGURE 24 – DC-COUPLED RAM MEMORY ADDRESS OR PRECHARGE DRIVER (POSITIVE-SUPPLY ONLY)