

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : SVCC
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : SGND1
LAYER 8 : BOT

Cable Docking

- VGA
- RJ-45
- CIR/Pwr btn
- SPDIF Out
- Stereo MIC
- Headphone Jack
- USB Port
- VOL Cntr

PAGE 38

SYSTEM CHARGER ISL6251AHAZ-
PAGE 39

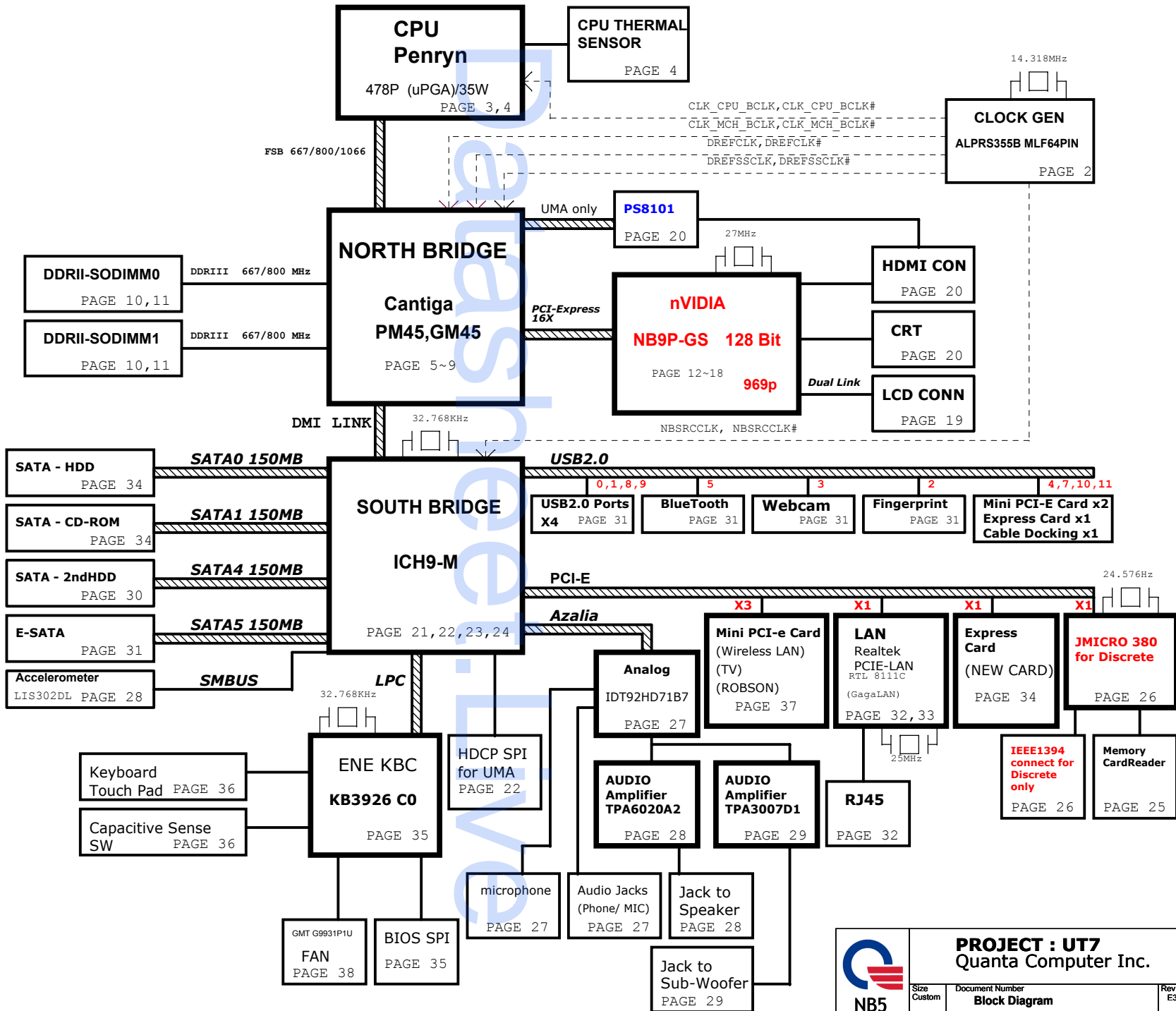
SYSTEM POWER ISL6237IRZ-T
PAGE 40

DDR II SMDDR_VTERM 1.8V/1.8VSUS(TPS51116REGR)
PAGE 44

VCCP +1.5V AND GMCH 1.05V(RT8204)
PAGE 44

VGACORE(1.025V)Oz8118
PAGE 43

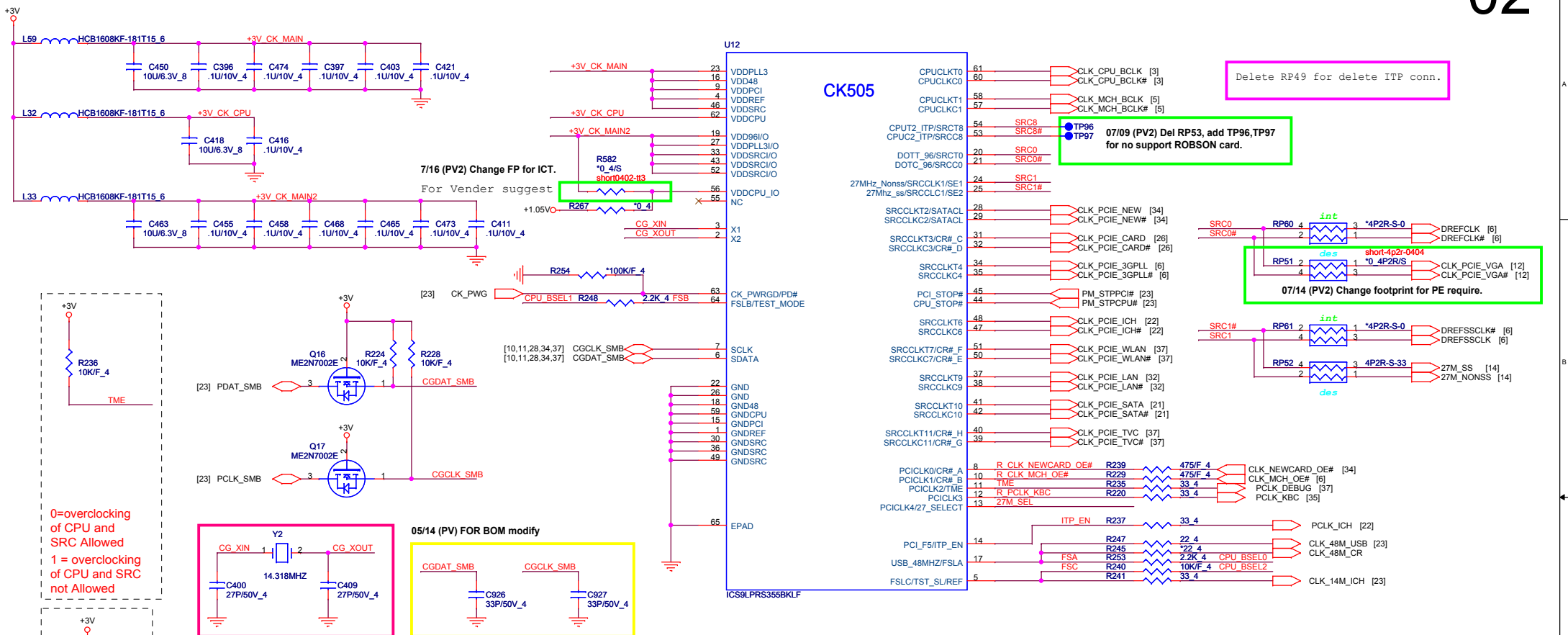
CPU CORE ISL6266A
PAGE 42



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Quanta Computer Inc.

NB5

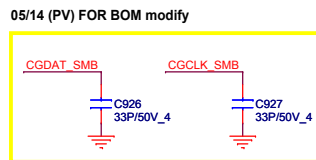
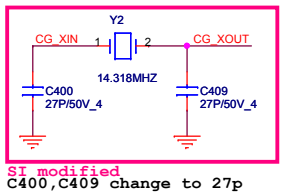
Size Custom	Document Number	Rev E3A
Block Diagram		
Date: Friday, July 18, 2008	Sheet 1	of 46



Delete RP49 for delete ITP conn.

07/09 (PV2) Del RP53, add TP96, TP97 for no support ROBSON card.

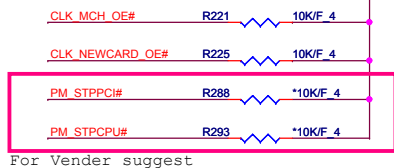
07/14 (PV2) Change footprint for PE require.



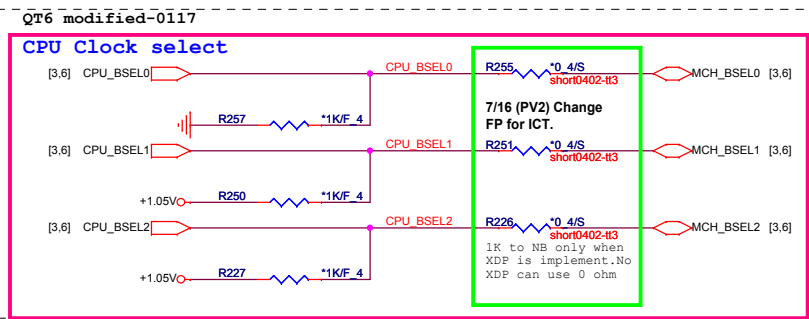
SI modified C400, C409 change to 27p

27M_SEL PIN13	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

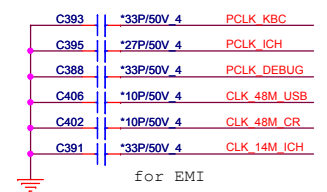
CK505 QFN64
 ICS ICS9LPRS355BKLF ALPRS355000
 Silego SLG8SP513VTR AL8SP513000
 Realtek RTM875N-606-VD-GR AL000875000



For Vender suggest



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	1	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33



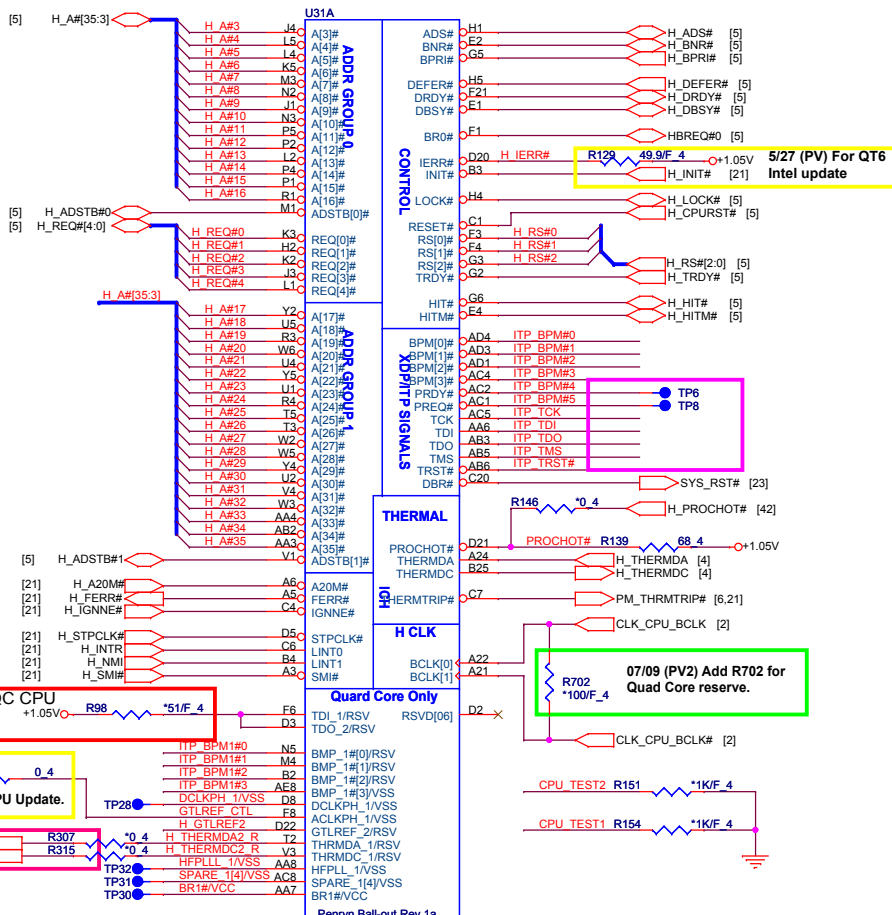
for EMI

0=overclocking of CPU and SRC Allowed
 1 = overclocking of CPU and SRC not Allowed

0=UMA
 1 = External VGA

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Size Custom	Document Number	Rev E3A
Clock Generator		
Date: Friday, July 18, 2008	Sheet 2 of 46	



NI for Quad Core

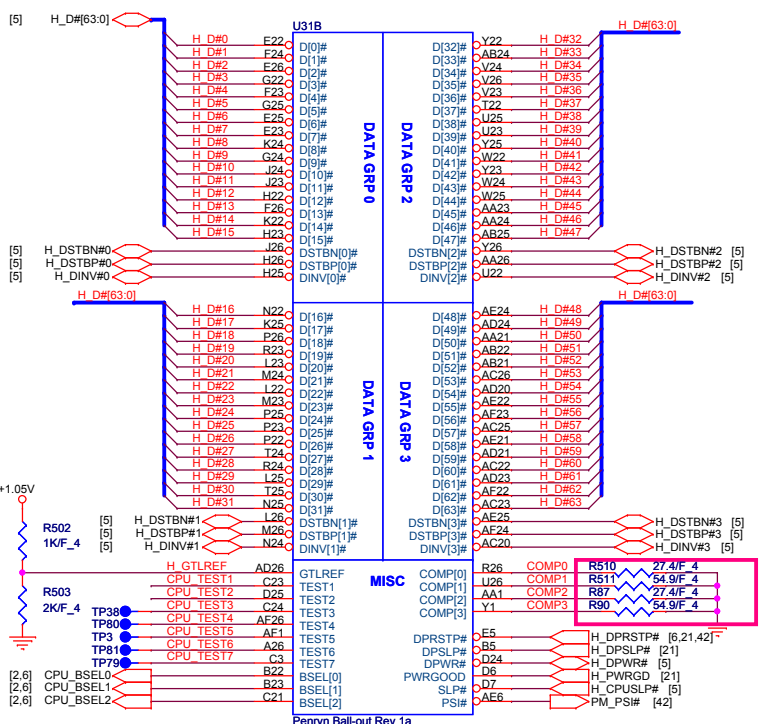
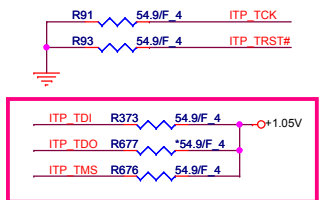
For QC CPU +1.05V 51/F 4

05/20 (PV) FOR INTEL CPU Update. TP28

For QC CPU R307, R315

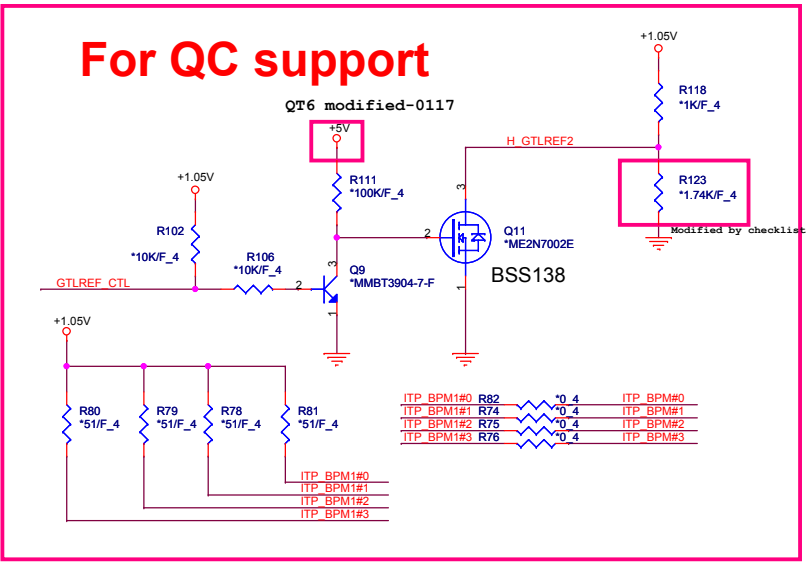
MODEL	UT7 Quad Core	UT6 Dual Core
R696	*0_4	0_4

Populate ITP700Flex for bringup



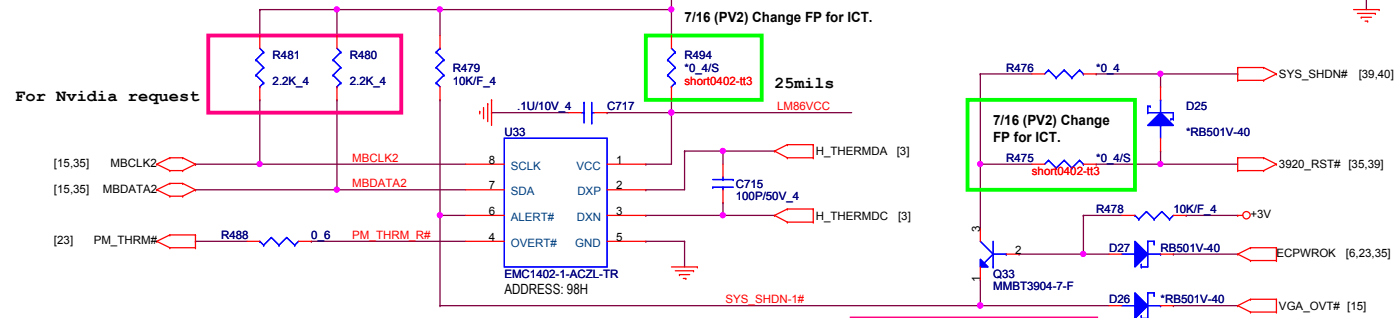
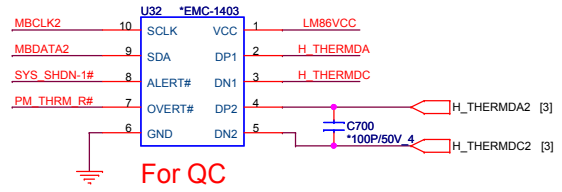
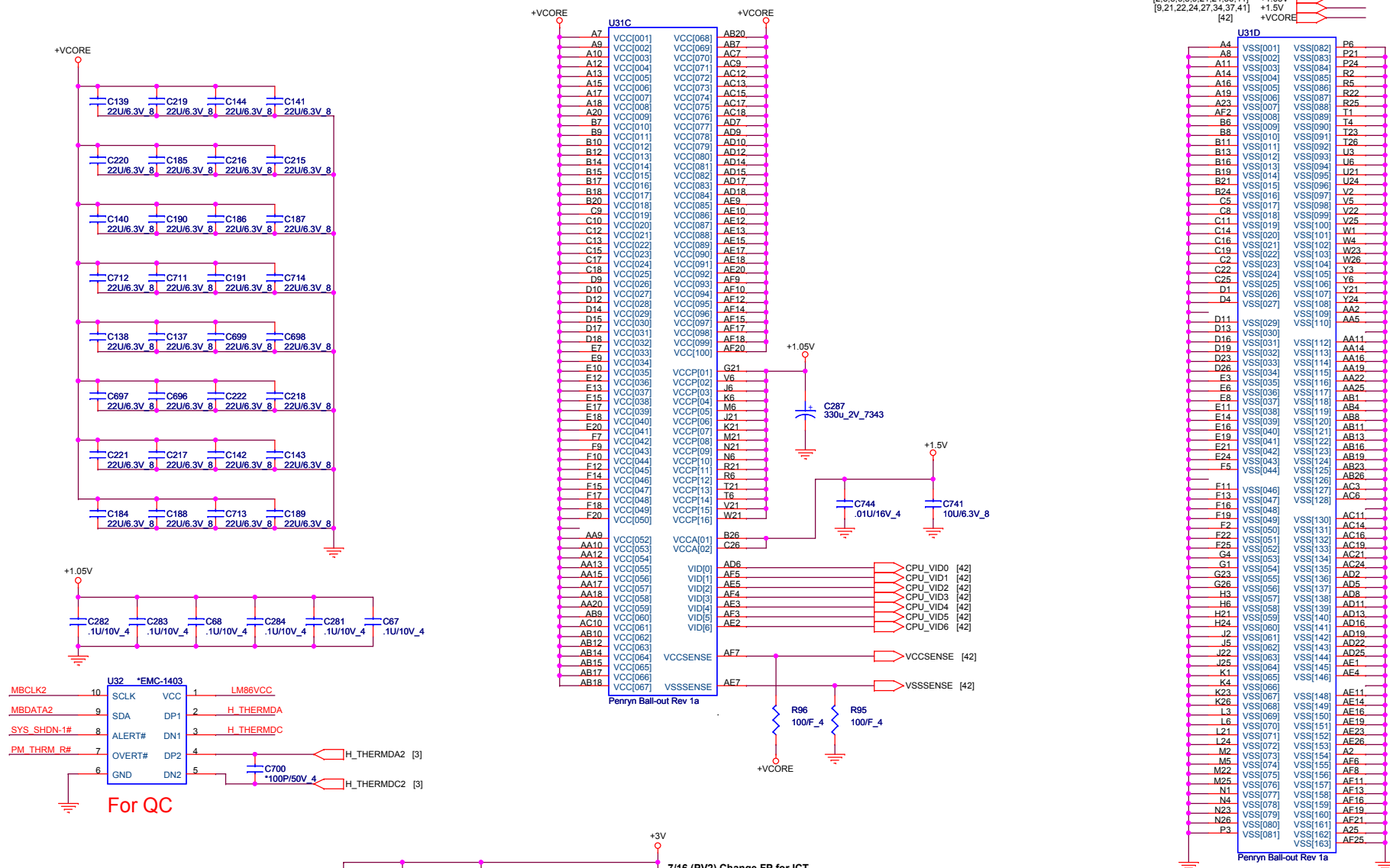
R503 --> 1.74K for Quad Core

	COMP0/2	COMP1/3
Dual Core	27.4 Ohm (CS02742FB19)	54.9 Ohm (CS05492FB19)
Quad Core	24.9 Ohm (CS0492FB29)	49.9 Ohm (CS04992FB31)



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Size Custom	Document Number	Rev
	Penryn 1/2	E3A
Date: Friday, July 18, 2008	Sheet 3 of 46	



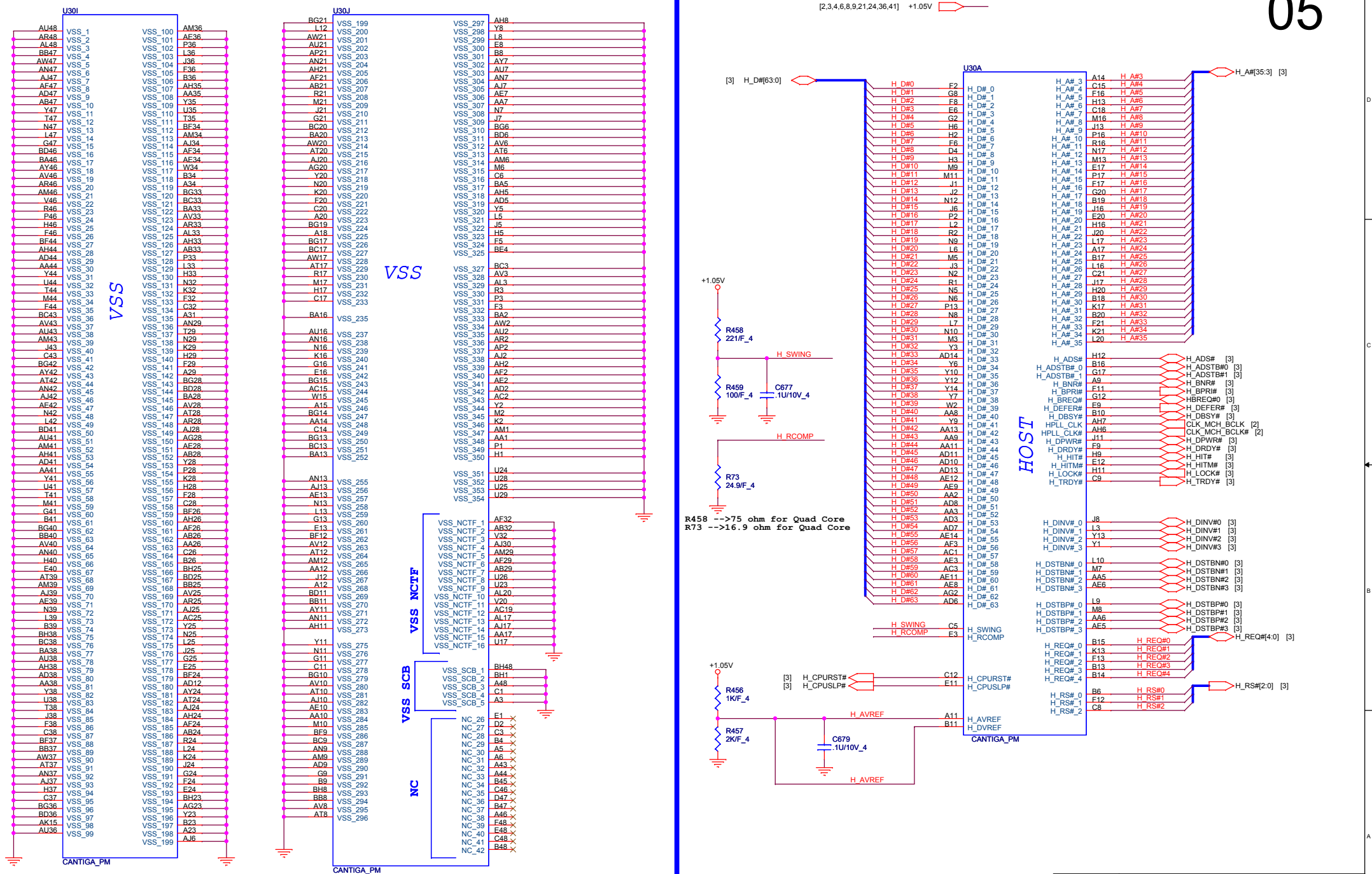
Delete net: SYS_SHDN-1#
QT6 Modified-0117

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Size Custom Document Number Penryn & TH Monitor 2/2 Rev E3A

Date: Friday, July 18, 2008 Sheet 4 of 46

[2,3,4,6,8,9,21,24,36,41] +1.05V



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Size Custom Document Number
Canitiga Host & VSS 1/5

Rev E3A

Date: Friday, July 18, 2008 Sheet 5 of 46

MCH_CFG_5 DMIX2 selection
Low = DMI X2
High = DMI X4 (Default)
MCH_CFG_16 FSB Dynamic ODT
Low = Dynamic ODT disabled
High = Dynamic ODT enabled (default)

MCH_CFG_9 PCI Express Graphic Lane
Low = Reverse Lane
High = Normal operation(Default)
MCH_CFG_19 DMI Lane Reverse
Low = Normal operation (Default)
High = Reverse Lanes

MCH_CFG_6 ITPM Host Interface
Low = The ITPM Host Interface is enabled
High = The ITPM Host Interface is disabled (default)

MCH_CFG_7 Intel(R) Management Engine Crypto
Low = Intel(R) Management Engine Crypto
High = The ITPM Host Interface is disabled (default)

MCH_CFG_10 PCIe Lookback Enable
Low = Enabled
High = Disabled (Default)

MCH_CFG_12/13 XOR/ALLZ/CLOCK Un-gating

MCH_CFG_13 MCH_CFG_12 Configuration
0 0 Reserved
0 0 XOR Mode enabled
0 1 All-Z Mode enabled
1 1 Normal operation (Default)

MCH_CFG_20
Digital Display Port (SDVO/DP/HDMI) Concurrent with PCIe
Low = Only digital display port (SDVO/DP/HDMI) or PCIe is operational (default)
High = Digital display port (SDVO/DP/HDMI) and PCIe are operating simultaneously via the PEG port

MCH_CFG2:0
000 = FSB1066
010 = FSB800
011 = FSB667
Others = Reserved

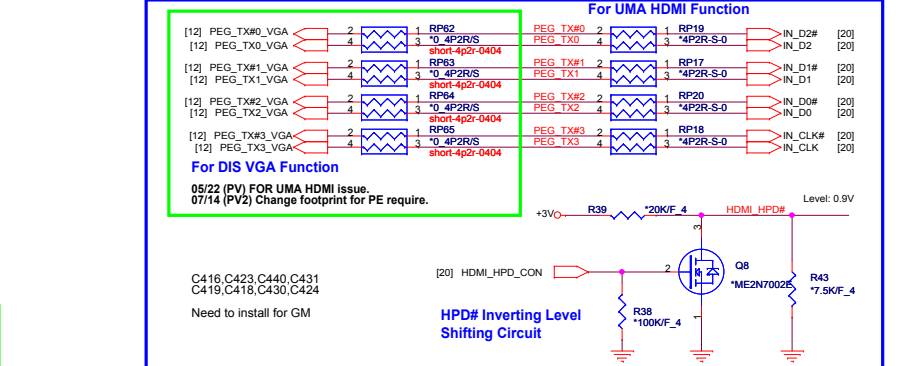
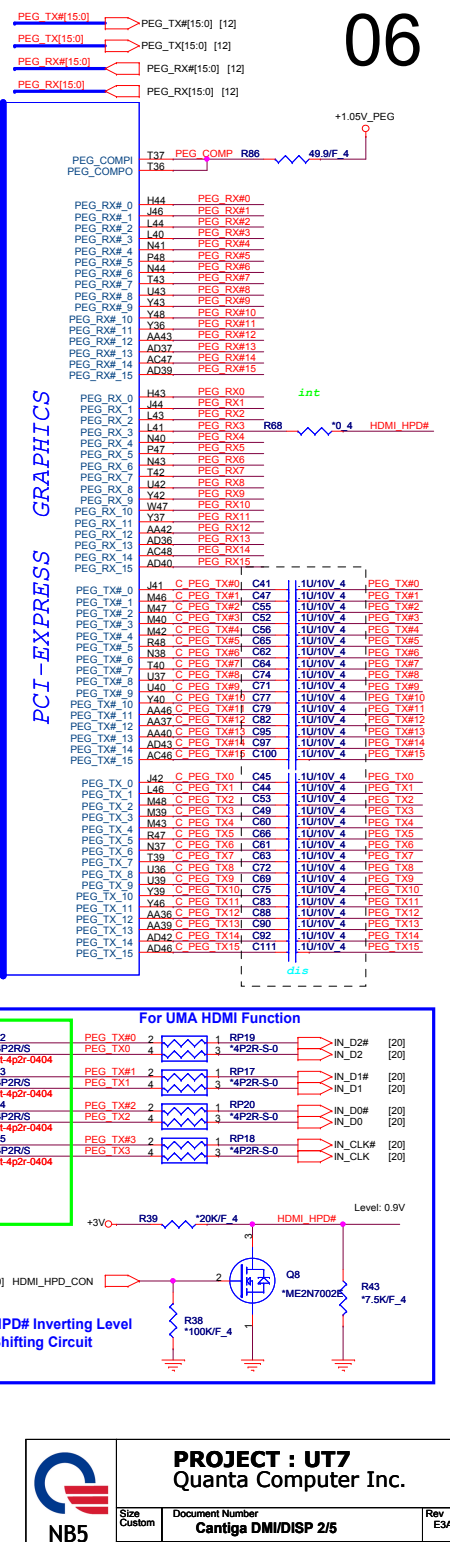
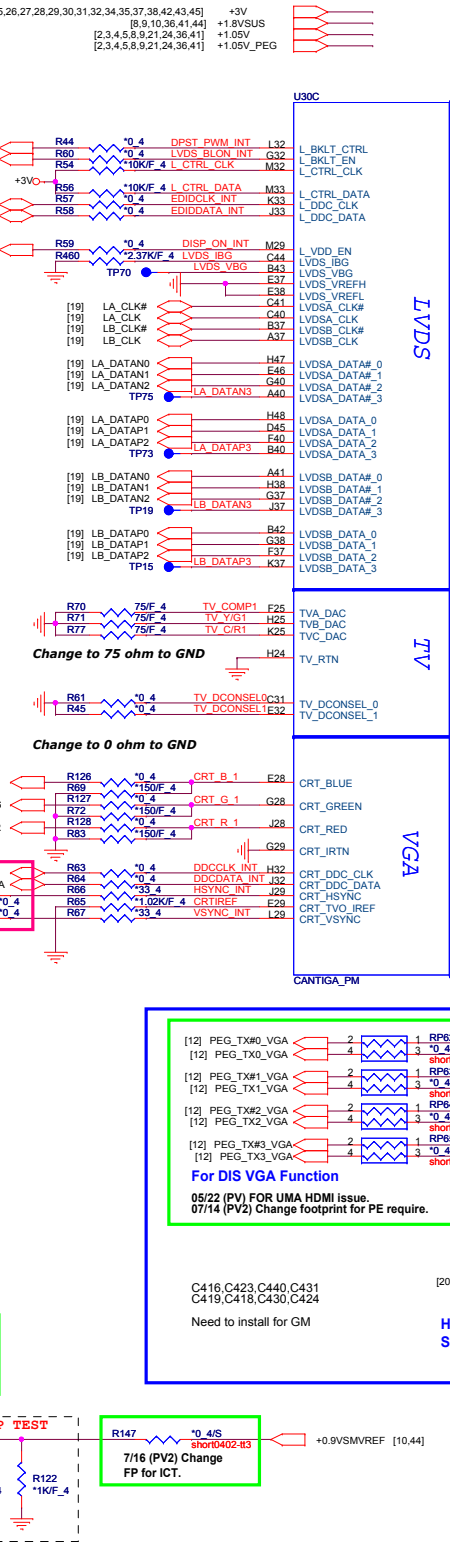
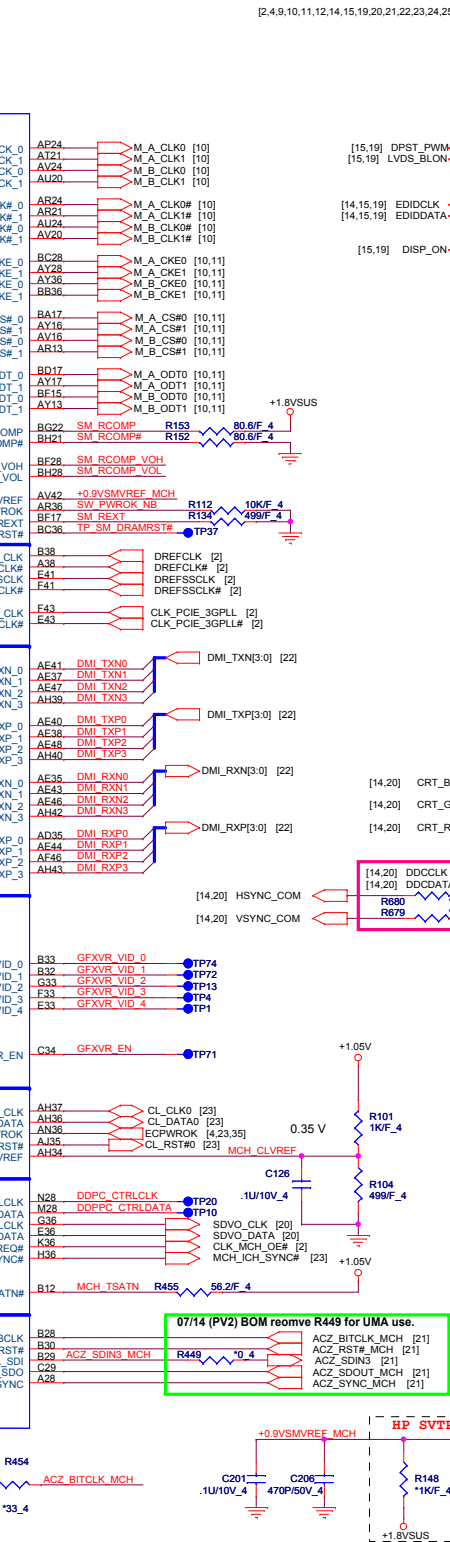
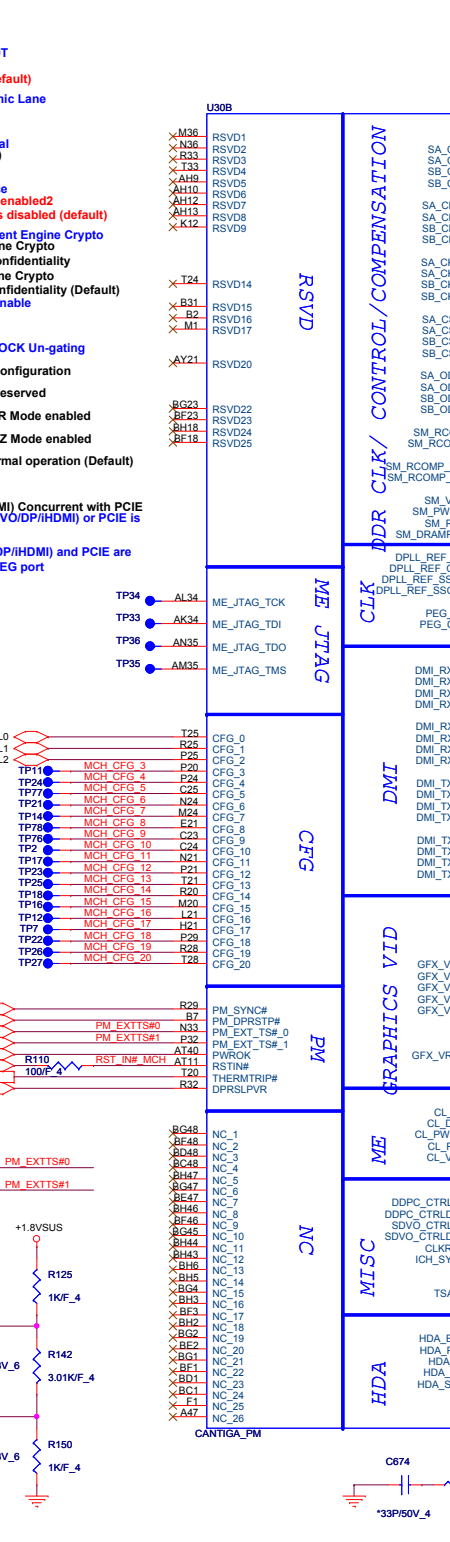
[2,3] MCH_BSEL0
[2,3] MCH_BSEL1
[2,3] MCH_BSEL2

[3,21,42] H_DPRSTP#
[10,11] PM_EXTTS#0
[11] PM_EXTTS#1
[23,42] DELAY_VR_PWRGND
[3,21] PM_THRMTRIP#
[23,42] DPRSLPVR

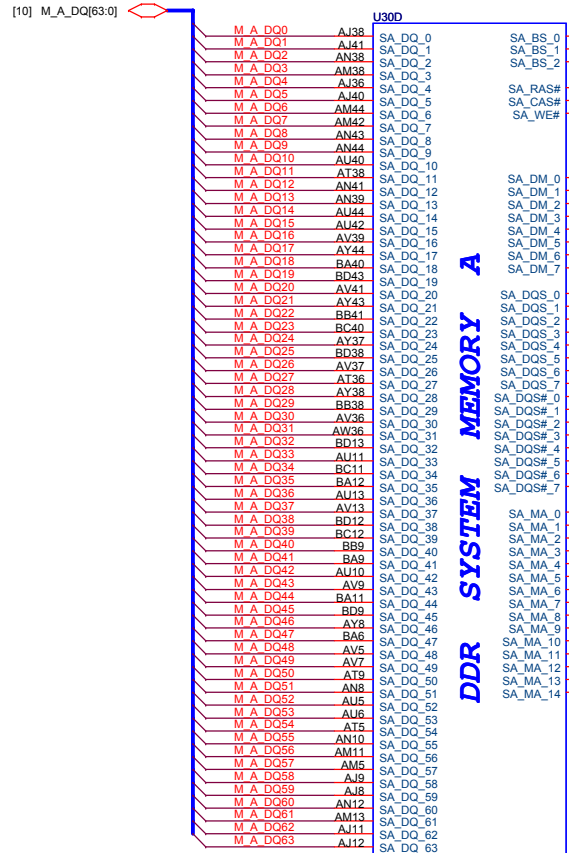
[23] PM_SYNC#
[3,21,42] H_DPRSTP#
[10,11] PM_EXTTS#0
[11] PM_EXTTS#1
[23,42] DELAY_VR_PWRGND
[3,21] PM_THRMTRIP#
[23,42] DPRSLPVR

[23] PM_SYNC#
[3,21,42] H_DPRSTP#
[10,11] PM_EXTTS#0
[11] PM_EXTTS#1
[23,42] DELAY_VR_PWRGND
[3,21] PM_THRMTRIP#
[23,42] DPRSLPVR

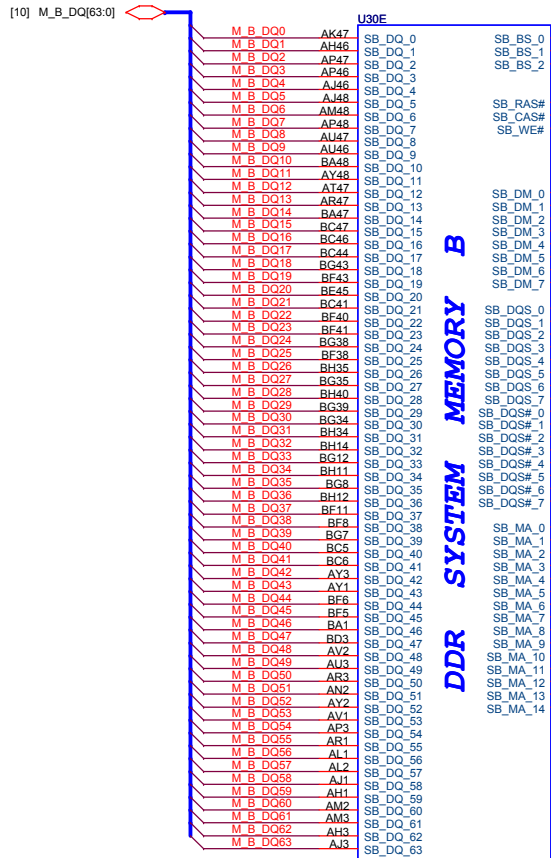
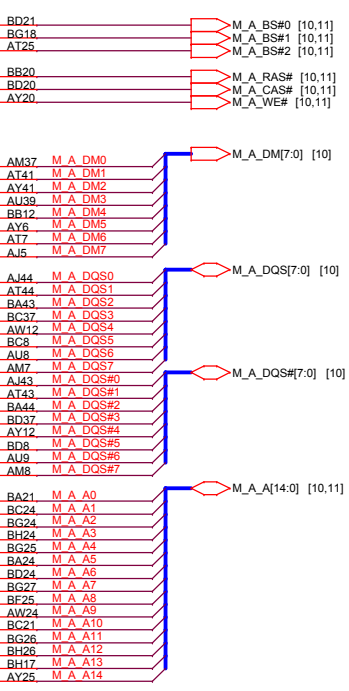
[23] PM_SYNC#
[3,21,42] H_DPRSTP#
[10,11] PM_EXTTS#0
[11] PM_EXTTS#1
[23,42] DELAY_VR_PWRGND
[3,21] PM_THRMTRIP#
[23,42] DPRSLPVR



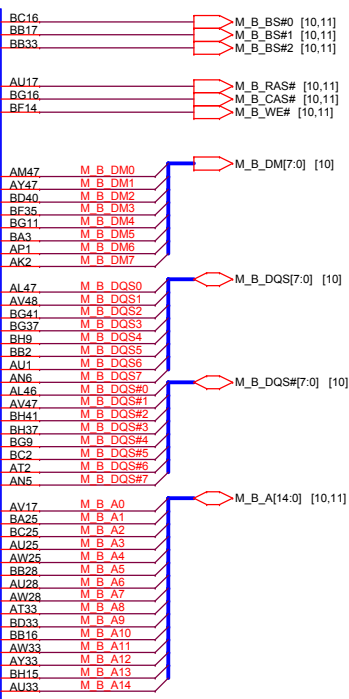
PROJECT : UT7
Quanta Computer Inc.
NB5
Date: Friday, July 16, 2008
Sheet 6 of 48



CANTIGA_PM



CANTIGA_PM



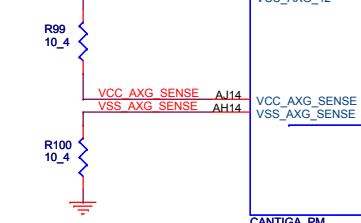
U30G

AP33	VCC_SM_1
AH32	VCC_SM_2
BG32	VCC_SM_3
BF32	VCC_SM_4
BD32	VCC_SM_5
BC32	VCC_SM_6
BB32	VCC_SM_7
BA32	VCC_SM_8
AY32	VCC_SM_9
AW32	VCC_SM_10
AV32	VCC_SM_11
AU32	VCC_SM_12
AT32	VCC_SM_13
AR32	VCC_SM_14
AP32	VCC_SM_15
AN32	VCC_SM_16
BH31	VCC_SM_17
BG31	VCC_SM_18
BF31	VCC_SM_19
BD31	VCC_SM_20
BC29	VCC_SM_21
BB29	VCC_SM_22
BA29	VCC_SM_23
AY29	VCC_SM_24
AW29	VCC_SM_25
AU29	VCC_SM_26
AT29	VCC_SM_27
AR29	VCC_SM_28
AP29	VCC_SM_29
AA29	VCC_SM_30
AA29	VCC_SM_31
AU29	VCC_SM_32
AT29	VCC_SM_33
AR29	VCC_SM_34
AP29	VCC_SM_35
BA36	VCC_SM_36/NC
BB24	VCC_SM_37/NC
BD16	VCC_SM_38/NC
BB21	VCC_SM_39/NC
AW16	VCC_SM_40/NC
AW13	VCC_SM_41/NC
AT13	VCC_SM_42/NC

VCC_SM_36 through VCC_SM_42 can be left as NC for DDR2 desigs.

+1.05V

Y26	VCC_AGX_1
AE25	VCC_AGX_2
AB25	VCC_AGX_3
AA25	VCC_AGX_4
AE24	VCC_AGX_5
AC24	VCC_AGX_6
AA24	VCC_AGX_7
Y24	VCC_AGX_8
AE23	VCC_AGX_9
AC23	VCC_AGX_10
AB23	VCC_AGX_11
AA23	VCC_AGX_12
AJ21	VCC_AGX_13
AG21	VCC_AGX_14
AE21	VCC_AGX_15
AC21	VCC_AGX_16
AA21	VCC_AGX_17
Y21	VCC_AGX_18
AH20	VCC_AGX_19
AE20	VCC_AGX_20
AE20	VCC_AGX_21
AC20	VCC_AGX_22
AB20	VCC_AGX_23
AA20	VCC_AGX_24
T17	VCC_AGX_25
T16	VCC_AGX_26
AM15	VCC_AGX_27
AL15	VCC_AGX_28
AE15	VCC_AGX_29
AJ15	VCC_AGX_30
AH15	VCC_AGX_31
AG15	VCC_AGX_32
AF15	VCC_AGX_33
AB15	VCC_AGX_34
AA15	VCC_AGX_35
Y15	VCC_AGX_36
U15	VCC_AGX_37
AN14	VCC_AGX_38
AM14	VCC_AGX_39
U14	VCC_AGX_40
T14	VCC_AGX_41
T14	VCC_AGX_42

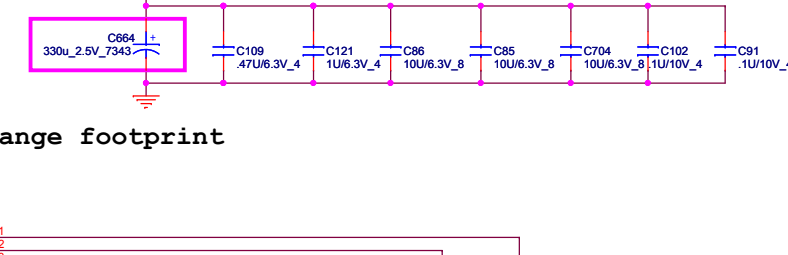
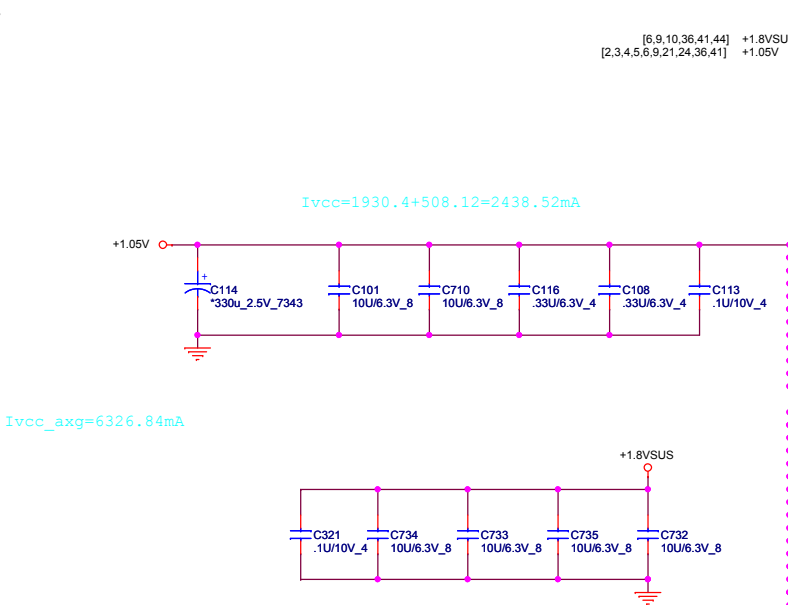
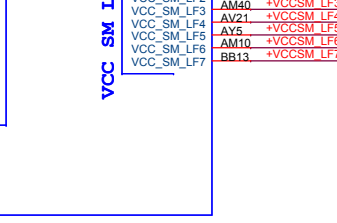


VCC AXG NCTF

W28	VCC_AGX_NCTF_1
V28	VCC_AGX_NCTF_2
W26	VCC_AGX_NCTF_3
V26	VCC_AGX_NCTF_4
W25	VCC_AGX_NCTF_5
V25	VCC_AGX_NCTF_6
W24	VCC_AGX_NCTF_7
V24	VCC_AGX_NCTF_8
W23	VCC_AGX_NCTF_9
V23	VCC_AGX_NCTF_10
AM21	VCC_AGX_NCTF_11
AL21	VCC_AGX_NCTF_12
AK21	VCC_AGX_NCTF_13
W21	VCC_AGX_NCTF_14
V21	VCC_AGX_NCTF_15
U21	VCC_AGX_NCTF_16
AM20	VCC_AGX_NCTF_17
AK20	VCC_AGX_NCTF_18
W20	VCC_AGX_NCTF_19
U20	VCC_AGX_NCTF_20
AM19	VCC_AGX_NCTF_21
AL19	VCC_AGX_NCTF_22
AK19	VCC_AGX_NCTF_23
W20	VCC_AGX_NCTF_24
AH19	VCC_AGX_NCTF_25
AG19	VCC_AGX_NCTF_26
AF19	VCC_AGX_NCTF_27
AE19	VCC_AGX_NCTF_28
AB19	VCC_AGX_NCTF_29
AA19	VCC_AGX_NCTF_30
Y19	VCC_AGX_NCTF_31
W19	VCC_AGX_NCTF_32
V19	VCC_AGX_NCTF_33
U19	VCC_AGX_NCTF_34
AM17	VCC_AGX_NCTF_35
AK17	VCC_AGX_NCTF_36
AH17	VCC_AGX_NCTF_37
AG17	VCC_AGX_NCTF_38
AF17	VCC_AGX_NCTF_39
AE17	VCC_AGX_NCTF_40
AC17	VCC_AGX_NCTF_41
AB17	VCC_AGX_NCTF_42
Y17	VCC_AGX_NCTF_43
W17	VCC_AGX_NCTF_44
V17	VCC_AGX_NCTF_45
U16	VCC_AGX_NCTF_46
AL16	VCC_AGX_NCTF_47
AK16	VCC_AGX_NCTF_48
AJ16	VCC_AGX_NCTF_49
AH16	VCC_AGX_NCTF_50
AG16	VCC_AGX_NCTF_51
AE16	VCC_AGX_NCTF_52
AE16	VCC_AGX_NCTF_53
AC16	VCC_AGX_NCTF_54
AB16	VCC_AGX_NCTF_55
AA16	VCC_AGX_NCTF_56
Y16	VCC_AGX_NCTF_57
W16	VCC_AGX_NCTF_58
V16	VCC_AGX_NCTF_59
U16	VCC_AGX_NCTF_60

VCC GFX NCTF

AV44	+VCCSM_LF1
BA37	+VCCSM_LF2
JAM40	+VCCSM_LF3
AV21	+VCCSM_LF4
AY5	+VCCSM_LF5
AM10	+VCCSM_LF6
BB13	+VCCSM_LF7



[6,9,10,36,41,44] +1.8VUSUS

[2,3,4,5,6,9,21,24,36,41] +1.05V

U30F

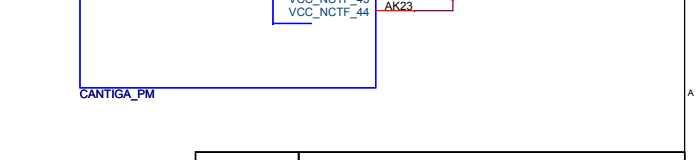
AG34	VCC_1
AC34	VCC_2
AB34	VCC_3
VCC_4	VCC_4
AA34	VCC_5
Y34	VCC_6
U34	VCC_7
V34	VCC_8
AM33	VCC_9
AK33	VCC_10
AJ33	VCC_11
AG33	VCC_12
AF33	VCC_13
AE33	VCC_14
AA33	VCC_15
Y33	VCC_16
W33	VCC_17
V33	VCC_18
U33	VCC_19
AH28	VCC_20
AF28	VCC_21
AC28	VCC_22
AA28	VCC_23
AJ26	VCC_24
AG26	VCC_25
AE26	VCC_26
AC26	VCC_27
AH25	VCC_28
AG25	VCC_29
AE25	VCC_30
AA24	VCC_31
AJ23	VCC_32
AH23	VCC_33
AF23	VCC_34
T32	VCC_35

VCC CORE

VCC_NCTF_1	AM32
VCC_NCTF_2	AL32
VCC_NCTF_3	AK32
VCC_NCTF_4	AJ32
VCC_NCTF_5	AH32
VCC_NCTF_6	AE32
VCC_NCTF_7	AC32
VCC_NCTF_8	AA32
VCC_NCTF_9	Y32
VCC_NCTF_10	W32
VCC_NCTF_11	U32
VCC_NCTF_12	AM30
VCC_NCTF_13	AL30
VCC_NCTF_14	AK30
VCC_NCTF_15	AH30
VCC_NCTF_16	AE30
VCC_NCTF_17	AC30
VCC_NCTF_18	AA30
VCC_NCTF_19	Y30
VCC_NCTF_20	W30
VCC_NCTF_21	U30
VCC_NCTF_22	V30
VCC_NCTF_23	W30
VCC_NCTF_24	V30
VCC_NCTF_25	U30
VCC_NCTF_26	U30
VCC_NCTF_27	AK29
VCC_NCTF_28	AJ29
VCC_NCTF_29	AH29
VCC_NCTF_30	AG29
VCC_NCTF_31	AE29
VCC_NCTF_32	AC29
VCC_NCTF_33	AA29
VCC_NCTF_34	Y29
VCC_NCTF_35	W29
VCC_NCTF_36	V29
VCC_NCTF_37	U29
VCC_NCTF_38	AK28
VCC_NCTF_39	AL28
VCC_NCTF_40	AK28
VCC_NCTF_41	AK26
VCC_NCTF_42	AK25
VCC_NCTF_43	AK24
VCC_NCTF_44	AK23

VCC NCTF

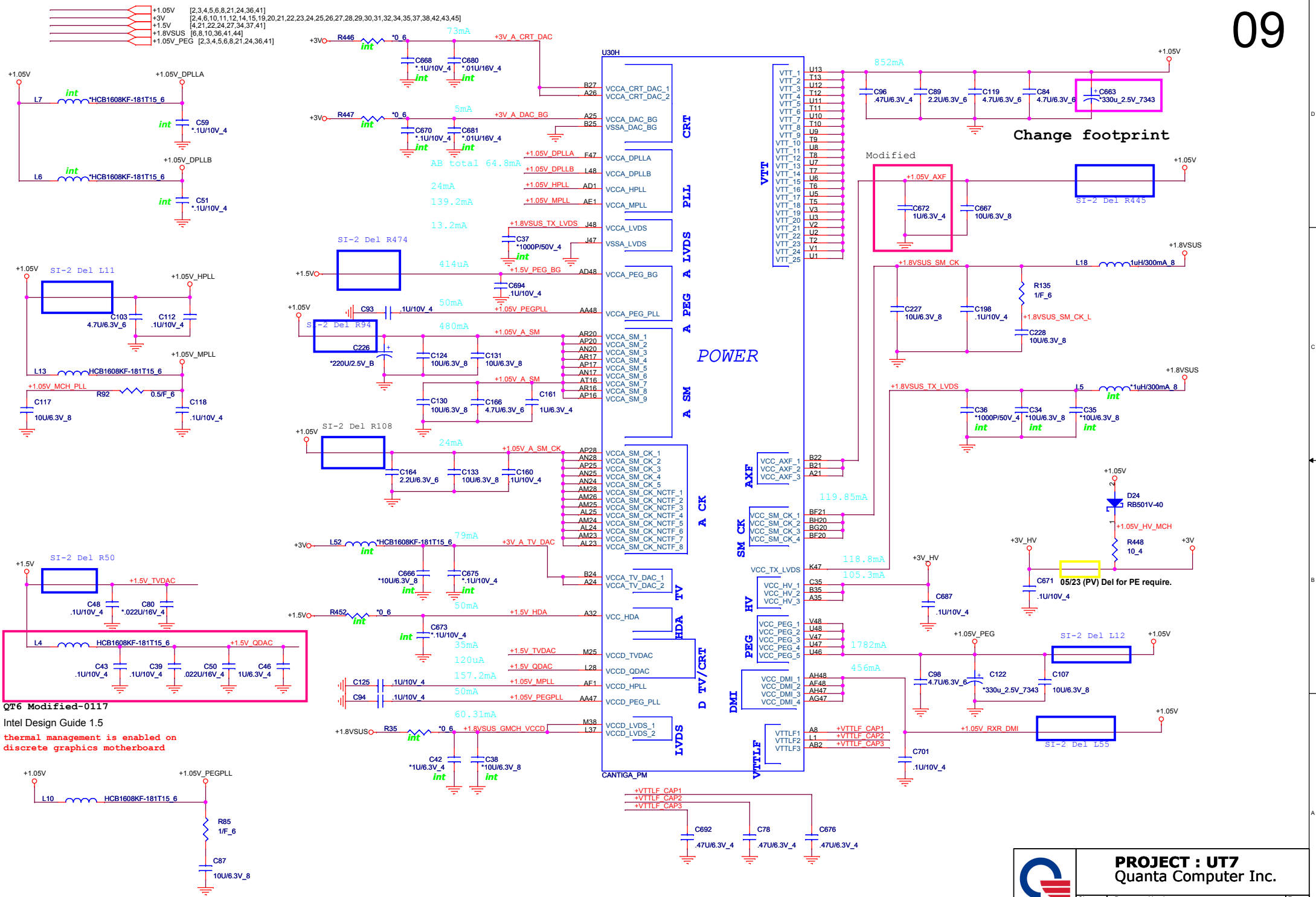
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VCC_NCTF_2	AL32
VCC_NCTF_3	AK32
VCC_NCTF_4	AJ32
VCC_NCTF_5	AH32
VCC_NCTF_6	AE32
VCC_NCTF_7	AC32
VCC_NCTF_8	AA32
VCC_NCTF_9	Y32
VCC_NCTF_10	W32
VCC_NCTF_11	U32
VCC_NCTF_12	AM30
VCC_NCTF_13	AL30
VCC_NCTF_14	AK30
VCC_NCTF_15	AH30
VCC_NCTF_16	AE30
VCC_NCTF_17	AC30
VCC_NCTF_18	AA30
VCC_NCTF_19	Y30
VCC_NCTF_20	W30
VCC_NCTF_21	U30
VCC_NCTF_22	V30
VCC_NCTF_23	W30
VCC_NCTF_24	V30
VCC_NCTF_25	U30
VCC_NCTF_26	U30
VCC_NCTF_27	AK29
VCC_NCTF_28	AJ29
VCC_NCTF_29	AH29
VCC_NCTF_30	AG29
VCC_NCTF_31	AE29
VCC_NCTF_32	AC29
VCC_NCTF_33	AA29
VCC_NCTF_34	Y29
VCC_NCTF_35	W29
VCC_NCTF_36	V29
VCC_NCTF_37	U29
VCC_NCTF_38	AK28
VCC_NCTF_39	AL28
VCC_NCTF_40	AK28
VCC_NCTF_41	AK26
VCC_NCTF_42	AK25
VCC_NCTF_43	AK24
VCC_NCTF_44	AK23



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Quanta Computer Inc.

Size Custom Document Number Cantiga Vcc 4/5 Rev E3A

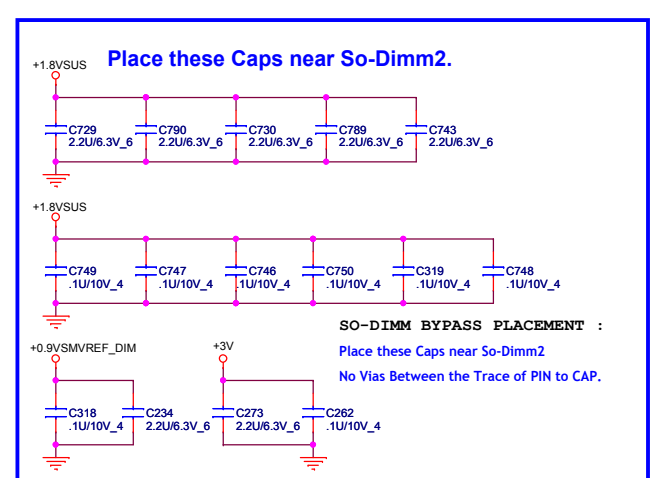
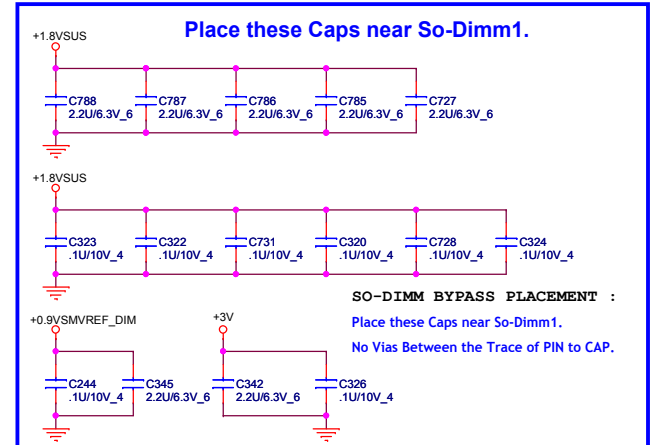
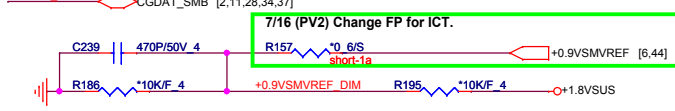
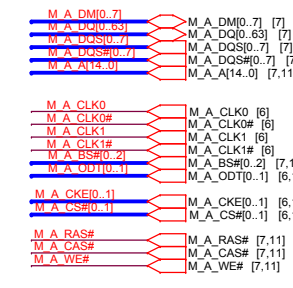
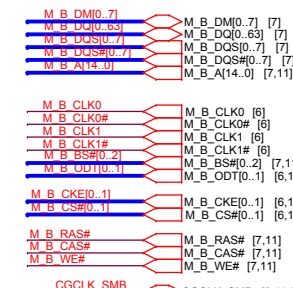
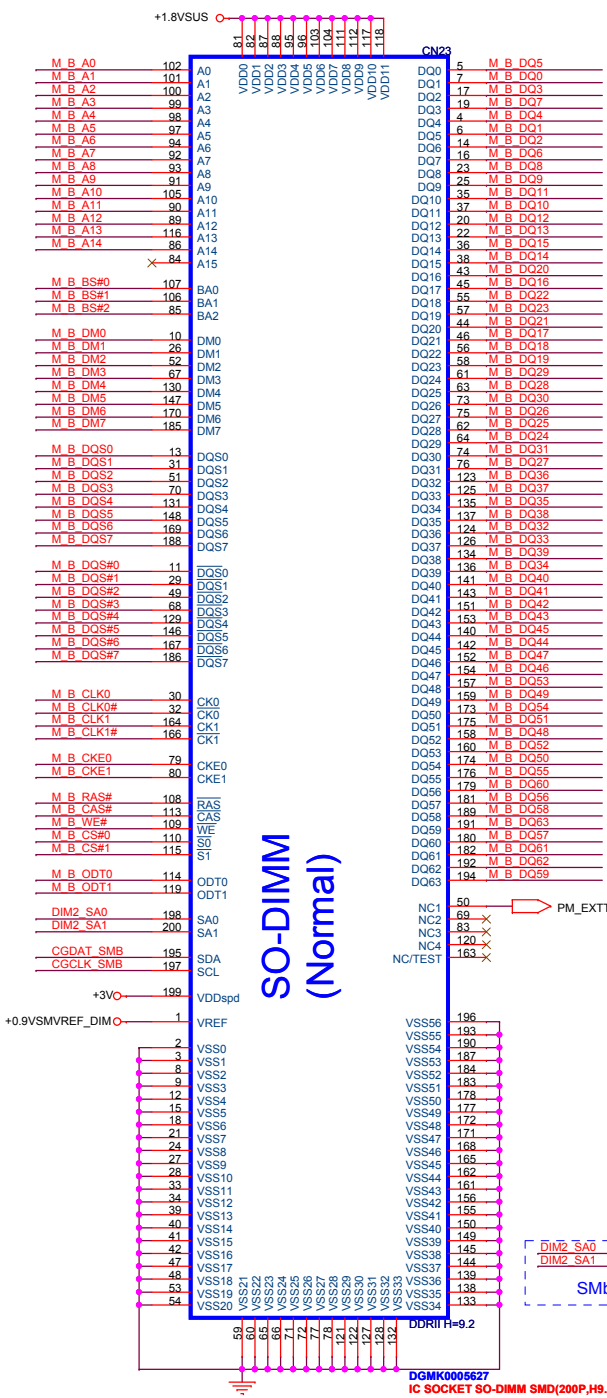
Date: Friday, July 18, 2008 Sheet 8 of 46



	PROJECT : UT7		Rev E3A
	Quanta Computer Inc.		
Size Custom	Document Number	Cantiga Power 5/5	
Date: Friday, July 18, 2008		Sheet 9	of 46

[2,4,6,9,11,12,14,15,19,20,21,22,23,24,25,26,27,28,29,30,31,32,34,35,37,38,42,43,45]

[6,8,9,36,41,44]



PROJECT : UT7
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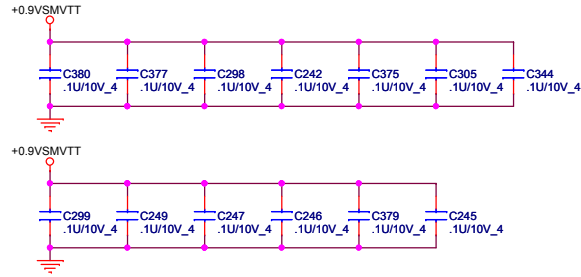
NB5

Size Custom Document Number **DDR2 DIMM** Rev E3A

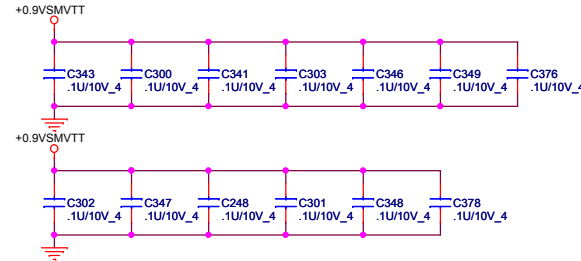
Date: Friday, July 18, 2008 Sheet 10 of 46

DDRII DUAL CHANNEL A,B.

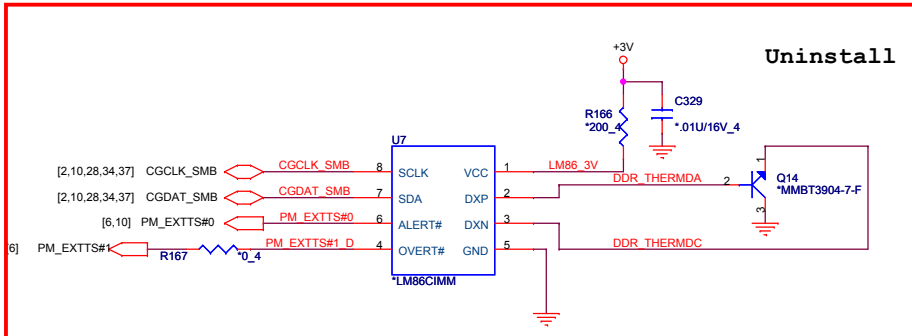
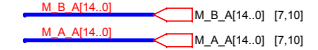
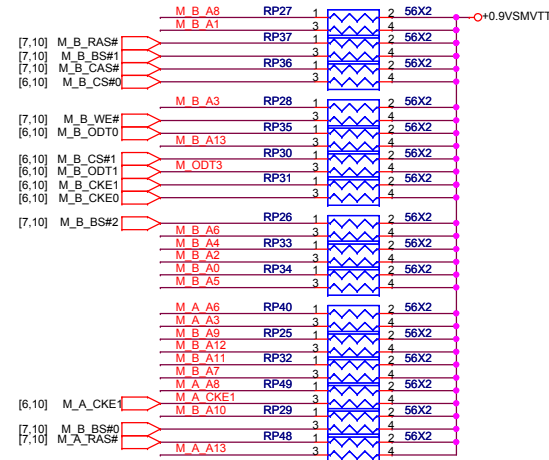
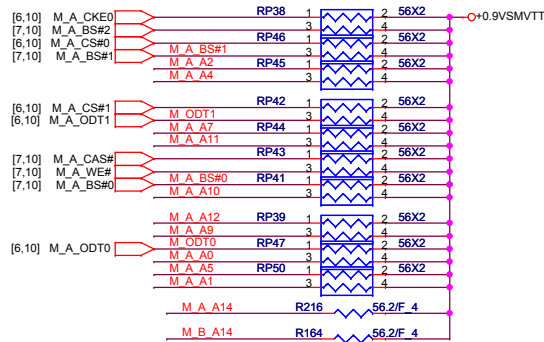
DDRII A CHANNEL



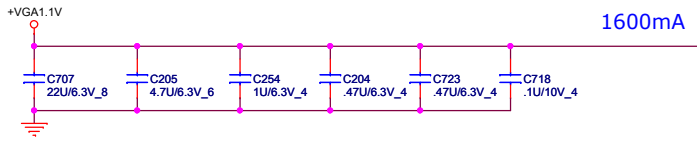
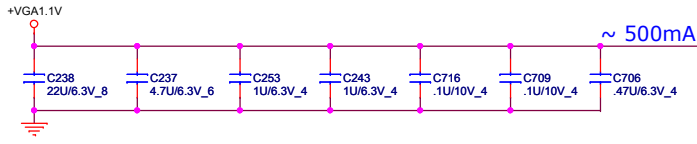
DDRII B CHANNEL



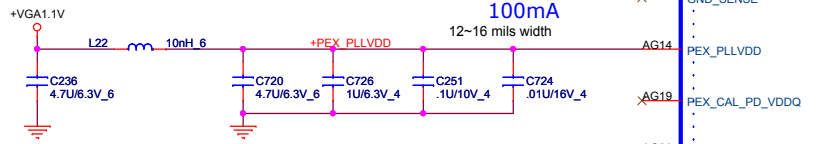
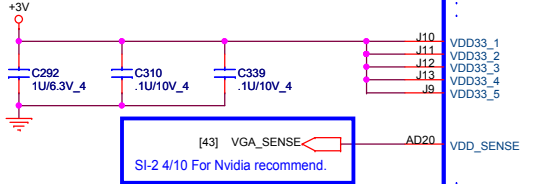
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM



[2,4,6,9,10,11,14,15,19,20,21,22,23,24,25,26,27,28,29,30,31,32,34,35,37,38,42,43,45] +3V [13,14,44] +VGA1.1V



Near BGA

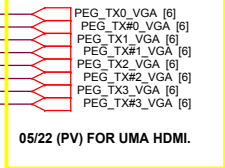


U35A
BG969-NVIDIA-NB9P-GS
COMMON

- AK16 PEX_IOVDD_1
- AK17 PEX_IOVDD_2
- AK21 PEX_IOVDD_3
- AK24 PEX_IOVDD_4
- AK27 PEX_IOVDD_5
- AG11 PEX_IOVDDQ_1
- AG12 PEX_IOVDDQ_2
- AG13 PEX_IOVDDQ_3
- AG15 PEX_IOVDDQ_3
- AG16 PEX_IOVDDQ_4
- AG17 PEX_IOVDDQ_5
- AG18 PEX_IOVDDQ_7
- AG22 PEX_IOVDDQ_8
- AG23 PEX_IOVDDQ_6
- AG24 PEX_IOVDDQ_9
- AG25 PEX_IOVDDQ_10
- AG26 PEX_IOVDDQ_12
- AJ14 PEX_IOVDDQ_13
- AJ15 PEX_IOVDDQ_14
- AJ19 PEX_IOVDDQ_15
- AJ21 PEX_IOVDDQ_16
- AJ22 PEX_IOVDDQ_17
- AJ24 PEX_IOVDDQ_18
- AJ25 PEX_IOVDDQ_19
- AJ27 PEX_IOVDDQ_20
- AK18 PEX_IOVDDQ_21
- AK20 PEX_IOVDDQ_22
- AK23 PEX_IOVDDQ_23
- AK26 PEX_IOVDDQ_24
- AL16 PEX_IOVDDQ_25

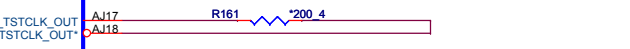
PCI EXPRESS

- PEX_RX0 AP17 PEG_TX0_VGA
- PEX_RX0* AP17 PEG_TX#0_VGA
- PEX_RX1* AN19 PEG_TX1_VGA
- PEX_RX1 AP19 PEG_TX#1_VGA
- PEX_RX2* AR19 PEG_TX2_VGA
- PEX_RX2 AP20 PEG_TX#2_VGA
- PEX_RX3* AR20 PEG_TX3_VGA
- PEX_RX3 AP20 PEG_TX#3_VGA
- PEX_RX3* AN22 PEG_TX4
- PEX_RX4* AP22 PEG_TX#4
- PEX_RX4 AP22 PEG_TX#5
- PEX_RX5* AR23 PEG_TX#5
- PEX_RX5 AP23 PEG_TX6
- PEX_RX6* AN23 PEG_TX#6
- PEX_RX6 AP25 PEG_TX7
- PEX_RX7* AP25 PEG_TX#7
- PEX_RX7 AP25 PEG_TX8
- PEX_RX8* AR26 PEG_TX#8
- PEX_RX8 AP26 PEG_TX9
- PEX_RX9* AN26 PEG_TX#9
- PEX_RX9 AP28 PEG_TX10
- PEX_RX10* AR28 PEG_TX#10
- PEX_RX10 AP29 PEG_TX11
- PEX_RX11* AR29 PEG_TX#11
- PEX_RX11 AP29 PEG_TX12
- PEX_RX12* AN29 PEG_TX#12
- PEX_RX12 AP31 PEG_TX13
- PEX_RX13* AR31 PEG_TX#13
- PEX_RX13 AP31 PEG_TX14
- PEX_RX14* AR32 PEG_TX#14
- PEX_RX14 AP34 PEG_TX15
- PEX_RX15* AR34 PEG_TX#15
- PEX_RX15 AP34 PEG_TX#15

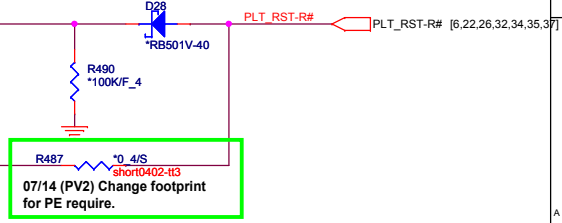


- PEX_TX0 AL17 C PEG_RX0 C171 .1U/10V_4
- PEX_TX0* AM17 C PEG_RX#0 C170 .1U/10V_4
- PEX_TX1 AM18 C PEG_RX1 C209 .1U/10V_4
- PEX_TX1* AM19 C PEG_RX#1 C210 .1U/10V_4
- PEX_TX2 AL19 C PEG_RX2 C172 .1U/10V_4
- PEX_TX2* AK19 C PEG_RX#2 C173 .1U/10V_4
- PEX_TX3 AL20 C PEG_RX3 C145 .1U/10V_4
- PEX_TX3* AM20 C PEG_RX#3 C146 .1U/10V_4
- PEX_TX4 AM21 C PEG_RX4 C211 .1U/10V_4
- PEX_TX4* AM22 C PEG_RX#4 C212 .1U/10V_4
- PEX_TX5 AL22 C PEG_RX5 C213 .1U/10V_4
- PEX_TX5* AK22 C PEG_RX#5 C214 .1U/10V_4
- PEX_TX6 AL23 C PEG_RX6 C147 .1U/10V_4
- PEX_TX6* AM23 C PEG_RX#6 C148 .1U/10V_4
- PEX_TX7 AM24 C PEG_RX7 C174 .1U/10V_4
- PEX_TX7* AK25 C PEG_RX#7 C175 .1U/10V_4
- PEX_TX8 AL25 C PEG_RX8 C149 .1U/10V_4
- PEX_TX8* AM26 C PEG_RX#8 C150 .1U/10V_4
- PEX_TX9 AL26 C PEG_RX9 C176 .1U/10V_4
- PEX_TX9* AM27 C PEG_RX#9 C177 .1U/10V_4
- PEX_TX10 AM28 C PEG_RX10 C151 .1U/10V_4
- PEX_TX10* AK28 C PEG_RX#10 C152 .1U/10V_4
- PEX_TX11 AL28 C PEG_RX11 C199 .1U/10V_4
- PEX_TX11* AK29 C PEG_RX#11 C200 .1U/10V_4
- PEX_TX12 AM29 C PEG_RX12 C178 .1U/10V_4
- PEX_TX12* AL29 C PEG_RX#12 C179 .1U/10V_4
- PEX_TX13 AM30 C PEG_RX13 C162 .1U/10V_4
- PEX_TX13* AM30 C PEG_RX#13 C163 .1U/10V_4
- PEX_TX14 AM31 C PEG_RX14 C156 .1U/10V_4
- PEX_TX14* AM32 C PEG_RX#14 C157 .1U/10V_4
- PEX_TX15 AM33 C PEG_RX15 C180 .1U/10V_4
- PEX_TX15* AP32 C PEG_RX#15 C181 .1U/10V_4

- PEX_REFCLK AR16 CLK_PCIE_VGA
- PEX_REFCLK* AR17 CLK_PCIE_VGA#



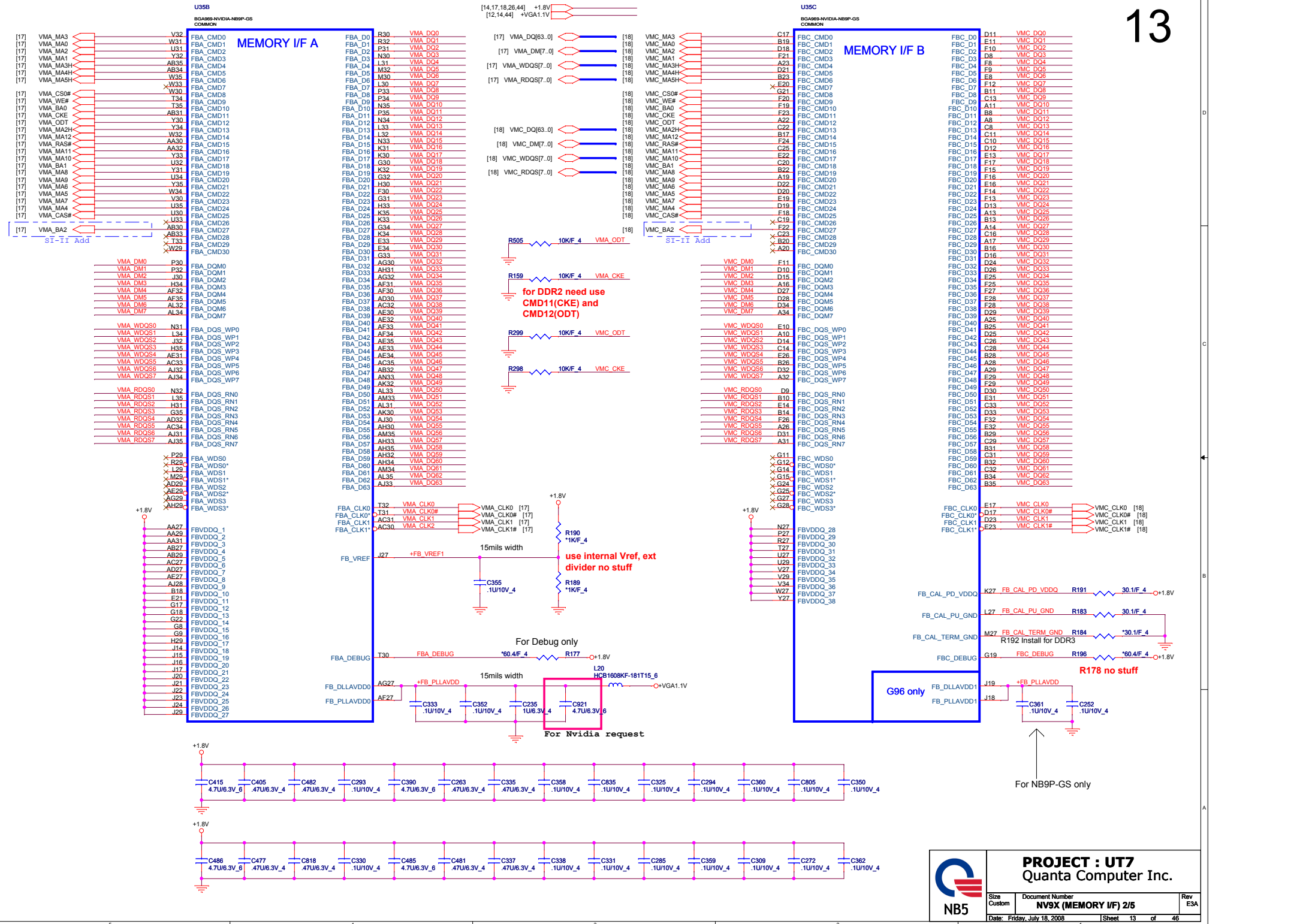
- PEX_RST# AM16 VGA_RST# R491 100/F_4
- PEX_RST#* AR13 PEX_CLKREQ# T5
- PEX_CLKREQ# AG21 PEX_TERM R165 2.49K/F_4
- PEX_TERM AP35 TESTMODE R486 10K/F_4
- TESTMODE



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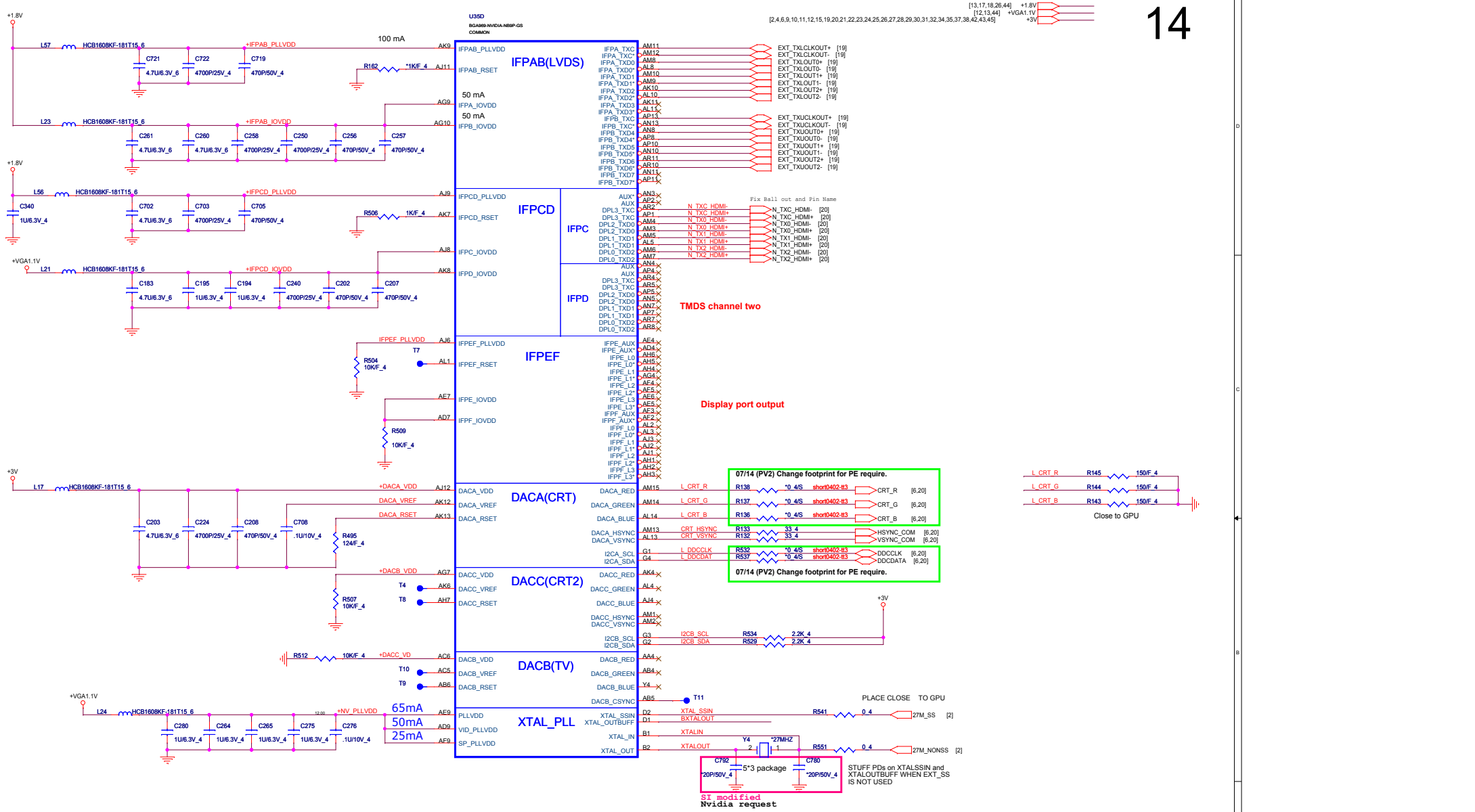
Size Custom Document Number **NV9X (PCIE I/F) 1/5** Rev E3A

Date: Friday, Jul 18, 2008 Sheet 12 of 46



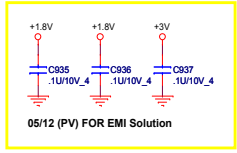
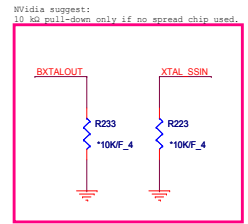
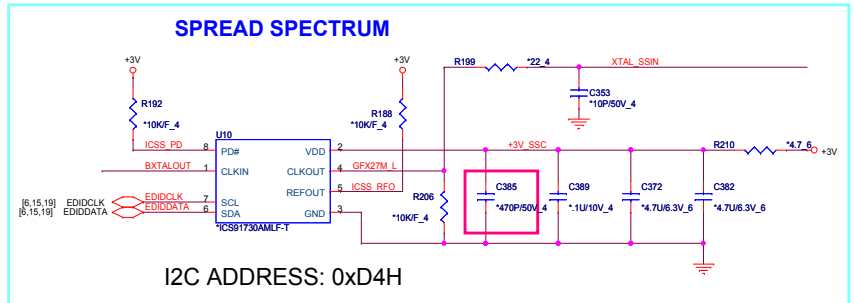
PROJECT : UT7
Quanta Computer Inc.

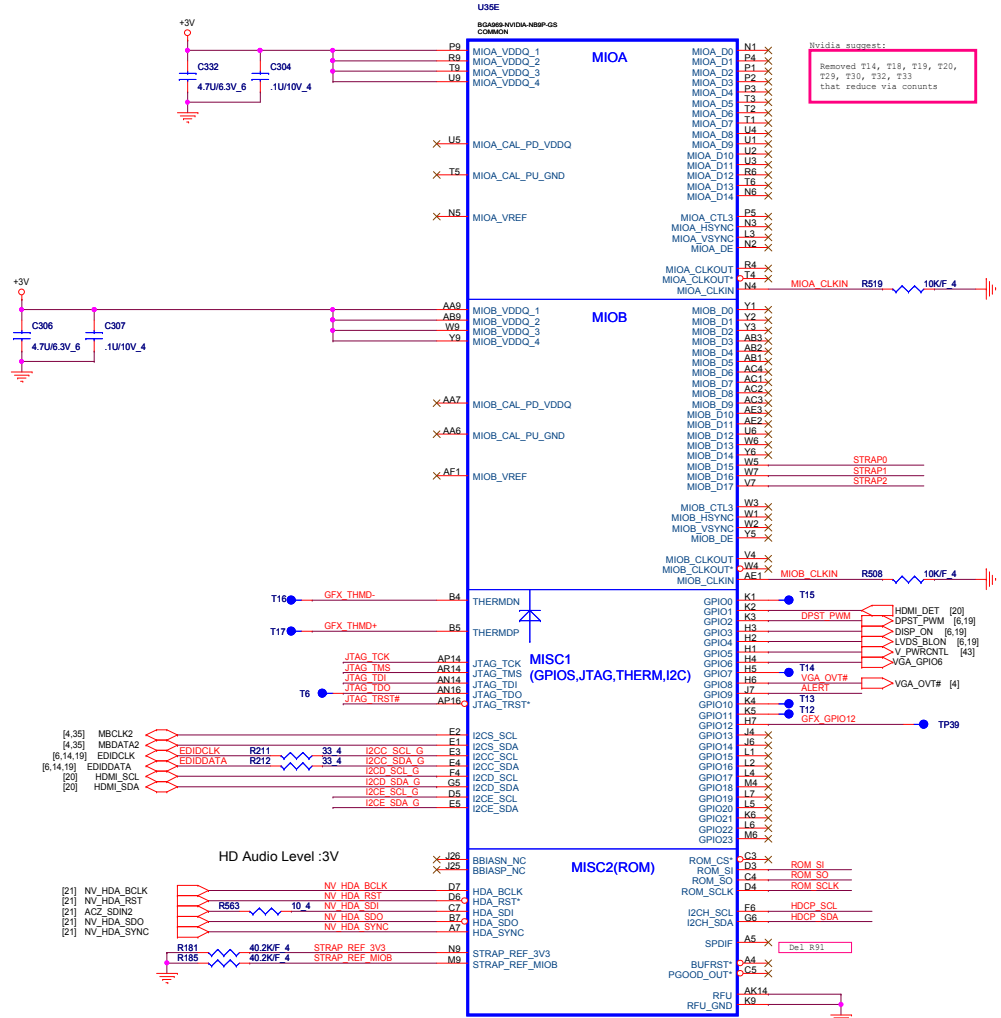
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Date: Friday, July 18, 2008	Sheet 13 of 46	



07/14 (PV2) Change footprint for PE require.

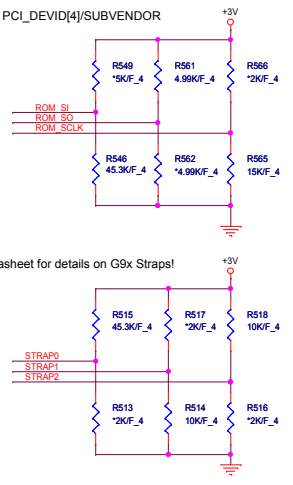
07/14 (PV2) Change footprint for PE require.





NB9P-GS (G96) Straps NB9M-GE (G98) Straps GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVDD VID0
6	OUT	N/A	NVDD VID1
7	OUT	N/A	FBVDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL

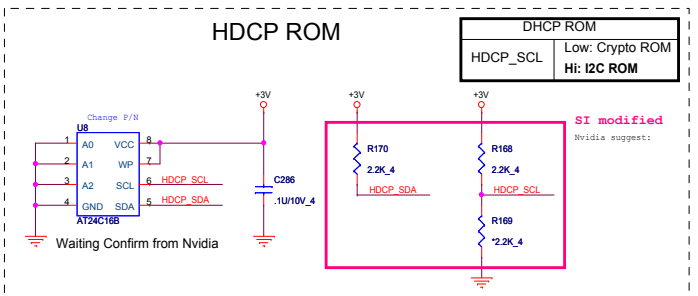


Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_277	TVMODE[2]	TVMODE[1]	TVMODE[0]	1000
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM100	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

Delete VGA thermal circuit

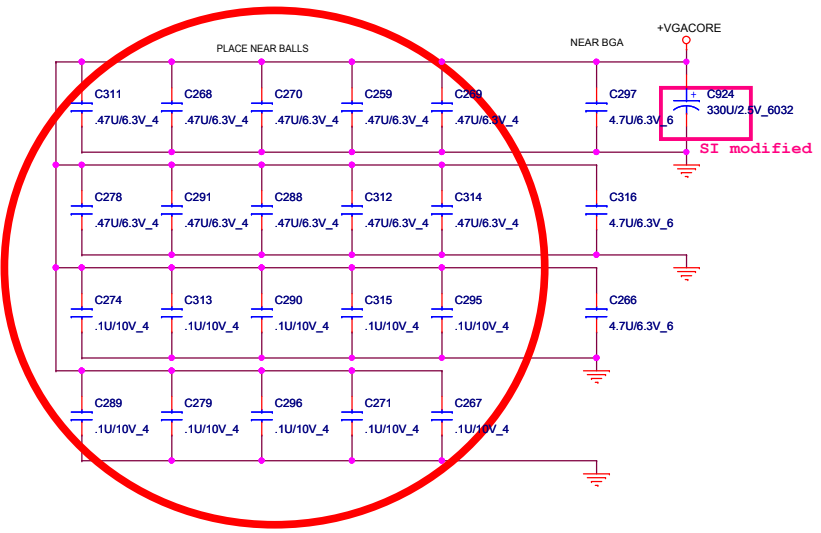
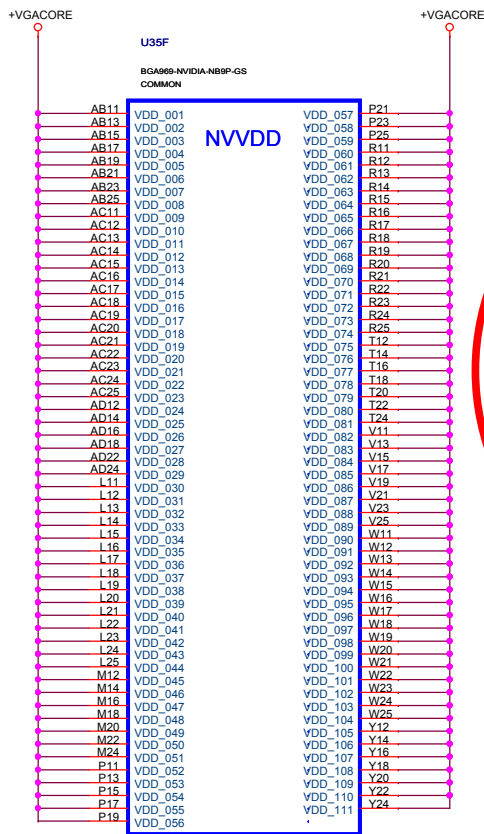


NB9X VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION	Vendor
0111	DDR2 32Mx16x8, 128bit, 512MB	Hynix HY5PS121621CFP-25
0110	DDR2 32Mx16x8, 128bit, 512MB	Qimonda HYB1S12161B2P-25
0101	DDR2 32Mx16x8, 128bit, 512MB	Samsung K4N51163QE-ZC25
0100	DDR2 32Mx16x8, 128bit, 512MB	Nanya/Elpida
0000	DDR2 64Mx16x8, 128bit, 1GB	Hynix
0001	DDR2 64Mx16x8, 128bit, 1GB	Samsung
0010	DDR2 64Mx16x8, 128bit, 1GB	Qimonda

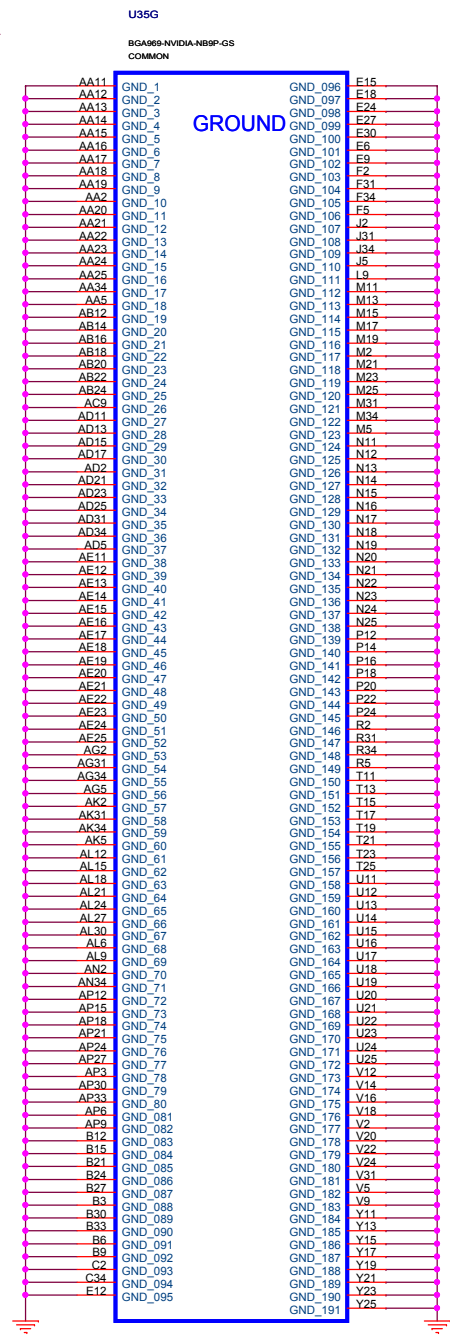
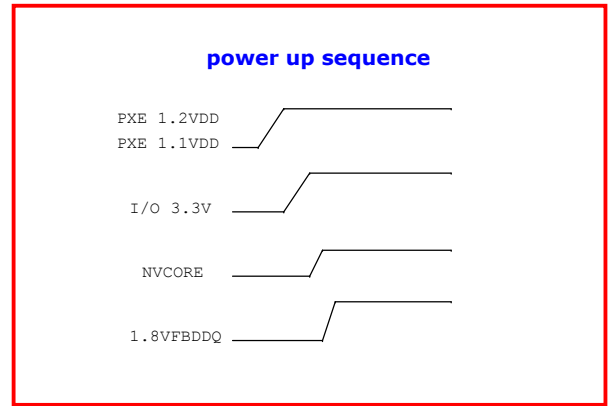
CS33572FB13 RES CHIP 35.7K 1/16W +-1% (0402)

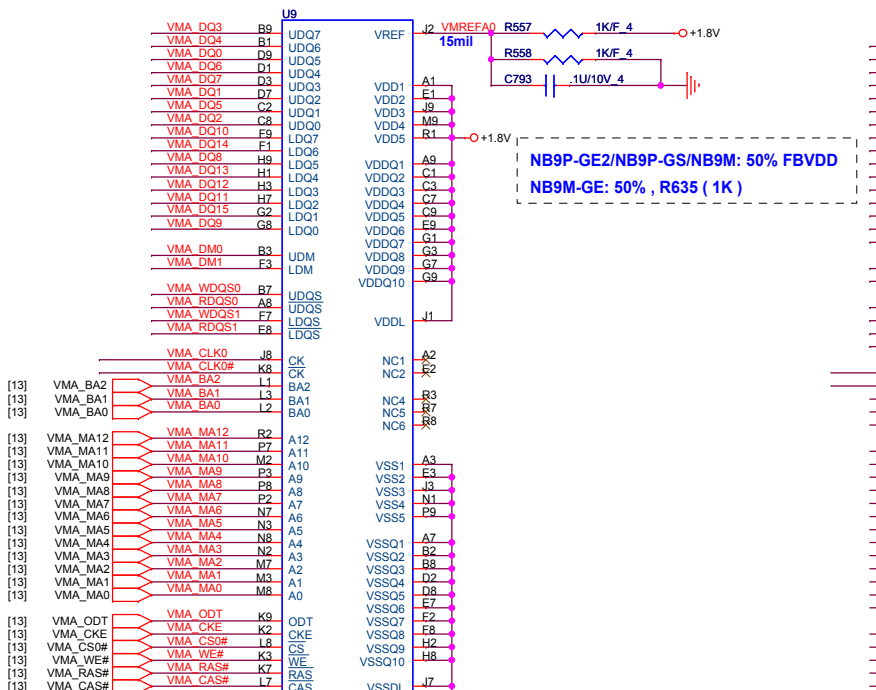
NVVDD Decoupling



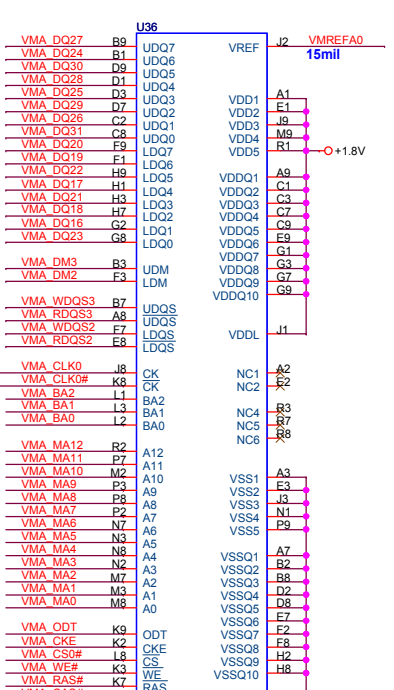
Follow Design Guide DG-03276-001 4.7uF x3 and 0.47x10 uF instead of 0.1uF x10

NB9M: VGACORE +0.90V (Normal) , +1.09V

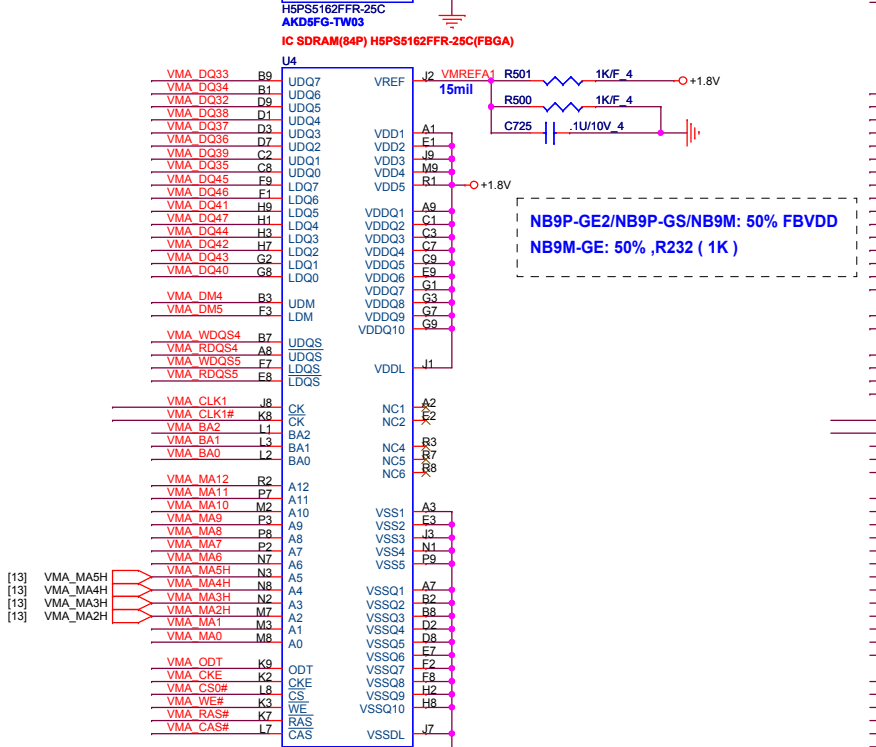




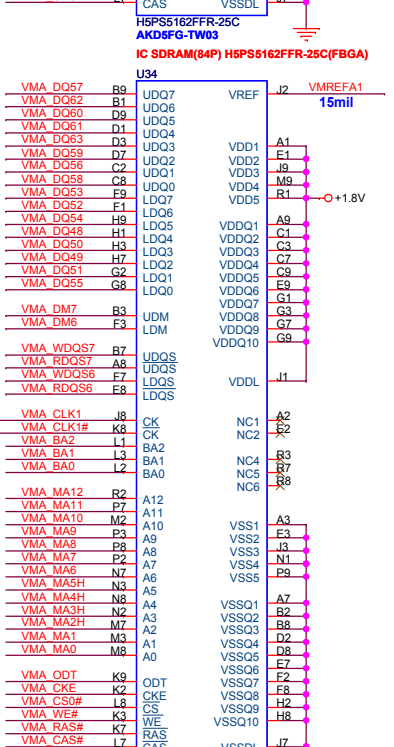
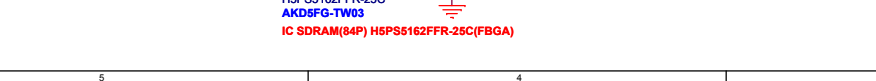
NB9P-GE2/NB9P-GS/NB9M: 50% FBVDD
 NB9M-GE: 50%, R635 (1K)



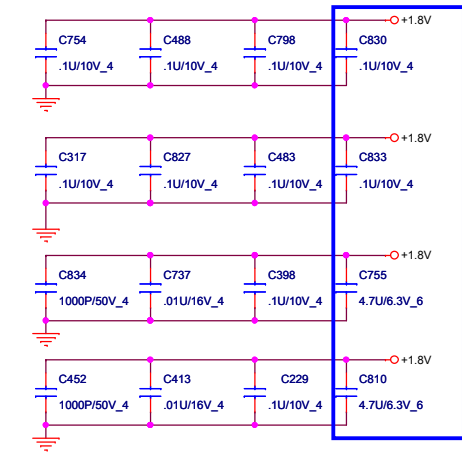
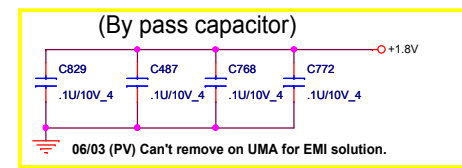
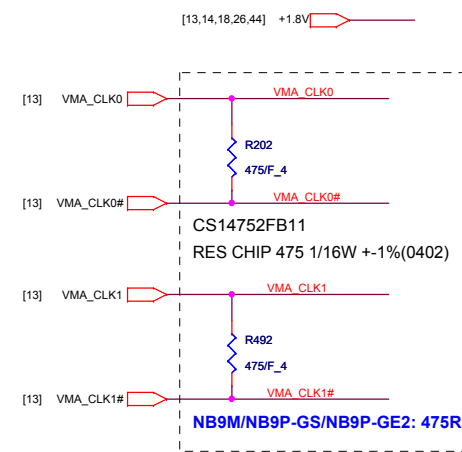
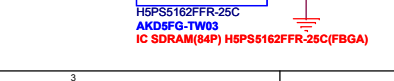
NB9P-GE2/NB9P-GS/NB9M: 50% FBVDD
 NB9M-GE: 50%, R232 (1K)



NB9P-GE2/NB9P-GS/NB9M: 50% FBVDD
 NB9M-GE: 50%, R232 (1K)



NB9P-GE2/NB9P-GS/NB9M: 50% FBVDD
 NB9M-GE: 50%, R232 (1K)



For DB:
 NB9P : AKD59G-T502(Samsung,32M*16)
 NB9M : AKD5FG-TW31(Hynix,32M*16)
 AKD5FG-T*03(Qimonda 32M*16)

- [13] VMA_DQ[63..0]
- [13] VMA_DM[7..0]
- [13] VMA_WDQS[7..0]
- [13] VMA_RDQS[7..0]

256Mb : AKD5JGAT*05
 512Mb : AKD59G-T*01



PROJECT : UT7
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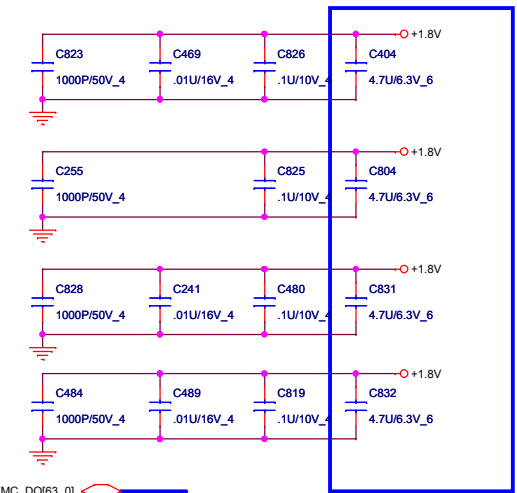
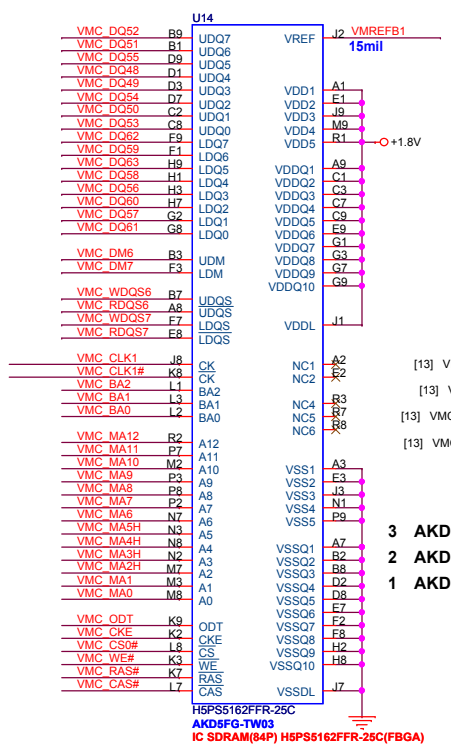
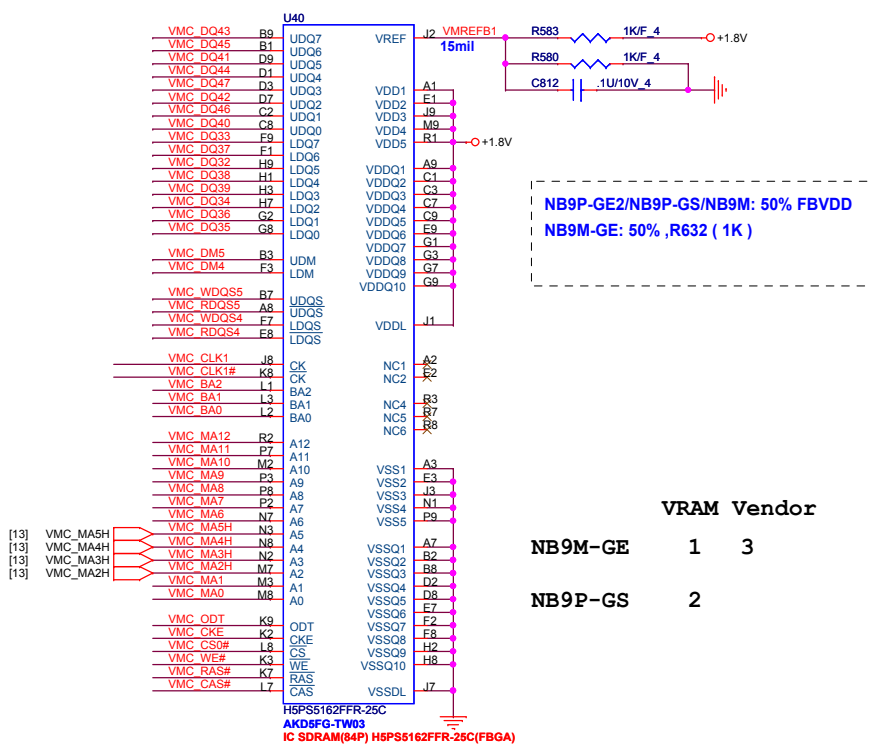
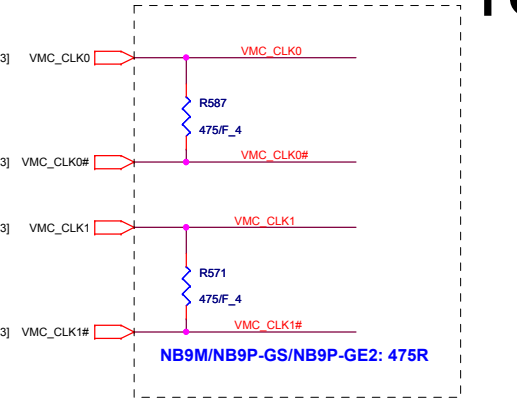
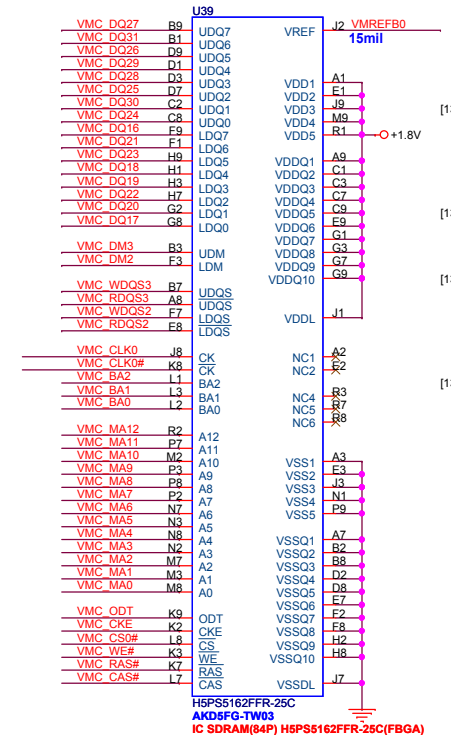
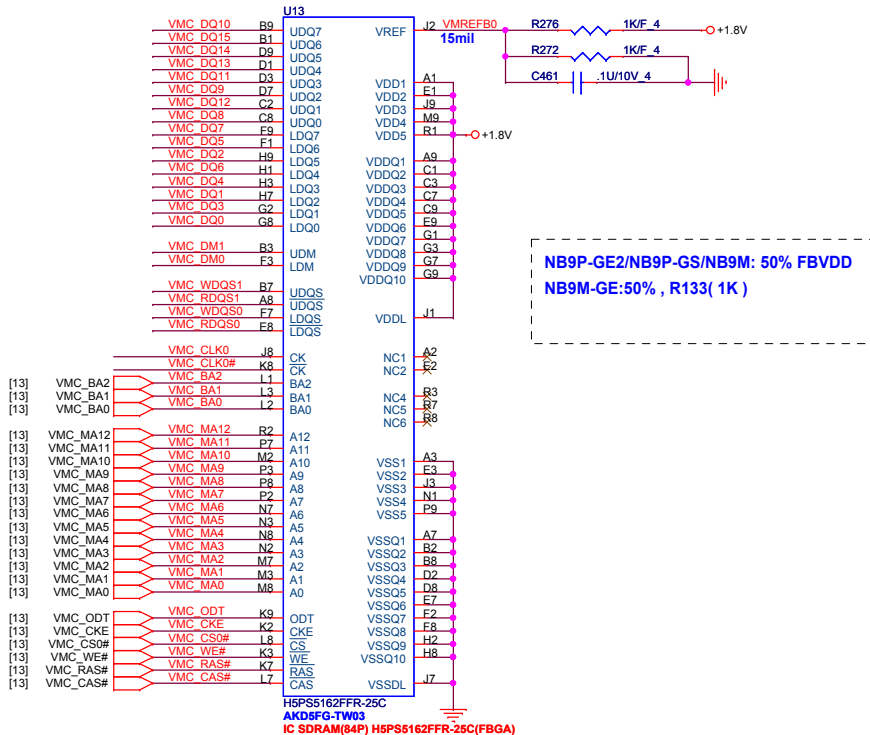
Size Custom	Document Number	Rev E3A
	NV9X VDRAM-1(GDDR2 BGA84)	
Date: Friday, July 18, 2008	Sheet 17	of 46

[13,14,17,26,44] +1.8V

**NB9P-GE2/NB9P-GS/NB9M: 50% FBVDD
NB9M-GE:50%, R133(1K)**

NB9M/NB9P-GS/NB9P-GE2: 475R

CS14752FB11 RES CHIP 475 1/16W +/-1%(0402)



VRAM Vendor

NB9M-GE	1	3
NB9P-GS	2	

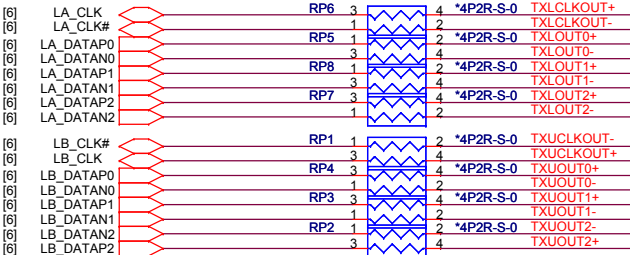
- 3 AKD5FG-T501 IC SDRAM(84P) K4N51163QG-HC25(FBGA) Samsung
- 2 AKD5FG-T*03 IC SDRAM(84P)HYB18T512161B2F-25(TFBGA) Qimonda
- 1 AKD5FG-TW31 IC SDRAM(84P) HY5PS121621CFP-25(FBGA) Hynix



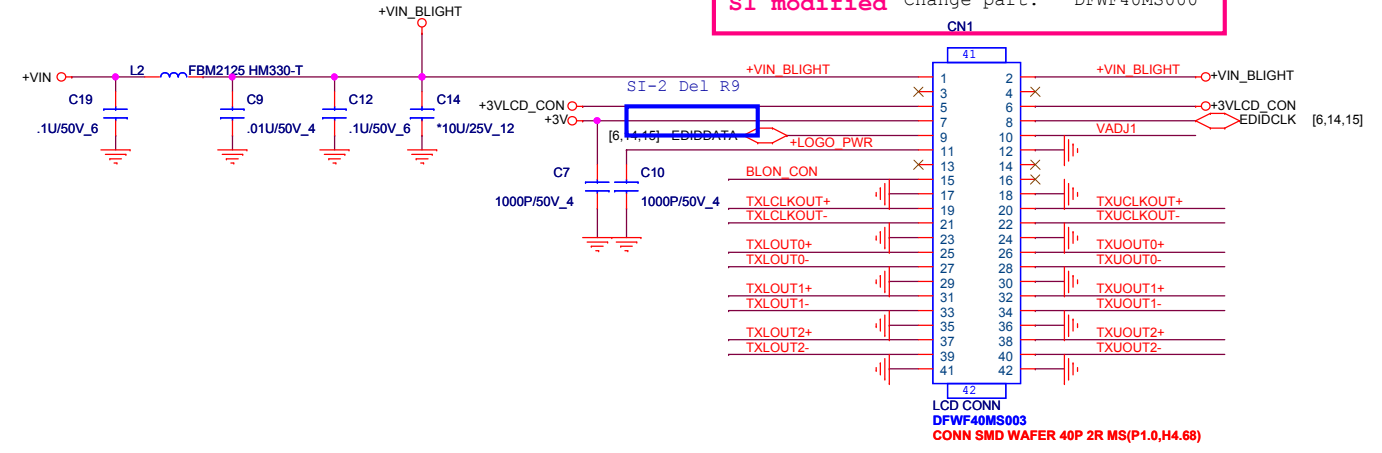
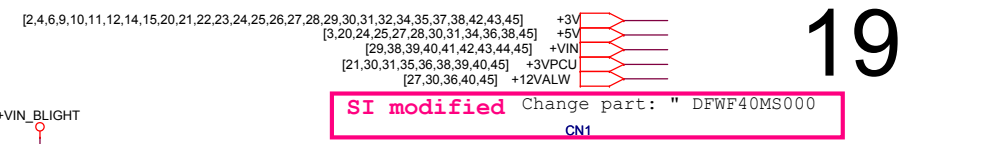
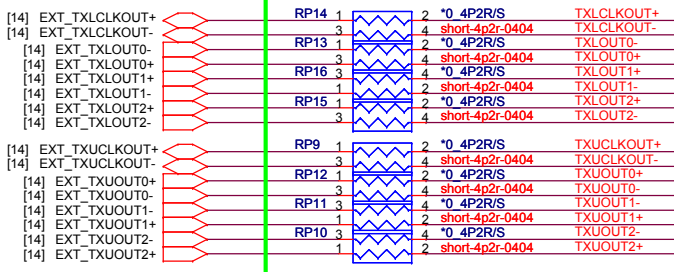
**PROJECT : UT7
Quanta Computer Inc.**

1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B

OPTION SIGNAL FROM NB FOR UMA VGA

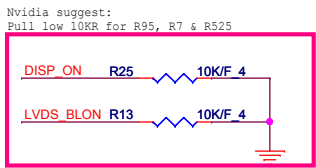
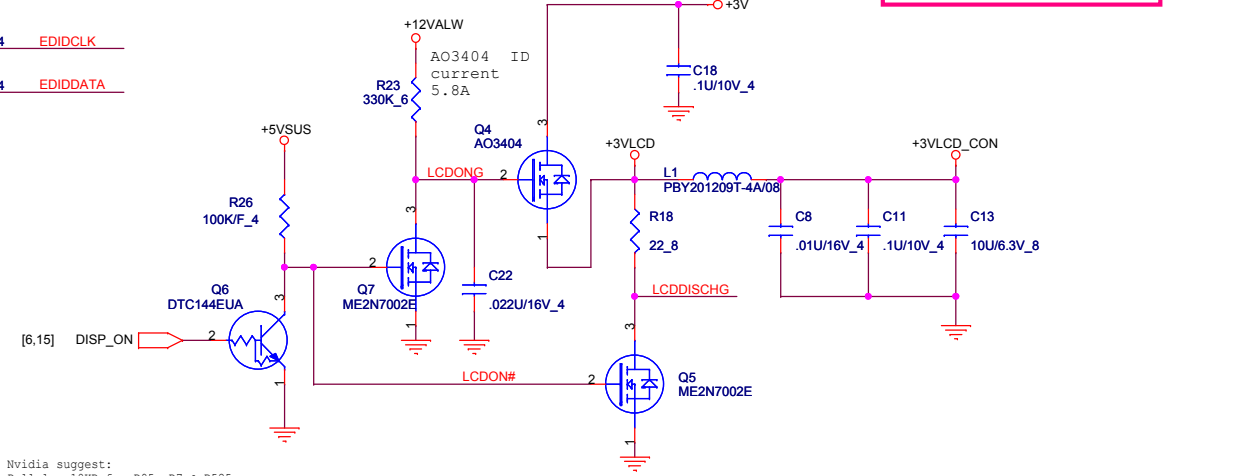
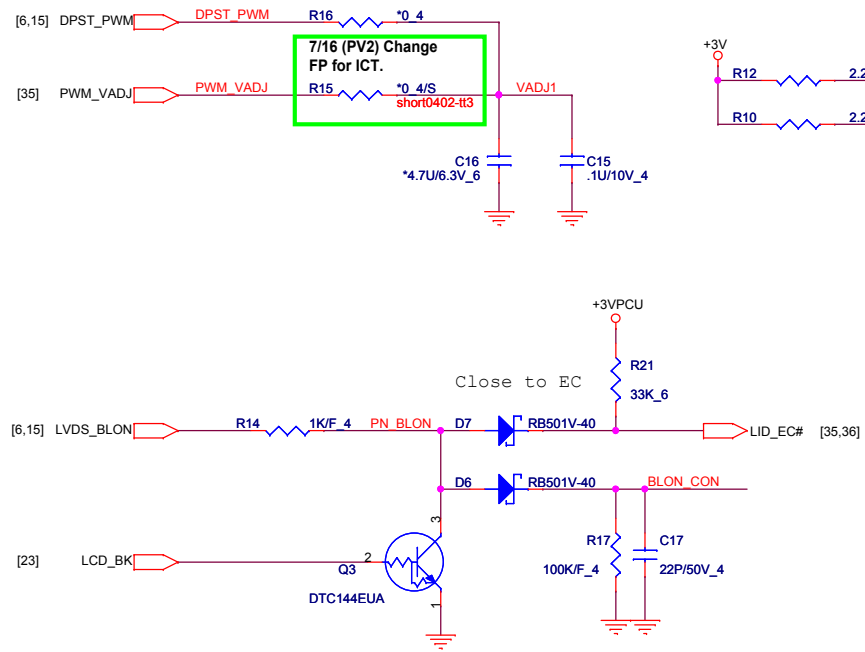


OPTION SIGNAL FROM Nvidia to VGA



+5V R11 75R/F 6 +LOGO_PWR
0090 use 100 ohm and must change back to 75ohm

SI modified
Del CN7, R88, C115
Remove Logo light2

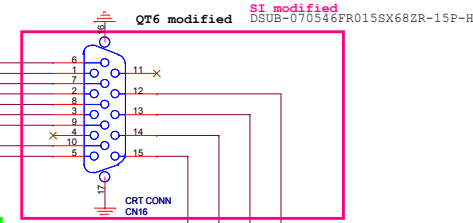
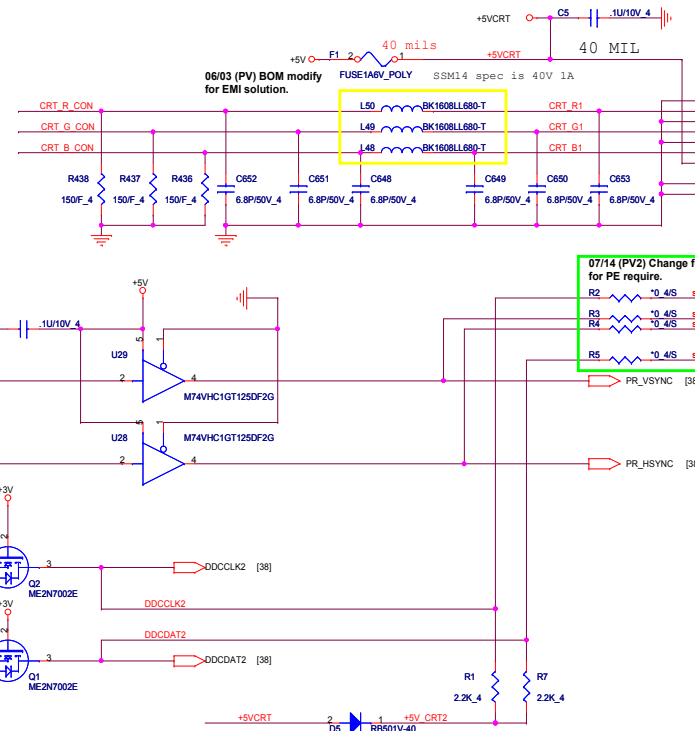


Nvidia suggest:
Pull low 10KR for R95, R7 & R525

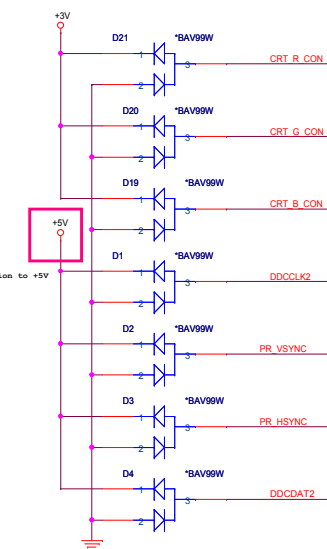
PROJECT : UT7
Quanta Computer Inc.

Size B	Document Number LCD CONN/Lid function	Rev E3A
Date: Friday, July 18, 2008		Sheet 19 of 46

CRT PORT

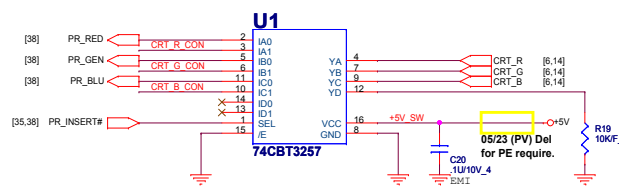


SI modified Change ESD protection to +5V

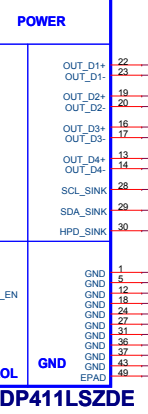
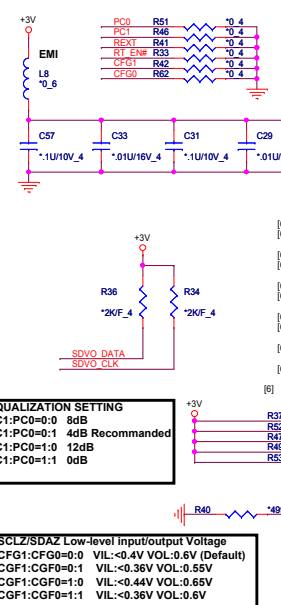


inputs	function
/E SET	Y - port 0
L L	Y - port 1
L H	Y - port 1
H X	Disconnect

CRT SWITCH

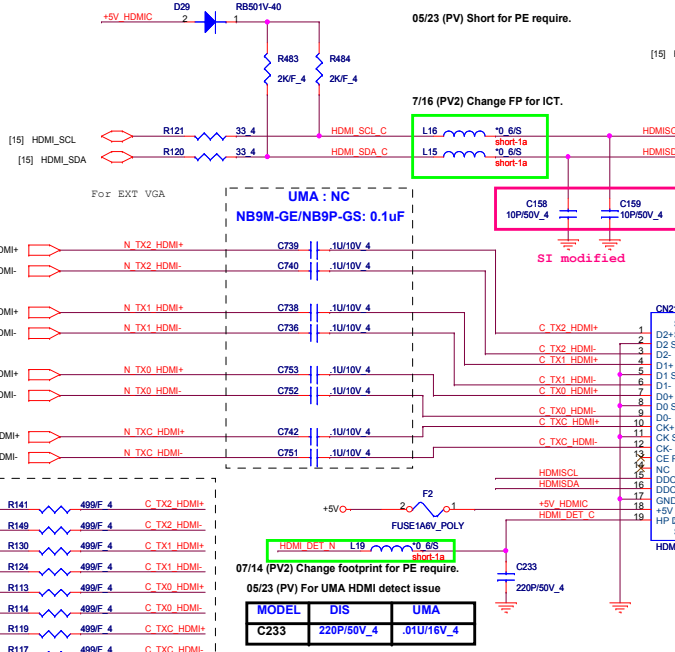


For UMA HDMI function



EQUALIZATION SETTING
 PC1:PC0=0:0 8dB
 PC1:PC0=0:1 4dB Recommended
 PC1:PC0=1:0 12dB
 PC1:PC0=1:1 0dB

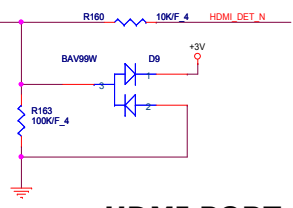
SCLZ/SDAZ Low-level input/output Voltage
 CFG1:CFG0=0:0 VIL:<0.4V VOL:0.6V (Default)
 CFG1:CFG0=0:1 VIL:<0.36V VOL:0.55V
 CFG1:CFG0=1:0 VIL:<0.44V VOL:0.65V
 CFG1:CFG0=1:1 VIL:<0.36V VOL:0.6V



05/23 (PV) Short for PE require.

7/16 (PV2) Change FP for ICT.

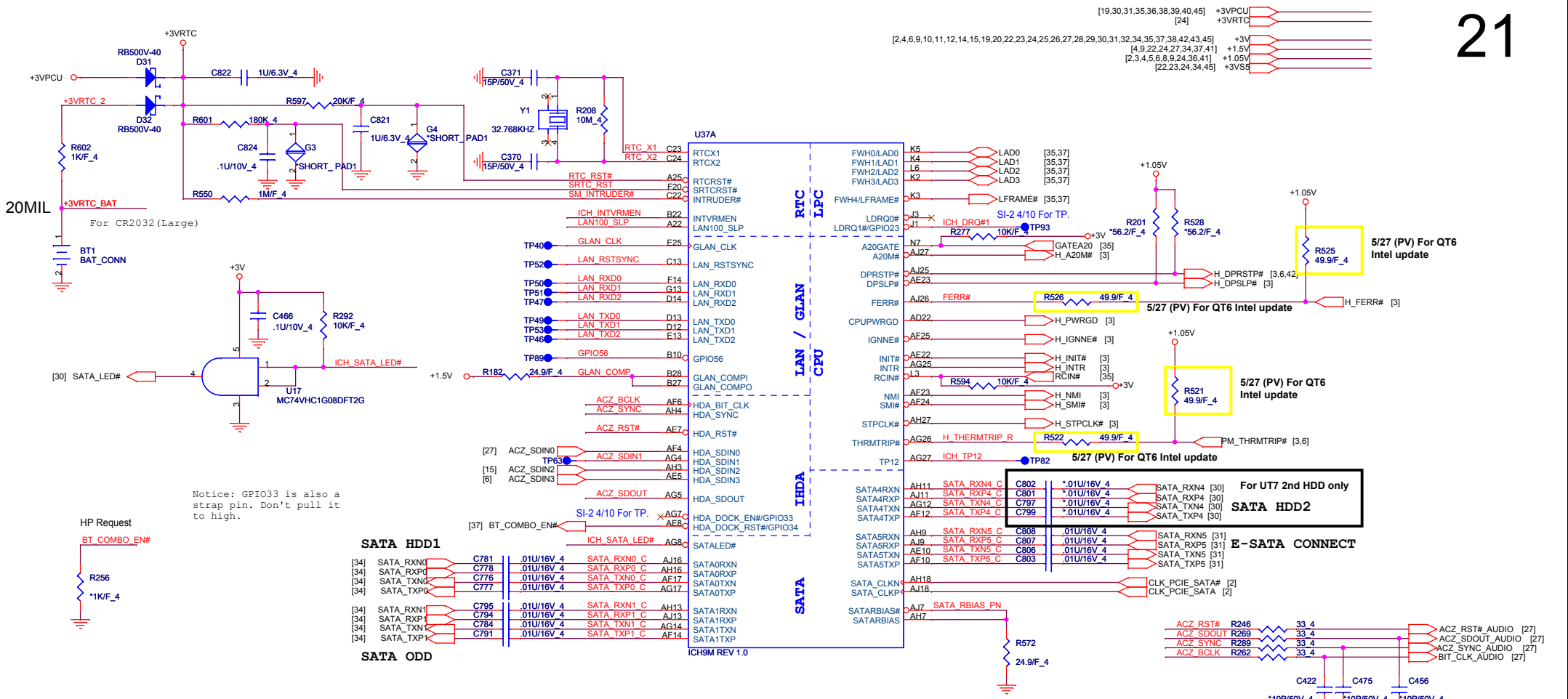
HDMI PORT



MODEL	DIS	UMA
C233	220P/50V_4	.01U/16V_4

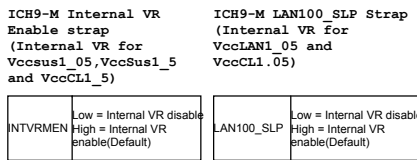
PROJECT : U7
Quanta Computer Inc.

Size C Document Number **CRT/PS8101 HDMI Conn** Rev ESA
 Date: Friday, July 18, 2008 Sheet 20 of 46



Notice: GPIO33 is also a strap pin. Don't pull it to high.

SB Strap



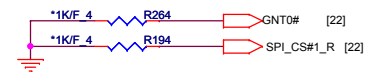
XOR Chain Entrance Strap

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIe port config bit 1

ICH9 Boot BIOS select

STRAP	PCI_GNT0#	SPL_CS#1
SPI	0	1
PCI	1	0
LPC	1	1

(default)



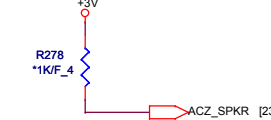
A16 swap override strap

PCI_GNT#3	Low = A16 swap override enabled	Hi = Default
PCI_GNT#3	Low = A16 swap override enabled	Hi = Default



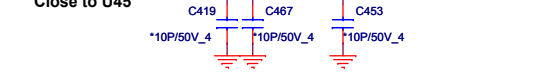
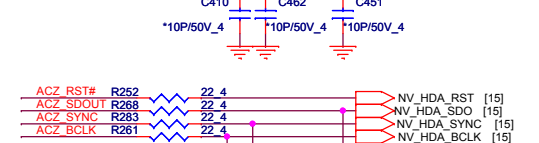
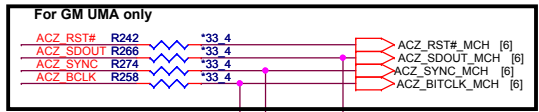
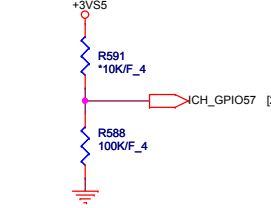
No Reboot Strap

ACZ_SPKR	Low: Default	Hi: No reboot
ACZ_SPKR	Low: Default	Hi: No reboot



TPM physical presence

ICH_GPIO57	Low: Default
ICH_GPIO57	Low: Default



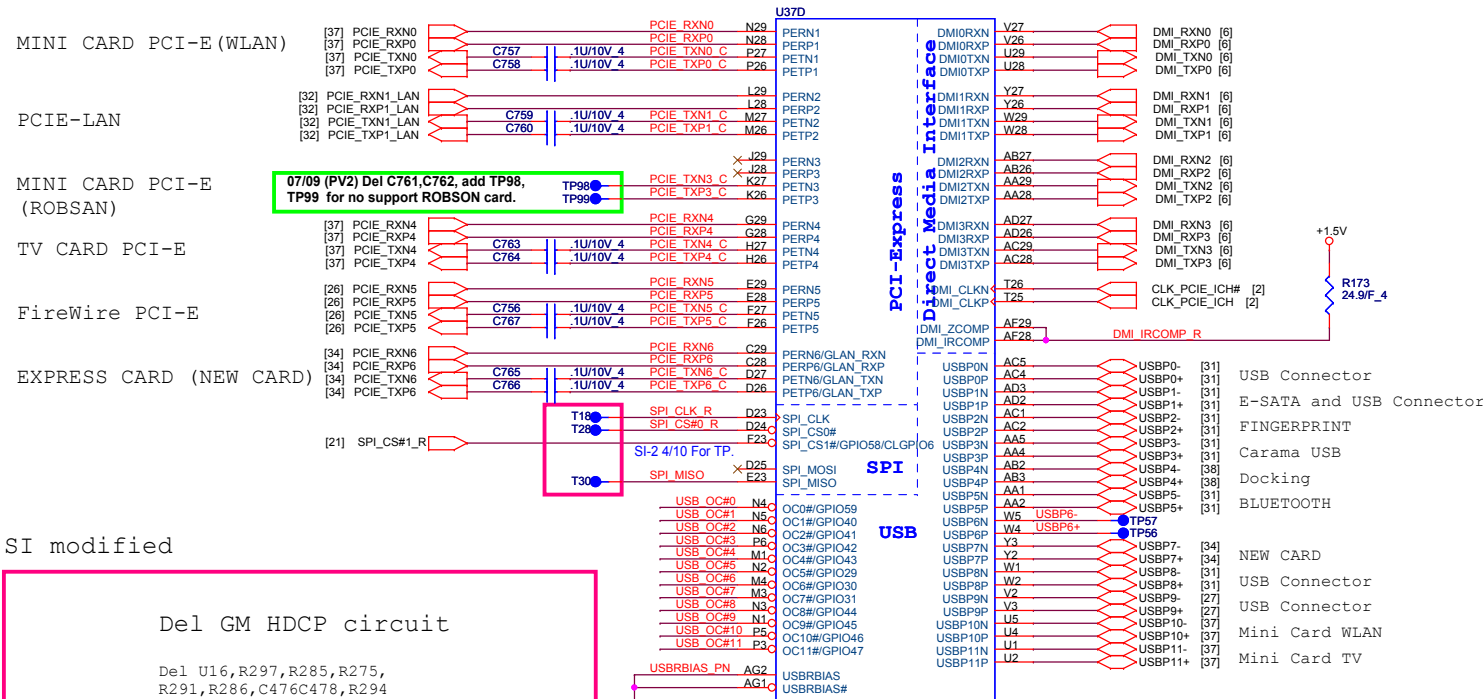
PROJECT : UT7
 Quanta Computer Inc.

Size Custom Document Number ICH9-M Host 1/4 Rev E3A

Date: Friday, July 18, 2008 Sheet 21 of 46

SWAP PCIE PORT6 to PORT2 (Lan and New card swap) -->Rename the port name by function and port

[2,4,6,9,10,11,12,14,15,19,20,21,23,24,25,26,27,28,29,30,31,32,34,35,37,38,42,43,45] +1.5V
 [23,31,37,41,42,43,45] +3V
 [21,23,24,34,45] +3VS5

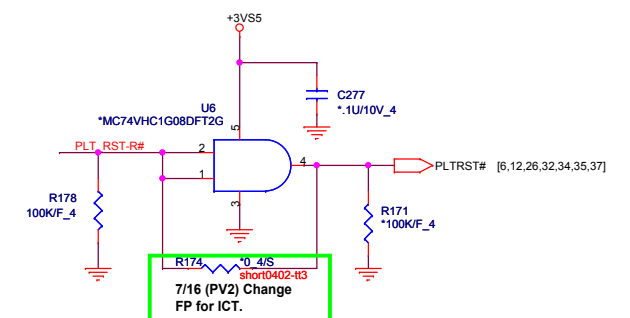
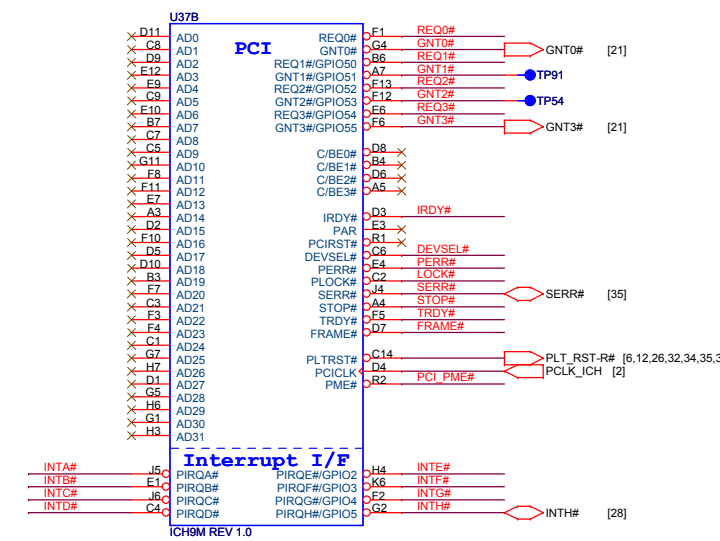
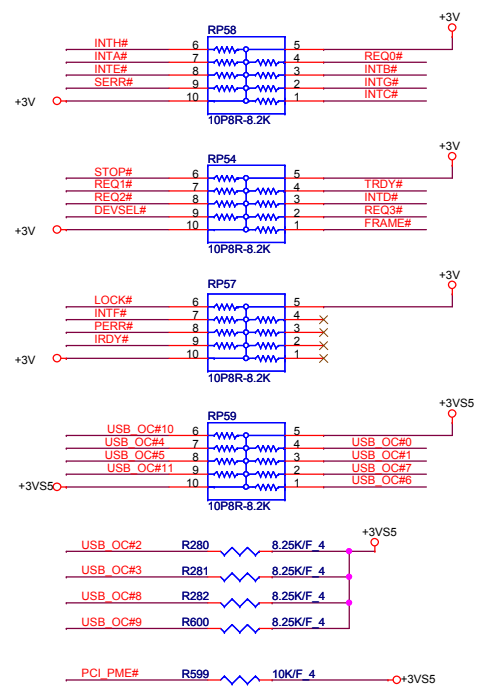


SI modified

Del GM HDCP circuit

Del U16, R297, R285, R275, R291, R286, C476C478, R294

512K byte SPI ROM
For HDCP only
For GM HDCP



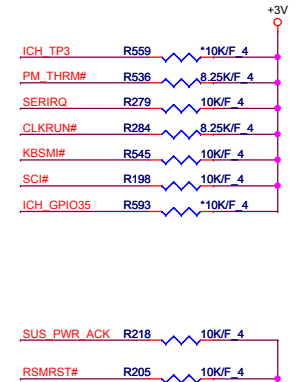
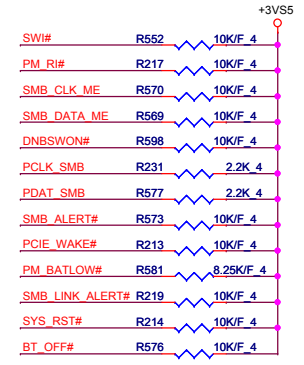
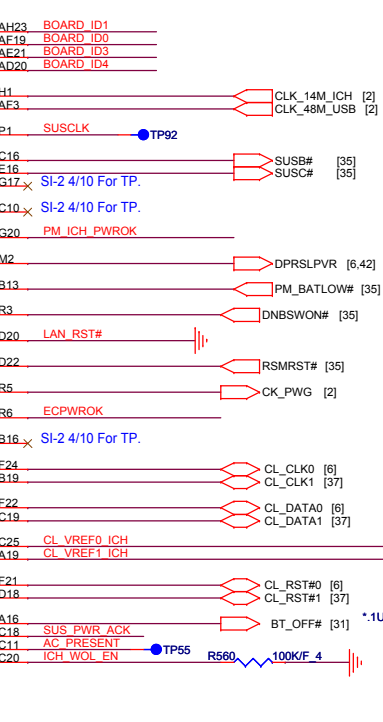
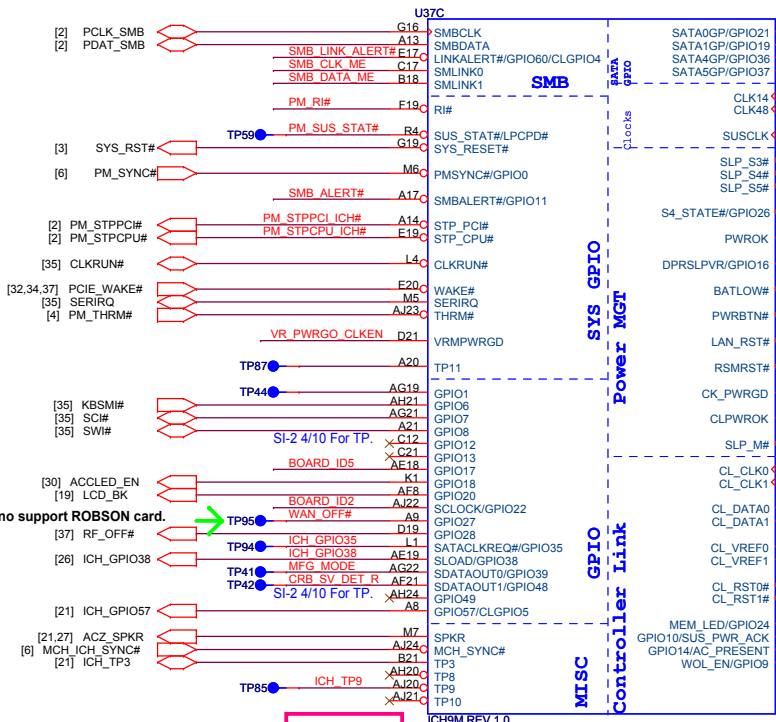
PROJECT : UT7
 Quanta Computer Inc.

NB5

Size Custom Document Number ICH9-M PCIE 2/4 Rev E3A

Date: Friday, July 18, 2008 Sheet 22 of 46

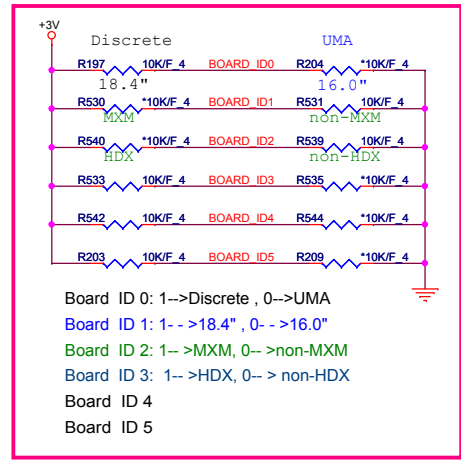
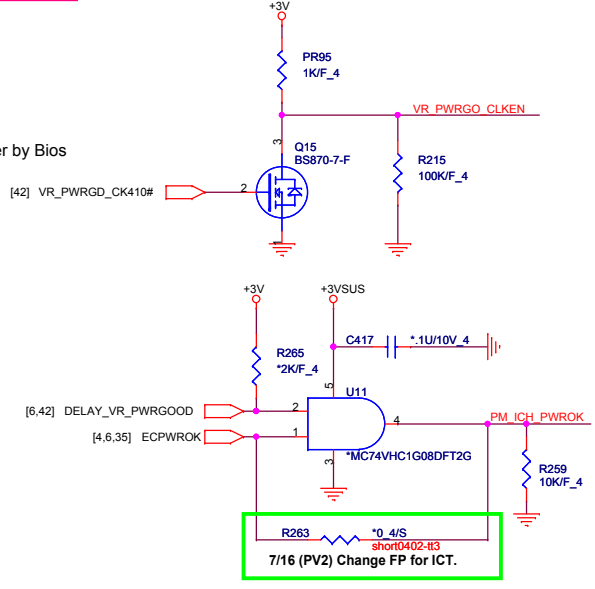
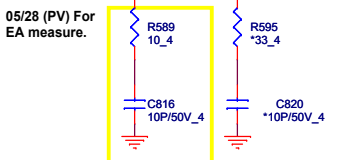
[2,4,6,9,10,11,12,14,15,19,20,21,22,24,25,26,27,28,29,30,31,32,34,35,37,38,42,43,45] +3V
 [21,22,24,34,45] +3VS5
 [31,37,41,42,43,45] +3VSUS



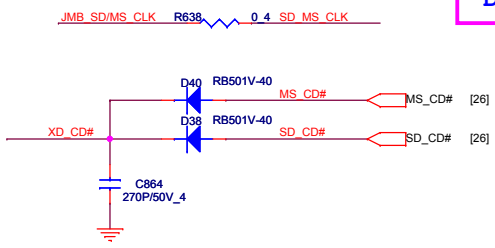
07/09 (PV2) Add TP95 for no support ROBSON card.

SI modified per T18, TP84, TP86

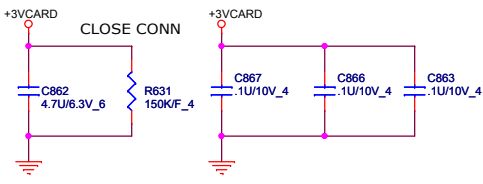
SI-2 Build
 Delete R574, G2 as Bios_Rec can be cover by Bios



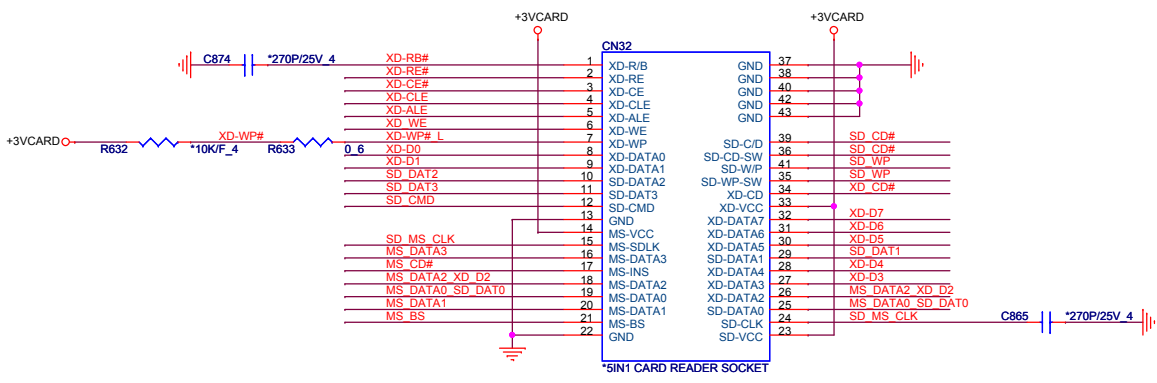
Delete JMB 385



Close to CN34



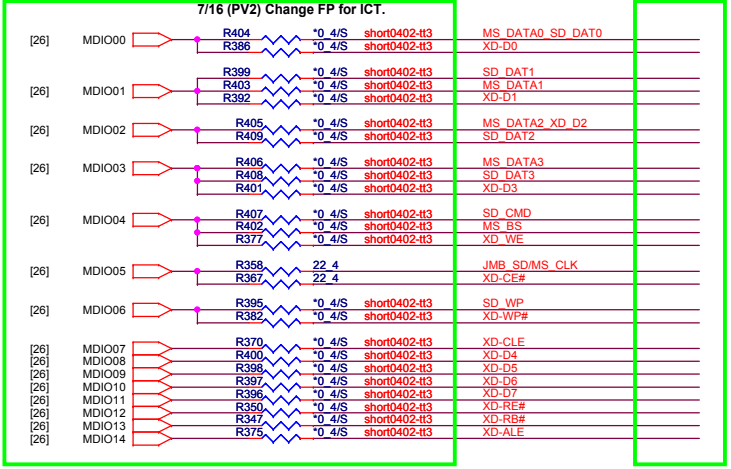
5 IN1 CARD READER
XD, MMC/SD, MS/MSP



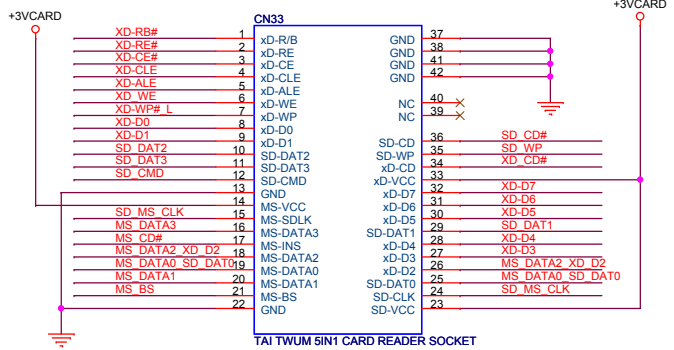
SI modified Footprint: "4in1-72700327123-43p-1"

	SD/MMC	MS	XD
MDID0	SD DAT0	MS D0	XD D0
MDID1	SD DAT1	MS D1	XD D1
MDID2	SD DAT2	MS D2	XD D2
MDID3	SD DAT3	MS D3	XD D3
MDID4	SD CMD	MS BS	XD WE#
MDID5	SD CLK	MS SCLK	XD CE#
MDID6	SD WP		XD WP#
MDID7			XD CLE
MDID8	SD DAT4		XD D4
MDID9	SD DAT5		XD D5
MDID10	SD DAT6		XD D6
MDID11	SD DAT7		XD D7
MDID12			XD RE#
MDID13			XD RB#
MDID14			XD ALE
CR1 LEDN	SD1 LED#	MS1 LED#	XD LED#
CR1 PCTLN	SD1 PCTL#	MS1 PCTL#	XD1 PCTL#
CR1 CD0	SD1 CD#		XD CV#
CR1 CD1		MS1 CD#	XD CD#

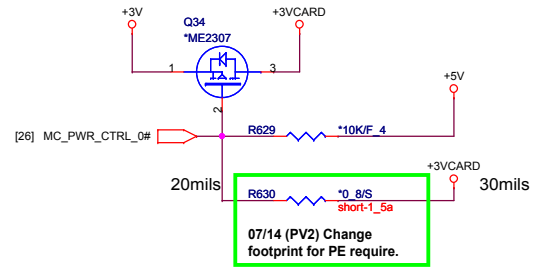
7/16 (PV2) Delete net for ICT.



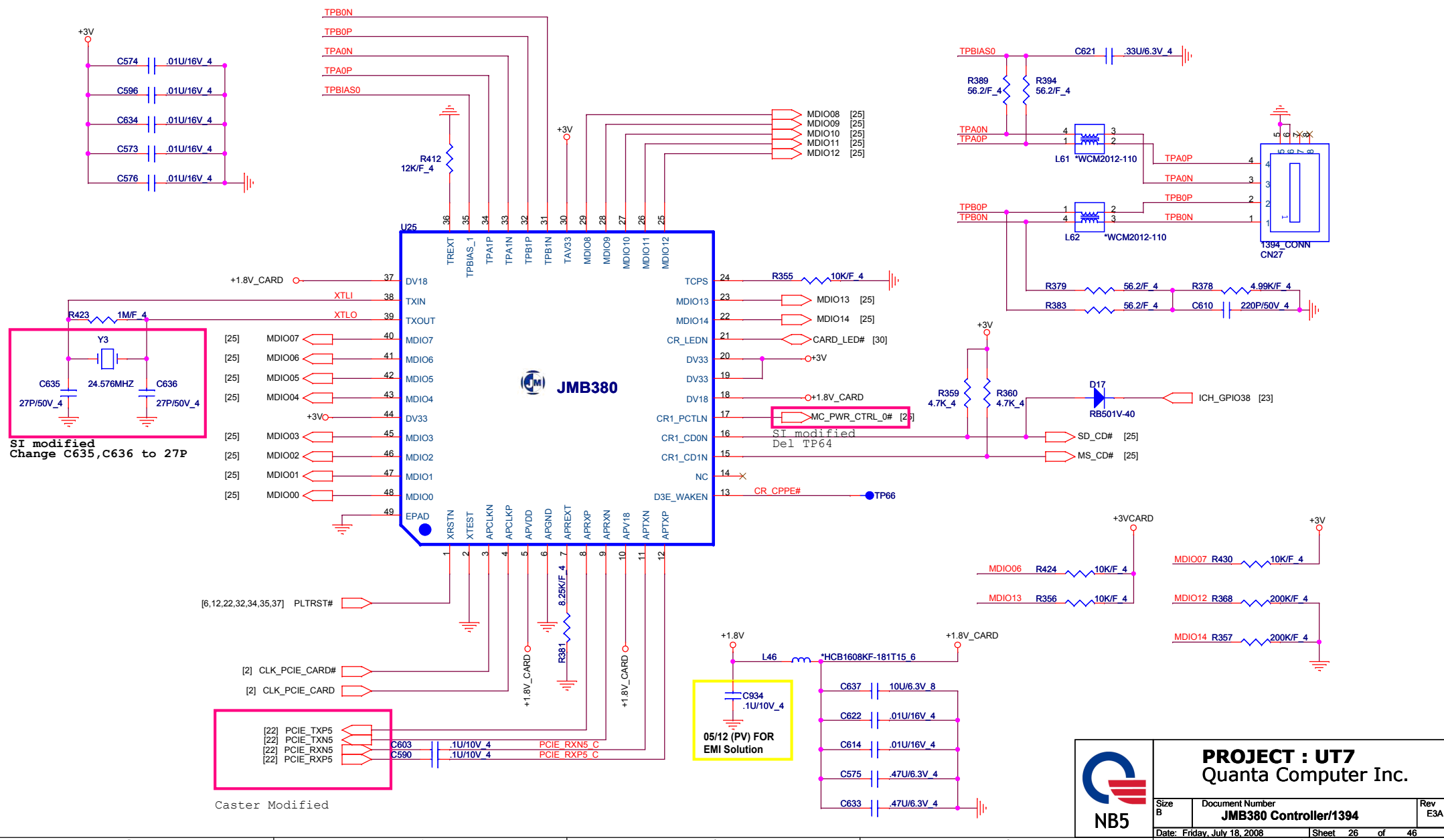
2ND SOURCE



SI modified Footprint: "7IN1-R015-B11-1M-42P-L"



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SI modified
Change C635, C636 to 27P

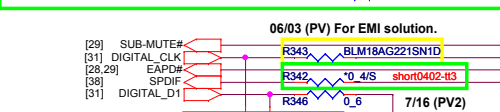
Caster Modified

05/12 (PV) FOR
EMI Solution

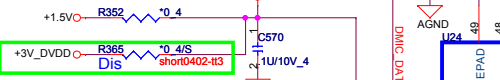


PROJECT : UT7 Quanta Computer Inc.		
Size B	Document Number JMB380 Controller/1394	Rev E3A
Date: Friday, July 18, 2008	Sheet 26	of 46

05/23 (PV) For IDT Dolby functionality.
07/14 (PV2) R697 change footprint for PE require.



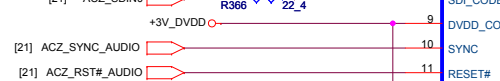
06/03 (PV) For EMI solution.
7/16 (PV2) Change FP for ICT.



07/14 (PV2) Change footprint for PE require.



07/14 (PV2) Change footprint for PE require.



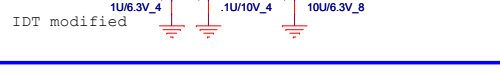
07/14 (PV2) Change footprint for PE require.



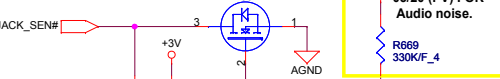
07/14 (PV2) Change footprint for PE require.



07/14 (PV2) Change footprint for PE require.



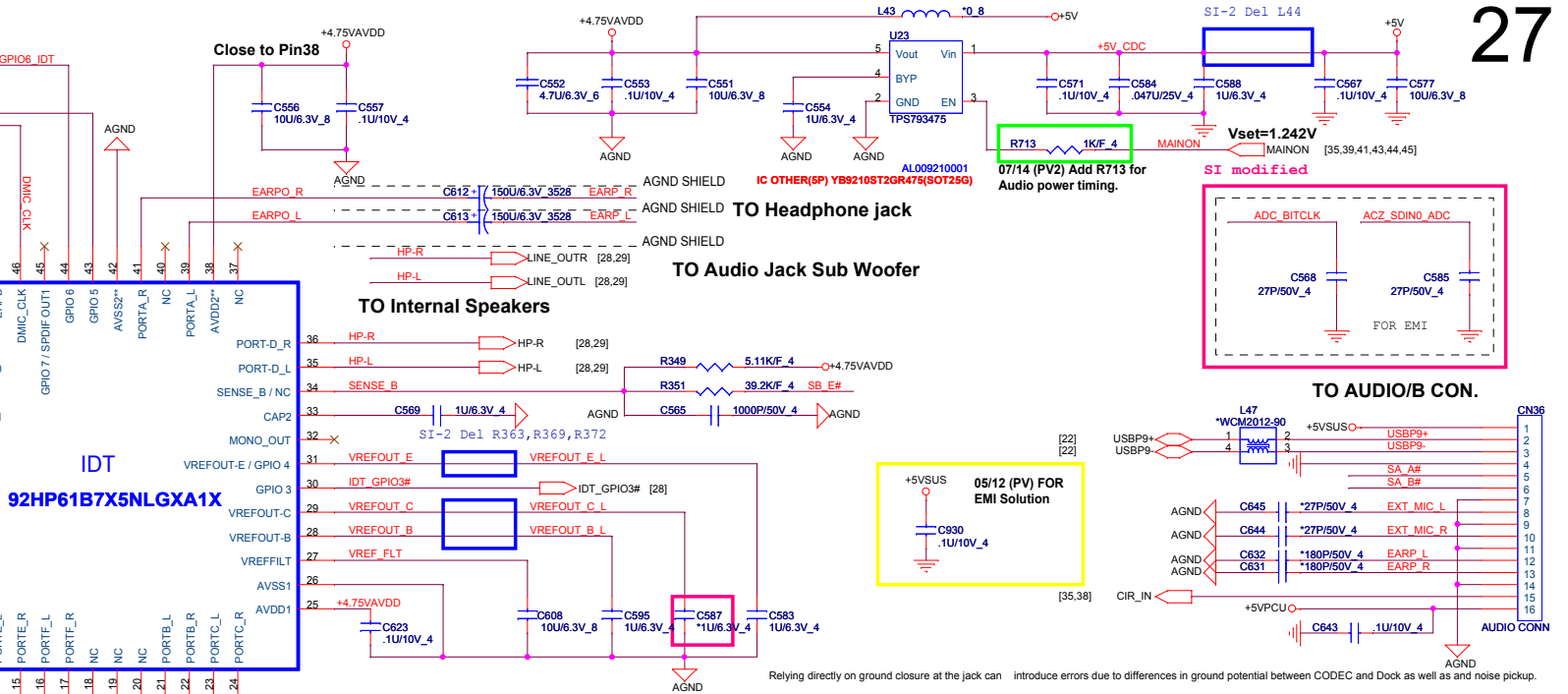
07/14 (PV2) Change footprint for PE require.



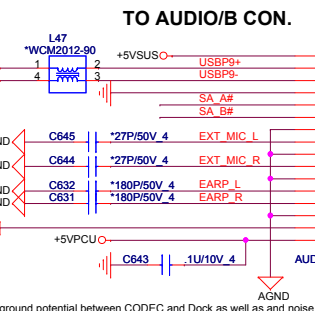
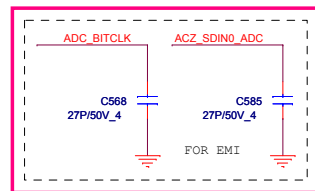
07/14 (PV2) Change footprint for PE require.



07/14 (PV2) Change footprint for PE require.



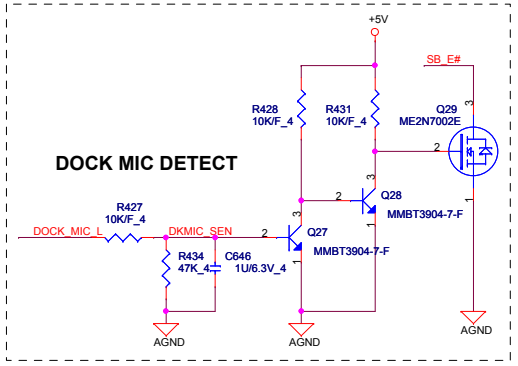
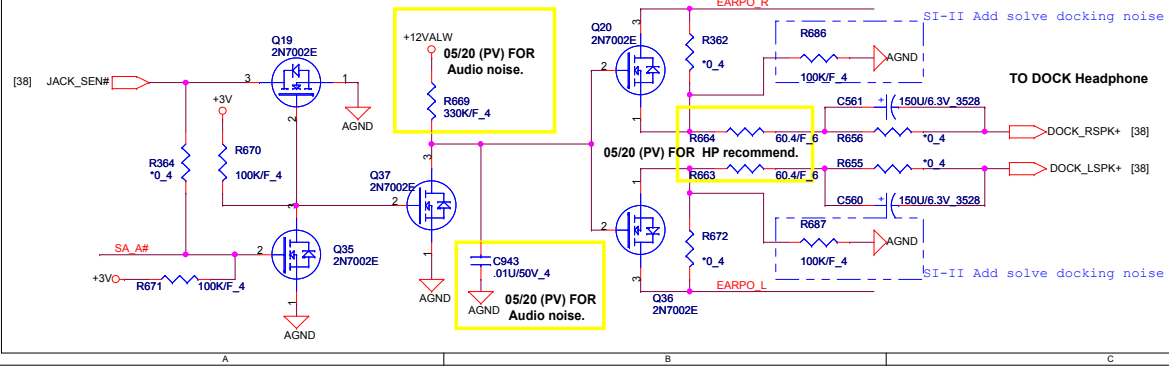
05/12 (PV) FOR EMI Solution
 +5VSUS
 C930
 .1U/10V_4



PORT	PLACE TO
MONO_OUT	X
PORT A	HP OUT
PORT B	M/B MIC
PORT C	X
PORT D	Internal Speakers
PORT E	Docking MIC
PORT F	X
DM	DIGITAL MIC

07/14 (PV2) Change footprint for PE require.

R380 *0.6/S short-1a
 R675 *0.6/S short-1a
 R341 *0.6/S short-1a
 R336 *0.6/S short-1a
 R429 *0.6/S short-1a
 R554 *0.6/S short-1a
 R603 *0.6/S short-1a
 SI-2 EMI Requests Add



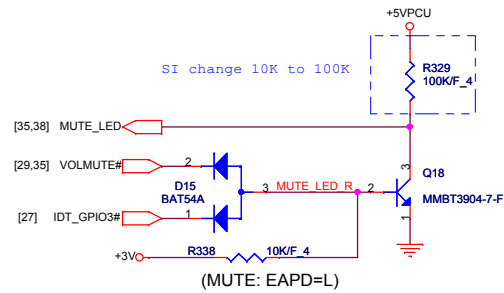
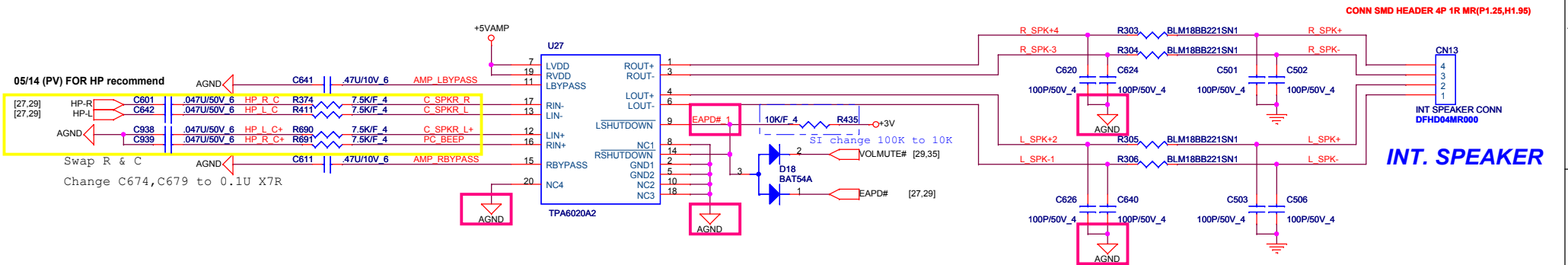
SA_A# -->EXT HP
 SA_B# -->EXT MIC
 SB_E#--> DOCK MIC
 Audio JACK: Normal Open

PROJECT : UT7
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Size Custom Document Number Azalia IDT92HD71B7 Rev E3A
 Date: Friday, July 18, 2008 Sheet 27 of 46

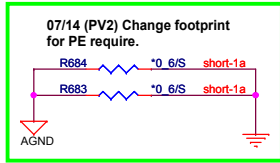
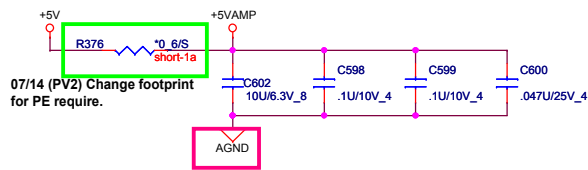
AUDIO AMPLIFIER

+3V [2,4,6,9,10,11,12,14,15,19,20,21,22,23,24,25,26,27,29,30,31,32,34,35,37,38,42,43,45]
 +5V [3,19,20,24,25,27,30,31,34,36,38,45]
 +5VPCU [27,35,40,41,42,43,44,45]
 +5VAMP [29]



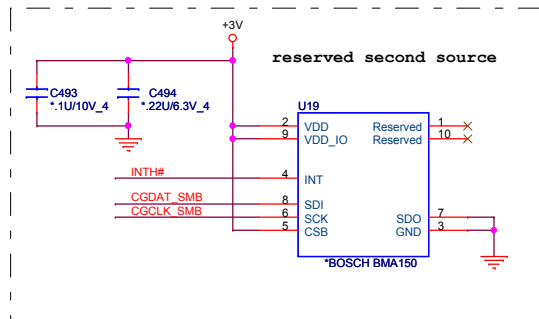
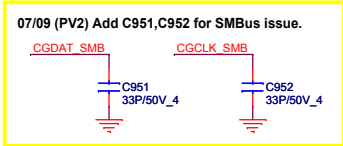
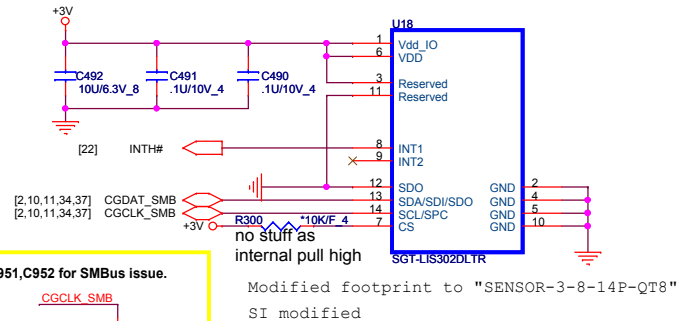
07/09 (PV2) Delete for 2ND FAN function.

Delete Gain set



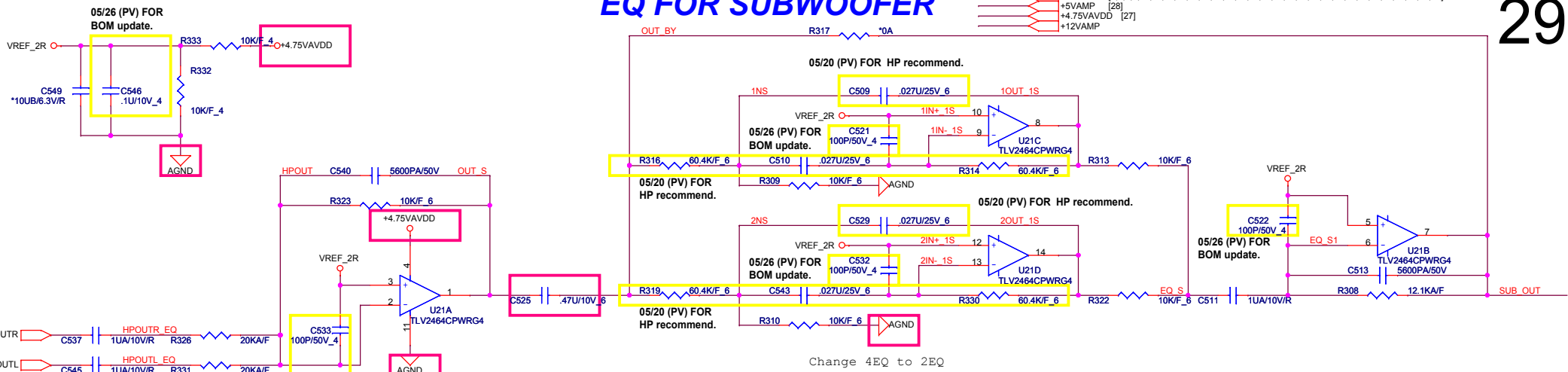
Del R373, R677, R676
 Del AMP_GND to AGND

Accelerometer Sensor

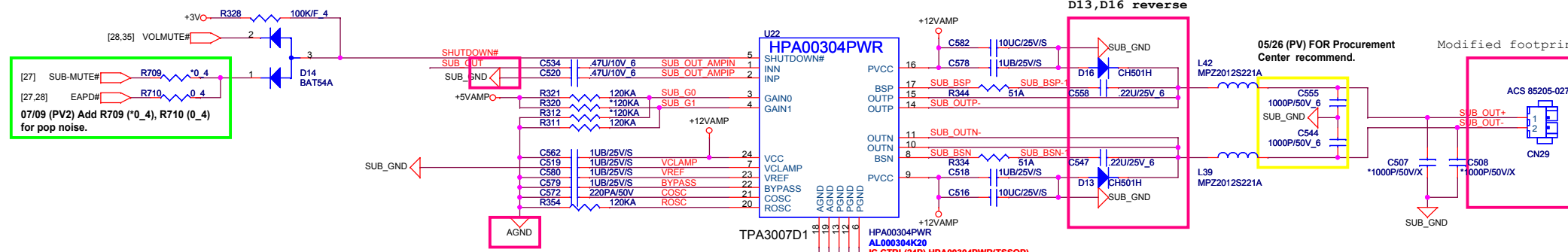


PROJECT : UT7
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EQ FOR SUBWOOFER



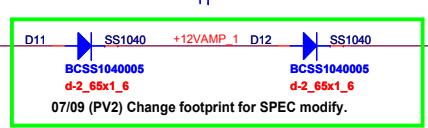
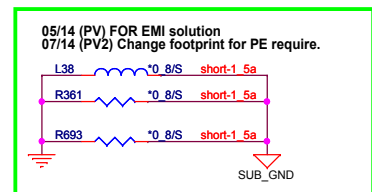
MODEL	UT6	UT7
R316	60.4K/F_6	40.2K/F_6
R319	60.4K/F_6	40.2K/F_6
R330	60.4K/F_6	80.6K/F_6
R314	60.4K/F_6	80.6K/F_6
C509	0.027U/25V_6	0.022U/50V_6
C510	0.027U/25V_6	0.022U/50V_6
C529	0.027U/25V_6	0.039U/16V_6
C543	0.027U/25V_6	0.039U/16V_6



Sub-Woofer power

Del HP_GND to GND

Delete L1003

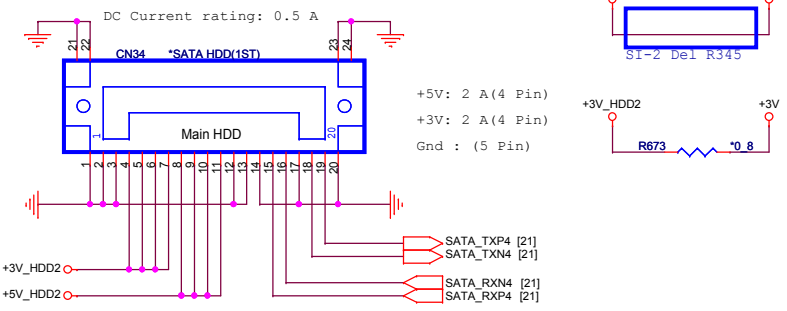


PROJECT : UT7
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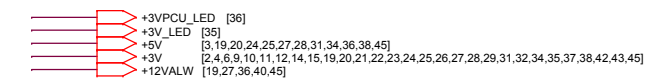
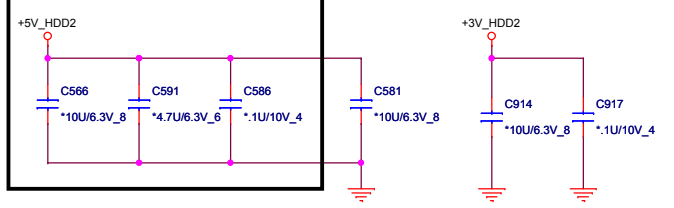
Size Custom Document Number **SUBWOOFER(EQ & AMP.)** Rev E3A

Date: Friday, July 18, 2008 Sheet 29 of 46

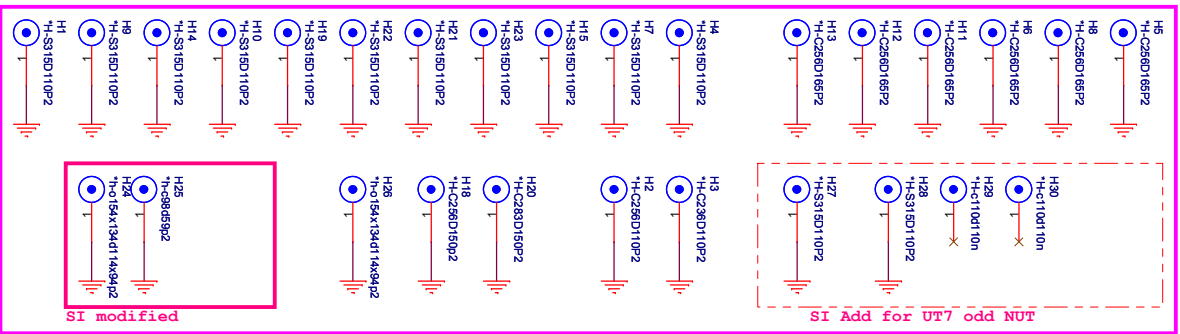
SATA_2 CONNECTOR



FOR UT7 2ND HDD ONLY.

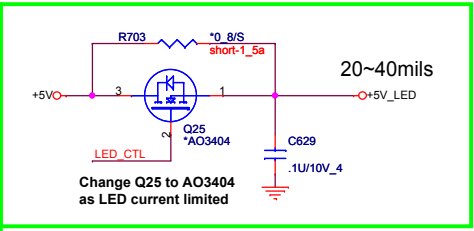
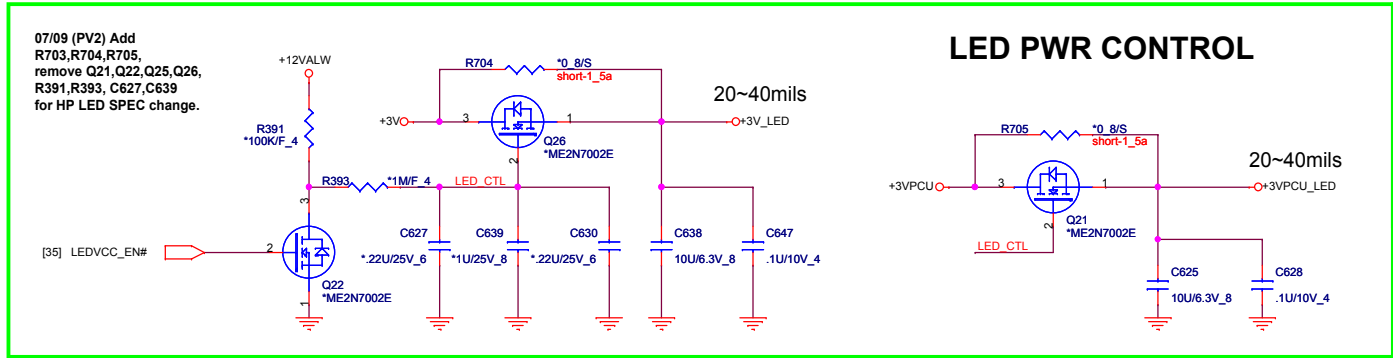
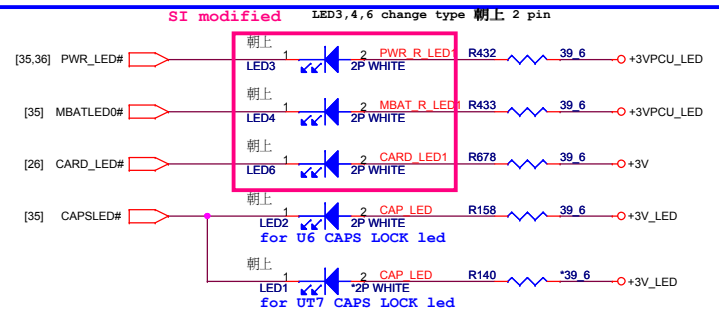
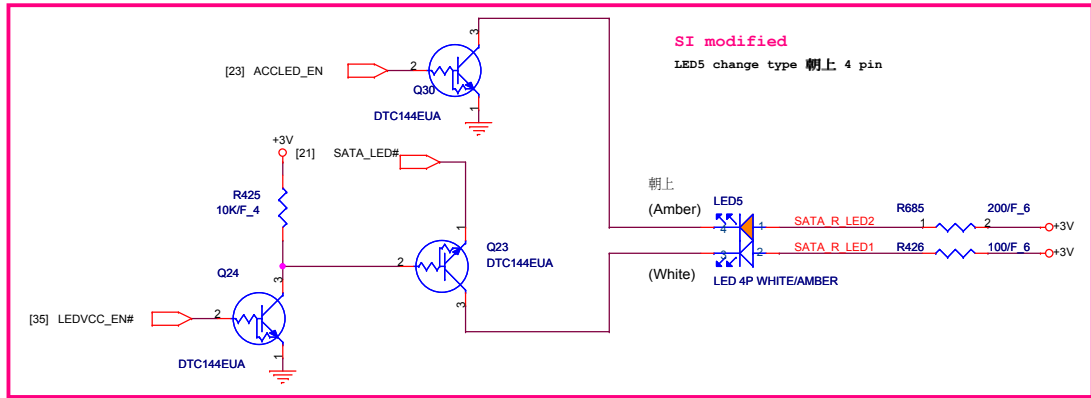
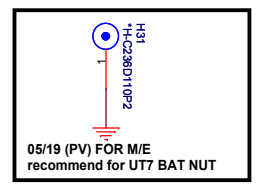
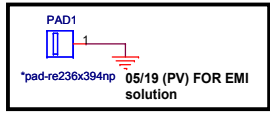


M/B Screw Hole

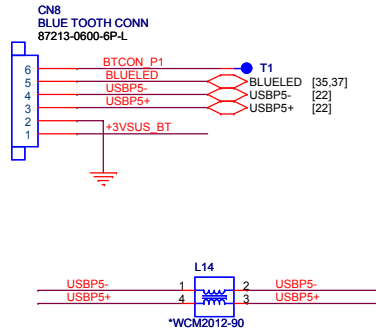
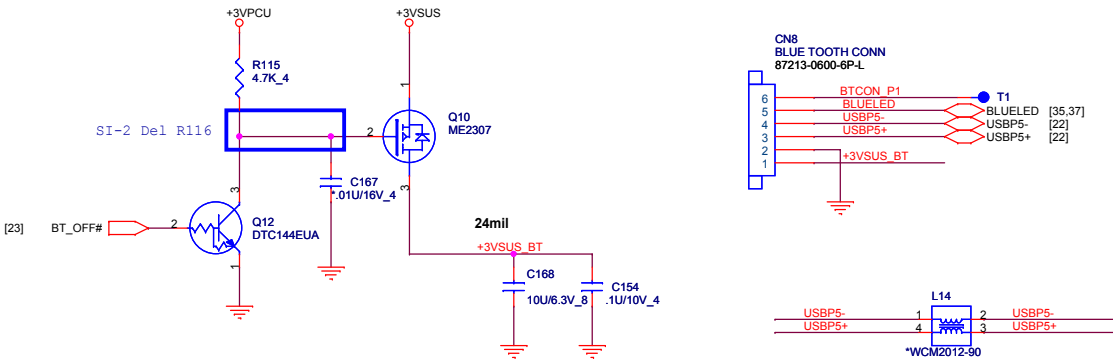


delete all PAD & change screw footprint

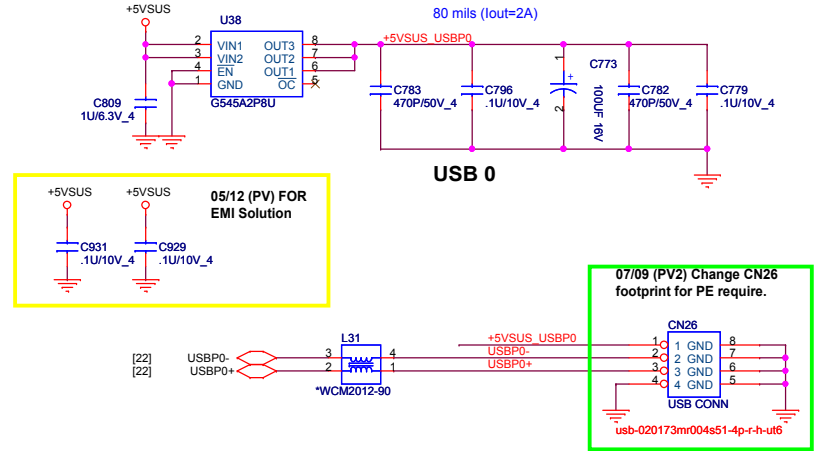
07/14 (PV2) Delete H16,H17 for no support ROBSON card.



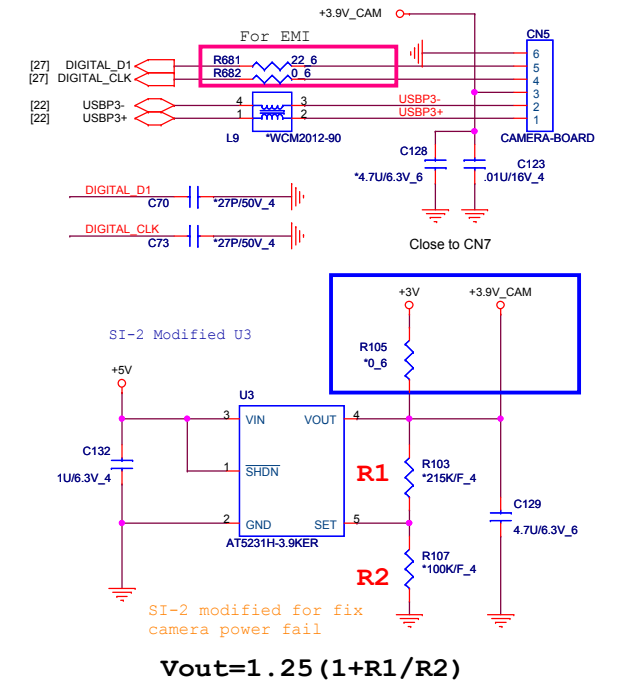
BLUETOOTH



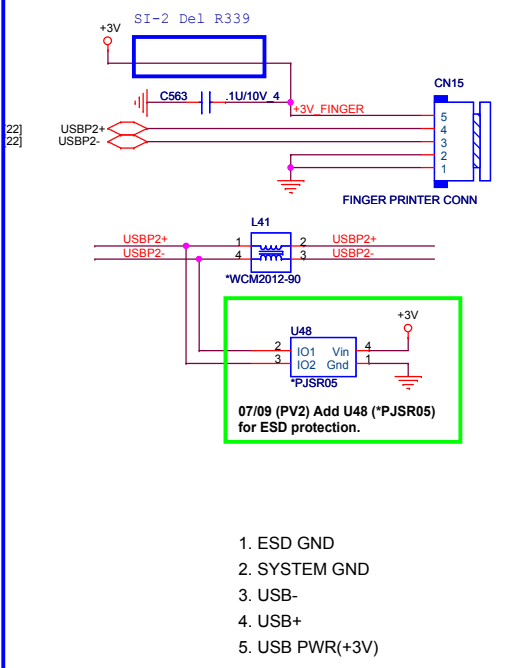
USBX1 and E-SATA



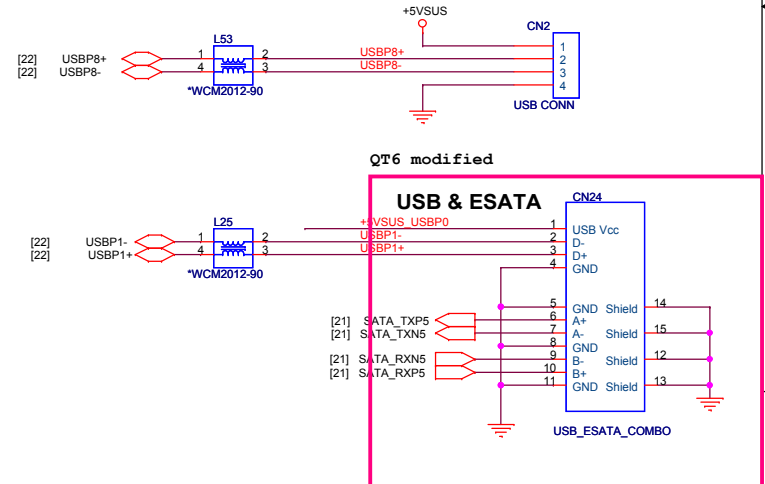
USB CAMERA /DIGITAL MIC CONNECT



USB fingerprint CON



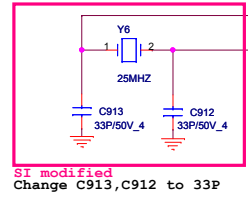
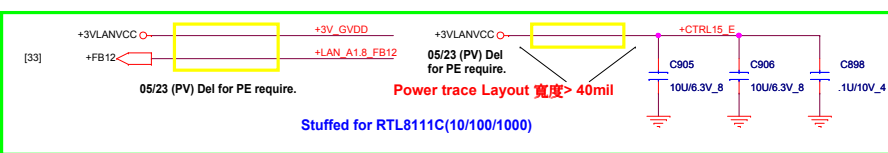
1. ESD GND
2. SYSTEM GND
3. USB-
4. USB+
5. USB PWR(+3V)



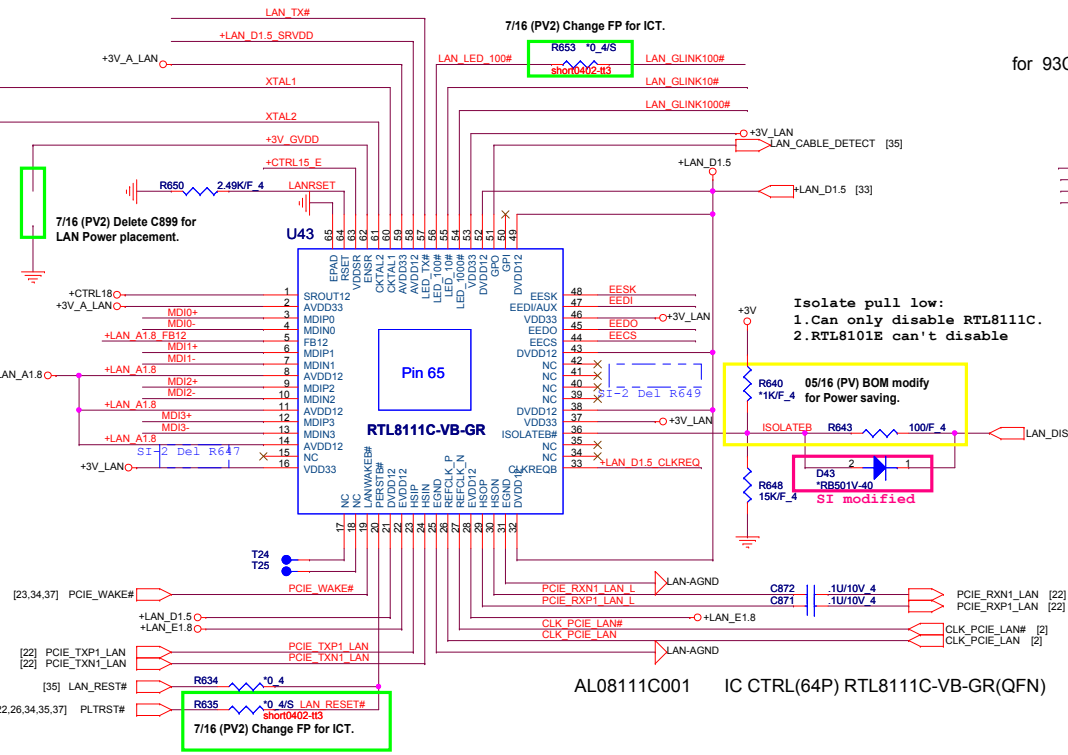
	PROJECT : UT7		Rev E3A
	Quantta Computer Inc.		
Size Custom	Document Number	BT/WC/FT/TS/ESATA/USB	
Date: Friday, July 18, 2008	Sheet	31	of 46

T : Stuffed for RTL8111C(10/100/1000)

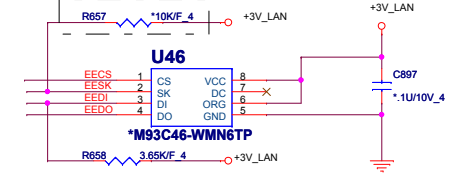
+LAN_D1.5 +LAN_D1.5_SRVDV 05/23 (PV) Del for PE require. +LAN_D1.5_CLKREQ Stuffed for 8102E/RTL8111C



SI modified change C913,C912 to 33P U18#63 wider than 40 mils U18#1 wider than 60 mils

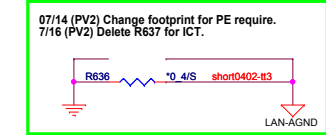


for 93C56 used. NC if 93C46 is used.



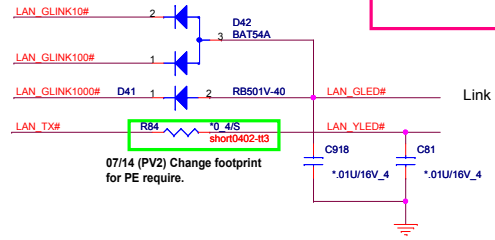
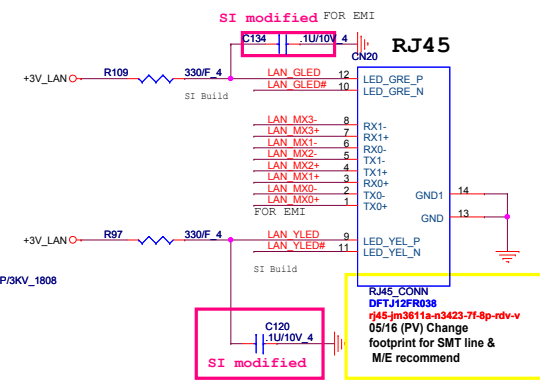
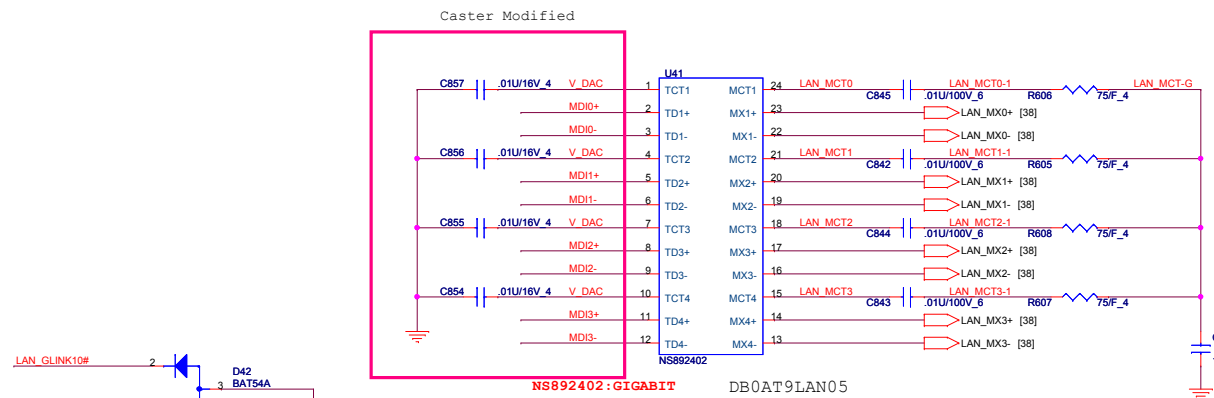
Isolate pull low: 1.Can only disable RTL8111C. 2.RTL8101E can't disable

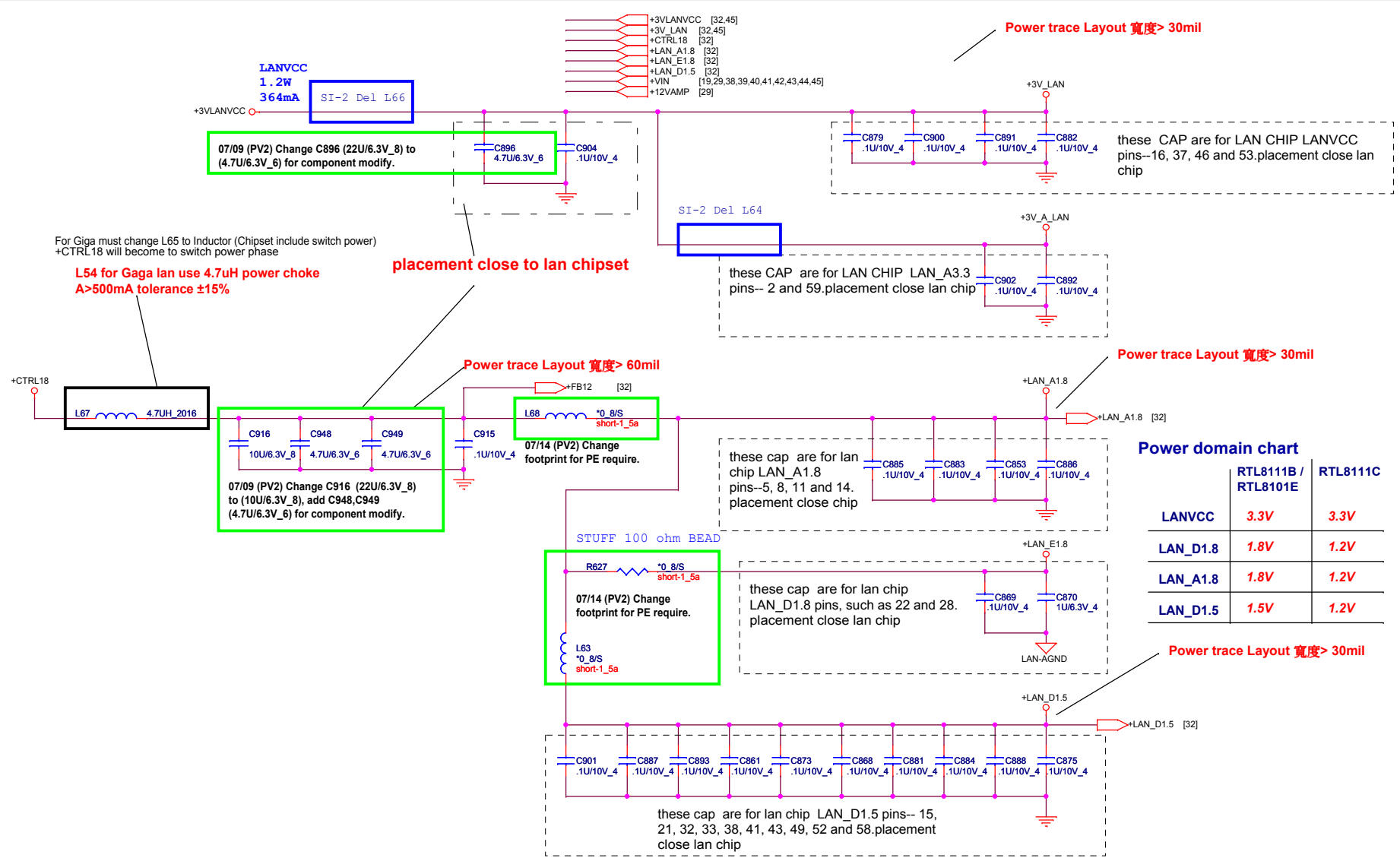
if ISOLATEB pin pull-low, the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)



07/14 (PV2) Change footprint for PE require. 7/16 (PV2) Delete R637 for ICT.

AL08111C001 IC CTRL(64P) RTL8111C-VB-GR(QFN)

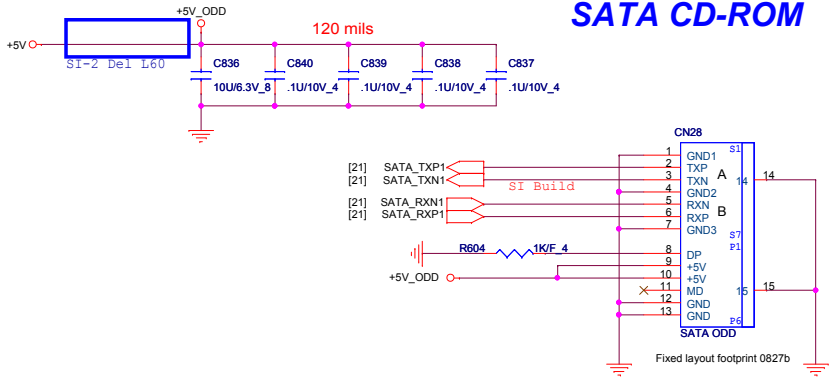




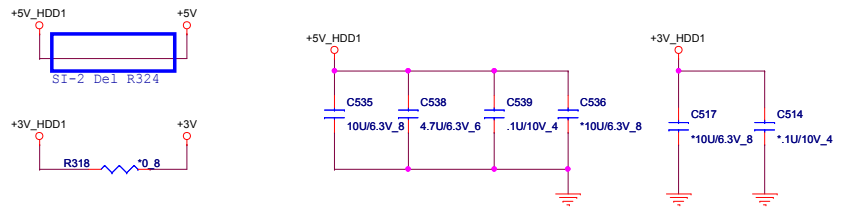
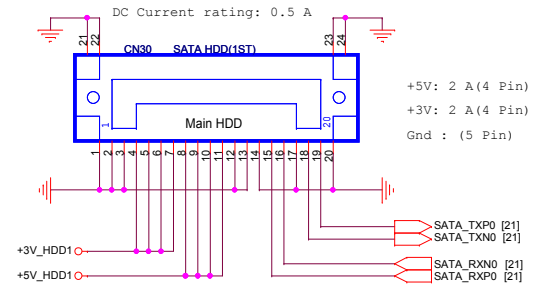
Power domain chart

	RTL8111B / RTL8101E	RTL8111C
LANVCC	3.3V	3.3V
LAN_D1.8	1.8V	1.2V
LAN_A1.8	1.8V	1.2V
LAN_D1.5	1.5V	1.2V

SATA CD-ROM

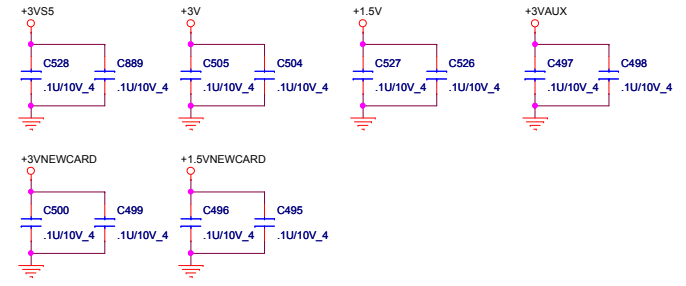
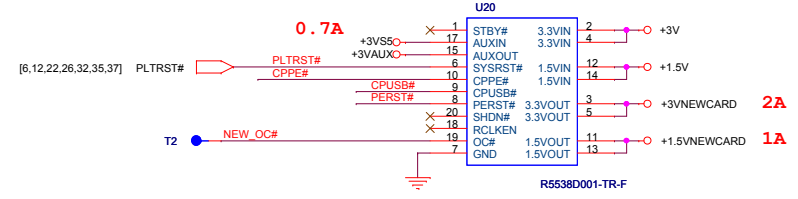
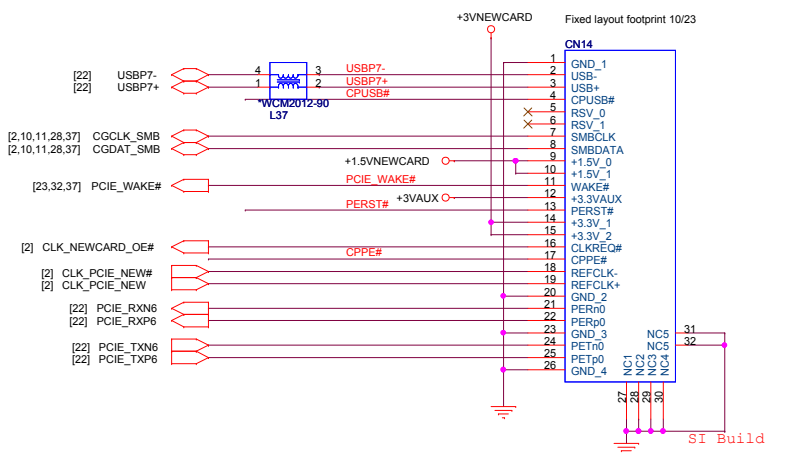


SATA_1 CONNECTOR

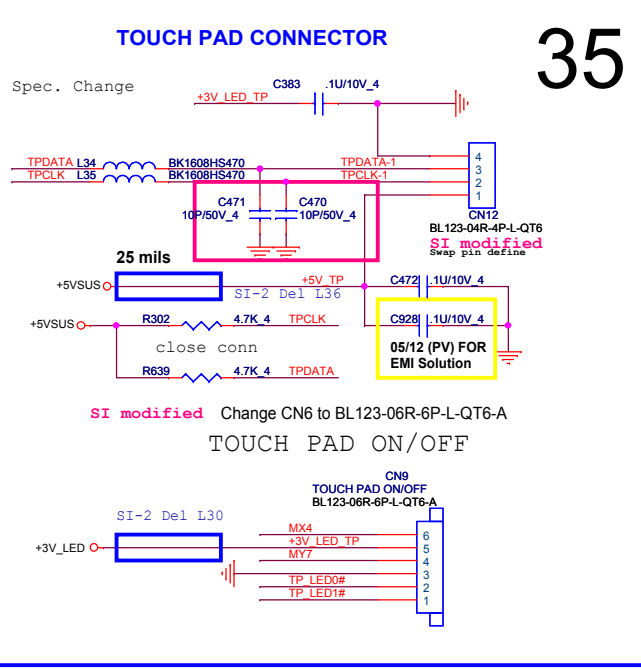
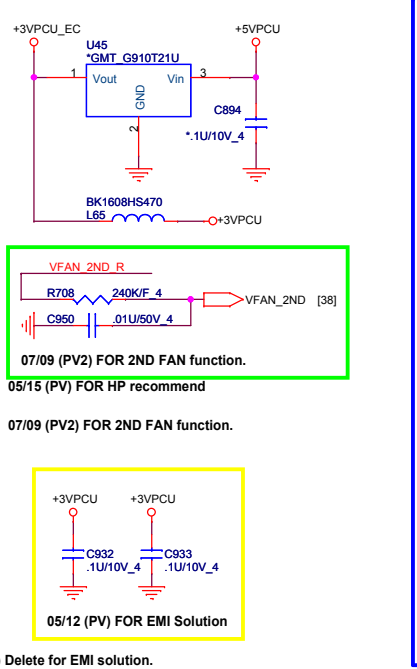
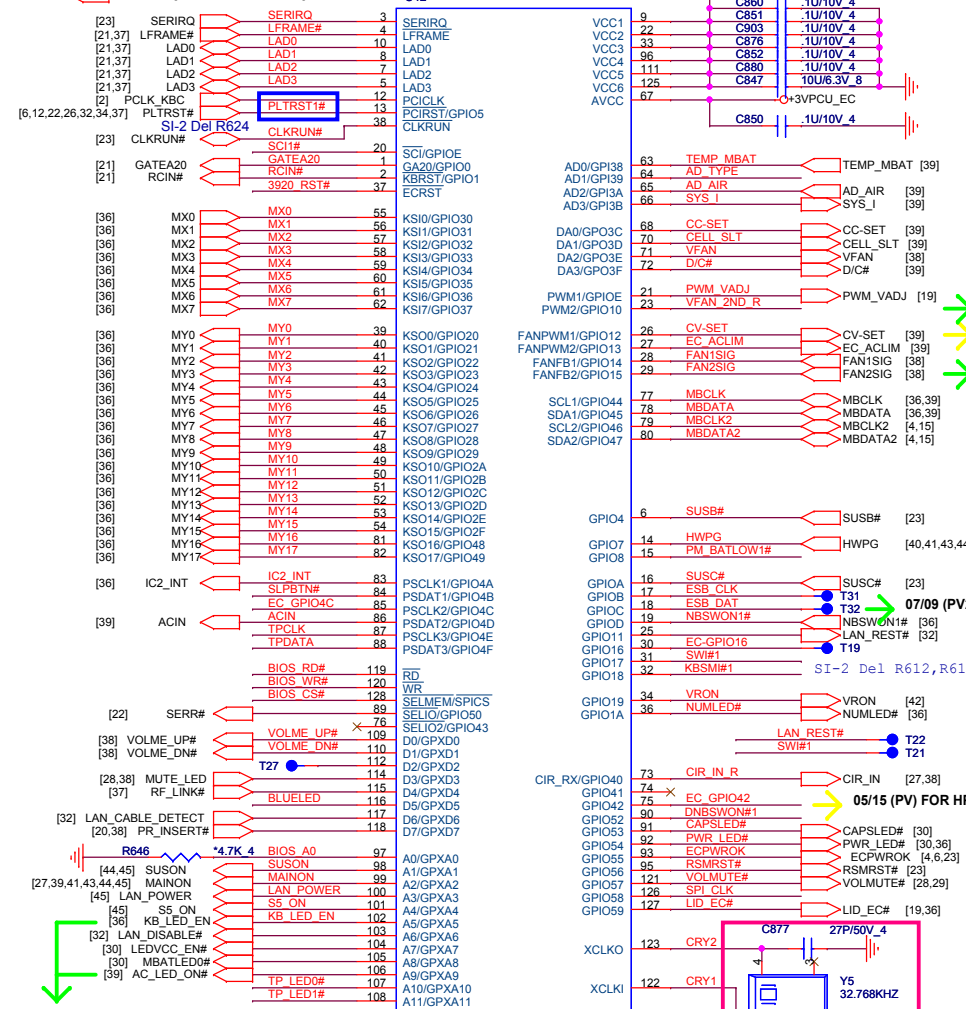


NEWCARD

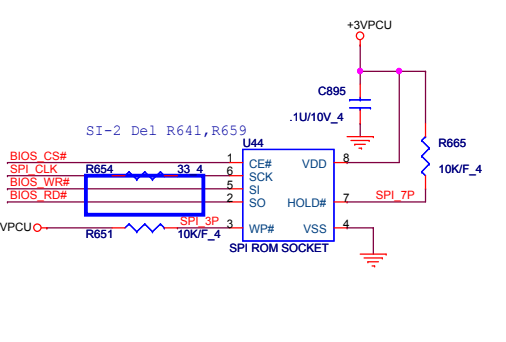
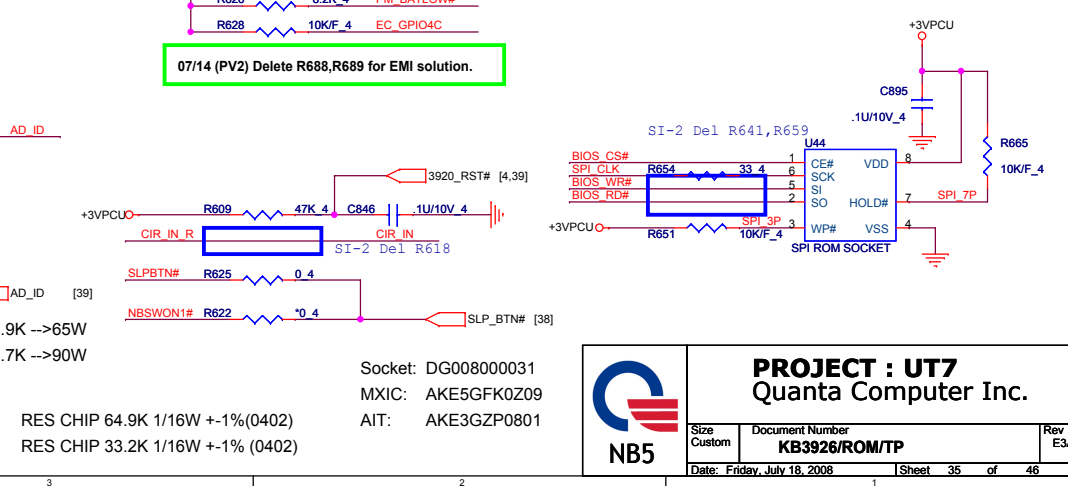
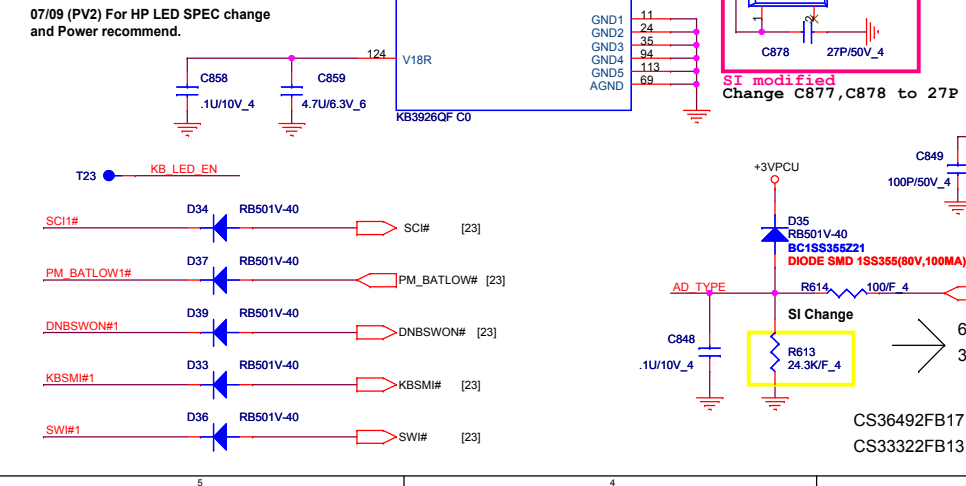
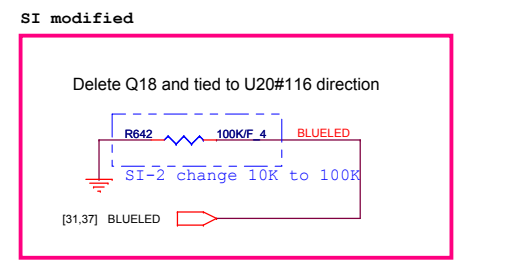
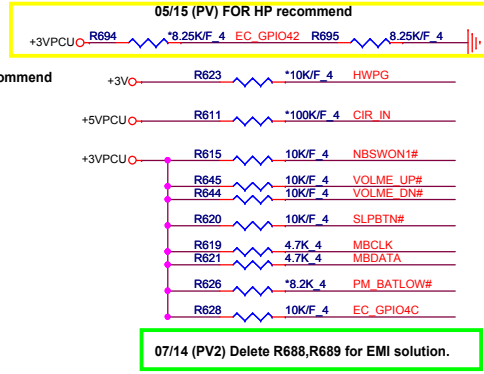
NEWCARD (PCIEXPRESS*1 + USB*1)



[2,4,6,9,10,11,12,14,15,19,20,21,22,23,24,25,26,27,28,29,30,31,32,34,37,38,42,43,45]
 +3V [19,21,30,31,36,38,39,40,45]
 +5VSUS [19,27,31,38,45]
 +5VPCU [27,28,40,41,42,43,44,45]



MODEL	UT7 120W (H)	UT6 90W (L)	UT6 65W (0.5V)
R694	8.25K/F_4	N/A	45.3K/F_4
R695	N/A	8.25K/F_4	8.25K/F_4

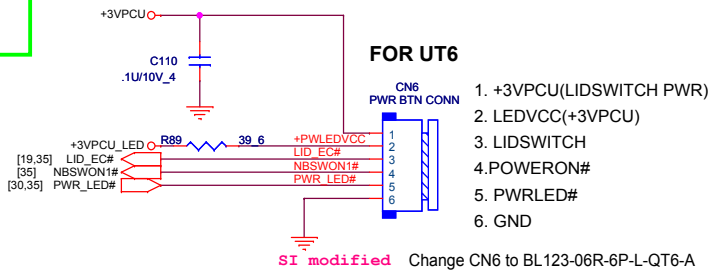
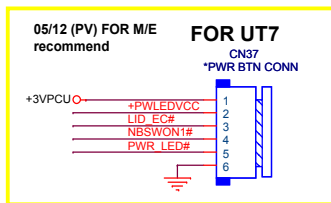
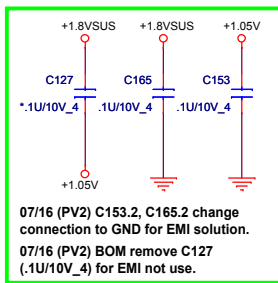


Socket: DG00800031
 MXIC: AKE5GFK0Z09
 AIT: AKE3GZP0801

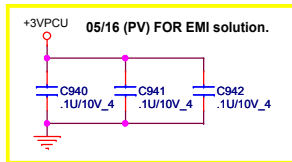
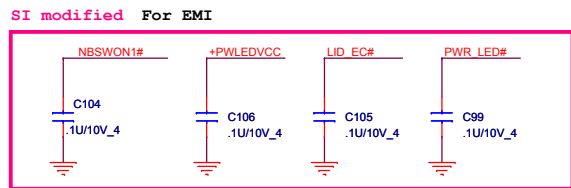
PROJECT : UT7
 Quanta Computer Inc.

NB5

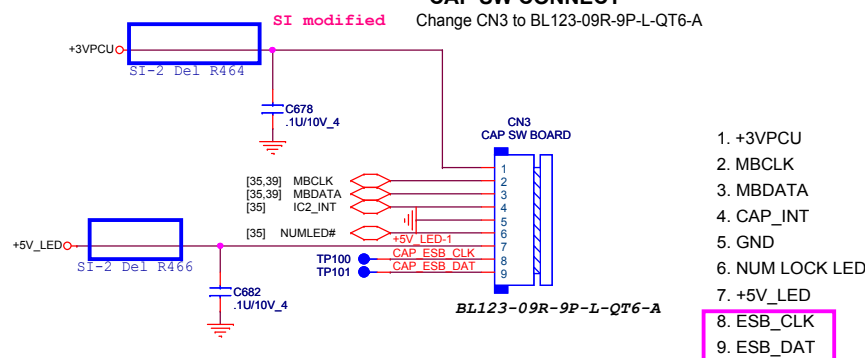
Size Custom	Document Number KB3926/ROM/TP	Rev E3A
Date: Friday, July 18, 2008	Sheet 35 of 46	



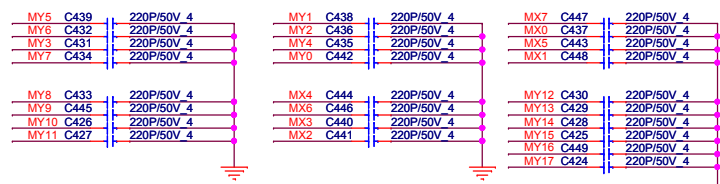
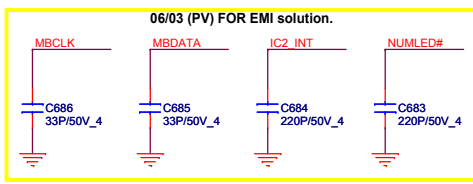
POWER BOTTOM CONNECT



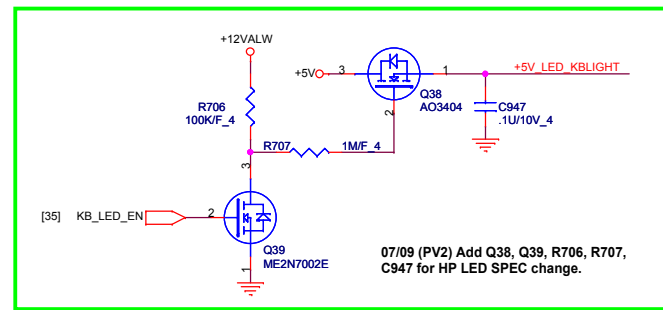
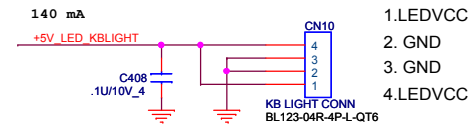
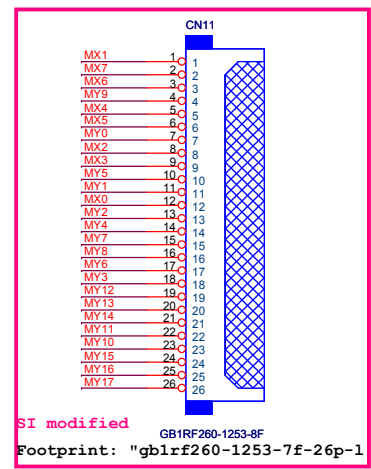
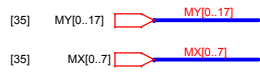
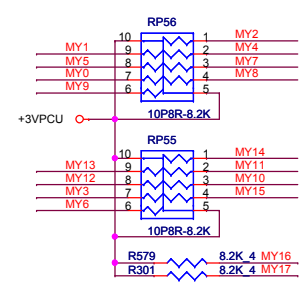
CAP SW CONNECT



07/14 (PV2) Delete L69,L70,C922,C923 for EMI solution.

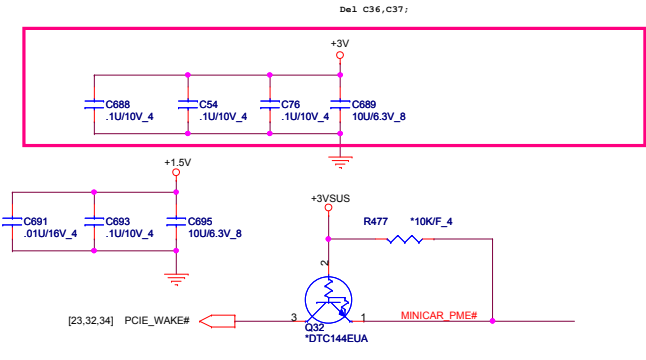
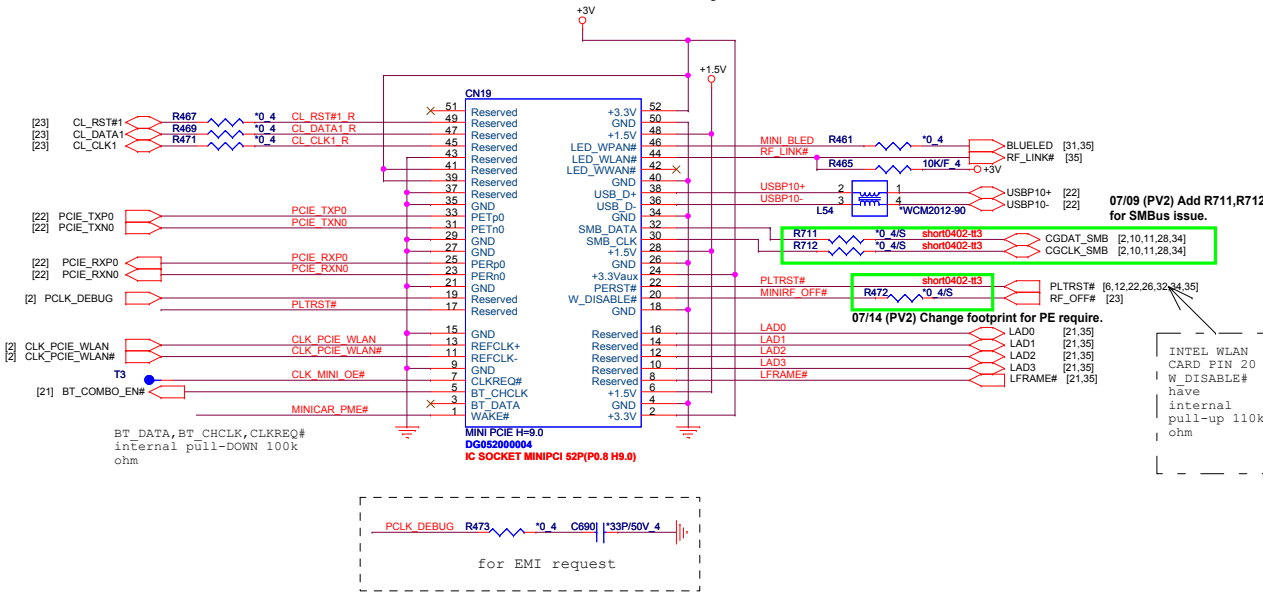


KEYBOARD PULL-UP



Mini PCI-E Card 1 WLAN

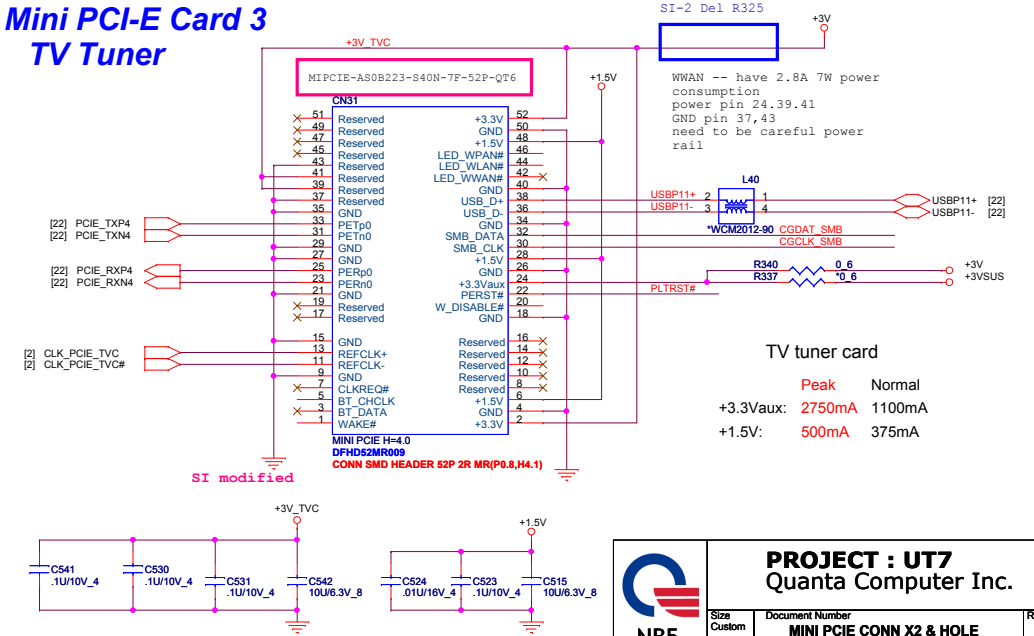
Delete R110,R78
+3V must have a 120mil plane
Each pin 25mil



Mini PCI-E Card 2 ROBSON

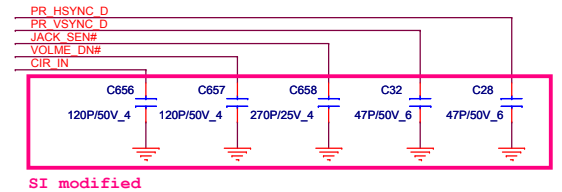
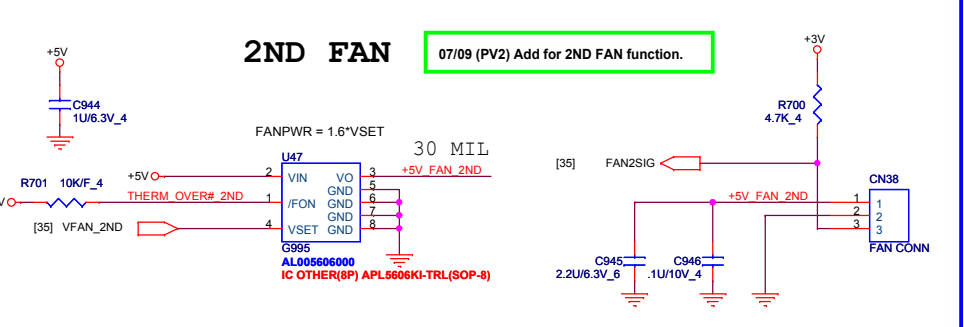
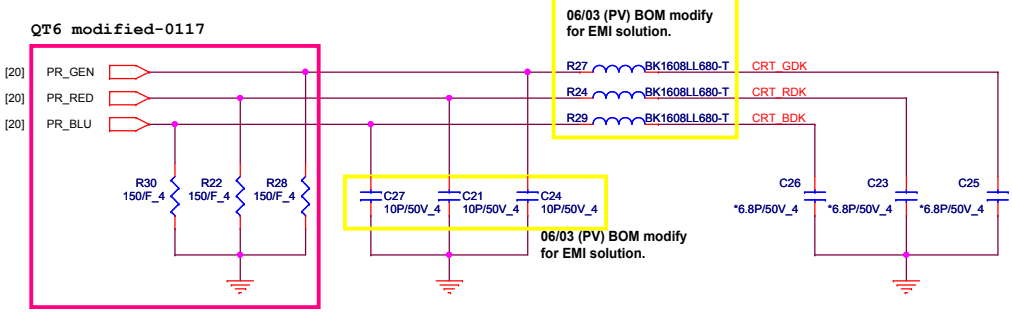
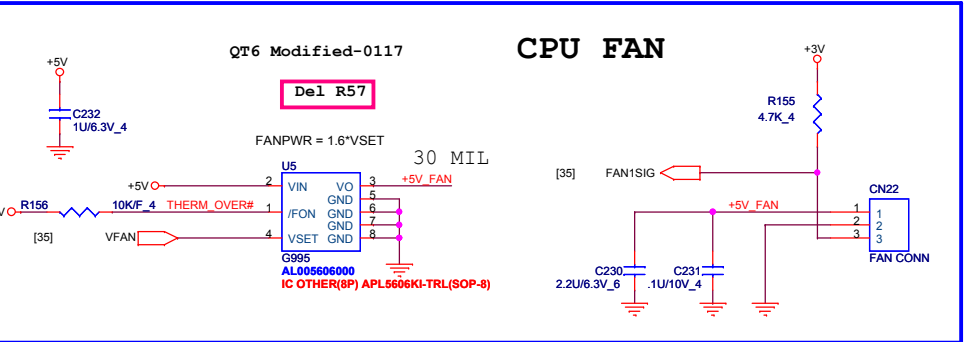
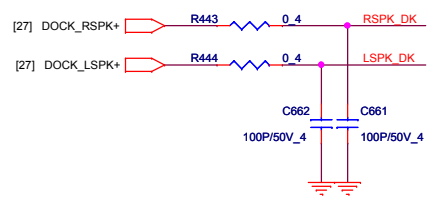
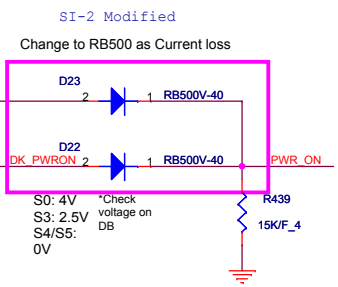
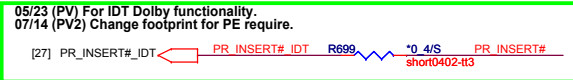
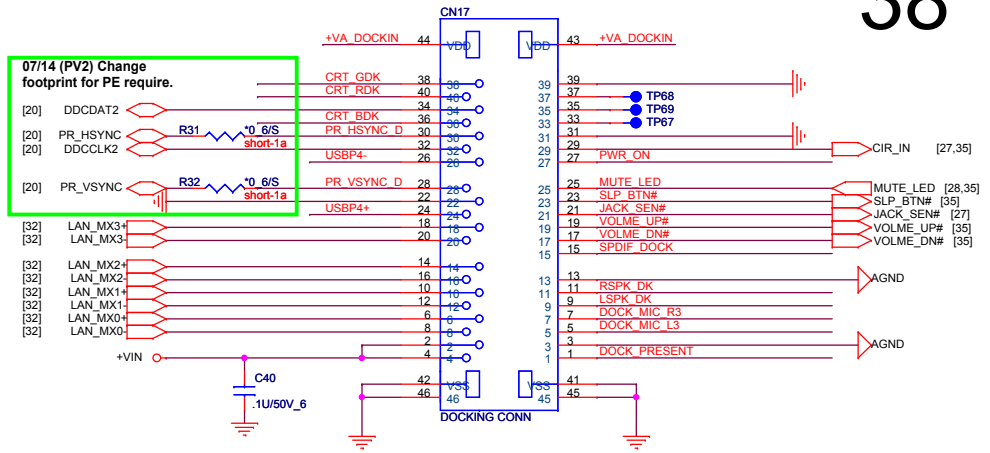
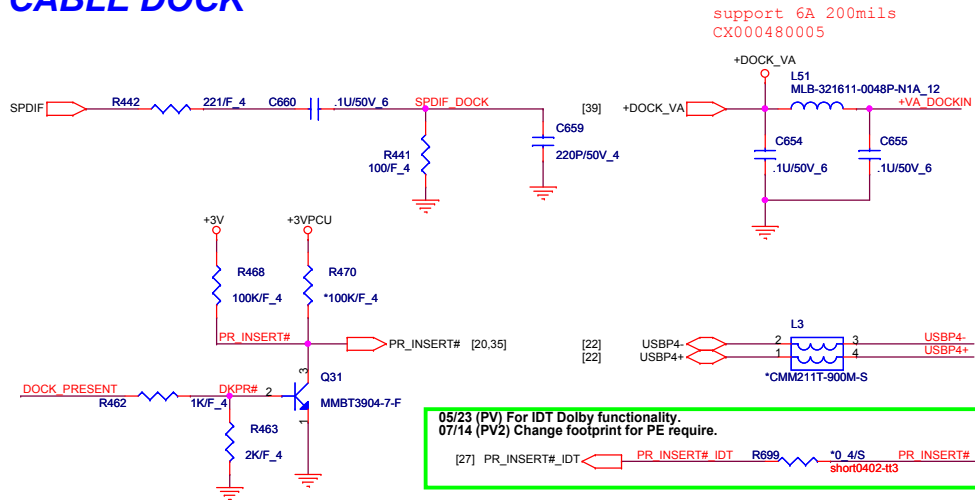
07/09 (PV2) Delete for no support ROBSON card.

Mini PCI-E Card 3 TV Tuner



PROJECT : UT7
Quanta Computer Inc.

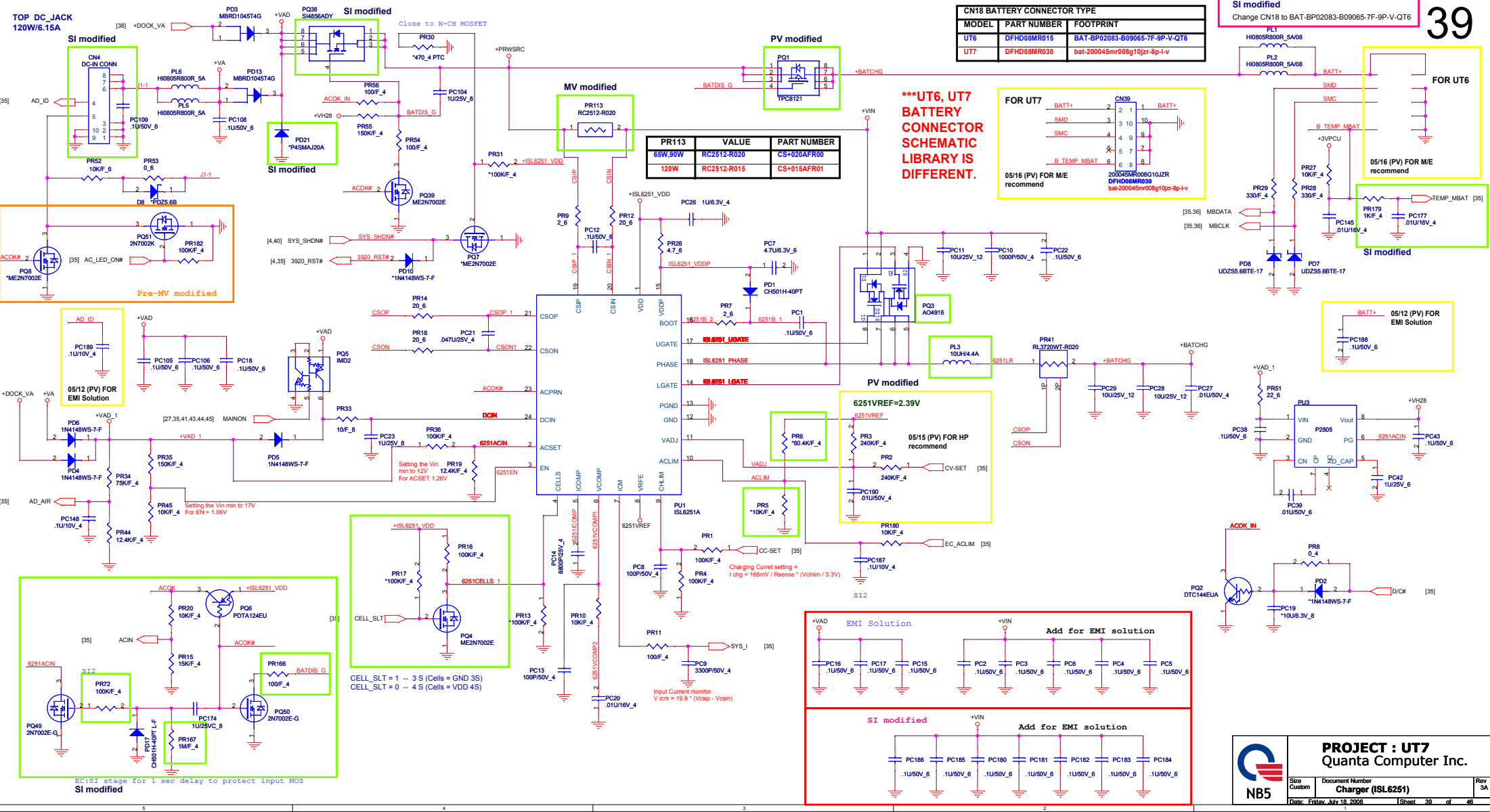
Size Custom	Document Number MINI PCIE CONN X2 & HOLE	Rev E3A
Date: Friday, July 18, 2008	Sheet 37 of 46	



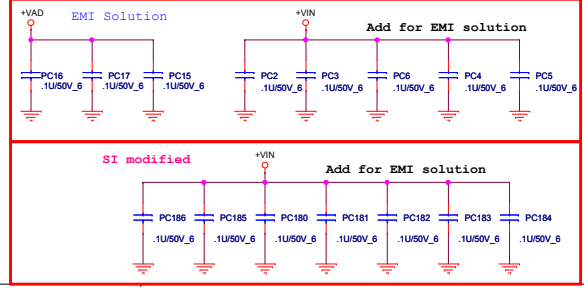
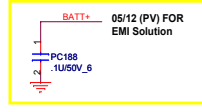
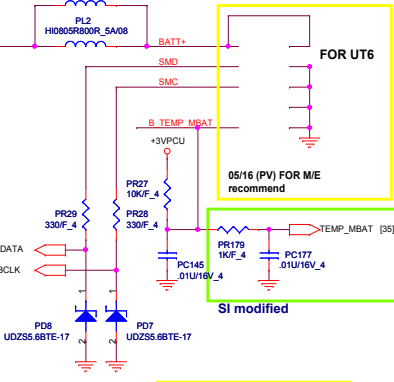
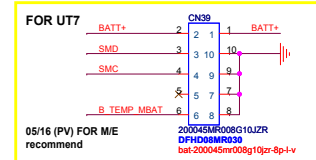
PROJECT : UT7
Quanta Computer Inc.

Size Custom	Document Number CABLE DOCKING/FAN	Rev E3A
Date: Friday, July 18, 2008	Sheet 38 of 46	

CN18 BATTERY CONNECTOR TYPE		
MODEL	PART NUMBER	FOOTPRINT
UT6	DFHD08MR015	BAT-8P02083-B09065-7F-8P-V-QT6
UT7	DFHD08MR030	bat-200445mr009g10zr-8p-l-v



PR113	VALUE	PART NUMBER
65W_90W	RC2512-R020	CS*020AFR00
120W	RC2512-R015	CS*015AFR01



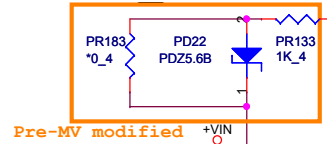
PROJECT : UT7
Quanta Computer Inc.

Size Custom Document Number **Charger (ISL6251)** Rev 3A

Date: Friday, July 18, 2008 Sheet 39 of 46

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+12V ALW

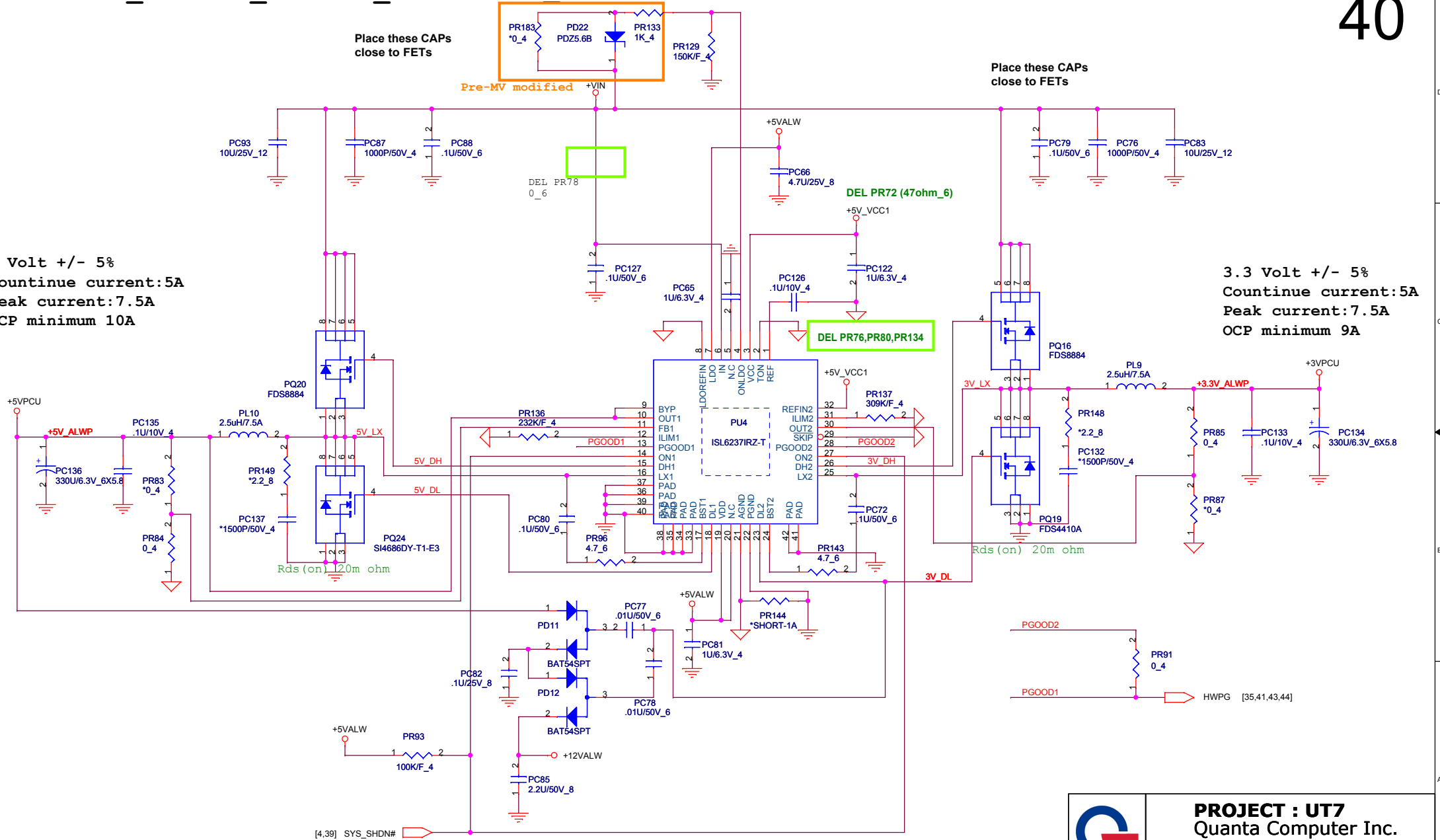
Place these CAPs close to FETs



Place these CAPs close to FETs

5 Volt +/- 5%
 Countinue current:5A
 Peak current:7.5A
 OCP minimum 10A

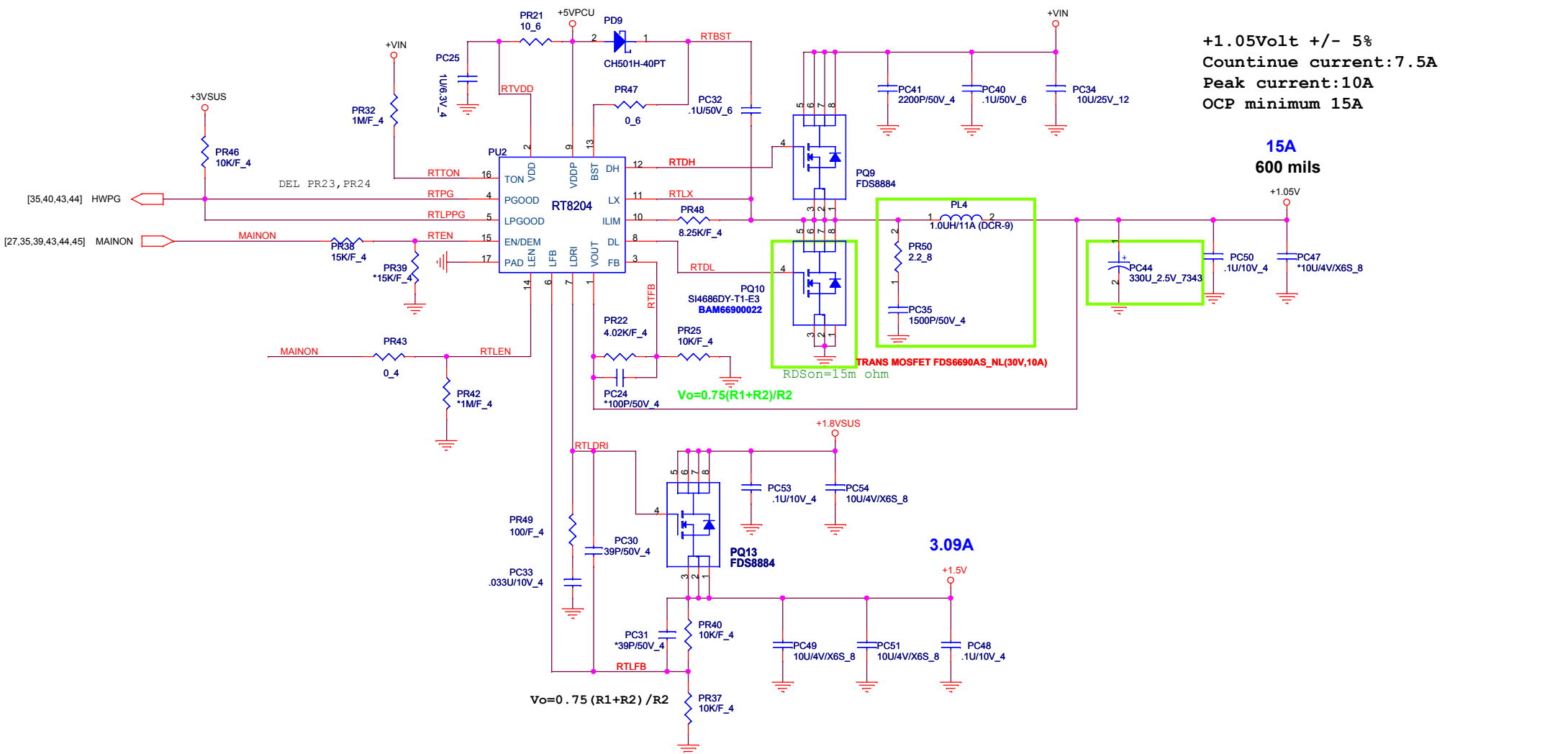
3.3 Volt +/- 5%
 Countinue current:5A
 Peak current:7.5A
 OCP minimum 9A



[4,39] SYS_SHDN#

	PROJECT : UT7 Quanta Computer Inc.	
	Size B Document Number +5V/+3V (ISL6237)	Rev 3A Date: Friday, July 18, 2008

VCCP1.05V & +1.5V




+1.05Volt +/- 5%
 Countinue current:7.5A
 Peak current:10A
 OCP minimum 15A

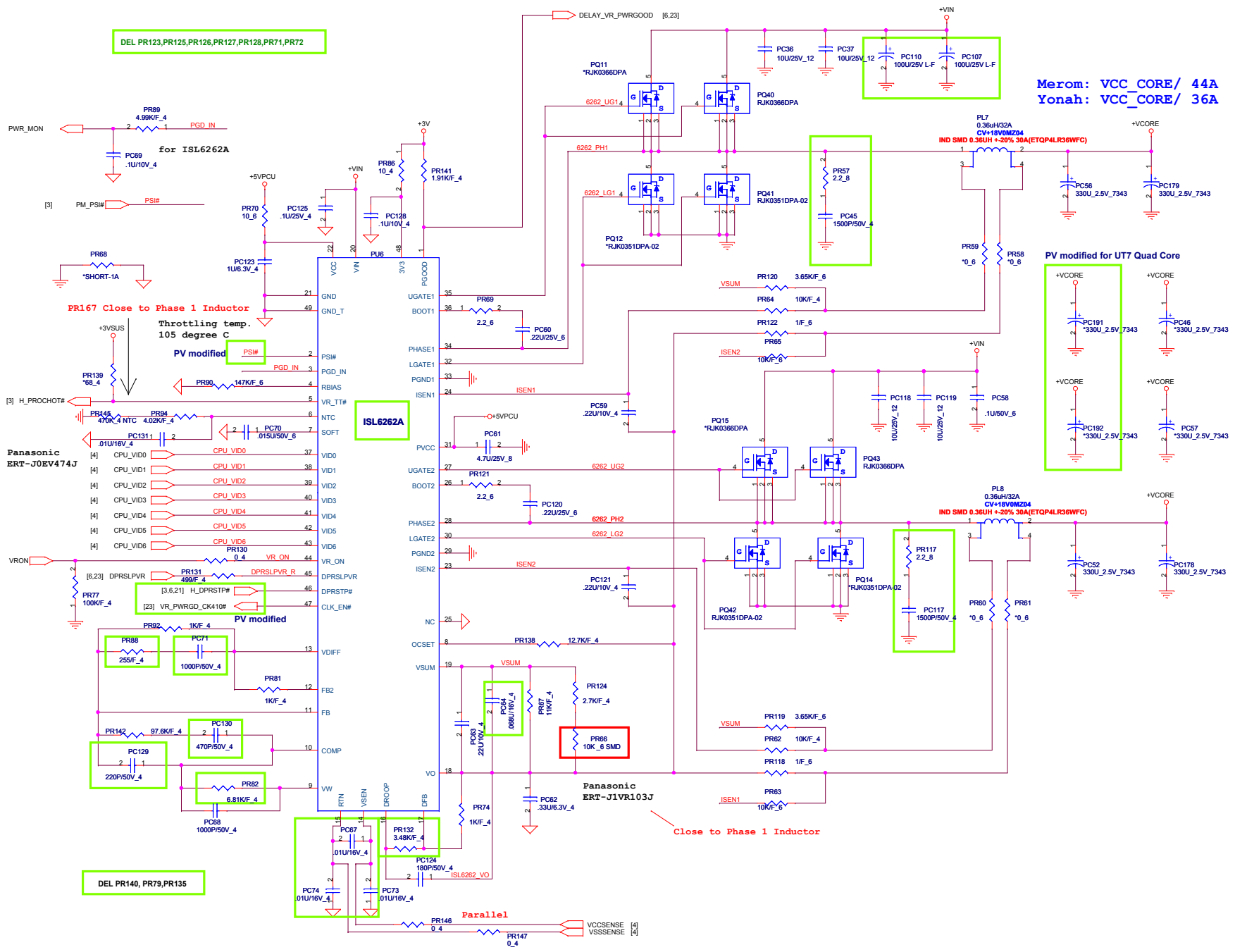
15A
600mils

3.09A

$V_o = 0.75(R1+R2)/R2$

$V_o = 0.75(R1+R2)/R2$

	PROJECT : UT7 Quanta Computer Inc.	
	Size B	Document Number +1.05V/+1.5V (RT8204)
Date: Friday, July 18, 2008		Sheet 41 of 46

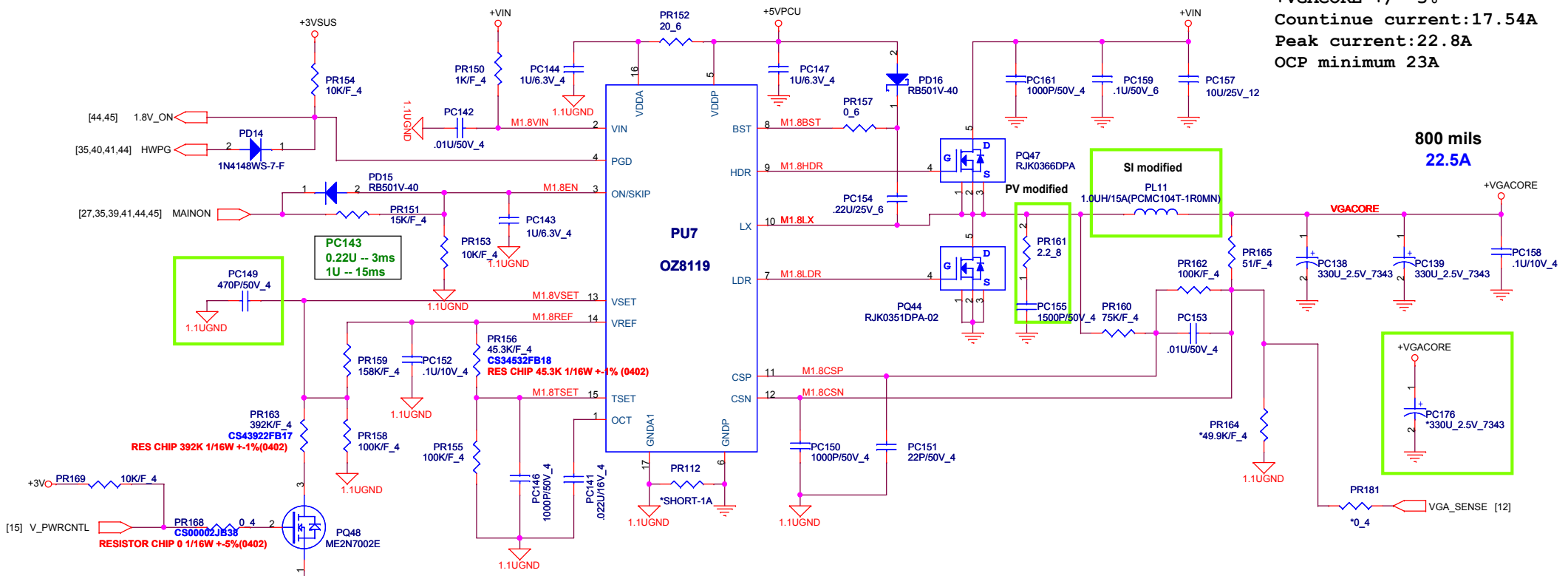


Merom: VCC_CORE/ 44A
 Yonah: VCC_CORE/ 36A

PV modified for UT7 Quad Core

Close to Phase 1 Inductor

	PROJECT : UT7	
	Quanta Computer Inc.	
	Size Custom Document Number CPU Core (ISL6266A) Date: Friday, July 18, 2008	Rev 3A Sheet 42 of 48



+VGACORE +/- 3%
Continue current: 17.54A
Peak current: 22.8A
OCP minimum 23A

800 mils
22.5A

VREF=2.75V +/-1.5%

NB9P-GS: PR163=392Kohm
Output = 0.9V

NB9M-GE: PR203=590Kohm
 NB9P-GS: PR203=768Kohm

CS45902FB10 RES CHIP 590K 1/16W +/-1%(0402)
 CS47682FB10 RES CHIP 768K 1/16W +/-1%(0402)

03/21 remove PD22, PR180, PR181

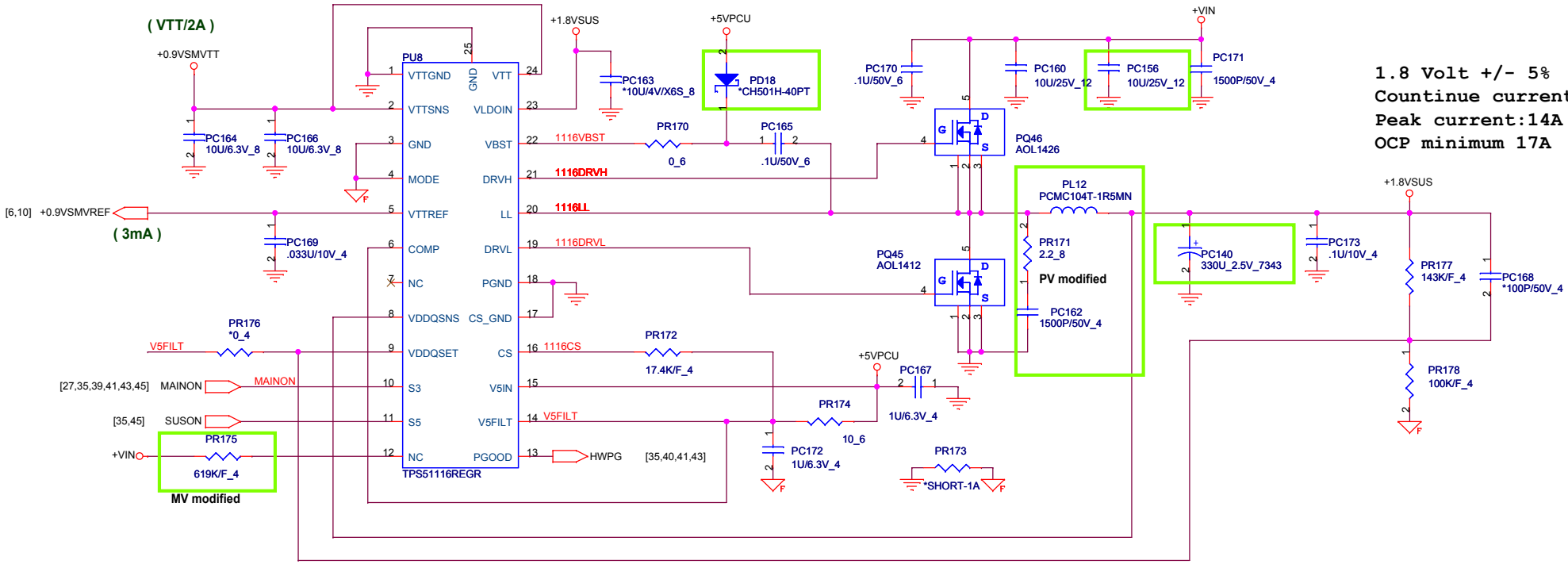
V_PWRCNTL	NB9P-GS
GPIO5	1.05V
Low	1.05V
High	0.9V

VGA_GPIO6	V_PWRCNTL		NB9P-GS	NB9M-GE
GPIO6	GPIO5			
Low	Low	MAX BAT	0.9V	0.9V
Low	High	SD DVD	0.9V	0.9V
High	Low	HD DVD	0.9V	0.9V
High	High	MAX PERF	1.05V	1.09V



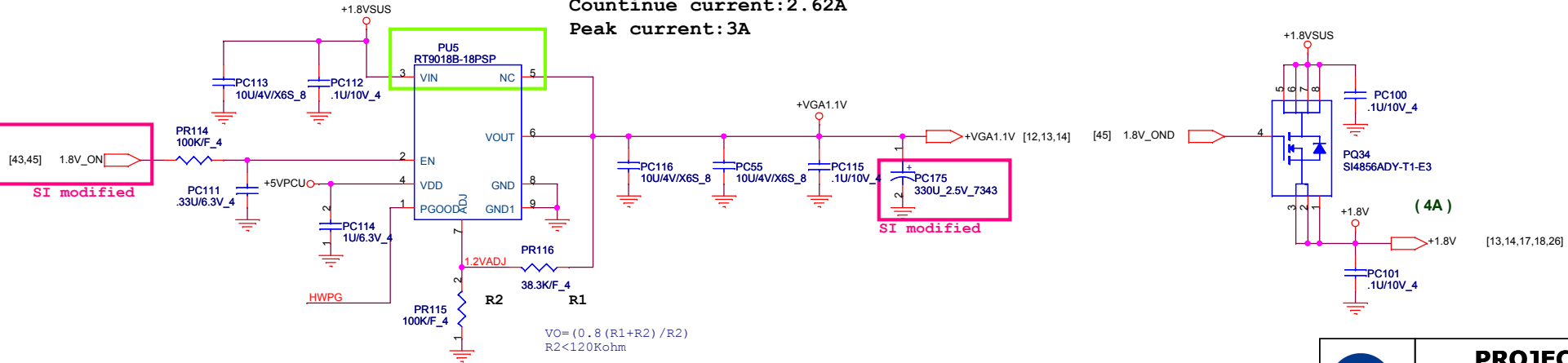
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Size B	Document Number	Rev 3A
	VGA CORE OZ8118	
Date: Friday, July 18, 2008	Sheet 43 of 46	



1.8 Volt +/- 5%
 Countinue current:6A
 Peak current:14A
 OCP minimum 17A

1.1 Volt +/- 5%
 Countinue current:2.62A
 Peak current:3A

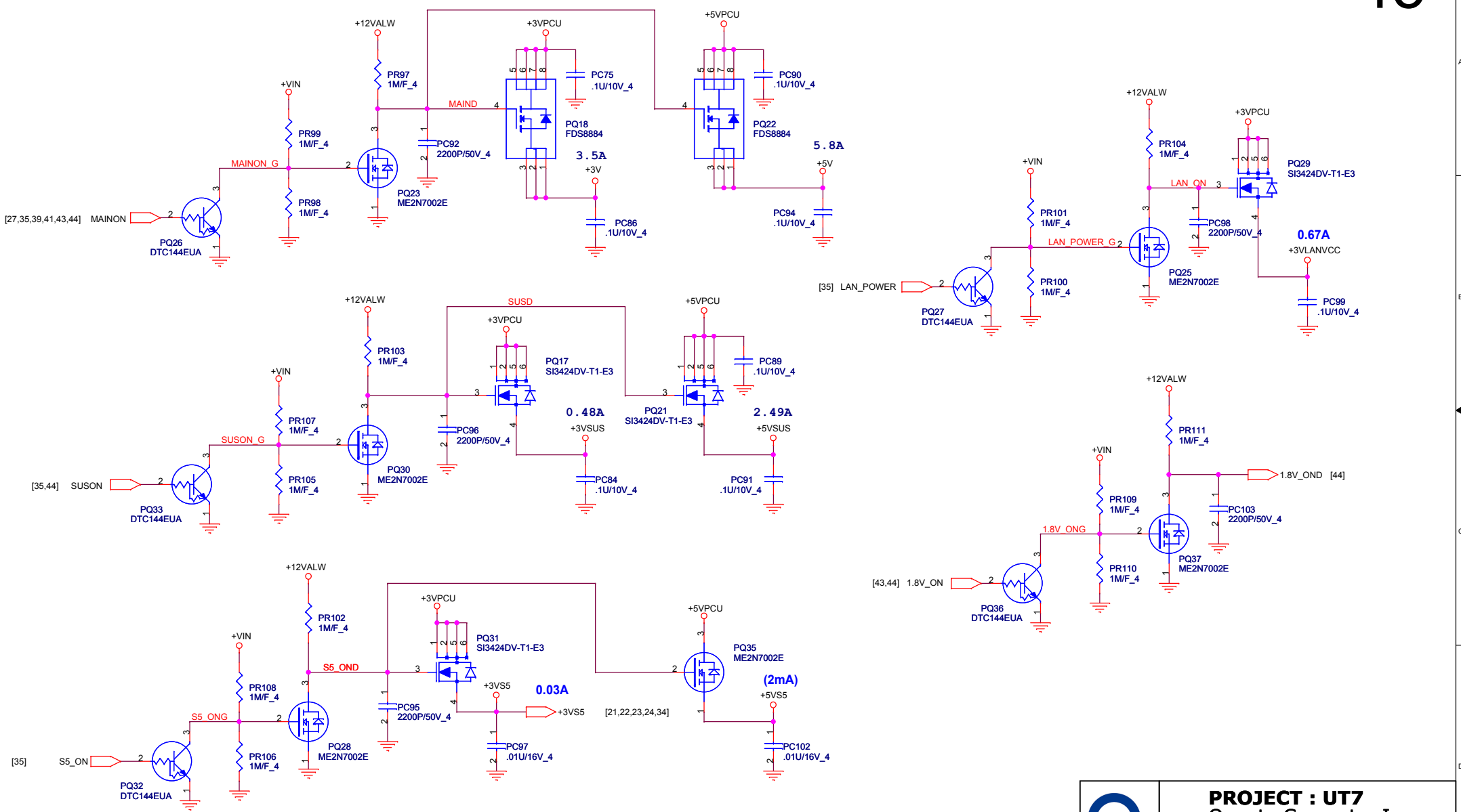


$$VO = (0.8 (R1+R2) / R2)$$

$$R2 < 120Kohm$$




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Size B	Document Number 1.8V/DDR_VTER/+1.8v/+1.1V	Rev 3A
Date: Friday, July 18, 2008 Sheet 44 of 46		



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Size B	Document Number DISCHARGE/3VS5/5VS5/LAN	Rev 3A
Date: Friday, July 18, 2008	Sheet 45 of 46	

	Voltage level	AC MODE				DC MODE			
		S0	S3	S4	S5	S0	S3	S4	S5
+3VPCU	3.3V +/- 5%	V	V	V	V	V	V	V	V
+5VPCU	5V +/- 5%	V	V	V	V	V	V	V	V
+3VRTC	3.3V +/- 5%	V	V	V	V	V	V	V	V
+3VS5	3.3V +/- 5%	V	V	V	V	V	V		
+5VS5	5V +/- 5%	V	V	V	V	V	V		
+3VSUS	3.3V +/- 5%	V	V			V	V		
+5VSUS	5V +/- 5%	V	V			V	V		
+1.8VSUS	1.8V +/- 5%	V	V			V	V		
+0.9VSMVTT	0.9V +/- 5%	V	V			V	V		
+1.5V	1.5V +/- 5%	V				V			
+1.05V	1.05V +/- 5%	V				V			
+VCORE	0.9~1.15V	V				V			
+VGA_CORE	0.9~1.2V	V				V			
+VGA1.1V	1.1V +/- 5%	V				V			
+1.8V	1.8V +/- 5%	V				V			
+3VLAVCC	3.3V +/- 5%	V				V			

	PROJECT : UT7 Quanta Computer Inc.	
	Size Custom Date: Friday, July 18, 2008	Document Number Voltage Sheet 46 of 46