

FEATURES

Small package: 10-lead MSOP
Programmable gains: 1, 10, 100, 1000
Digital or pin-programmable gain setting

Wide supply: ± 5 V to ± 15 V

Excellent dc performance

High CMRR 120 dB, G = 100
 Low gain drift: 10 ppm/ $^{\circ}$ C
 Low offset drift: 1.2 μ V/ $^{\circ}$ C, G = 1000

Excellent ac performance

Fast settling time: 615 ns to 0.001%
 High slew rate: 20 V/ μ s
 Low distortion:
 High CMRR over frequency: 80 dB to 50 kHz
 Low noise: 8 nV/ \sqrt Hz, G = 1000
 Low power: 4 mA

APPLICATIONS

Data acquisition
 Biomedical analysis
 Test and measurement

GENERAL DESCRIPTION

The AD8253 is an instrumentation amplifier with digitally programmable gains that has $G\Omega$ input impedance, low output noise, and low distortion making it suitable for interfacing with sensors and driving high sample rate analog-to-digital converters (ADCs). It has high bandwidth of 10 MHz, low THD and fast settling time of 615 ns to 0.001%. Offset drift and gain drift are specified to 1.2 μ V/ $^{\circ}$ C and 10 ppm/ $^{\circ}$ C, respectively for G = 1000. In addition to its wide input common voltage range, it boasts a high common-mode rejection of 80 dB at G = 1 from dc to 50 kHz. The combination of precision dc performance coupled with high speed capabilities make the AD8253 an excellent candidate for data acquisition. Furthermore, this monolithic solution simplifies design and manufacturing, and boosts performance of instrumentation by maintaining a tight match of internal resistors and amplifiers.

The AD8253 user interface consists of a parallel port that allows users to set the gain in one of two different ways (see Figure 1 for the functional block diagram). A 2-bit word sent via a bus can be latched using the WR input. An alternative is to use transparent gain mode where the state of logic levels at the gain port determines the gain.

FUNCTIONAL BLOCK DIAGRAM

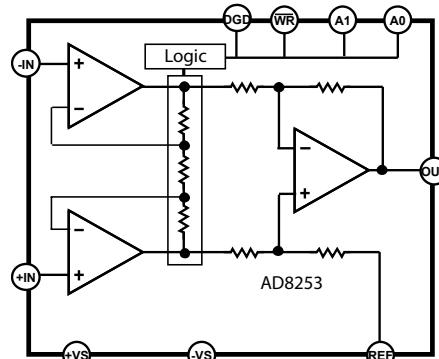


Figure 1.

Table 1. Instrumentation and Difference Amplifiers by Category

High Performance	Low Cost	High Voltage	Mil Grade	Low Power	Digital Gain
AD8220 ¹	AD623 ¹	AD628	AD620	AD627 ¹	AD8231 ¹
AD8221	AD8553 ¹	AD629	AD621		AD8250
AD8222			AD524		AD8251
AD8224 ¹			AD526	AD624	AD8555 ¹
			AD624		AD8556 ¹
					AD8557 ¹

¹ Rail-to-rail output.

The AD8253 is available in a 10-lead MSOP package and is specified over the -40° C to $+85^{\circ}$ C temperature range, making it an excellent solution for applications where size and packing density are important considerations.

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REVISION HISTORY

4/07—Revision 0: Initial Version

SPECIFICATIONS

$+V_S = +15\text{ V}$, $-V_S = -15\text{ V}$, $V_{REF} = 0\text{ V}$ @ $T_A = 25^\circ\text{C}$, $G = 1$, $R_L = 2\text{ k}\Omega$, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
COMMON-MODE REJECTION RATIO (CMRR)					
CMRR to 60 Hz with 1 kΩ Source Imbalance	$+IN = -IN = -10\text{ V}$ to $+10\text{ V}$	80			dB
G = 1		100			dB
G = 10		120			dB
G = 100		120			dB
G = 1000					dB
CMRR to 50 kHz	$+IN = -IN = -10\text{ V}$ to $+10\text{ V}$	80			dB
G = 1					dB
G = 10					dB
G = 100					dB
G = 1000					dB
NOISE					
Voltage Noise, 1 kHz, RTI					
G = 1		40			nV/ $\sqrt{\text{Hz}}$
G = 10		9			nV/ $\sqrt{\text{Hz}}$
G = 100		8			nV/ $\sqrt{\text{Hz}}$
G = 1000		8			nV/ $\sqrt{\text{Hz}}$
0.1 Hz to 10 Hz, RTI					
G = 1		2.5			μV p-p
G = 10		2.5			μV p-p
G = 100					μV p-p
G = 1000					μV p-p
Current Noise, 1 kHz		5			pA/ $\sqrt{\text{Hz}}$
Current Noise, 0.1 Hz to 10 Hz		60			pA p-p
VOLTAGE OFFSET					
Offset RTI V_{os}	G = 1, 10, 100, 1000				μV
Over Temperature	T = -40°C to $+85^\circ\text{C}$				μV
Average TC	T = -40°C to $+85^\circ\text{C}$				$\mu\text{V}/^\circ\text{C}$
Offset Referred to the Input vs. Supply (PSR)	$V_S = \pm 5\text{ V}$ to $\pm 15\text{ V}$				$\mu\text{V}/\text{V}$
INPUT CURRENT					
Input Bias Current		5	30		nA
Over Temperature	T = -40°C to $+85^\circ\text{C}$		40		nA
Average TC			400		pA/ $^\circ\text{C}$
Input Offset Current		5	30		nA
Over Temperature	T = -40°C to $+85^\circ\text{C}$		30		nA
Average TC			160		pA/ $^\circ\text{C}$
DYNAMIC RESPONSE					
Small Signal –3 dB Bandwidth					
G = 1		10			MHz
G = 10		6			MHz
G = 100		3			MHz
G = 1000		0.3			MHz
Settling Time 0.01%	$\Delta OUT = 10\text{ V}$ step				
G = 1		585			ns
G = 10		648			ns
G = 100					ns
G = 1000					ns

Parameter	Conditions	Min	Typ	Max	Unit
Settling Time 0.001%	$\Delta OUT = 10 \text{ V step}$		615	685	ns
G = 1					ns
G = 10					ns
G = 100					ns
G = 1000					ns
Slew Rate					
G = 1		20			V/ μs
G = 10		25			V/ μs
G = 100		25			V/ μs
G = 1000		25			V/ μs
Total Harmonic Distortion	f = 1 kHz, $R_L = 10 \text{ k}\Omega$, G = 1				dB
GAIN					
Gain Range	G = 1, 10, 100, 1000	1	1000		V/V
Gain Error	OUT = $\pm 10 \text{ V}$				
G = 1		0.03			%
G = 10		0.04			%
G = 100					%
G = 1000					%
Gain Nonlinearity	OUT = -10 V to +10 V				
G = 1	$R_L = 10 \text{ k}\Omega, 2 \text{ k}\Omega, 600 \Omega$	6			ppm
G = 10	$R_L = 10 \text{ k}\Omega, 2 \text{ k}\Omega, 600 \Omega$	10			ppm
G = 100	$R_L = 10 \text{ k}\Omega, 2 \text{ k}\Omega, 600 \Omega$				ppm
G = 1000	$R_L = 10 \text{ k}\Omega, 2 \text{ k}\Omega, 600 \Omega$				ppm
Gain vs. Temperature	All gains	10			ppm/ $^{\circ}\text{C}$
INPUT					
Input Impedance		1			
Differential		1			$\text{G}\Omega \text{pF}$
Common Mode					$\text{G}\Omega \text{pF}$
Input Operating Voltage Range	$V_s = \pm 5 \text{ V to } \pm 15 \text{ V}$	- $V_s + 1.0$	+ $V_s - 1.1$		V
Over Temperature	T = -40°C to +85°C	- $V_s + 1.1$	+ $V_s - 1.4$		V
OUTPUT					
Output Swing		-13.5	+13.5		V
Over Temperature	T = -40°C to +85°C	-13.5	+13.5		V
Short-Circuit Current		37			mA
REFERENCE INPUT					
R_{IN}		20			k Ω
I_{IN}	+IN, -IN, REF = 0		1		μA
Voltage Range		- V_s	+ V_s		V
Gain to Output		1 ± 0.0001			V/V
DIGITAL LOGIC					
Digital Ground Voltage, DGND	Referred to GND	- $V_s + 4.25$	0	+ $V_s - 2.7$	V
Digital Input Voltage Low	Referred to GND	DGND		2.1	V
Digital Input Voltage High	Referred to GND	2.8		+ V_s	V
Digital Input Current			1		μA
Gain Switching Time ¹				325	ns
t_{SU}	See Figure 2 timing diagram	20			ns
t_{HD}		10			ns
t_{WR_LOW}		20			ns
t_{WR_HIGH}		40			ns

Parameter	Conditions	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range		± 5		± 15	V
Quiescent Current, $+I_S$			4.1	4.5	mA
Quiescent Current, $-I_S$			3.7	4.5	mA
Over Temperature	$T = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$			4.5	mA
TEMPERATURE RANGE					
Specified Performance		-40		+85	$^{\circ}\text{C}$

¹ Add time for the output to slew and settle to calculate the total time for a gain change.

TIMING DIAGRAM

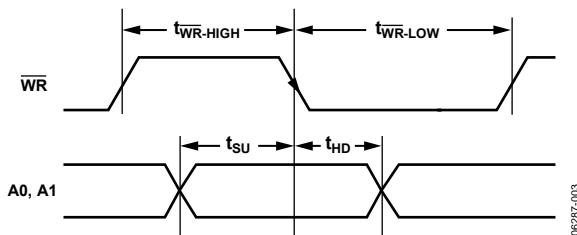


Figure 2. Timing Diagram for Latched Gain Mode (See the Timing for Latched Gain Mode Section)

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ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	$\pm 17\text{ V}$
Power Dissipation	See Figure 3
Output Short-Circuit Current	Indefinite ¹
Common-Mode Input Voltage	$\pm V_S$
Differential Input Voltage	$\pm V_S$
Digital Logic Inputs	$\pm V_S$
Storage Temperature Range	-65°C to +125°C
Operating Temperature Range ²	-40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	140°C
θ_{JA} (4-Layer JEDEC Standard Board)	112°C/W
Package Glass Transition Temperature	140°C

¹ Assumes the load is referenced to mid supply.

² Temperature for specified performance is -40°C to +85°C. For performance to +125°C, see the **Error! Reference source not found.** section.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the AD8253 package is limited by the associated rise in junction temperature (T_J) on the die. The plastic encapsulating the die locally reaches the junction temperature. At approximately 140°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8253. Exceeding a junction temperature of 140°C for an extended period can result in changes in silicon devices, potentially causing failure.

The still-air thermal properties of the package and PCB (θ_{JA}), the ambient temperature (T_A), and the total power dissipated in the package (P_D) determine the junction temperature of the die. The junction temperature is calculated as

$$T_J = T_A + (P_D \times \theta_{JA})$$

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the

package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). Assuming the load (R_L) is referenced to midsupply, the total drive power is $V_S/2 \times I_{OUT}$, some of which is dissipated in the package and some in the load ($V_{OUT} \times I_{OUT}$).

The difference between the total drive power and the load power is the drive power dissipated in the package.

$$P_D = \text{Quiescent Power} + (\text{Total Drive Power} - \text{Load Power})$$

$$P_D = (V_S \times I_S) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L} \right) - \frac{V_{OUT}^2}{R_L}$$

In single-supply operation with R_L referenced to $-V_S$, worst case is $V_{OUT} = V_S/2$.

Airflow increases heat dissipation, effectively reducing θ_{JA} . In addition, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA} .

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature on a 4-layer JEDEC standard board.

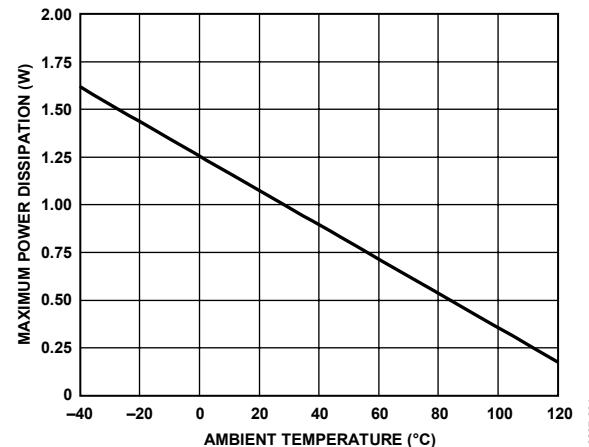


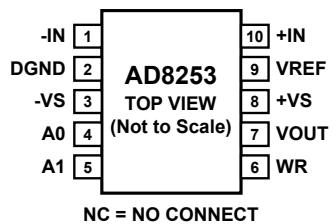
Figure 3. Maximum Power Dissipation vs. Ambient Temperature

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



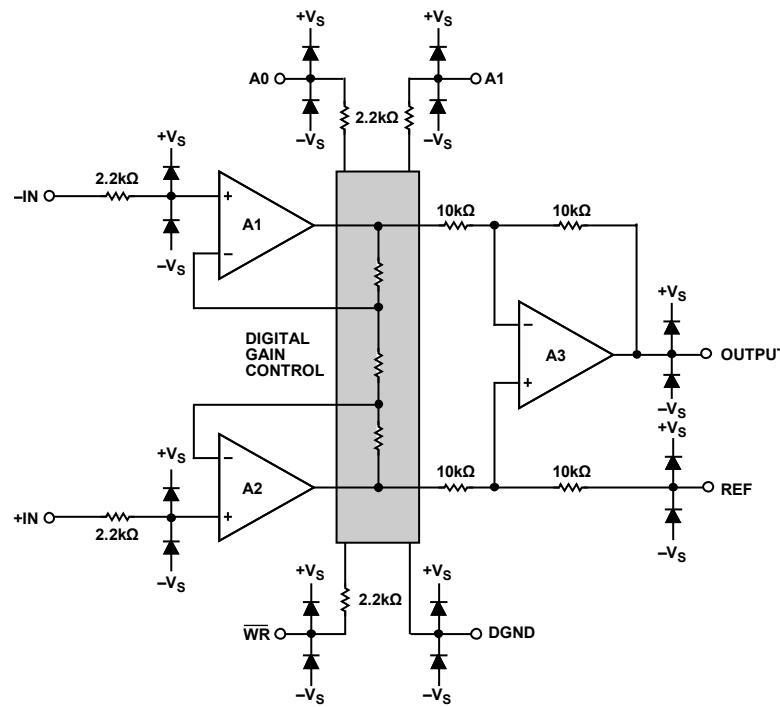
2	DGND	differential input. Digital Ground.
3	-Vs	Negative Supply Terminal.
4	A0	Gain Setting Pin (LSB).
5	A1	Gain Setting Pin (MSB).
6	WR	Write Enable.
7	OUT	Output Terminal.
8	+Vs	Positive Supply Terminal.
9	REF	Reference Voltage Terminal.
10	+IN	Noninverting Input Terminal. True differential input.

Figure 4. 10-Lead MSOP (RM-10) Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Name	Description
1	-IN	Inverting Input Terminal. True

THEORY OF OPERATION



06287-050

Figure 5. Simplified Schematic

The AD8253 is a monolithic instrumentation amplifier based on the classic, three op amp topology as shown in Figure 5. It is fabricated on the Analog Devices, Inc. proprietary *i*CMOS process that provides precision, linear performance ,and a robust digital interface. A parallel interface allows users to digitally program gains of 1, 10, 100, and 1000. Gain control is achieved by switching resistors in an internal, precision, resistor array (as shown in Figure 5). Although the AD8253 has a voltage feedback topology, gain bandwidth product increases for gains of 1, 10, and 100 because each gain has its own frequency compensation. This results in maximum bandwidth at higher gains.

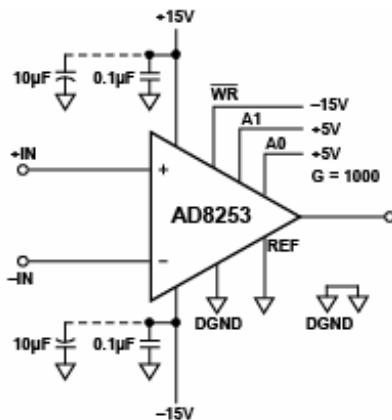
All internal amplifiers employ distortion cancellation circuitry and achieve high linearity and ultralow THD. Laser trimmed resistors allow for a maximum gain error of less than 0.03% for $G = 1$, and minimum CMRR of 120 dB for $G = 1000$. A pinout optimized for high CMRR over frequency enables the AD8253 to offer CMRR over frequency of 80 dB at 50 kHz ($G = 1$). The balanced input reduces the parasitics that, in the past, had adversely affected CMRR performance.

GAIN SELECTION

This section shows users how to configure the AD8253 for basic operation. Logic low and Logic high voltage limits are listed in the Specifications section. Typically, logic low is 0 V and logic high is 5 V; both voltages are measured with respect to DGND. Refer to the specifications table (Table 2) for the permissible voltage range of DGND. The gain of the AD8253 can be set using two methods.

Transparent Gain Mode

The easiest way to set the gain is to program it directly via a logic high or logic low voltage applied to A0 and A1. Figure 6 shows an example of this gain setting method, referred to throughout the data sheet as transparent gain mode. Tie WR to the negative supply to engage transparent gain mode. In this mode, any change in voltage applied to A0 and A1 from logic low to logic high, or vice versa, immediately results in a gain change. Table 5 is the truth table for transparent gain mode and Figure 6 shows the AD8253 configured in transparent gain mode.



NOTE:
1. IN TRANSPARENT GAIN MODE, WR IS TIED TO $-V_S$.
THE VOLTAGE LEVELS ON A0 AND A1 DETERMINE
THE GAIN. IN THIS EXAMPLE, BOTH A0 AND A1 ARE
SET TO LOGIC HIGH, RESULTING IN A GAIN OF 1000.

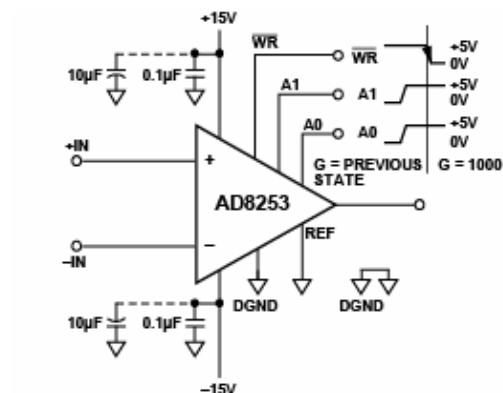
Figure 6. Transparent Gain Mode, A_0 and A_1 = High, $G = 1000$

Table 5. Truth Table Logic Levels for Transparent Gain Mode

WR	A1	A0	Gain
-V _S	Low	Low	1
-V _S	Low	High	10
-V _S	High	Low	100
-V _S	High	High	1000

Latched Gain Mode

Some applications have multiple programmable devices such as multiplexers or other programmable gain instrumentation amplifiers on the same PCB. In such cases, devices can share a data bus. The gain of the AD8253 can be set using WR as a latch, allowing other devices to share A0 and A1. Figure 7 shows a schematic using this method, known as latched gain mode. The AD8253 is in this mode when WR is held at logic high or logic low, typically 5 V and 0 V, respectively. The voltages on A0 and A1 are read on the downward edge of the WR signal as it transitions from logic high to logic low. This latches in the logic levels on A0 and A1, resulting in a gain change. See the truth table listing in Table 6 for more on these gain changes.



NOTE:
1. ON THE DOWNWARD EDGE OF WR, AS IT TRANSITIONS FROM LOGIC HIGH TO LOGIC LOW, THE VOLTAGES ON A0 AND A1 ARE READ AND LATCHED IN, RESULTING IN A GAIN CHANGE. IN THIS EXAMPLE, THE GAIN SWITCHES TO G = 1000.

Figure 7. Latched Gain Mode, G = 1000

Table 6. Truth Table Logic Levels for Latched Gain Mode

WR	A1	A0	Gain
High to Low	Low	Low	Change to 1
High to Low	Low	High	Change to 10
High to Low	High	Low	Change to 100
High to Low	High	High	Change to 1000
Low to Low	X ¹	X ¹	No Change
Low to High	X ¹	X ¹	No Change
High to High	X ¹	X ¹	No Change

¹ X = don't care.

Upon power-up, the AD8253 defaults to a gain of 1 when in latched gain mode. In contrast, if the AD8253 is configured in transparent gain mode, it starts at the gain indicated by the voltage levels on A0 and A1 upon power-up.

Timing for Latched Gain Mode

In latched gain mode, logic levels at A0 and A1 have to be held for a minimum setup time, t_{SU} , before the downward edge of WR latches in the gain. Similarly, they must be held for a minimum hold time of t_{HD} after the downward edge of WR to ensure that the gain is latched in correctly. After t_{HD} , A0 and A1 may change logic levels but the gain does not change (until the next downward edge of WR). The minimum duration that WR can be held high is $t_{\overline{WR-HIGH}}$, and $t_{\overline{WR-LOW}}$ is the minimum duration that WR can be held low. Digital timing specifications are listed in Table 2. The time required for a gain change is dominated by the settling time of the amplifier. A timing diagram is shown in Figure 8.

When sharing a data bus with other devices, logic levels applied to those devices can potentially feed through to the output of the AD8253. Feedthrough can be minimized by decreasing the edge rate of the logic signals. Furthermore, careful layout of the PCB also reduces coupling between the digital and analog portions of the board.

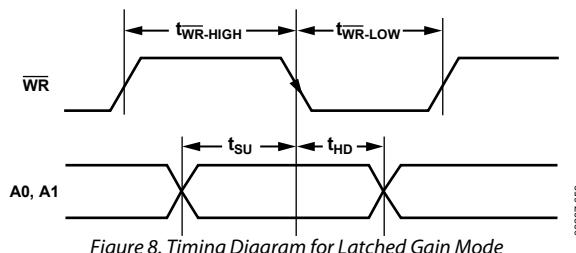
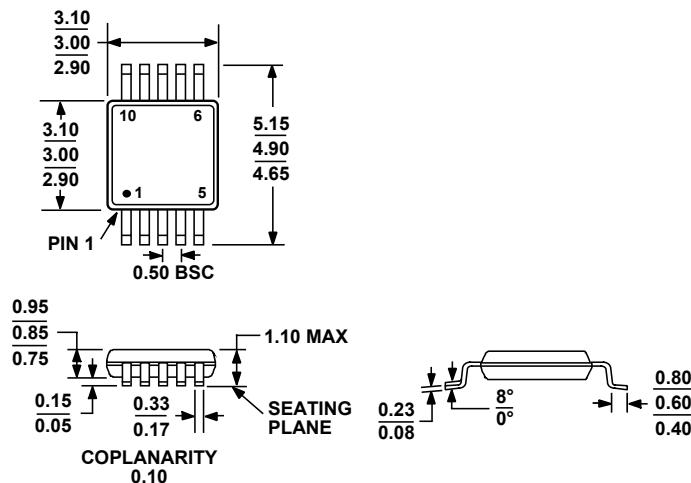


Figure 8. Timing Diagram for Latched Gain Mode

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OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-BA

Figure 9. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)

Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8253ARMZ ¹	-40°C to +85°C	10-Lead MSOP	RM-10	YOK
AD8253ARMZ-RL ¹	-40°C to +85°C	10-Lead MSOP	RM-10	YOK
AD8253ARMZ-R7 ¹	-40°C to +85°C	10-Lead MSOP	RM-10	YOK
AD8253-EVALZ ¹		Evaluation Board		

¹ Z = RoHS compliant part.

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AD8253 10 MHz, 20 V/s, G = 1, 10, 100, 1000 iCMOS® Programmable Gain Instrumentation Amplifier

Data Sheets

- [Rev PrA, 09/2007 \(pdf, 690K\)](#)
- [Lead\(Pb\) - Free Data](#)

[Email PDF](#)[\(Data Sheet Help\)](#)**Application Notes**

pdf(192k)

Evaluation Boards**Price, Packaging, and Availability****Product Description**

The AD8253 is an instrumentation amplifier with digitally programmable gains that has $G\Omega$ input impedance, low output noise, and low distortion making it suitable for interfacing with sensors and...[More](#)

This part is not yet released to manufacturing. For more information and samples please contact the [Amplifiers and Comparators Group](#).

Specifications

Single/Dual Supply	Dual
Gain Setting Method	Pin, Software
Gain Range (min to max)	1000
Bandwidth G=10 (kHz typ)	8000kHz
CMRR (dB)	100dB
Vnoise RTI 1-10 Hz μ Vp-p	1 μ V p-p
Temperature Range	-40 to +85
Supply Current (max)	4.5mA

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Features

- Small package: 10-lead MSOP
- Programmable gains: 1, 10, 100, 1000
- Digital or pin-programmable gain setting
- Wide supply: ± 5 V to ± 15 V
- Excellent dc performance
 - High CMRR 120 dB, G = 100
 - Low gain drift: 10 ppm/ $^{\circ}$ C
 - Low offset drift: 1.2 \bullet V/ $^{\circ}$ C, G = 1000
- Excellent ac performance
 - Fast settling time: 615 ns to 0.001%
 - High slew rate: 20 V/ μ s
 - Low distortion:
 - High CMRR over frequency: 80 dB to 50 kHz
 - Low noise: 8 nV/ \sqrt Hz, G = 1000
 - Low power: 4 mA

Price, Packaging, and Availability

 Print Table

AD8253 Model Options

Model	Status	Package	Pins	Temp Range	Price* (1000 pcs.)	Available	RoHS Compliant	Samples Cart	Purchase Cart
AD8253-EVALZ	Pre-Release	EVALUATION BOARDS	-	Ind	-	-	Y	Contact ADI	Contact ADI
AD8253ARMZ	Pre-Release	10 ld MSOP	10	Ind	-	-	Y Material Declaration	Contact ADI	Contact ADI
AD8253ARMZ-R7	Pre-Release	10 ld MSOP	10	Ind	-	-	Y Material Declaration	Contact ADI	Contact ADI
AD8253ARMZ-RL	Pre-Release	10 ld MSOP	10	Ind	-	-	Y Material Declaration	Contact ADI	Contact ADI

The USA list pricing shown is for BUDGETARY USE ONLY, shown in United States dollars (FOB USA per unit for the stated volume), and is subject to change. International prices may differ due to local duties, taxes, fees and exchange rates. For volume-specific price or delivery quotes, please contact your local Analog Devices, Inc. sales office or authorized distributor. Pricing displayed for Evaluation Boards and Kits is based on 1-piece pricing.

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Part#	Description	Single/Dual Supply	Vcc-Vee	Gain Setting Method	Bandwidth G=10 (kHz typ)	Gain min.	Gain max.	Min CMRR @ 60 Hz Min Gain	Min CMRR @ 60Hz Max Gain	Vnoise RTI 1-10 Hz μ Vp-p	Price* (1000 pcs.)
AD8214	High CMV Threshold Detec	Single	5V to 65V	Resistor	-	1	100	80dB	80dB	2.2	\$0.75
AD522	Diff Amp	Dual	10V to 36V	Resistor	3	1	1,000	75dB	100dB	4	**
AD8215	High CMV Shunt Mon	Single	4.5V to 5.5V	fixed	450	20	20	100dB	100dB	7	\$1.20
AD526	Software Programmable	Dual	9V to 33V	Software	350	1	16	-	-	3	\$6.31
AD8216	High BW 65 V Diff Amp	Single	4.5V to 5.5V	fixed	3000	3	3	80dB	80dB	20	\$1.60
AD621	Precision IA	Dual	4.6V to 18V	Pin	800	10	100	93dB	110dB	0.28	\$4.04
AD8220	R-R JFET IA	Single/Dual	4.6V to 36V	Resistor	800	1	1,000	78dB	94dB	0.8	\$2.29
AD623	S.S R-R IA	Single/Dual	2.7V to 12V	Resistor	100	1	1,000	70dB	105dB	2	\$1.38
AD8221	High Performance IA	Dual	4.6V to 36V	Resistor	562	1	1,000	80dB	130dB	0.25	\$1.99
AD625	Programmable Gain IA	Dual	12V to 36V	Resistor	400	1	10,000	70dB	110dB	0.3	\$8.68
AD8222	Dual High Performance IA	Dual	-	Resistor	750	1	10,000	80dB	130dB	0.25	\$3.59
AD627	Micropower IA	Single/Dual	2.2V to 36V	Resistor	30	5	1,000	77dB	77dB	1.2	\$2.53

AD8223	S.S R-R IA	Single/Dual	3V to 25V	Resistor	200	5	1,000	70dB	105dB	2	**
AD629	High CMV DA	Dual	5V to 36V	fixed	500	-	-	77dB	77dB	15	\$2.81
AD8224	Dual JFET R-R IA	Single/Dual	4.6V to 36V	Resistor	800	1	1,000	78dB	94dB	0.8	\$4.12
AD8202	High CMV DA	Single	3.5V to 12V	fixed	50	-	-	82dB	82dB	10	\$1.49
AD8225	Fixed G=5 IA	Dual	3.4V to 36V	fixed	900	-	-	86dB	86dB	1.5	\$3.25
AD8205	S.S Diff Amp	Single	4.5V to 5.5V	fixed	50	-	-	78dB	78dB	20	\$1.49
AD8230	Zero Drift IA	Single/Dual	8V to 16V	Resistor	2	2	1,000	-	110dB	3	\$2.95
AD8210	Bi-Directional Shunt Mon	Single	4.5V to 5.5V	fixed	500	20	20	100dB	100dB	7	\$1.79
AD8231	Zero Drift Software Prog	Single	3V to 6V	Pin; Software	700	1	128	80dB	110dB	0.7	\$1.69
AD8212	High CMV Shunt Mon	Single	7V to 65V	Resistor	1000	1	1,000	100dB	100dB	1.1	\$0.92
AD8250	Software Programmable	Dual	10V to 34V	Pin; Software	3000	1	10	80dB	98dB	1	\$4.95
AD524	Precision IA	Dual	12V to 36V	Pin	400	1	1,000	70dB	110dB	0.3	\$9.41
AD8251	Software Programmable	Dual	10V to 34V	Pin; Software	2500	1	8	80dB	98dB	1.2	\$4.95
AD622	Low Cost IA	Dual	5.2V to 36V	Resistor	800	1	1,000	66dB	103dB	0.3	\$2.48
AD8253	Software Programmable	Dual	10V to 34V	Pin; Software	8000	1	1,000	80dB	120dB	1	**

AD626	Diff Amp	Single/Dual	2.4V to 12V	Pin	100	10	100	55dB	55dB	2	\$3.66
AD8270	Dual Diff Amp	Dual	5V to 36V	Pin	10000	0.5	2	70dB	80dB	1	\$1.89
AD8129	Low Cost Diff Amp	Single/Dual	4.5V to 25V	Resistor	200000	10	-	94dB	-	-	\$1.55
AD8273	Dual Audio Diff Amp	Dual	5V to 36V	Pin	20000	0.5	2	77dB	-	2	\$1.65
AD8206	S.S Diff Amp	Single	4.5V to 5.5V	fixed	100	-	-	76dB	76dB	20	\$1.35
AD8290	Sensor Amp	-	2.6V to 5.5V	fixed	-	50	50	-	-	0.75	\$1.50
AD8213	Dual High CMV Shunt Mon	Single	4.5V to 5.5V	fixed	500	20	20	100dB	100dB	7	\$1.99
AD8553	Zero Drift IA	Single	1.8V to 5.5V	Resistor	1	0.1	10,000	80dB	120dB	0.7	\$1.30
AD624	Precision IA	Dual	12V to 36V	Pin	400	1	1,000	70dB	110dB	0.3	\$11.79
AD8203	High CMV DA	Single	4.5V to 5.5V	fixed	60	-	-	82dB	82dB	10	\$1.35
AD8211	High CMV Shunt Mon	Single	4.5V to 5.5V	fixed	500	20	20	100dB	100dB	7	\$0.80
AD620	General Purpose IA	Dual	4.6V to 36V	Resistor	800	1	10,000	73dB	110dB	0.28	\$3.14
AD628	High CMV DA	Single/Dual	4.5V to 36V	Pin; Resistor	600	0.1	100	75dB	75dB	15	\$1.76
AD8555	Sensor Amp	Single	5.5V to 2.7V	Software	n/a	70	1,280	80dB	96dB	0.5	\$3.08

AD8556	Sen/Filter Amp	Single	2.7V to 5.5V	Software	n/a	70	1,280	80dB	94dB	0.5	\$2.85
AD8557	Sensor Amp	Single	2.7V to 5.5V	Software	-	28	1,300	75dB	86dB	-	\$2.10
AMP03	Precision Diff Amp	Dual	12V to 36V	fixed	3000	-	-	85dB	85dB	2	\$2.78

* The pricing listed here is provided only for budgetary purposes as recommended list price in U.S. Dollars in the United States ex factor per unit for the stated volume. Pricing displayed for Evaluation Boards and Kits is based on 1-piece pricing.

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