

(NPN) TIP41, TIP41A, TIP41B, TIP41C (PNP) TIP42, TIP42A, TIP42B, TIP42C



ON Semiconductor®

<http://onsemi.com>

Complementary Silicon Plastic Power Transistors

... designed for use in general purpose amplifier and switching applications.

- ESD Ratings: Machine Model, C; > 400 V
Human Body Model, 3B; > 8000 V
- Epoxy Meets UL 94, V-0 @ 1/8"
- Pb-Free Package is Available*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage TIP41, TIP42 TIP41A, TIP42A TIP41B, TIP42B TIP41C, TIP42C	V_{CEO}	40 60 80 100	Vdc
Collector-Base Voltage TIP41, TIP42 TIP41A, TIP42A TIP41B, TIP42B TIP41C, TIP42C	V_{CB}	40 60 80 100	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current— Continuous Peak	I_C	6.0 10	Adc
Base Current	I_B	2.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	65 0.52	Watts W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	2.0 0.016	Watts W/ $^\circ\text{C}$
Unclamped Inductive Load Energy (Note 1)	E	62.5	mJ
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

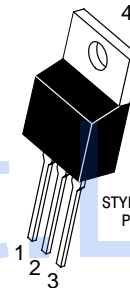
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	57	$^\circ\text{C}/\text{W}$

1. $I_C = 2.5 \text{ A}$, $L = 20 \text{ mH}$, $\text{P.R.F.} = 10 \text{ Hz}$, $V_{CC} = 10 \text{ V}$, $R_{BE} = 100 \Omega$.

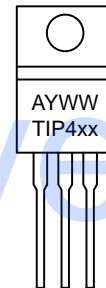
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

6 A COMPLEMENTARY SILICON POWER TRANSISTORS 40 – 60 – 80 – 100 V, 65 W

MARKING DIAGRAM



STYLE 1:
PIN 1: BASE
2: COLLECTOR
3: EMITTER
4: COLLECTOR



TO-220AB
CASE 221A-09
STYLE 1

xx = Specific Device Code:
1, 2, 1A, 1B, 1C, 2A, 2B, 2C
A = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
TIP41	TO-220AB	50 Units / Rail
TIP41A	TO-220AB	50 Units / Rail
TIP41B	TO-220AB	50 Units / Rail
TIP41C	TO-220AB	50 Units / Rail
TIP41CG	TO-220AB (Pb-Free)	50 Units / Rail
TIP42	TO-220AB	50 Units / Rail
TIP42A	TO-220AB	50 Units / Rail
TIP42B	TO-220AB	50 Units / Rail
TIP42C	TO-220AB	50 Units / Rail
TIP42CG	TO-220AB (Pb-Free)	50 Units / Rail

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ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (Note 2) ($I_C = 30\text{ mAdc}$, $I_B = 0$)	TIP41, TIP42 TIP41A, TIP42A TIP41B, TIP42B TIP41C, TIP42C	$V_{CEO(sus)}$	40 60 80 100	– – – – Vdc
Collector Cutoff Current ($V_{CE} = 30\text{ Vdc}$, $I_B = 0$) ($V_{CE} = 60\text{ Vdc}$, $I_B = 0$)	TIP41, TIP41A, TIP42, TIP42A TIP41B, TIP41C, TIP42B, TIP42C	I_{CEO}	– –	0.7 0.7 mAdc
Collector Cutoff Current ($V_{CE} = 40\text{ Vdc}$, $V_{EB} = 0$) ($V_{CE} = 60\text{ Vdc}$, $V_{EB} = 0$) ($V_{CE} = 80\text{ Vdc}$, $V_{EB} = 0$) ($V_{CE} = 100\text{ Vdc}$, $V_{EB} = 0$)	TIP41, TIP42 TIP41A, TIP42A TIP41B, TIP42B TIP41C, TIP42C	I_{CES}	– – – –	400 400 400 400 μAdc
Emitter Cutoff Current ($V_{BE} = 5.0\text{ Vdc}$, $I_C = 0$)		I_{EBO}	–	1.0 mAdc
ON CHARACTERISTICS (Note 2)				
DC Current Gain ($I_C = 0.3\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$) ($I_C = 3.0\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$)		h_{FE}	30 15	– 75 –
Collector–Emitter Saturation Voltage ($I_C = 6.0\text{ Adc}$, $I_B = 600\text{ mAdc}$)		$V_{CE(sat)}$	–	1.5 Vdc
Base–Emitter On Voltage ($I_C = 6.0\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$)		$V_{BE(on)}$	–	2.0 Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain — Bandwidth Product ($I_C = 500\text{ mAdc}$, $V_{CE} = 10\text{ Vdc}$, $f_{test} = 1.0\text{ MHz}$)		f_T	3.0	– MHz
Small–Signal Current Gain ($I_C = 0.5\text{ Adc}$, $V_{CE} = 10\text{ Vdc}$, $f = 1.0\text{ kHz}$)		h_{fe}	20	– –

2. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

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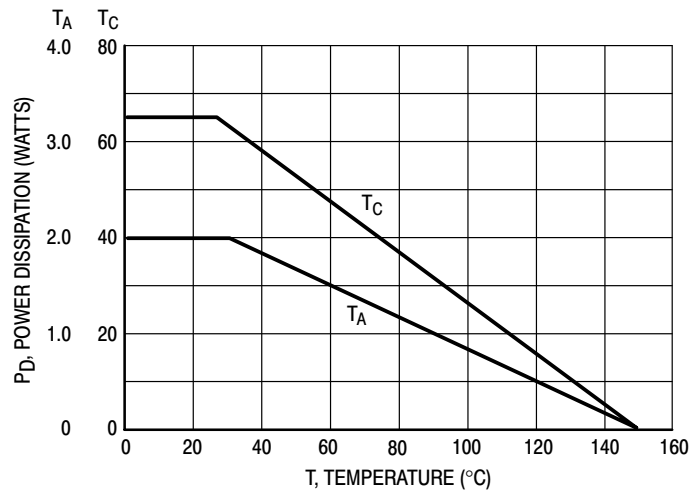


Figure 1. Power Derating

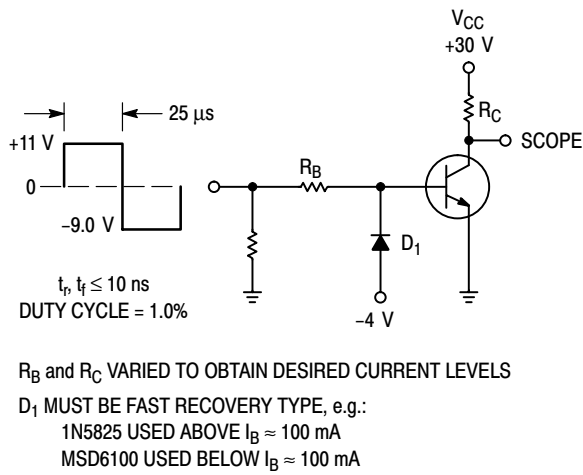


Figure 2. Switching Time Test Circuit

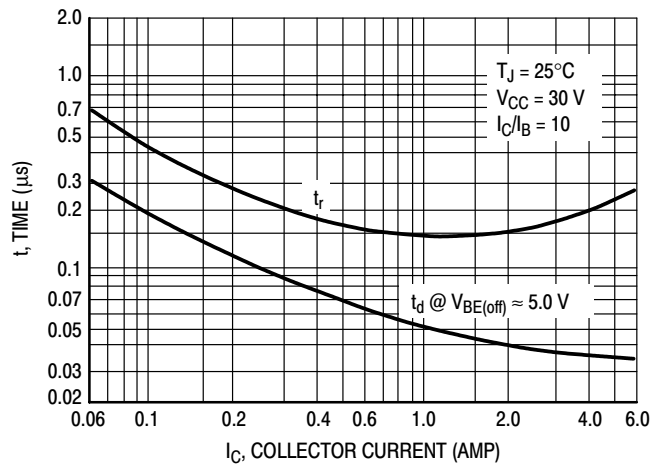


Figure 3. Turn-On Time

(NPN) TIP41, TIP41A, TIP41B, TIP41C (PNP) TIP42, TIP42A, TIP42B, TIP42C

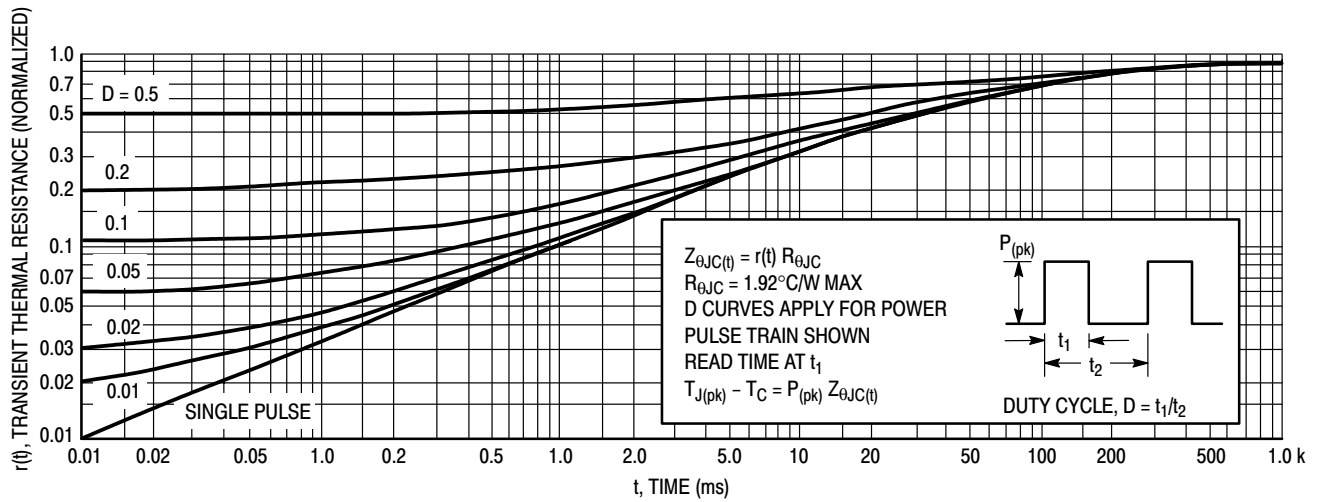


Figure 4. Thermal Response

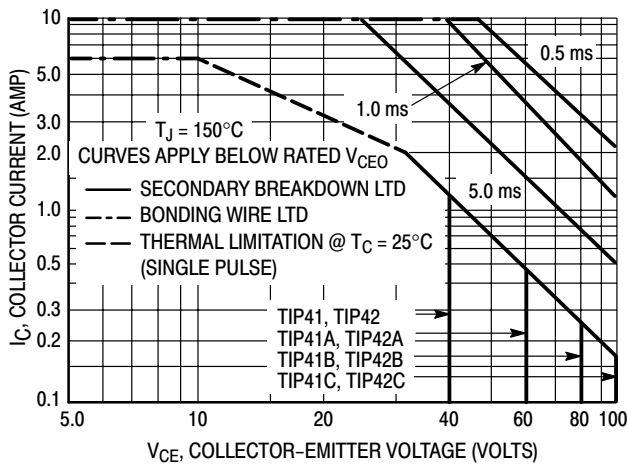


Figure 5. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

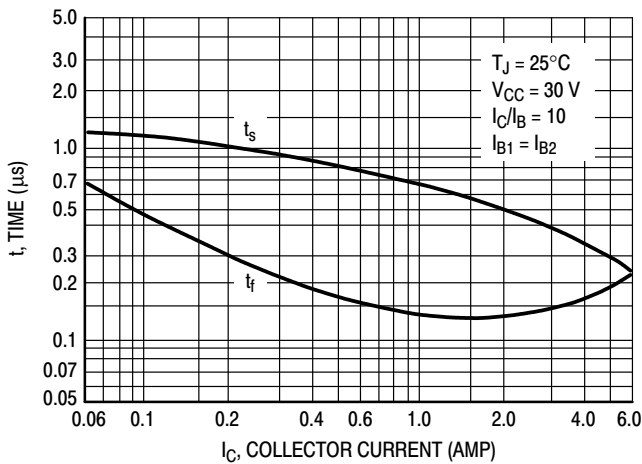


Figure 6. Turn-Off Time

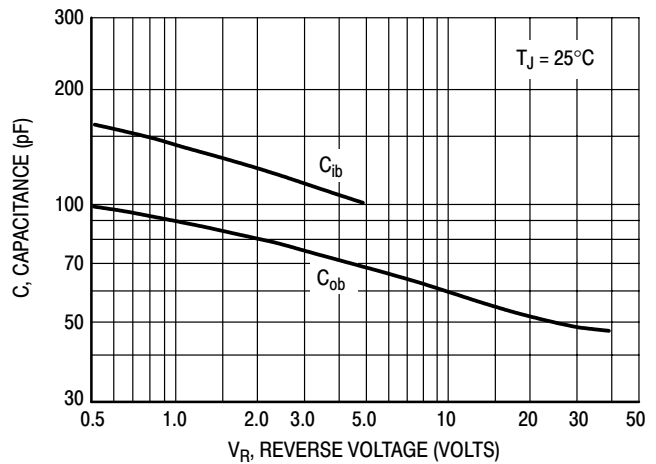


Figure 7. Capacitance

(NPN) TIP41, TIP41A, TIP41B, TIP41C (PNP) TIP42, TIP42A, TIP42B, TIP42C

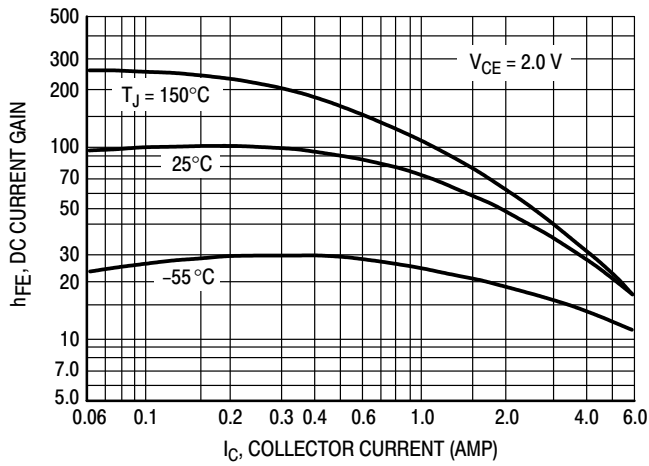


Figure 8. DC Current Gain

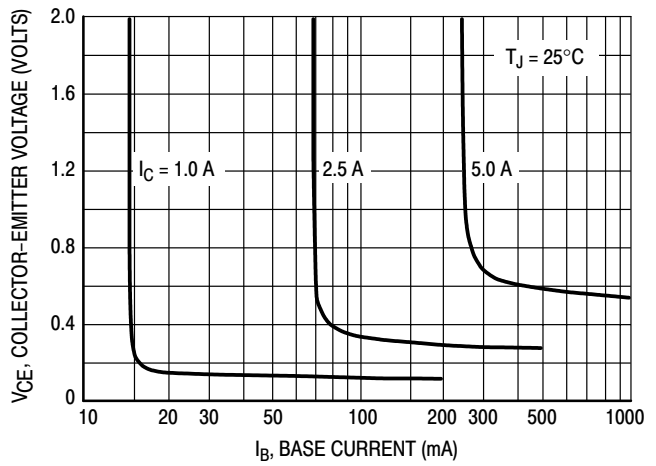


Figure 9. Collector Saturation Region

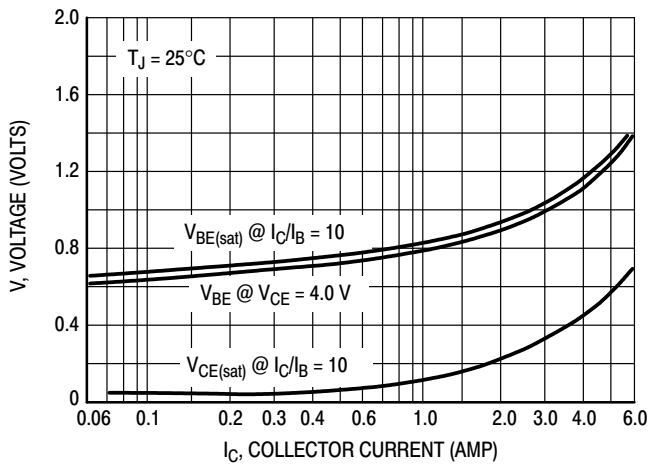


Figure 10. "On" Voltages

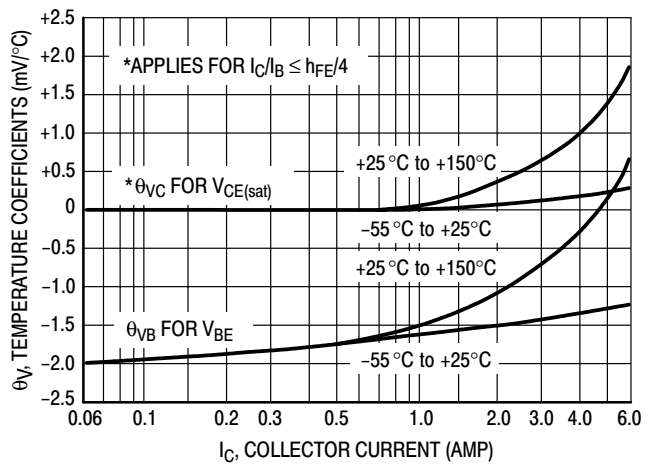


Figure 11. Temperature Coefficients

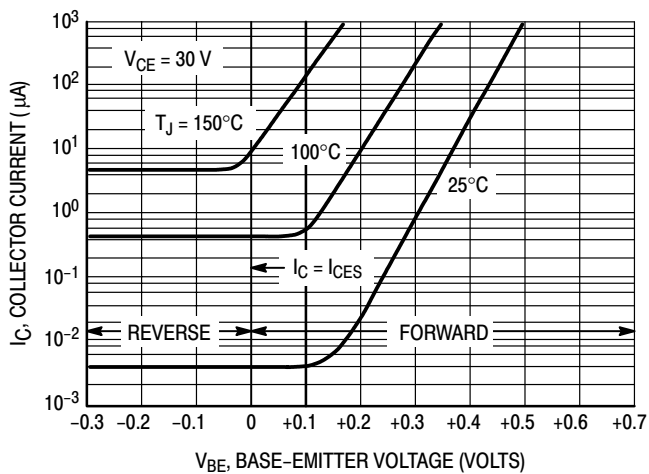


Figure 12. Collector Cut-Off Region

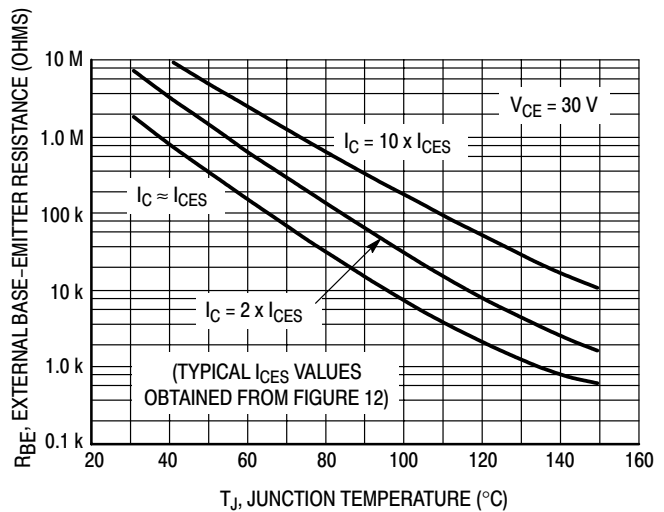
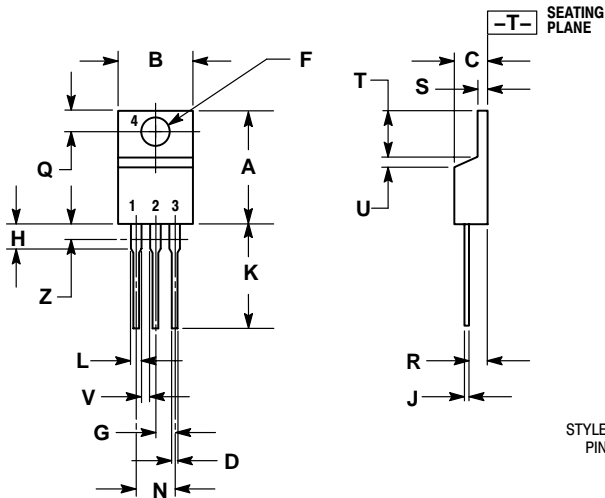


Figure 13. Effects of Base-Emitter Resistance

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PACKAGE DIMENSIONS


TO-220AB
CASE 221A-09
ISSUE AA



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

- STYLE 1:
1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

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