

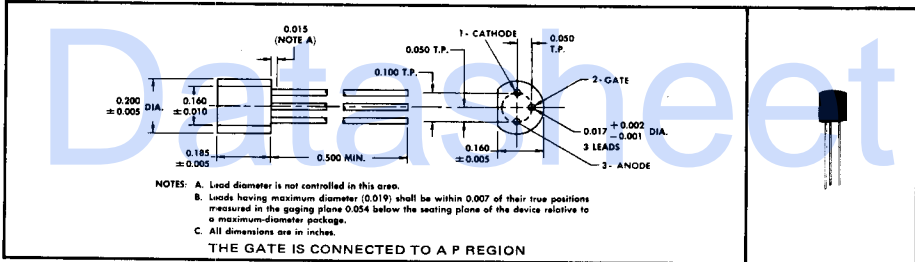
TYPES TIC44, TIC45, TIC46, TIC47 P-N-P-N PLANAR SILICON REVERSE-BLOCKING TRIODE THYRISTORS

SILECT† THYRISTORS‡
600 mA DC • 30 thru 200 VOLTS

Rugged, One-Piece Construction with Standard TO-18 100-mil Pin-Circle Configuration

mechanical data

These thyristors are encapsulated in a plastic compound specifically designed for this purpose, using a highly mechanized process developed by Texas Instruments. The case will withstand soldering temperatures without deformation. These devices exhibit stable characteristics under high-humidity conditions and are capable of meeting MIL-STD-202C method 106B. The thyristors are insensitive to light.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	TIC44	TIC45	TIC46	TIC47	UNIT
Static Off-State Voltage, V_D (See Note 1)	30	60	100	200	V
Repetitive Peak Off-State Voltage, V_{DRM} (See Note 1)	30	60	100	200	V
Static Reverse Voltage, V_R (See Note 1)	30	60	100	200	V
Repetitive Peak Reverse Voltage, V_{RRM} (See Note 1)	30	60	100	200	V
Continuous or RMS On-State Current at (or below) 55°C Case Temperature (See Note 2)	600				mA
Continuous or RMS On-State Current at (or below) 25°C Free-Air Temperature (See Note 3)	300				mA
Average On-State Current (180° Conduction Angle) at (or below) 55°C Case Temperature (See Note 4)	430				mA
Surge On-State Current (See Note 5)	6				A
Peak Negative Gate Voltage	8				V
Peak Positive Gate Current (Pulse Width ≤ 300 μs)	1				A
Peak Gate Power Dissipation (Pulse Width ≤ 300 μs)	4				W
Operating Free-Air Temperature Range	-55 to 125				°C
Storage Temperature Range	-55 to 150				°C
Lead Temperature 1/16 Inch from Case for 10 Seconds	260				°C

- NOTES: 1. These values apply when the gate-cathode resistance $R_{GK} \leq 1 \text{ k}\Omega$.
2. These values apply for continuous d-c operation with resistive load. Above 55°C derate according to Figure 5.
3. These values apply for continuous d-c operation with resistive load. Above 25°C derate according to Figure 6.
4. This value may be applied continuously under single-phase, 60-Hz, half-sine-wave operation with resistive load. Above 55°C derate according to Figure 5.
5. This value applies for one 60-Hz half sine wave when the device is operating at (or below) rated values of peak reverse voltage and on-state current. Surge may be repeated after the device has returned to original thermal equilibrium.

†Trademark of Texas Instruments

‡U. S. Patent No. 3,439,238

TYPES TIC44, TIC45, TIC46, TIC47

P-N-P-N PLANAR SILICON REVERSE-BLOCKING TRIODE THYRISTORS

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_D Static Off-State Current	$V_D = \text{Rated } V_D, R_{GK} = 1 \text{ k}\Omega, T_A = 125^\circ\text{C}$		50	μA
I_R Static Reverse Current	$V_R = \text{Rated } V_R, R_{GK} = 1 \text{ k}\Omega, T_A = 125^\circ\text{C}$		50	μA
I_{GT} Gate Trigger Current (See Note 6)	$V_{AA} = 6 \text{ V}, R_L = 100 \Omega, t_{p(g)} \geq 20 \mu\text{s}$		200	μA
V_{GT} Gate Trigger Voltage (See Note 6)	$V_{AA} = 6 \text{ V}, R_L = 100 \Omega, t_{p(g)} \geq 20 \mu\text{s}$		0.8	V
	$V_{AA} = 6 \text{ V}, R_L = 100 \Omega, t_{p(g)} \geq 20 \mu\text{s}, T_A = 125^\circ\text{C}$	0.2		
I_H Holding Current	$R_L = 100 \Omega, R_{GK} = 1 \text{ k}\Omega$		5	mA
V_T On-State Voltage	$I_T = 300 \text{ mA}, R_{GK} \geq 1 \text{ k}\Omega, \text{ See Note 7}$		1.4	V

NOTES: 6. When measuring these parameters, a 1-k Ω resistor should be used between gate and cathode to prevent triggering by random noise.

7. This parameter is measured using pulse techniques. $t_w = 1 \text{ ms}$, duty cycle $\leq 1\%$.

switching characteristics at 25°C free-air temperature

PARAMETER	TEST CONDITIONS	TYP	UNIT
t_{gt} Gate-Controlled Turn-On Time	$V_{AA} = 30 \text{ V}, R_L = 50 \Omega, R_G = 20 \text{ k}\Omega, V_{in} = 20 \text{ V}, \text{ See Figure 1}$	3.5	μs
t_q Circuit-Commutated Turn-Off Time	$V_{AA} = 30 \text{ V}, R_L = 50 \Omega, I_{RM} = 1 \text{ A}, \text{ See Figure 2}$	6.8	μs

thermal characteristics

PARAMETER	MAX	UNIT
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	75	$^\circ\text{C/W}$
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	275	

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PARAMETER MEASUREMENT INFORMATION

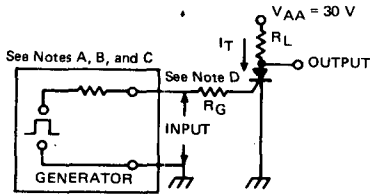
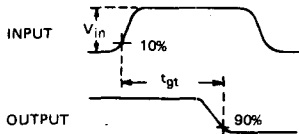


FIGURE 1—TURN-ON TIME

- NOTES:
- A. V_{in} is measured with gate and cathode terminals connected as shown and anode terminal open.
 - B. The input waveform of Figure 1 has the following characteristics: $t_r < 40$ ns, $t_w \geq 20$ μ s.
 - C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r < 14$ ns, $R_{in} \geq 10$ M Ω , $C_{in} < 12$ pF.
 - D. R_G includes the total resistance of the generator and the external resistor.

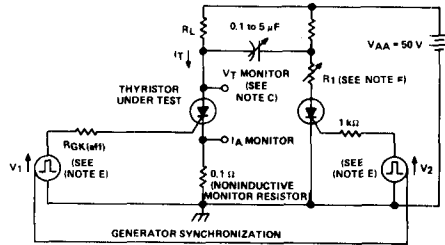
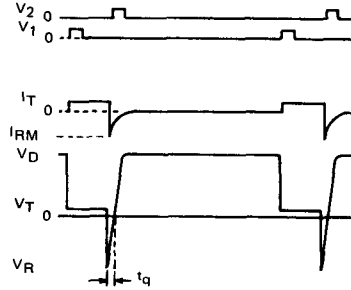


FIGURE 2—COMMUTATING TURN-OFF TIME

- NOTES:
- E. Pulse generators for V_1 and V_2 are synchronized to provide an anode current waveform with the following characteristics: $t_w = 50$ to 300 μ s, duty cycle = 1%. The pulse widths of V_1 and V_2 are ≥ 10 μ s.
 - F. Resistor R_1 is adjusted for $I_{RM} = 1$ A.

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THERMAL INFORMATION

The minimum heat-sink requirements may be calculated for any on-state current, heat-sink combination by the following procedure:

1. Determine worst-case power dissipation from Figure 3.
2. Calculate maximum allowable case-to-free-air thermal resistance by use of the equation.

$$R_{\theta CA} = \frac{T_J - T_A}{P_{A(av)}} - R_{\theta JC}$$

where: T_J = Junction temperature

T_A = Free-air temperature

$P_{A(av)}$ = Average anode power dissipation (see Figure 3 for worst-case values)

$R_{\theta JC}$ = Junction-to-case thermal resistance = 75°C/W maximum.

3. Determine area of heat sink from Figure 4.

EXAMPLE

Determine: Minimum size of 1/16"-thick aluminum heat sink for safe operation of thyristor at an average current of 0.4 A with a conduction angle of 180°

Given: Maximum $T_J = 125^\circ\text{C}$

$T_A = 35^\circ\text{C}$

$R_{\theta JC} = 75^\circ\text{C/W}$

Solution: From Figure 3, $P_{A(av)} = 0.84\text{ W}$ for 0.4 A with 180° conduction angle. Using the equation of step 2 above:

$$R_{\theta CA} = \frac{125^\circ\text{C} - 35^\circ\text{C}}{0.84\text{ W}} - 75^\circ\text{C/W} = 32^\circ\text{C/W}$$

Figure 4 shows that for $R_{\theta CA}$ of 32°C/W, the area is 18 sq. in. The minimum dimensions of the sides should be:

$$\sqrt{\frac{\text{area}}{2}} \times \sqrt{\frac{\text{area}}{2}} = \sqrt{\frac{18}{2}} \times \sqrt{\frac{18}{2}} = 3'' \times 3''$$

- NOTES: 8. The thyristor is mounted in the center of a square heat sink vertically positioned in still free air with both sides exposed. The heat-sink area is twice the area of one side.
9. $R_{\theta CA}$ includes the case to heat sink thermal resistance, $R_{\theta CHS}$, in addition to the heat-sink-to-free-air thermal resistance, $R_{\theta HSA}$, and is defined by the equation, $R_{\theta CA} = R_{\theta CHS} + R_{\theta HSA}$.

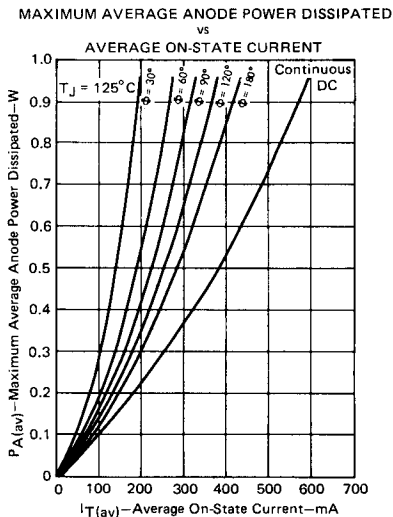


FIGURE 3

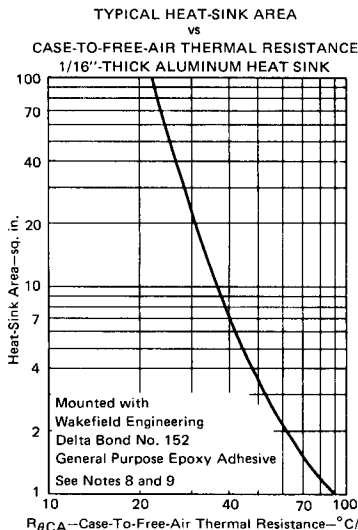


FIGURE 4

TYPES TIC44, TIC45, TIC46, TIC47 P-N-P-N PLANAR SILICON REVERSE-BLOCKING TRIODE THYRISTORS

THERMAL INFORMATION

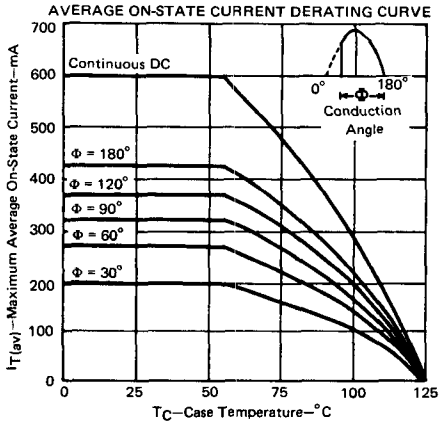


FIGURE 5

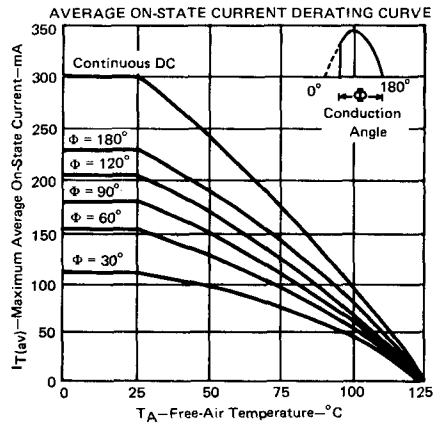


FIGURE 6

TYPICAL CHARACTERISTICS

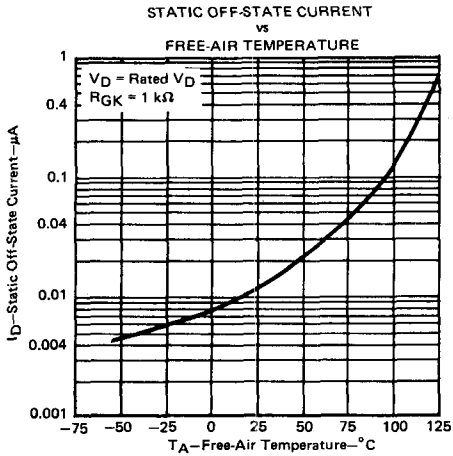


FIGURE 7

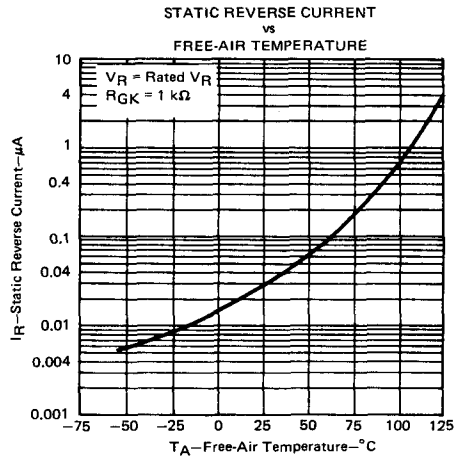


FIGURE 8

TYPES TIC44, TIC45, TIC46, TIC47

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TYPICAL CHARACTERISTICS

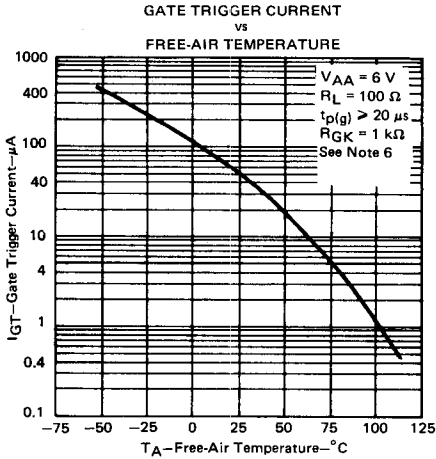


FIGURE 9

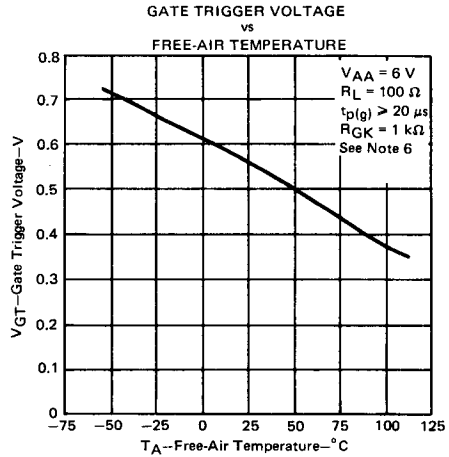


FIGURE 10

NOTE 6: When measuring these parameters, a 1-k Ω resistor should be used between gate and cathode to prevent triggering by random noise.

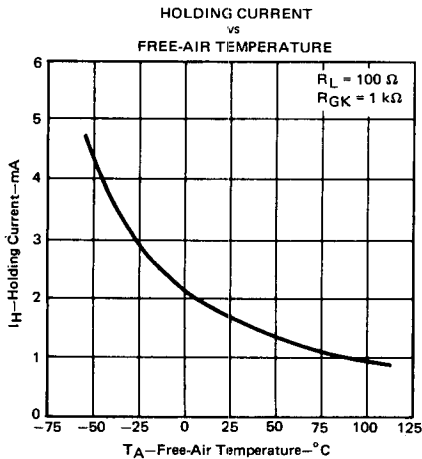


FIGURE 11

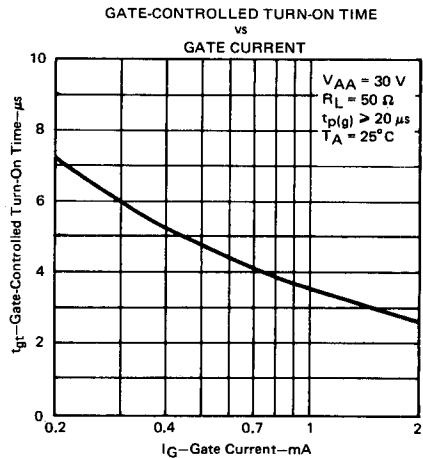


FIGURE 12

THYRISTOREN

THYRISTORS

Typ type	I _T A	V _{DRM} V	I _{TSM} A	I _{GT} max mA
2N 3001	0,35	30	6	0,02
2N 3002	0,35	60	6	0,02
2N 3003	0,35	100	6	0,02
2N 3004	0,35	200	6	0,02
2N 3005	0,35	30	6	0,2
2N 3006	0,35	60	6	0,2
2N 3007	0,35	100	6	0,2
2N 3008	0,35	200	6	0,2
TIC 44	0,6	30	6	0,2
TIC 45	0,6	60	6	0,2
TIC 46	0,6	100	6	0,2
TIC 47	0,6	200	6	0,2
TIC 60	0,8	30	6	0,2
TIC 61	0,8	60	6	0,2
TIC 62	0,8	100	6	0,2
TIC 63	0,8	150	6	0,2
TIC 64	0,8	200	6	0,2
2N 5060	0,8	30	6	0,2
2N 5061	0,8	60	6	0,2
2N 5062	0,8	100	6	0,2
2N 5063	0,8	150	6	0,2
2N 5064	0,8	200	6	0,2
2N 1595	1	50	15	10
2N 1596	1	100	15	10
2N 1597	1	200	15	10
2N 1598	1	300	15	10
2N 1599	1	400	15	10
TI 145 AO	1,6	50	30	25
TI 145 A1	1,6	100	30	25
TI 145 A2	1,6	200	30	25
TI 145 A3	1,6	300	30	25
TI 145 A4	1,6	400	30	25
TIC 39 Y	2	30	20	0,2
TIC 39 F	2	50	20	0,2
TIC 39 A	2	100	20	0,2
TIC 39 B	2	200	20	0,2
TIC 39 C	2	300	20	0,2
TIC 39 D	2	400	20	0,2
TIC 106 Y	5	30	30	0,2
TIC 106 F	5	50	30	0,2
TIC 106 A	5	100	30	0,2
TIC 106 B	5	200	30	0,2
TIC 106 C	5	300	30	0,2
TIC 106 D	5	400	30	0,2
TIC 116	Siehe Datenblatt Seite 2-155; See Data Sheet Page 2-155			
TIC 126	Siehe Datenblatt Seite 2-155; See Data Sheet Page 2-155			
TIC 236	Siehe Datenblatt Seite 2-165; See Data Sheet Page 2-165			
TIC 246	Siehe Datenblatt Seite 2-165; See Data Sheet Page 2-165			
TIC 253	Siehe Datenblatt Seite 2-167; See Data Sheet Page 2-167			
TIC 263	Siehe Datenblatt Seite 2-167; See Data Sheet Page 2-167			

V _{GT} max V	I _H max mA	V _T max @ V	Gehäuse package
0,7	3	1,2	TO-18
0,7	3	1,2	TO-18
0,7	3	1,2	TO-18
0,7	3	1,2	TO-18
0,8	5	1,2	TO-18
0,8	5	1,2	TO-18
0,8	5	1,2	TO-18
0,8	5	1,2	TO-18
0,8	5	1,4	Silect
0,8	5	1,4	Silect
0,8	5	1,4	Silect
0,8	5	1,4	Silect
0,8	5	1,7	TO-92
0,8	5	1,7	TO-92
0,8	5	1,7	TO-92
0,8	5	1,7	TO-92
0,8	5	1,7	TO-92
0,8	5	1,7	TO-92
0,8	5	1,7	TO-92
0,8	5	1,7	TO-92
0,8	5	1,7	TO-92
3	25	2	TO-5
3	25	2	TO-5
3	25	2	TO-5
3	25	2	TO-5
3	25	2	TO-5
3,5	25	2	TO-5
3,5	25	2	TO-5
3,5	25	2	TO-5
3,5	25	2	TO-5
3,5	25	2	TO-5
1	5	1,75	TO-39
1	5	1,75	TO-39
1	5	1,75	TO-39
1	5	1,75	TO-39
1	5	1,75	TO-39
1	5	1,75	TO-39
1	5	1,7	TO-66P
1	5	1,7	TO-66P
1	5	1,7	TO-66P
1	5	1,7	TO-66P
1	5	1,7	TO-66P
1	5	1,7	TO-66P