ATWILC1000A-MUT

IEEE 802.11 b/g/n Link Controller SoC

Datasheet

Description

ATWILC1000A is a single chip IEEE® 802.11 b/g/n Radio/Baseband/MAC link controller optimized for low-power mobile applications. ATWILC1000A supports single stream 1x1 802.11n mode providing up to 72Mbps PHY rate. The ATWILC1000A features fully integrated Power Amplifier, LNA, Switch, and Power Management. Implemented in 65nm CMOS technology, the ATWILC1000A offers very low power consumption while simultaneously providing high performance and minimal bill of materials.

The ATWILC1000A supports two and three Bluetooth coexistence protocols. The ATWILC1000A provides multiple peripheral interfaces including UART, SPI, I^2C, and SDIO. The only external clock source needed for the ATWILC1000A is a high-speed crystal or oscillator with a wide range of reference clock frequencies supported (12-40MHz). The ATWILC1000A is available in both QFN and Wafer Level Chip Scale Package (WLCSP) packaging.

Datasheet.Live

Features

- IEEE 802.1 b/g/n 20MHz (1x1) solution
- Single spatial stream in 2.4GHz ISM band
- Integrated PA and T/R Switch
- Superior Sensitivity and Range via advanced PHY signal processing
- Advanced Equalization and Channel Estimation
- Advanced Carrier and Timing Synchronization
- Wi-Fi Direct and Soft-AP support
- Supports IEEE 802.11 WEP, WPA, WPA2 Security
- Supports China WAPI security
- Superior MAC throughput via hardware accelerated two-level A-MSDU/A-MPDU frame aggregation and block acknowledgement
- On-chip memory management engine to reduce host load
- SPI, SDIO, UART, and I^2C host interfaces
- 2/3 wire Bluetooth coexistence interface
- Operating temperature range of -40°C to +85°C
- Power save modes:
  - <1µA Deep Power Down mode typical @3.3V I/O
  - 280µA Doze mode with chip settings preserved (used for beacon monitoring)
  - On-chip low power sleep oscillator
  - Fast host wake-up from Doze mode by a pin or host I/O transaction

Table of Contents

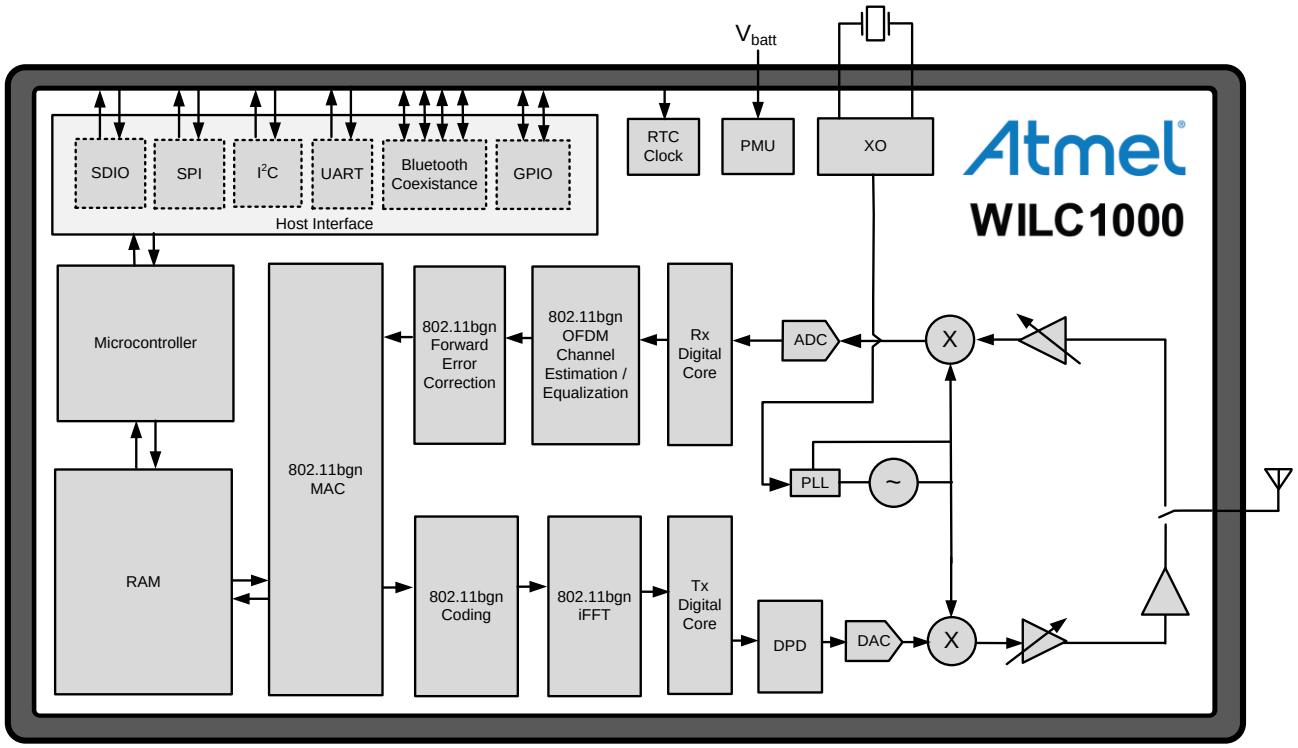
1 Ordering Information and IC Marking

Table 1-1. Ordering Details

Atmel Official Part Number (for ordering)	Package Type	IC Marking
ATWILC1000A-MU-T	5x5 QFN in Tape and Reel	ATWILC1000A

2 Block Diagram

Figure 2-1. ATWILC1000A Block Diagram



3 Pin-Out and Package Information

3.1 Pin Description

ATWILC1000A is offered in an exposed pad 40-pin QFN package. This package has an exposed paddle that must be connected to the system board ground. The QFN package pin assignment is shown in Figure 3-1. The color shading is used to indicate the pin type as follows: green – power, red – analog, blue – digital I/O, yellow – digital input, grey – unconnected or reserved. The ATWILC1000A pins are described in Table 3-1.

Figure 3-1. Pin Assignment

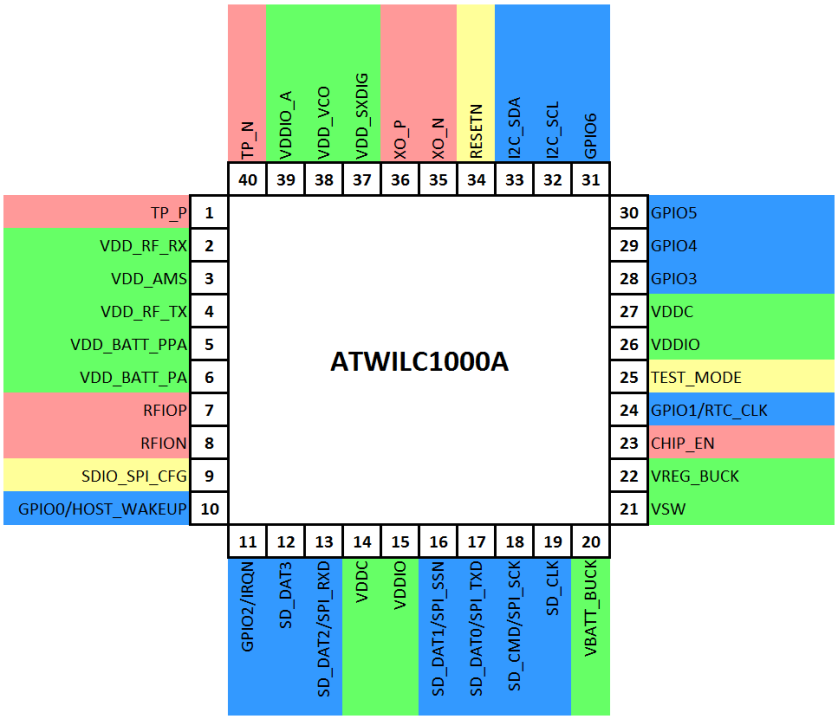


Table 3-1. Pin Description

Pin #	Pin Name	Pin Type	Description
1	TP_P	Analog	Test Pin/Customer No Connect
2	VDD_RF_RX	Power	Tuner RF Supply (see Section 9.1 and Table 9-3)
3	VDD_AMS	Power	Tuner BB Supply (see Section 9.1 and Table 9-3)
4	VDD_RF_TX	Power	Tuner RF Supply (see Section 9.1 and Table 9-3)
5	VDD_BATT_PPA	Power	PA 1st Stage Supply (see Section 9.1 and Table 9-3)
6	VDD_BATT_PA	Power	PA 2nd Stage Supply (see Section 9.1 and Table 9-3)
7	RFIOP	Analog	Pos RF Differential I/O (see Table 9-3)
8	RFION	Analog	Neg RF Differential I/O (see Table 9-3)
9	SDIO_SPI_CFG	Digital Input	Tie to 1 for SPI, 0 for SDIO
10	GPIO0/HOST_WAKE	Digital I/O, Programmable Pull-Up	GPIO0/SLEEP Mode Control
11	GPIO2/IRQN	Digital I/O, Programmable Pull-Up	GPIO2/Device Interrupt
12	SD_DAT3	Digital I/O, Programmable Pull-Up	SDIO Data3
13	SD_DAT2/SPI_RXD	Digital I/O, Programmable Pull-Up	SDIO Data2/SPI Data Rx
14	VDDC	Power	Digital Core Power Supply (see Section 9.1 and Table 9-3)
15	VDDIO	Power	Digital I/O Power Supply (see Section 9.1 and Table 9-3)
16	SD_DAT1/SPI_SSN	Digital I/O, Programmable Pull-Up	SDIO Data1/SPI Slave Select
17	SD_DAT0/SPI_TXD	Digital I/O, Programmable Pull-Up	SDIO Data0/SPI Data Tx
18	SD_CMD/SPI_SCK	Digital I/O, Programmable Pull-Up	SDIO Command/SPI Clock
19	SD_CLK	Digital I/O, Programmable Pull-Up	SDIO Clock

Pin #	Pin Name	Pin Type	Description
20	VBATT_BUCK	Power	Battery Supply for DC/DC Converter (see Section 9.1 and Table 9-3)
21	VSW	Power	Switching output of DC/DC Converter (see Section 9.1 and Table 9-3)
22	VREG_BUCK	Power	Core Power from DC/DC Converter (see Section 9.1 and Table 9-3)
23	CHIP_EN	Analog	PMU Enable
24	GPIO1/RTC_CLK	Digital I/O, Programmable Pull-Down	GPIO1/32kHz Clock Input
25	TEST_MODE	Digital Input	Test Mode – Customer Tie to GND
26	VDDIO	Power	Digital I/O Power Supply (see Section 9.1 and Table 9-3)
27	VDDC	Power	Digital Core Power Supply (see Section 9.1 and Table 9-3)
28	GPIO3	Digital I/O, Programmable Pull-Up	GPIO3/SPI_SCK_Flash
29	GPIO4	Digital I/O, Programmable Pull-Up	GPIO4/SPI_SSN_Flash
30	GPIO5	Digital I/O, Programmable Pull-Up	GPIO5/SPI_TXD_Flash
31	GPIO6	Digital I/O, Programmable Pull-Up	GPIO6/SPI_RXD_Flash
32	I2C_SCL[1]	Digital I/O, Programmable Pull-Up	I^2C Slave Clock
33	I2C_SDA[1]	Digital I/O, Programmable Pull-Up	I^2C Slave Data
34	RESETN	Digital Input	Active-Low Hard Reset
35	XO_N	Analog	Crystal Oscillator N
36	XO_P	Analog	Crystal Oscillator P
37	VDD_SXDIG	Power	SX Power Supply (see Section 9.1 and Table 9-3)
38	VDD_VCO	Power	VCO Power Supply (see Section 9.1 and Table 9-3)
39	VDDIO_A	Power	Tuner VDDIO Power Supply (see Section 9.1 and Table 9-3)
40	TPN	Analog	Test Pin/Customer No Connect
41	PADDLE VSS	Power	Connect to System Board Ground

Note: 1. All digital IO have 2mA drive strength expect for I2C_SCL/SDA which have 4mA.

3.2 Package Description

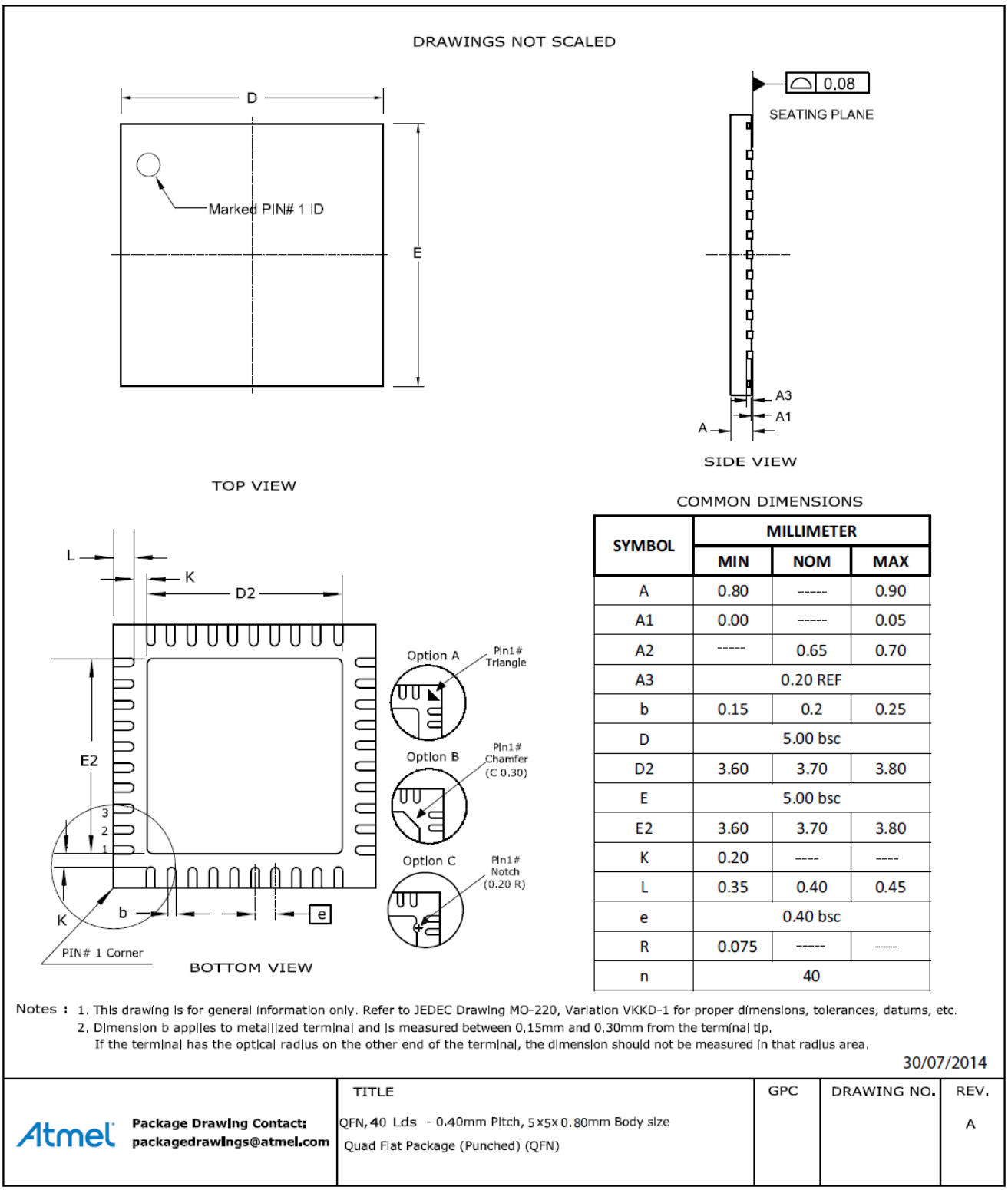
The ATWILC1000A QFN package information is provided in Table 3-2.

Table 3-2. QFN Package Information

Parameter	Value	Units	Tolerance
Package Size	5x5	mm	±0.1mm
QFN Pad Count	40		
Total Thickness	0.85	mm	±0.05mm
QFN Pad Pitch	0.40	mm	
Pad Width	0.20	mm	
Exposed Pad size	3.7x3.7	mm	

The ATWILC1000A 40L QFN package view is shown in Figure 3-2.

Figure 3-2. QFN Package



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	-----	0.90
A1	0.00	-----	0.05
A2	-----	0.65	0.70
A3		0.20 REF	
b	0.15	0.2	0.25
D		5.00 bsc	
D2	3.60	3.70	3.80
E		5.00 bsc	
E2	3.60	3.70	3.80
K	0.20	----	----
L	0.35	0.40	0.45
e		0.40 bsc	
R	0.075	-----	----
n		40	

The QFN package is a qualified Green Package.

4 Electrical Specifications

4.1 Absolute Ratings

Table 4-1. Absolute Maximum Ratings

Characteristic	Symbol	Min	Max	Unit
Core Supply Voltage	VDDC	-0.3	1.5	V
I/O Supply Voltage	VDDIO	-0.3	5.0	V
Battery Supply Voltage	VBATT	-0.3	5.0	V
Digital Input Voltage	V_{IN}	-0.3	VDDIO	V
Analog Input Voltage	V_{AIN}	-0.3	1.5	V
ESD Human Body Model	V_{ESDHBM}	-1000, -2000 (see notes below)	+1000, +2000 (see notes below)	V
Storage Temperature	T_A	-65	150	ºC
Junction Temperature			125	ºC
RF input power max			23	dBm

Notes:
1. V_{IN} corresponds to all the digital pins.
2. V_{AIN} corresponds to the following analog pins: VDD_RF_RX, VDD_RF_TX, VDD_AMS, RFIOP, RFION, XO_N, XO_P, VDD_SXDIG, VDD_VCO.
3. For V_{ESDHBM}, each pin is classified as Class 1, or Class 2, or both:
   - The Class 1 pins include all the pins (both analog and digital)
   - The Class 2 pins are all digital pins only
   - V_{ESDHBM} is ±1kV for Class1 pins. V_{ESDHBM} is ±2kV for Class2 pins

4.2 Recommended Operating Conditions

Table 4-2. Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Units
I/O Supply Voltage Low Range	$VDDIO_L$	1.62	1.80	2.00	V
I/O Supply Voltage Mid Range	$VDDIO_M$	2.00	2.50	3.00	V
I/O Supply Voltage High Range	$VDDIO_H$	3.00	3.30	3.60	V
Battery Supply Voltage	VBATT	2.5[A]	3.60	4.20	
Operating Temperature		-40		85	ºC

Notes:
1. ATWILC1000A is functional across this range of voltages; however, optimal RF performance is guaranteed for VBATT in the range 3.0V < VBATT < 4.2V.
2. I/O supply voltage is applied to the following pins: VDDIO_A, VDDIO.
3. Battery supply voltage is applied to following pins: VDD_BATT_PPA, VDD_BATT_PA, VBATT_BUCK.
4. Refer to Section 9.1 and Table 9-3 for the details of power connections.

4.3 DC Electrical Characteristics

Table 4-3 provides the DC characteristics for the ATWILC1000A digital pads.

Table 4-3. DC Electrical Characteristics

VDDIO Condition	Characteristic	Min	Max	Unit
$VDDIO_L$	Input Low Voltage V_{IL}	-0.30	0.60	V
	Input High Voltage V_{IH}	VDDIO-0.60	VDDIO+0.30	V
	Output Low Voltage V_{OL}		0.45	V
	Output High Voltage V_{OH}	VDDIO-0.50		V
$VDDIO_M$	Input Low Voltage V_{IL}	-0.30	0.63	V
	Input High Voltage V_{IH}	VDDIO-0.60	VDDIO+0.30	V
	Output Low Voltage V_{OL}		0.45	V
	Output High Voltage V_{OH}	VDDIO-0.50		V
$VDDIO_H$	Input Low Voltage V_{IL}	-0.30	0.65	V
	Input High Voltage V_{IH}	VDDIO-0.60	VDDIO+0.30 (up to 3.60)	V
	Output Low Voltage V_{OL}		0.45	V
	Output High Voltage V_{OH}	VDDIO-0.50		V
All	Output Loading		20	pF
All	Digital Input Load		6	pF

5 Clocking

5.1 Crystal Oscillator

Table 5-1. Crystal Oscillator Parameters

Parameter	Min	Typ	Max	Units
Crystal Resonant Frequency	12	26	40	MHz
Crystal Equivalent Series Resistance		50	150	Ω
Stability – Initial Offset[1]	-100		100	ppm
Stability - Temperature and Aging	-25		25	ppm

Note: 1. Initial offset must be calibrated to maintain ±25ppm in all operating conditions. This calibration is performed during final production testing.

The block diagram in Figure 5-1(a) shows how the internal Crystal Oscillator (XO) is connected to the external crystal. The XO has 5pF internal capacitance on each terminal XO_P and XO_N. To bypass the crystal oscillator with an external reference, an external signal capable of driving 5pF can be applied to the XO_N terminal as shown Figure 5-1(b).

Figure 5-1. XO Connections: (a) The Crystal Oscillator is Used, (b) The Crystal Oscillator is Bypassed

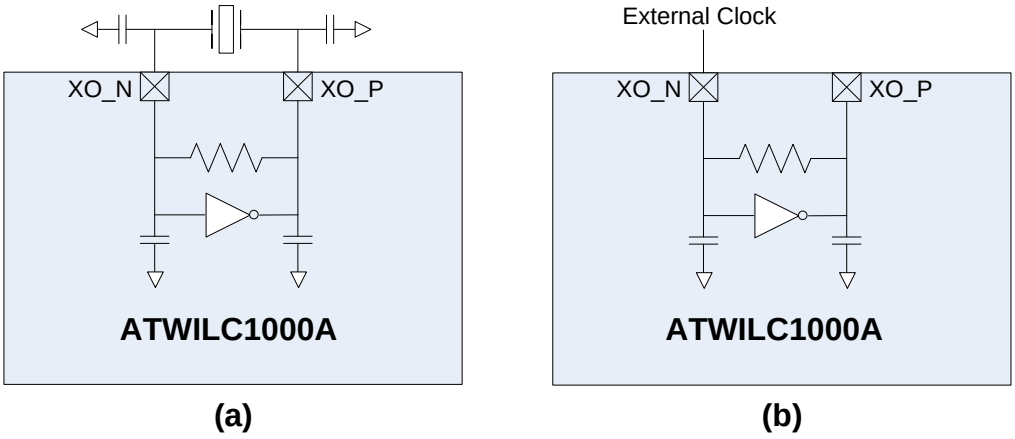


Table 5-2 specifies the electrical and performance requirements for the external clock.

Table 5-2. Bypass Clock Specification

Parameter	Min	Max	Unit	Comments
Oscillation frequency	12	32	MHz	Must be able to drive 5pF load @ desired frequency
Voltage swing	0.5	1.2	V_{pp}	Must be AC coupled
Stability – Temperature and Aging	-25	+25	ppm	
Phase Noise		-130	dBc/Hz	At 10kHz offset
Jitter (RMS)		<1psec		Based on integrated phase noise spectrum from 1kHz to 1MHz

5.2 Low-Power Oscillator

ATWILC1000A has an internally-generated 32kHz clock to provide timing information for various sleep functions. Alternatively, ATWILC1000A allows for an external 32kHz clock to be used for this purpose, which is provided through Pin 24 (RTC_CLK). Software selects whether the internal clock or external clock is used.

The internal low-power clock is ring-oscillator based and has accuracy within 10,000ppm. When using the internal low-power clock, the advance wakeup time in beacon monitoring mode has to be increased by about 1% of the sleep time to compensate for the oscillator inaccuracy. For example, for the DTIM interval value of 1, wakeup time has to be increased by 1ms.

For any application targeting very low power consumption, an external 32kHz RTC clock should be used.

6 CPU and Memory Subsystems

6.1 Processor

ATWILC1000A has a Cortus APS3 32-bit processor. This processor performs many of the MAC functions, including but not limited to association, authentication, power management, security key management, and MSDU aggregation/de-aggregation. In addition, the processor provides flexibility for various modes of operation, such as STA and AP modes.

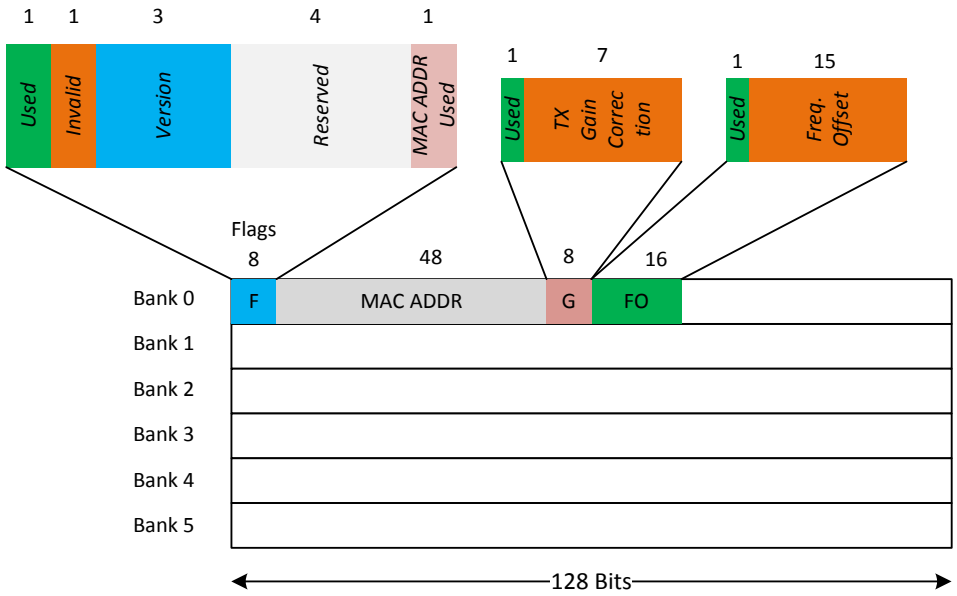
6.2 Memory Subsystem

The APS3 core uses a 128KB instruction/boot ROM along with a 128KB instruction RAM and a 64KB data RAM. In addition, the device uses a 128KB shared RAM, accessible by the processor and MAC, which allows the APS3 core to perform various data management tasks on the TX and RX data packets.

6.3 Non-Volatile Memory (EFuse)

ATWILC1000A has 768 bits of non-volatile EFuse memory that can be read by the CPU after device reset. This non-volatile one-time-programmable (OTP) memory can be used to store customer-specific parameters, such as MAC address; various calibration information, such as TX power, crystal frequency offset, etc; and other software-specific configuration parameters. The EFuse is partitioned into six 128-bit banks. Each bank has the same bit map, which is shown in Figure 6-1. The purpose of the first 80 bits in each bank is fixed, and the remaining 48 bits are general-purpose software dependent bits, or reserved for future use. Since each bank can be programmed independently, this allows for several updates of the device parameters following the initial programming, e.g. updating MAC address. Refer to ATWILC1000A Programming Guide for the EFuse programming instructions.

Figure 6-1. EFuse Bit Map



7 WLAN Subsystem

The WLAN subsystem is composed of the Media Access Controller (MAC) and the Physical Layer (PHY). The following two subsections describe the MAC and PHY in detail.

7.1 MAC

7.1.1 Features

The ATWILC1000A IEEE802.11 MAC supports the following functions:

- IEEE 802.11b/g/n
- IEEE 802.11e WMM QoS EDCA/PCF multiple access categories traffic scheduling
- Advanced IEEE 802.11n features:
  - Transmission and reception of aggregated MPDUs (A-MPDU)
  - Transmission and reception of aggregated MSDUs (A-MSDU)
  - Immediate Block Acknowledgement
  - Reduced Interframe Spacing (RIFS)
- Support for IEEE802.11i and WFA security with key management
  - WEP 64/128
  - WPA-TKIP
  - 128-bit WPA2 CCMP (AES)
- Support for WAPI security
- Advanced power management
  - Standard 802.11 Power Save Mode
  - Wi-Fi Alliance WMM-PS (U-APSD)
- RTS-CTS and CTS-self support
- Supports either STA or AP mode in the infrastructure basic service set mode
- Supports independent basic service set (IBSS)

7.1.2 Description

The ATWILC1000A MAC is designed to operate at low power while providing high data throughput. The IEEE 802.11 MAC functions are implemented with a combination of dedicated datapath engines, hardwired control logic, and a low-power, high-efficiency microprocessor. The combination of dedicated logic with a programmable processor provides optimal power efficiency and real-time response while providing the flexibility to accommodate evolving standards and future feature enhancements.

Dedicated datapath engines are used to implement data path functions with heavy computational. For example, an FCS engine checks the CRC of the transmitting and receiving packets, and a cipher engine performs all the required encryption and decryption operations for the WEP, WPA-TKIP, WPA2 CCMP-AES, and WAPI security requirements.

Control functions which have real-time requirements are implemented using hardwired control logic modules. These logic modules offer real-time response while maintaining configurability via the processor. Examples of hardwired control logic modules are the channel access control module (implements EDCA/HCCA, Beacon TX control, interframe spacing, etc.), protocol timer module (responsible for the Network Access Vector, back-off timing, timing synchronization function, and slot management), MPDU handling module, aggregation/de-aggregation module, block ACK controller (implements the protocol requirements for burst block communication), and TX/RX control FSMs (coordinate data movement between PHY-MAC interface, cipher engine, and the DMA interface to the TX/RX FIFOs).

The MAC functions implemented solely in software on the microprocessor have the following characteristics:

- Functions with high memory requirements or complex data structures. Examples are association table management and power save queuing.
- Functions with low computational load or without critical real-time requirements. Examples are authentication and association.

- Functions which need flexibility and upgradeability. Examples are beacon frame processing and QoS scheduling.

7.2 PHY

7.2.1 Features

The ATWILC1000A IEEE802.11 PHY supports the following functions:

- Single antenna 1x1 stream in 20MHz channels
- Supports IEEE 802.11b DSSS-CCK modulation: 1, 2, 5.5, 11Mbps
- Supports IEEE 802.11g OFDM modulation: 6, 9, 12,18, 24, 36, 48, 54Mbps
- Supports IEEE 802.11n HT modulations MCS0-7, 20MHz, 800 and 400ns guard interval: 6.5, 7.2, 13.0, 14.4, 19.5, 21.7, 26.0, 28.9, 39.0, 43.3, 52.0, 57.8, 58.5, 65.0, 72.2Mbps
- IEEE 802.11n mixed mode operation
- Per packet TX power control
- Advanced channel estimation/equalization, automatic gain control, CCA, carrier/symbol recovery, and frame detection

7.2.2 Description

The ATWILC1000A WLAN PHY is designed to achieve reliable and power-efficient physical layer communication specified by IEEE 802.11 b/g/n in single stream mode with 20MHz bandwidth. Advanced algorithms have been employed to achieve maximum throughput in a real world communication environment with impairments and interference. The PHY implements all the required functions such as FFT, filtering, FEC (Viterbi decoder), frequency and timing acquisition and tracking, channel estimation and equalization, carrier sensing and clear channel assessment, as well as the automatic gain control.

7.3 Radio

7.3.1 Receiver Performance

Radio Performance under Typical Conditions: VBAT=3.6V; VDDIO=3.3V; Temp: 25°C.

Table 7-1. Receiver Performance

Parameter	Description	Unit	Minimum	Typical	Maximum
Frequency		MHz	2,412		2,484
Sensitivity 802.11b	1Mbps DSS	dBm		-98	
	2Mbps DSS	dBm		-94	
	5.5Mbps DSS	dBm		-92	
	11Mbps DSS	dBm		-88	
Sensitivity 802.11g	6Mbps OFDM	dBm		-90	
	9Mbps OFDM	dBm		-89	
	12Mbps OFDM	dBm		-88	
	18Mbps OFDM	dBm		-85	
	24Mbps OFDM	dBm		-83	
	36Mbps OFDM	dBm		-80	

Parameter	Description	Unit	Minimum	Typical	Maximum
	48Mbps OFDM	dBm		-76	
	54Mbps OFDM	dBm		-74	
Sensitivity 802.11n (BW=20MHz)	MCS 0	dBm		-89	
	MCS 1	dBm		-87	
	MCS 2	dBm		-85	
	MCS 3	dBm		-82	
	MCS 4	dBm		-77	
	MCS 5	dBm		-74	
	MCS 6	dBm		-72	
	MCS 7	dBm		-71	
Maximum Receive Signal Level	1-11Mbps DSS	dBm	-10	0	
	6-54Mbps OFDM	dBm	-10	0	
	MCS 0 – 7	dBm	-10	0	
Adjacent Channel Rejection	1Mbps DSS (30MHz offset)	dB		50	
	11Mbps DSS (25MHz offset)	dB		43	
	6Mbps OFDM (25MHz offset)	dB		40	
	54Mbps OFDM (25MHz offset)	dB		25	
	MCS 0 – 20MHz BW (25MHz offset)	dB		40	
	MCS 7 – 20MHz BW (25MHz offset)	dB		20	
Cellular Blocker Immunity	776-794MHz CDMA	dBm		-14	
	824-849MHz GSM	dBm		-10	
	880-915MHz GSM	dBm		-10	
	1710-1785MHz GSM	dBm		-15	
	1850-1910MHz GSM	dBm		-15	
	1850-1910MHz WCDMA	dBm		-24	
	1920-1980MHz WCDMA	dBm		-24	

7.3.2 Transmitter Performance

Radio Performance under Typical Conditions: VBAT=3.6V; VDDIO=3.3V; Temp: 25°C.

Table 7-2. Transmitter Performance

Parameter	Description	Unit	Minimum	Typical[3]	Maxi-mum
Frequency		MHz	2,412		2,484
Output Power	802.11b DSSS 1Mbps	dBm		20.6[1]	
	802.11b DSSS 11Mbps	dBm		20.6[1]	
	802.11g OFDM 6Mbps	dBm		20.5[1]	
	802.11g OFDM 54Mbps	dBm		17.8[1]	
	802.11n HT20 MCS 0	dBm		18.8[1]	
	802.11n HT20 MCS 7	dBm		15.3[1]	
Tx Power Accuracy		dB		±1.5[2]	
Carrier Suppression		dBc		30.0	
Out of Band Transmit Power	76-108	dBm/Hz		-125	
	776-794	dBm/Hz		-125	
	869-960	dBm/Hz		-125	
	925-960	dBm/Hz		-125	
	1570-1580	dBm/Hz		-125	
	1805-1880	dBm/Hz		-125	
	1930-1990	dBm/Hz		-125	
	2110-2170	dBm/Hz		-125	
Harmonic Output Power	2nd	dBm/MHz		-33	
	3rd	dBm/MHz		-38	

Notes: 1. Measured at 802.11 spec compliant EVM/Spectral Mask.
2. Measured at RF Pin assuming 50Ω differential.
3. RF performance guaranteed for Temp range -30 to 85deg. 1dB derating in performance at -40 deg.

8 External Interfaces

ATWILC1000A external interfaces include I²C Slave for control, SPI Slave and SDIO Slave for control and data transfer, SPI Master for external Flash, I²C Master for external EEPROM, UART for debug, control, and data transfer, General Purpose Input/Output (GPIO) pins, and a Wi-Fi/Bluetooth coexistence interface. With the exception of the SPI Slave and SDIO Slave host interfaces, which are selected using the dedicated SDIO_SPI_CFG pin, the other interfaces can be assigned to various pins by programming the corresponding pin muxing control register for each pin to a specific value between 0 and 6.The default values of these registers are 0, which is GPIO mode. The summary of the available interfaces and their corresponding pin mux settings is shown in Table 8-1. For specific programming instructions refer to ATWILC1000A Programming Guide.

Table 8-1. Pin-Mux Matrix of External Interfaces

Pin Name	Mux 0	Mux 1	Mux 2	Mux3	Mux4	Mux6
GPIO0/HOST_WAKE	GPIO_0	I_HOST_WAKEUP		O_UART_TXD	IO_I2C_MASTER_SCL	IO_COE
GPIO2/IRQN	GPIO_2	O_IRQN		I_UART_RXD		IO_COE
SD_DAT3	GPIO_7	IO_SD_DAT3		O_UART_TXD		IO_COE
SD_DAT2/SPI_RXD		IO_SD_DA2	I_SPI_RXD			
SD_DAT1/SPI_SSN		IO_SD_DAT1	IO_SPI_SSN			
SD_DAT0/SPI_TXD		IO_SD_DAT0	O_SPI_TXD			
SD_CMD/SPI_SCK		IO_SD_CMD	IO_SPI_SCK			
SD_CLK	GPIO_8	I_SD_CLK		I_UART_RXD		IO_COE
GPIO1/RTC_CLK	GPIO_1	I_RTC_CLK		I_UART_RXD	IO_I2C_MASTER_SDA	IO_COE
GPIO3	GPIO_3	O_SPI_SCK_FLASH		I_UART_RXD		IO_COE
GPIO4	GPIO_4	O_SPI_SSN_FLASH	IO_I2C_MASTER_SCL			IO_COE
GPIO5	GPIO_5	O_SPI_TXD_FLASH		O_UART_TXD		IO_COE
GPIO6	GPIO_6	I_SPI_RXD_FLASH	IO_I2C_MASTER_SDA			IO_COE
I2C_SCL		IO_I2C_SCL		I_RTC_CLK	IO_I2C_MASTER_SCL	IO_COE
I2C_SDA		IO_I2C_SDA			IO_I2C_MASTER_SDA	IO_COE

8.1 I²C Slave Interface

The I²C Slave interface, used primarily for control by the host processor, is a two-wire serial interface consisting of a serial data line (SDA, Pin 33) and a serial clock (SCL, Pin 32). It responds to the seven bit address value 0x60. The ATWILC1000A I²C supports I²C bus Version 2.1 - 2000 and can operate in standard mode (with data rates up to 100Kb/s) and fast mode (with data rates up to 400Kb/s).

The I²C Slave is a synchronous serial interface. The SDA line is a bidirectional signal and changes only while the SCL line is low, except for STOP, START, and RESTART conditions. The output drivers are open-drain to perform wire-AND functions on the bus. The maximum number of devices on the bus is limited by only the maximum capacitance specification of 400pF. Data is transmitted in byte packages.

For specific information, refer to the Philips Specification entitled “The I²C -Bus Specification, Version 2.1”.

The I²C Slave timing is provided in Figure 8-1 and Table 8-2.

Figure 8-1. I²C Slave Timing Diagram

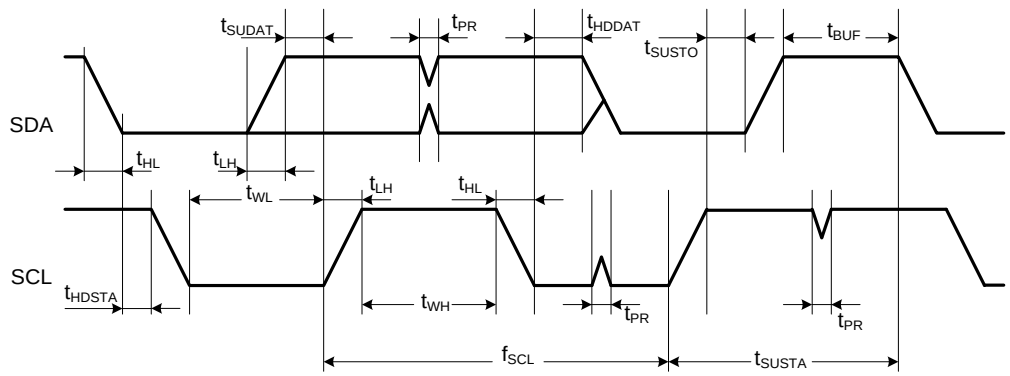


Table 8-2. I²C Slave Timing Parameters

Parameter	Symbol	Min	Max	Units	Remarks
SCL Clock Frequency	f_{SCL}	0	400	kHz	
SCL Low Pulse Width	t_{WL}	1.3		µs	
SCL High Pulse Width	t_{WH}	0.6		µs	
SCL, SDA Fall Time	t_{HL}		300	ns	
SCL, SDA Rise Time	t_{LH}		300	ns	This is dictated by external components
START Setup Time	t_{SUSTA}	0.6		µs	
START Hold Time	t_{HDSTA}	0.6		µs	
SDA Setup Time	t_{SUDAT}	100		ns	
SDA Hold Time	t_{HDDAT}	0 40		ns ns	Slave and Master Default Master Programming Option
STOP Setup time	t_{SUSTO}	0.6		µs	
Bus Free Time Between STOP and START	t_{BUF}	1.3		µs	
Glitch Pulse Reject	t_{PR}	0	50	ns	

8.2 I²C Master Interface

ATWILC1000A provides an I²C bus master, which is intended primarily for accessing an external EEPROM memory through a software-defined protocol. The I²C Master is a two-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA can be configured on one of the following pins: GPIO1 (pin 24), GPIO6 (pin 31), or I2C_SDA (pin 33). SCL can be configured on one of the following pins: GPIO0 (pin 10), GPIO4 (pin 29), or I2C_SCL (pin 32). For more specific instructions refer to ATWILC1000A Programming Guide.

The I²C Master interface supports three speeds:

- Standard mode (100kb/s)
- Fast mode (400kb/s)
- High-speed mode (3.4Mb/s)

The timing diagram of the I²C Master interface is the same as that of the I²C Slave interface (see Figure 8-1). The timing parameters of I²C Master are shown in Table 8-3.

Table 8-3. I²C Master Timing Parameters

Parameter	Symbol	Standard Mode		Fast Mode		High-Speed Mode		Units
		Min	Max	Min	Max	Min	Max	
SCL Clock Frequency	f_{SCL}	0	100	0	400	0	3400	kHz
SCL Low Pulse Width	t_{WL}	4.7		1.3		0.16		µs
SCL High Pulse Width	t_{WH}	4		0.6		0.06		µs
SCL Fall Time	t_{HLSCL}		300		300	10	40	ns
SDA Fall Time	t_{HLSDA}		300		300	10	80	ns

Parameter	Symbol	Standard Mode		Fast Mode		High-Speed Mode		Units
		Min	Max	Min	Max	Min	Max	
SCL Rise Time	t_{LHSCL}		1000		300	10	40	ns
SDA Rise Time	t_{LHSDA}		1000		300	10	80	ns
START Setup Time	t_{SUSTA}	4.7		0.6		0.16		µs
START Hold Time	t_{HDSTA}	4		0.6		0.16		µs
SDA Setup Time	t_{SUDAT}	250		100		10		ns
SDA Hold Time	t_{HDDAT}	5		40		0	70	ns
STOP Setup time	t_{SUSTO}	4		0.6		0.16		µs
Bus Free Time Between STOP and START	t_{BUF}	4.7		1.3				µs
Glitch Pulse Reject	t_{PR}			0	50			µs

8.3 SPI Slave Interface

ATWILC1000A provides a Serial Peripheral Interface (SPI) that operates as a SPI slave. The SPI Slave interface can be used for control and for serial I/O of 802.11 data. The SPI Slave pins are mapped as shown in Table 8-4. The RXD pin is same as Master Output, Slave Input (MOSI), and the TXD pin is same as Master Input, Slave Output (MISO). The SPI Slave is a full-duplex slave-synchronous serial interface that is available immediately following reset when pin 9 (SDIO_SPI_CFG) is tied to VDDIO.

Table 8-4. SPI Slave Interface Pin Mapping

Pin #	SPI Function
9	CFG: Must be tied to VDDIO
16	SSN: Active Low Slave Select
18	SCK: Serial Clock
13	RXD: Serial Data Receive (MOSI)
17	TXD: Serial Data Transmit (MISO)

When the SPI is not selected, i.e., when SSN is high, the SPI interface will not interfere with data transfers between the serial-master and other serial-slave devices. When the serial slave is not selected, its transmitted data output is buffered, resulting in a high impedance drive onto the serial master receive line.

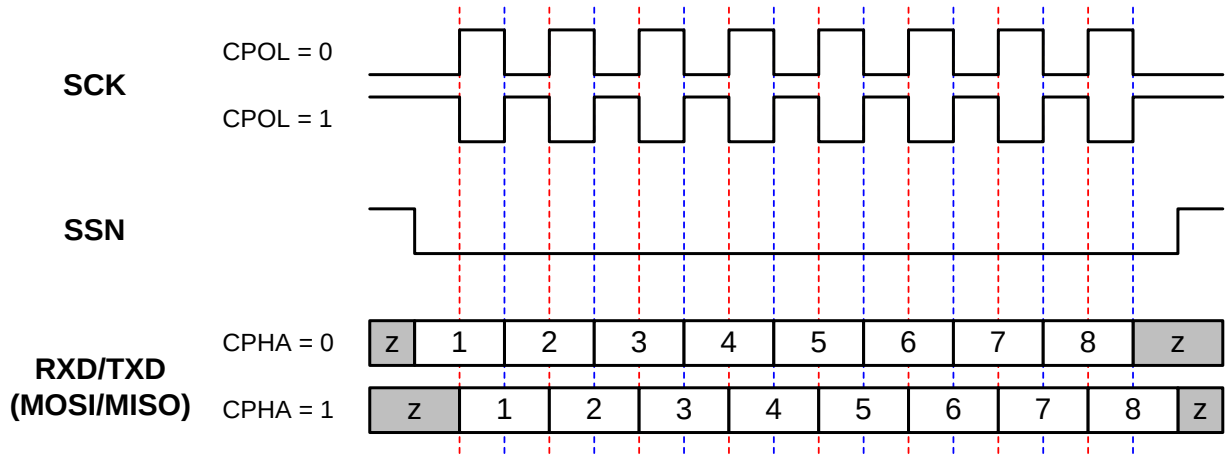
The SPI Slave interface responds to a protocol that allows an external host to read or write any register in the chip as well as initiate DMA transfers. For the details of the SPI protocol and more specific instructions refer to ATWILC1000A Programming Guide.

The SPI Slave interface supports four standard modes as determined by the Clock Polarity (CPOL) and Clock Phase (CPHA) settings. These modes are illustrated in 0 and Figure 8-2. The red lines in Figure 8-2 correspond to Clock Phase = 0 and the blue lines correspond to Clock Phase = 1.

Table 8-5. SPI Slave Modes

Mode	CPOL	CPHA
0	0	0
1	0	1
2	1	0
3	1	1

Figure 8-2. SPI Slave Clock Polarity and Clock Phase Timing



The SPI Slave timing is provided in Figure 8-3 and Table 8-6.

Figure 8-3. SPI Slave Timing Diagram

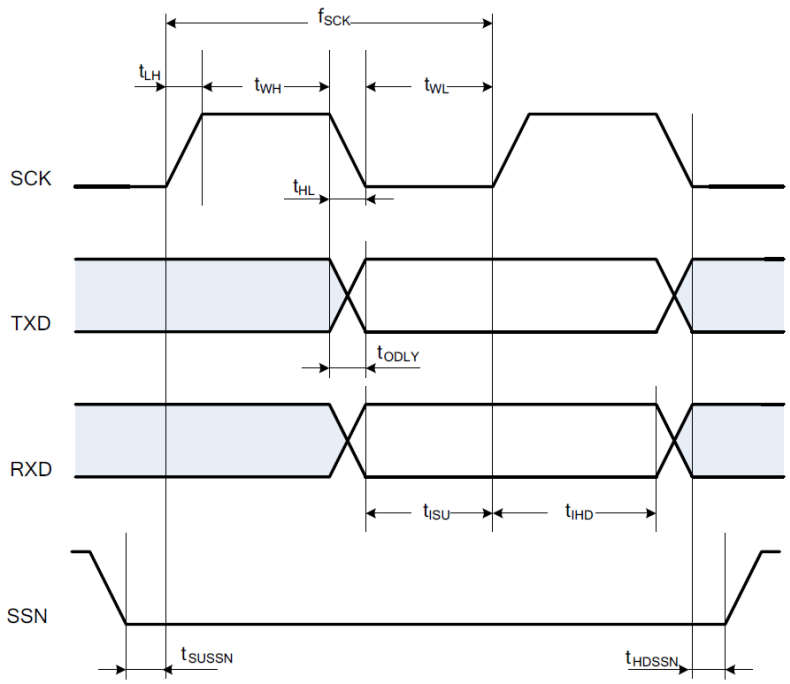


Table 8-6. SPI Slave Timing Parameters

Parameter	Symbol	Min	Max	Units
Clock Input Frequency	f_{SCK}		48	MHz
Clock Low Pulse Width	t_{WL}	15		ns
Clock High Pulse Width	t_{WH}	15		ns
Clock Rise Time	t_{LH}		10	ns
Clock Fall Time	t_{HL}		10	ns
Input Setup Time	t_{ISU}	5		ns
Input Hold Time	t_{IHD}	5		ns
Output Delay	t_{ODLY}	0	20	ns
Slave Select Setup Time	t_{SUSSN}	5		ns
Slave Select Hold Time	t_{HDSSN}	5		ns

8.4 SPI Master Interface

ATWILC1000A provides a SPI Master interface for accessing external flash memory. The SPI Master pins are mapped as shown in Table 8-7. The TXD pin is same as Master Output, Slave Input (MOSI), and the RXD pin is same as Master Input, Slave Output (MISO). The SPI Master interface supports all four standard modes of clock polarity and clock phase shown in 0. External SPI flash memory is accessed by a processor programming commands to the SPI Master interface, which in turn initiates a SPI master access to the flash. For more specific instructions refer to ATWILC1000A Programming Guide.

Table 8-7. SPI Master Interface Pin Mapping

Pin #	Pin Name	SPI Function
28	GPIO3	SCK: Serial Clock Output
29	GPIO4	SCK: Active Low Slave Select Output
30	GPIO5	TXD: Serial Data Transmit Output (MOSI)
31	GPIO6	RXD: Serial Data Receive Input (MISO)

The SPI Master timing is provided in Figure 8-4 and Table 8-8.

Figure 8-4. SPI Master Timing Diagram

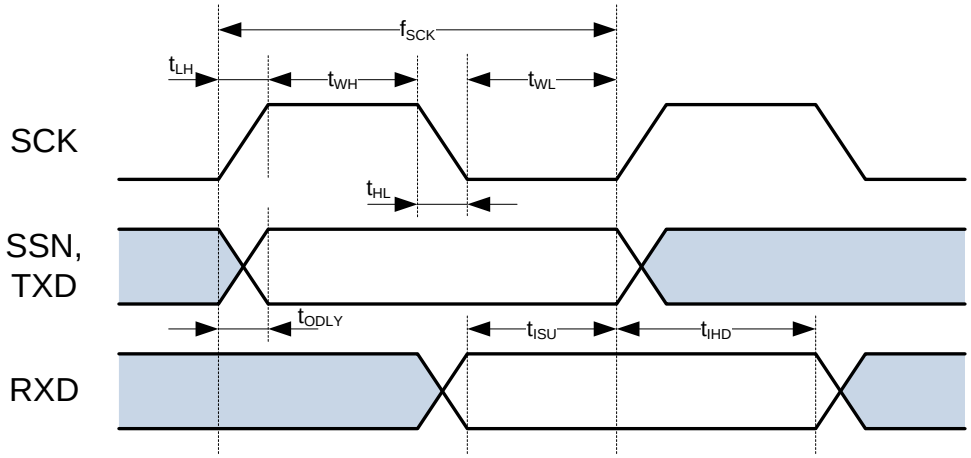


Table 8-8. SPI Master Timing Parameters

Parameter	Symbol	Min	Max	Units
Clock Output Frequency	f_{SCK}		48	MHz
Clock Low Pulse Width	t_{WL}	5		ns
Clock High Pulse Width	t_{WH}	5		ns
Clock Rise Time	t_{LH}		5	ns
Clock Fall Time	t_{HL}		5	ns
Input Setup Time	t_{ISU}	5		ns
Input Hold Time	t_{IHD}	5		ns
Output Delay	t_{ODLY}	0	5	ns

8.5 SDIO Slave Interface

The ATWILC1000A SDIO Slave is a full speed interface. The interface supports the 1-bit/4-bit SD transfer mode at the clock range of 0-50MHz. The Host can use this interface to read and write from any register within the chip as well as configure the ATWILC1000A for data DMA. To use this interface, pin 9 (SDIO_SPI_CFG) must be grounded. The SDIO Slave pins are mapped as shown in Table 8-9.

Table 8-9. SDIO Interface Pin Mapping

Pin #	SPI Function
9	CFG: Must be tied to ground
12	DAT3: Data 3
13	DAT2: Data 2
16	DAT1: Data 1
17	DAT0: Data 0
18	CMD: Command
19	CLK: Clock

When the SDIO card is inserted into an SDIO aware host, the detection of the card will be via the means described in SDIO specification. During the normal initialization and interrogation of the card by the host, the card will identify itself as an SDIO device. The host software will obtain the card information in a tuple (linked list) format and determine if that card's I/O function(s) are acceptable to activate. If the card is acceptable, it will be allowed to power up fully and start the I/O function(s) built into it.

The SD memory card communication is based on an advanced 9-pin interface (Clock, Command, 4 Data and 3 Power lines) designed to operate at maximum operating frequency of 50MHz.

The SDIO Slave interface has the following features:

- Meets SDIO card specification version 2.0
- Host clock rate variable between 0 and 50MHz
- 1 bit/4-bit SD bus modes supported
- Allows card to interrupt host
- Responds to Direct read/write (IO52) and Extended read/write (IO53) transactions.
- Supports Suspend/Resume operation

The SDIO Slave interface timing is provided in Figure 8-5 and Table 8-10.

Figure 8-5. SDIO Slave Timing Diagram

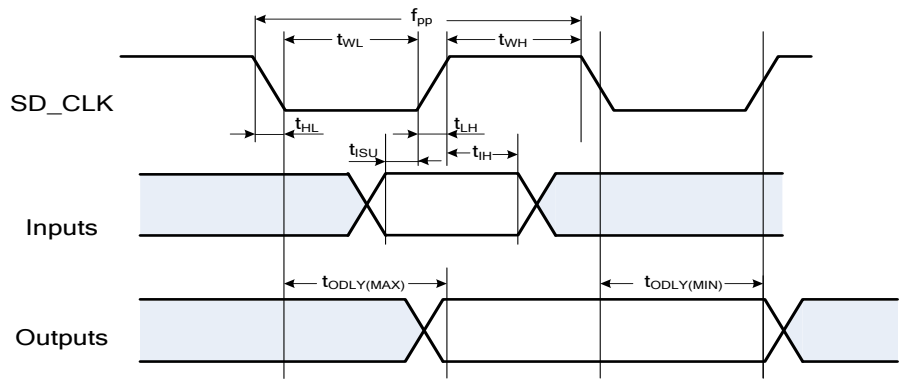


Table 8-10. SDIO Slave Timing Parameters

Parameter	Symbol	Min	Max	Units
Clock Input Frequency	f_{PP}	0	50	MHz
Clock Low Pulse Width	t_{WL}	10		ns
Clock High Pulse Width	t_{WH}	10		ns
Clock Rise Time	t_{LH}		10	ns
Clock Fall Time	t_{HL}		10	ns
Input Setup Time	t_{ISU}	5		ns
Input Hold Time	t_{IH}	5		ns
Output Delay	t_{ODLY}	0	14	ns

8.6 UART

ATWILC1000A has a Universal Asynchronous Receiver/Transmitter (UART) interface for serial communication. It is intended primarily for debugging, and it can also be used for control or data transfer if the baud rate is sufficient for a given application. The UART is compatible with the RS-232 standard, where ATWILC1000A operates as Data Terminal Equipment (DTE). It has a two-pin RXD/TXD interface, where RXD can be enabled on one of four alternative pins and TXD can be enabled on one of three alternative pins by programming their corresponding pin mux control registers to 3 (see Table 8-1).

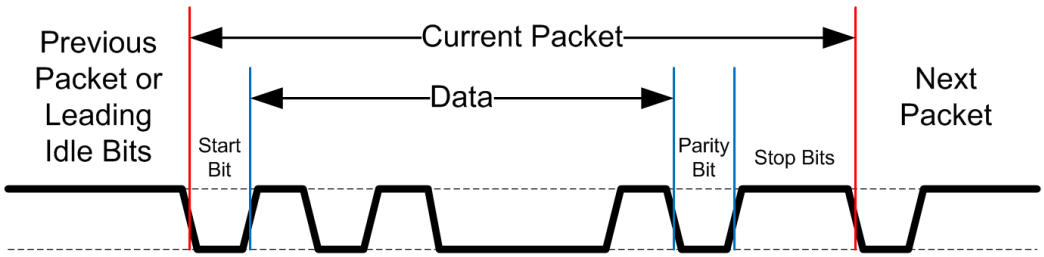
The UART features programmable baud rate generation with fractional clock division, which allows transmission and reception at a wide variety of standard and non-standard baud rates. The UART input clock is selectable between 10MHz, 5MHz, 2.5MHz, and 1.25MHz. The clock divider value is programmable as 13 integer bits and 3 fractional bits (with 8.0 being the smallest recommended value for normal operation). This results in the maximum supported baud rate of 10MHz/8.0 = 1.25MBd.

The UART can be configured for seven or eight bit operation, with or without parity, with four different parity types (odd, even, mark, or space), and with one or two stop bits. It also has Rx and Tx FIFOs, which ensure reliable high speed reception and low software overhead transmission. FIFO size is 4 x 8 for both Rx and Tx direction. The UART also has status registers showing the number of received characters available in the FIFO and various error conditions, as well the ability to generate interrupts based on these status bits.

An example of UART receiving or transmitting a single packet is shown in Figure 8-6. This example shows 7-bit data (0x45), odd parity, and two stop bits.

For more specific instructions refer to ATWILC1000A Programming Guide.

Figure 8-6. Example of UART Rx or Tx Packet



8.7 Wi-Fi/Bluetooth Coexistence

ATWILC1000A supports 2-wire and 3-wire Wi-Fi/Bluetooth Coexistence signaling conforming to the IEEE 802.15.2-2003 standard, Part 15.2. The type of coexistence interface used (2 or 3 wire) is chosen to be compatible with the specific Bluetooth device used in a given application. Table 8-11 shows a usage example of the 2-wire interface using the GPIO3 and GPIO4 pins; 3-wire interface using the GPIO3, GPIO4, and GPIO5 pins; For more specific instructions on configuring Coexistence refer to ATWILC1000A Programming Guide.

Table 8-11. Coexistence Pin Assignment Example

Pin Name	Function	Target	Pin #	2-wire	3-wire
GPIO3	BT_Req	BT is requesting to access the medium to transmit or receive. Goes high on TX or RX slot	28	Used	Used
GPIO4	BT_Pri	Priority of the BT packets in the requested slot. High to indicate high priority and low for normal.	29	Not Used	Used
GPIO5	WL_Act	Device response to the BT request. High - BT_req is denied and BT slot blocked.	30	Used	Used

Pin Name	Function	Target	Pin #	2-wire	3-wire
GPIO6	Ant_SW	Direct control on Antenna (coex bypass)	31	Optional	Optional

8.8 GPIOs

Nine General Purpose Input/Output (GPIO) pins, labeled GPIO 0-8, are available to allow for application specific functions. Each GPIO pin can be programmed as an input (the value of the pin can be read by the host or internal processor) or as an output (the output values can be programmed by the host or internal processor), where the default mode after power-up is input. GPIOs 7 and 8 are only available when the host does not use the SDIO interface, which shares two of its pins with these GPIOs. Therefore, for SDIO-based applications, seven GPIOs (0-6) are available. For more specific usage instructions refer to ATWILC1000A Programming Guide.

9 Power Management

9.1 Power Architecture

ATWILC1000A uses an innovative power architecture to eliminate the need for external regulators and reduce the number of off-chip components. This architecture is shown in Figure 9-1. The Power Management Unit (PMU) has a DC/DC Converter that converts VBATT to the core supply used by the digital and RF/AMS blocks. Table 9-1 shows the typical values for the digital and RF/AMS core voltages. The PA and EFuse are supplied by dedicated LDOs, and the VCO is supplied by a separate LDO structure.

Figure 9-1. Power Architecture

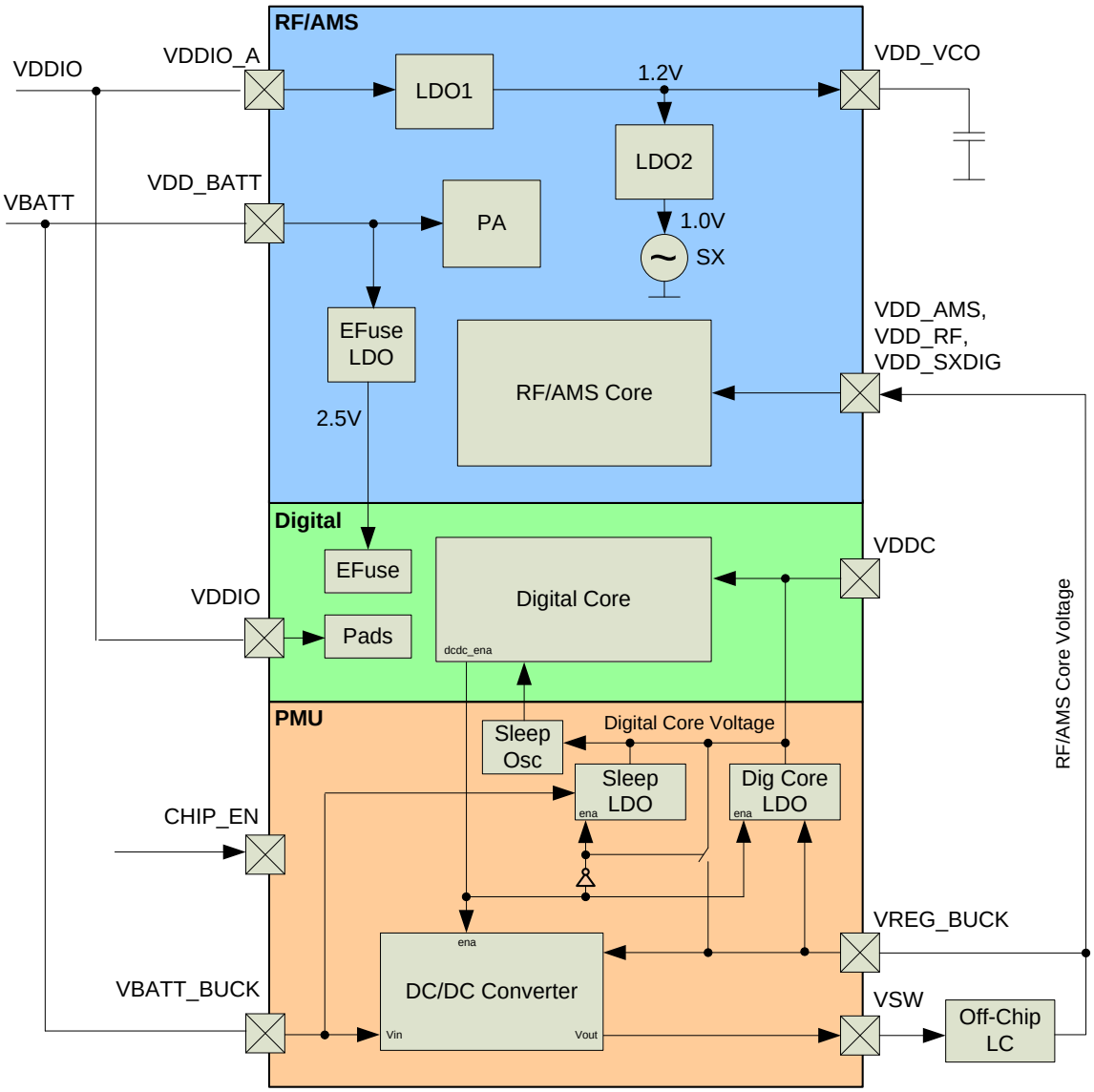


Table 9-1. PMU Output Voltages

Parameter	Typical
RF/AMS Core Voltage (VREG_BUCK)	1.35V
Digital Core Voltage (VDDC)	1.10V

The power connections in Figure 9-1 provide a conceptual framework for understanding the ATWILC1000A power architecture. Refer to the reference design for an example of power supply connections, including proper isolation of the supplies used by the digital and RF/AMS blocks.

9.2 Power Consumption

9.2.1 Description of Device States

ATWILC1000A has several Devices States:

- ON_Transmit – Device is actively transmitting an 802.11 signal
- ON_Receive – Device is actively receiving an 802.11 signal
- ON_Doze – Device is on but is neither transmitting nor receiving
- Power_Down – Device core supply off (Leakage)

9.2.2 Controlling the Device States

Table 9-2 shows how to switch between the device states using the following:

- CHIP_EN – Device pin (pin #23) used to enable DC/DC Converter
- VDDIO – I/O supply voltage from external supply

Table 9-2. Device States

Device State	CHIP_EN	VDDIO	Power Consumption[1]	
			I_{VBATT}	I_{VDDIO}
ON_Transmit	VDDIO	On	230mA @ 18dBm	29mA
ON_Receive	VDDIO	On	68mA	29mA
ON_Doze	VDDIO	On	280µA	<10µA
Power_Down	GND	On	<0.5µA	<0.2µA

Note: 1. Conditions: VBAT @ 3.6v, IO@1.8V

9.2.3 Restrictions for Power States

When no power supplied to the device, i.e., the DC/DC Converter output and VDDIO are both off (at ground potential). In this case, a voltage cannot be applied to the device pins because each pin contains an ESD diode from the pin to supply. This diode will turn on when voltage higher than one diode-drop is supplied to the pin.

If a voltage must be applied to the signal pads while the chip is in a low power state, the VDDIO supply must be on, so the SLEEP or Power_Down state must be used.

Similarly, to prevent the pin-to-ground diode from turning on, do not apply a voltage that is more than one diode-drop below ground to any pin.

9.3 Power-Up/Down Sequence

The power-up/down sequence for ATWILC1000A is shown in Figure 9-2. The timing parameters are provided in Table 9-3.

Figure 9-2. Power Up/Down Sequence

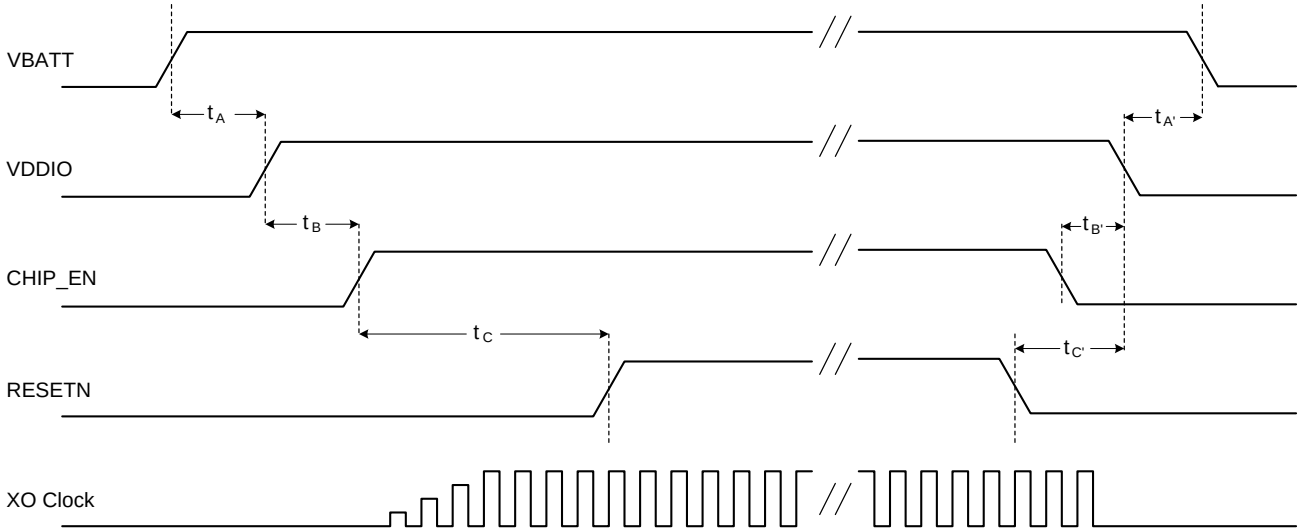


Table 9-3. Power-Up/Down Sequence Timing

Parameter	Min	Max	Units	Description	Notes
t_A	0		ms	VBATT rise to VDDIO rise	VBATT and VDDIO can rise simultaneously or can be tied together. VDDIO must not rise before VBATT.
t_B	0		ms	VDDIO rise to CHIP_EN rise	CHIP_EN must not rise before VDDIO. CHIP_EN must be driven high or low, not left floating.
t_C	5		ms	CHIP_EN rise to RESETN rise	This delay is needed because XO clock must stabilize before RESETN removal. RESETN must be driven high or low, not left floating.
t_A	0		ms	VDDIO fall to VBATT fall	VBATT and VDDIO can fall simultaneously or can be tied together. VBATT must not fall before VDDIO.
t_B	0		ms	CHIP_EN fall to VDDIO fall	VDDIO must not fall before CHIP_EN. CHIP_EN and RESETN can fall simultaneously.
t_C	0		ms	RESETN fall to VDDIO fall	VDDIO must not fall before RESETN. RESETN and CHIP_EN can fall simultaneously.

9.4 Digital I/O Pin Behavior during Power-Up Sequences

The following table represents digital IO Pin states corresponding to device power modes.

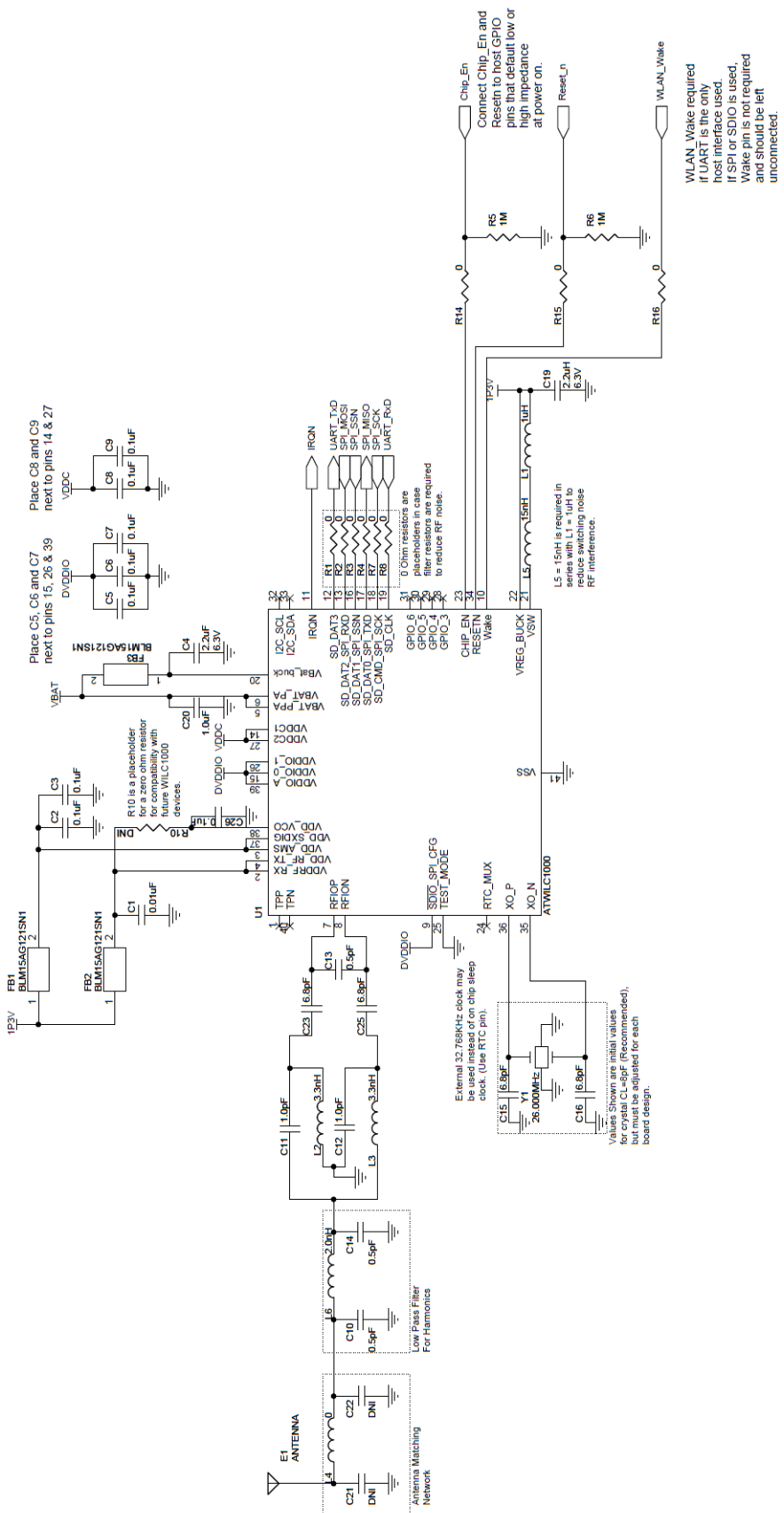
Table 9-4. Digital I/O Pin Behavior in Different Device States

Device State	VDDIO	CHIP_EN	RESETN	Output Driver	Input Driver	Pull Up/Down Resistor (96kΩ)
Power_Down: core supply off	High	Low	Low	Disabled (Hi-Z)	Disabled	Disabled
Power-On Reset: core supply on, hard reset on	High	High	Low	Disabled (Hi-Z)	Disabled	Enabled
Power-On Default: core supply on, device out of reset but not programmed yet	High	High	High	Disabled (Hi-Z)	Enabled	Enabled
On_Doze/ On_Transmit/ On_Receive: core supply on, device programmed by firmware	High	High	High	Programmed by firmware for each pin: Enabled or Disabled	Opposite of Output Driver state	Programmed by firmware for each pin: Enabled or Disabled

10 Reference Design

The ATWILC1000A reference design schematic is shown in Figure 10-1.

Figure 10-1. ATWILC10 Reference Schematic



11 Reference Documentation and Support

11.1 Reference Documents

Atmel offers a set of collateral documentation to ease integration and device ramp.

The following list of documents available on Atmel web or integrated into development tools.

To enable fast development contact your local FAE or visit the http://www.atmel.com/.

Title	Content
Datasheet	This Document
Design Files Package	User Guide, Schematic, PCB layout, Gerber, BOM & System notes on: RF/Radio Full Test Report, radiation pattern, design guide-lines, temperature performance, ESD.
Platform Getting started Guide	How to use package: Out of the Box starting guide, HW limitations and notes, SW Quick start guidelines.
HW Design Guide	Best practices and recommendations to design a board with the product, Including: Antenna Design for Wi-Fi (layout recommendations, types of an-tennas, im-pedance matching, using a power amplifier etc), SPI/UART protocol between Wi-Fi SoC and the Host MCU.
SW Design Guide	Integration guide with clear description of: High level Arch, overview on how to write a networking application, list all API, parameters and structures. Features of the device, SPI/handshake protocol between device and host MCU, flow/se-quence/state diagram & timing.
SW Programmer Guide	Explain in details the flow chart and how to use each API to implement all generic use cases (e.g. start AP, start STA, provisioning, UDP, TCP, http, TLS, p2p, errors manage-ment, connection/transfer recovery mechanism/state dia-gram) - usage & sample App note

For a complete listing of development-support tools & documentation, visit http://www.atmel.com/,

Or contact the nearest Atmel field representative.

12 Revision History

Doc Rev.	Date	Comments
42351C	02/2015	DS update new Atmel format.
42351B	11/2014	Major document update, new sections added, replaced text in most sections, new and updated drawings.
42351A	07/2014	Initial document release.

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