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MCS16C451

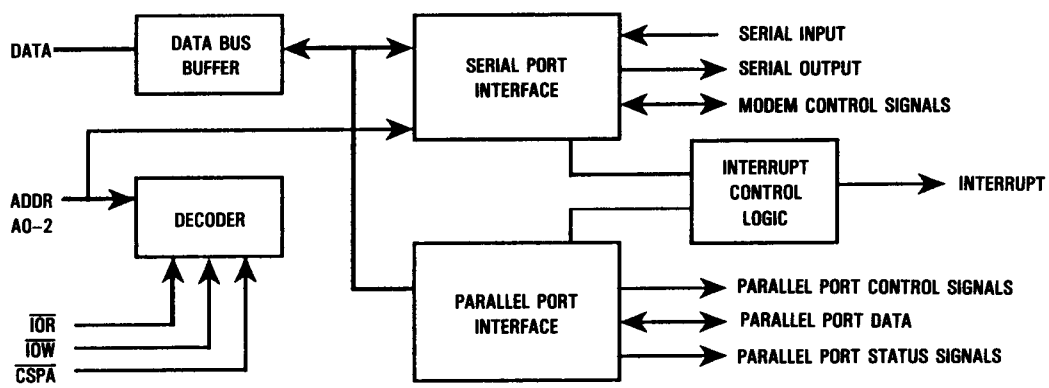
Advance Information

Multifunction I/O Control Chip for PC/XT/AT

The MCS16C451 is a multifunction chip designed for motherboards or add-in cards compatible with IBM PC/XT* and AT* systems. The MCS16C451 has an NS 16450 compatible asynchronous communications element to build a serial port and a bidirectional parallel port interface that supports a Centronics type printer and allows the parallel port to receive data from external devices.

- Supports Flexible PC/XT and AT Port Address Decoding
- 100% Compatible with NS 16450/NS 8250 UART
- One Full-Duplex Asynchronous Receiver/Transmitter
- Programmable Serial Interface Characters
- Programmable Baud Rate for each Receiver and Transmitter
- Full Modem Control Functions
- Double Buffering in Character Mode
- False Start Bit Detection
- Centronics Printer Interface
- Parallel Port Extended Mode Supports Bidirectional Input and Output
- Parallel Port Supports Level Sensitive, Readable Interrupt Pending Status
- Direct Drive for Parallel Port Interface
- 68-Pin PLCC Package

BLOCK DIAGRAM



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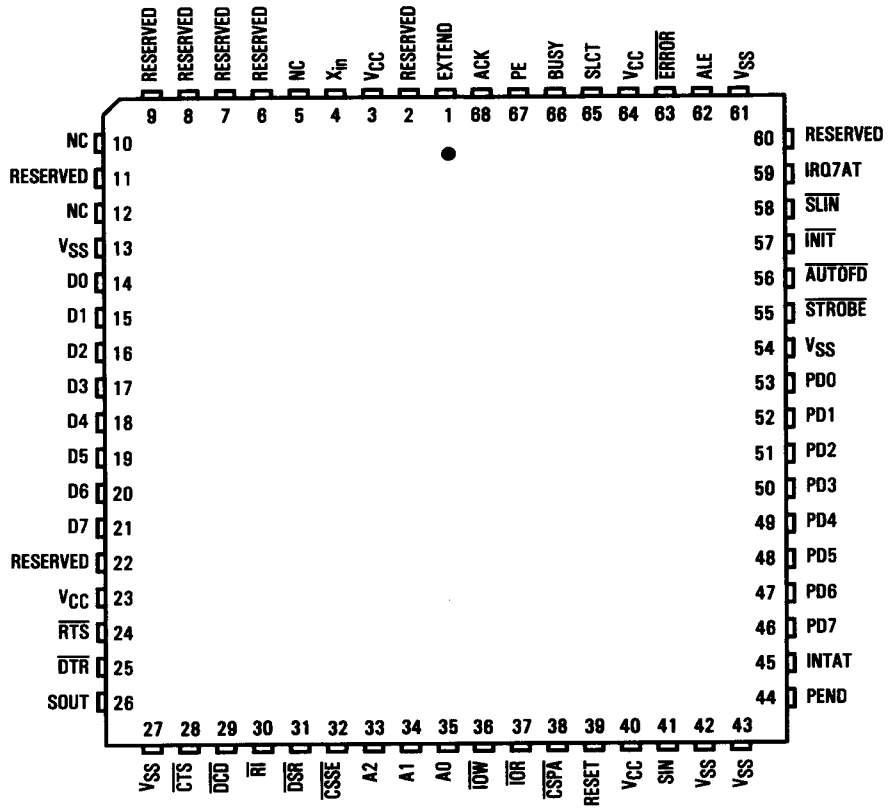
PIN ASSIGNMENT



PIN DESCRIPTIONS

Symbol	Pin	I/O	Pin Description
EXTEND	1	I	Extended mode is selected when this pin is set to zero. In extended mode, parallel data becomes an 8-bit parallel and bidirectional interface.
XIN	4	I	External clock input. Connects the main timing reference to the UART.
D0 D1 D2 D3 D4 D5 D6 D7	14 15 16 17 18 19 20 21	I/O	CPU Data Bus bit.
$\overline{RTS}$	24	O	Request to send. When low, informs the modem or data set that UART is ready to send data.
$\overline{DTR}$	25	O	Data terminal ready. When low, $\overline{DTR}$ informs the modem or data set that the UART is ready to receive data.
SOUT	26	O	Serial data output.
$\overline{CTS}$	28	I	Clear to send. When low, indicates that the modem or data set is ready to receive data.
$\overline{DCD}$	29	I	Data carrier detect. When low, indicates the modem or data set has detected a data carrier.
$\overline{RI}$	30	I	Ring indicator. When low, indicates a telephone ringing signal has been detected by the modem or data set.
$\overline{DSR}$	31	I	Data set ready. When low, indicates that the modem or data set is ready to establish the communication link and transfer data with the UART.
$\overline{CSSE}$	32	I	Serial port select. When this signal is low, the serial port is selected.
$\overline{CSPA}$	38	I	Parallel port select. When this signal is low, the parallel port is selected.

PIN DESCRIPTIONS (Continued)

Symbol	Pin	I/O	Pin Description
A0 A1 A2	35 34 33	I	CPU address bus bit.
$\overline{IOW}$	36	I	I/O write strobe. When this signal is low, the CPU can write data to the UART or the parallel port.
$\overline{IOR}$	37	I	I/O read strobe. When this signal is low, the CPU can read status information or data from the UART or the parallel port.
RESET	39	I	Clears the parallel port control register and all serial port registers.
SIN	41	I	Serial data input from the model or data set.
PEND	44	O	Bus buffer output. PEND is low when the serial port or the parallel port is read.
INTAT	45	O	Serial port interrupt for AT.
PD0 PD1 PD2 PD3 PD4 PD5 PD6 PD7	53 52 51 50 49 48 47 46	I/O	Parallel port Data Bus bit.
$\overline{STROBE}$	55	I/O	Printer strobe. When low, clocks data into the printer.
$\overline{AUTOFD}$	56	I/O	Printer autofeed. When low, causes a line feed after each line is printed.
$\overline{INIT}$	57	I/O	Printer initialize. When low, the printer starts the initialization routine.
$\overline{SLIN}$	58	I/O	Printer select. When low, selects the printer.
IRQ7AT	59	O	Parallel port interrupt for AT.
ALE	62	I	Address latch enable active high.
$\overline{ERROR}$	63	I	Printer error. When low, indicates a printer error.
SLCT	65	I	Printer selected. When high, indicates that the printer is selected.
BUSY	66	I	Printer busy. When high, indicates that the printer cannot accept data.
PE	67	I	End of paper. When high, indicates that the printer detects an end of paper.
ACK	68	I	Printer acknowledge. When high, indicates that the printer has received data.
V_{CC}	3, 23, 40, 64		+5 volt supply.
V_{SS}	13, 27, 42, 43, 54, 61		Ground.
Reserved	2, 6, 7, 8, 9, 11, 22, 60		Tied to V_{SS}.
NC	5, 10, 12		

Functional Description

The MCS16C451 is a single device solution that serves one serial port and one bidirectional parallel port for the IBM PC/XT and AT compatible systems.

The serial port interface converts data from peripheral devices or modems from serial-in-data to parallel-out-data. Data transmitted from the CPU is converted from parallel-in-data to serial-out-data. The status of the parallel/ asynchronous receiver transmitter can be read during any CPU operation. Status includes type and condition of the transfer operations in progress, and error conditions.

The MCS16C451 provides a bidirectional parallel data port that supports a parallel Centronics type printer. Information received from the serial communications port can be printed from the parallel/asynchronous receiver transmitter. The parallel port and serial port together, provide PC/AT compatible computers with a single device serving two system ports.

The MCS16C451 uses an oscillator as the input clock source.

The MCS16C451 can be connected to standard parallel and serial connectors on either an XT and AT compatible system. The external components required include a high powered driving device. Refer to Figure 1 for a block diagram of application circuitry.

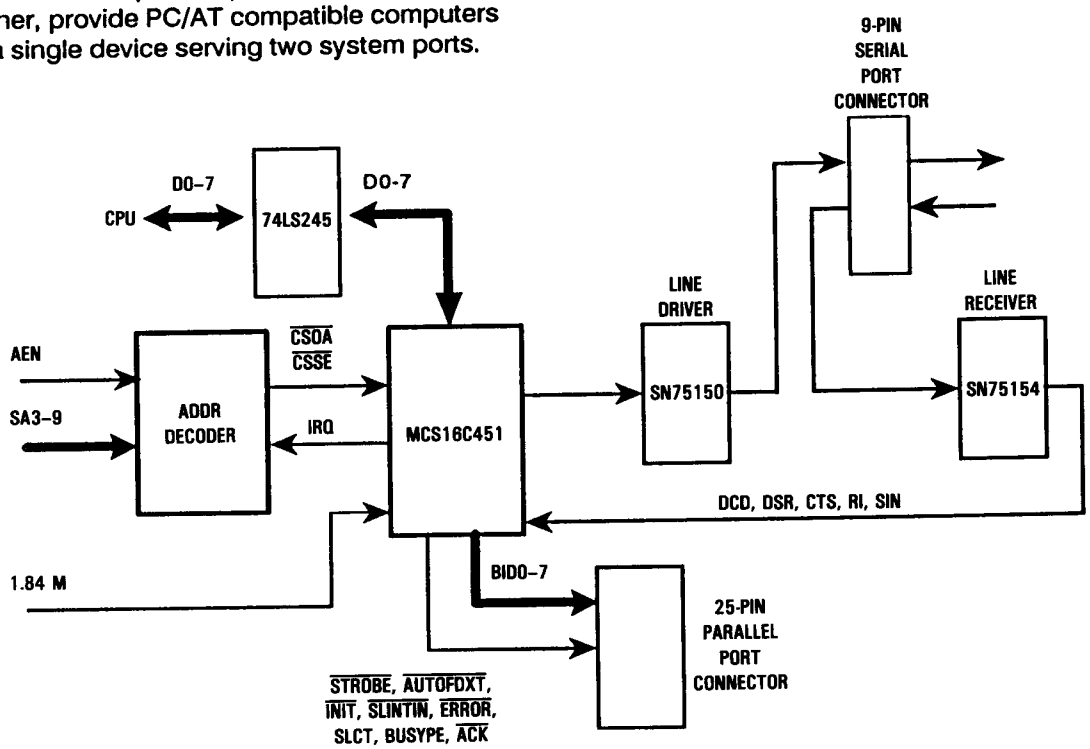


Figure 1 Application Circuitry Block Diagram

Serial Port Interface

The serial port interface has three types of internal registers. A programmable baud rate generator divides the timing reference clock input by a divisor between one and (2^{16} - 1).

Control registers

Bit Rate Select Register DLL
(Division Latch LSB)
Bit Rate Select Register DLM
(Division Latch MSB)
Line Control Register
Interrupt Enable Register
Interrupt Identification Register
Modem Control Register

Status registers

Line Status Registers
Modem Status Register

Data registers

Receiver Buffer Register
Transmitter Holding Register
Scratch Register

Table 1 summarizes the serial port registers.

Table 1 Serial Port Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Receiver Buffer Register (read only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)
Transmitter Holding Register (write only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Interrupt Enable Register	0	0	0	0	Enable Modem Status Interrupt	Enable Receiver Line Status Interrupt	Enable Trans-mitter Holding Register Interrupt	Enable Received Data Avail-able Interrpt
Interrupt Identification Register	0	0	0	0	0	Interrupt ID Bit 1	Interrupt ID Bit 0	"0" 1F Interrpt Pending
Line Control Register	Divisor Latch Address Bit	Set Break	Stick Parity	Even Parity Select	Parity Enable	Number of Stop Bits	Word Length Select Bit 1	Word Length Select Bit 0
Modem Control Register	0	0	0	Loop	Out 2	Out 1	Request to Send	Data Terminal Ready
Line Status Register	0	Trans-mitter Empty	Trans-mitter Holding Register Empty	Break Interrupt	Framing Error	Parity Error	Overrun Error	Data Ready
Modem Status Register . .	Data Carrier Detect	Ring Indicator	Data Ready Set	Clear to Send	Delta Receive Line Signal Detect	Trailing Edge Ring Indicator	Delta Data Set Ready	Delta Clear to Send
Status Control Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Address, Read, and Write inputs are used with the Divisor Latch Access bit (DLAB) in the Line Control register bit 7 [LCR(7)] to select the register to be read or written. Refer to Table 2 for register select states.

Table 2 Serial Port Internal Register Selection

DLAB	A2	A1	A0	Register
0	0	0	0	Receiver buffer register (read only)
0	0	0	0	Transmitter holding register (write only)
0	0	0	1	Interrupt enable register
x	0	1	0	Interrupt identification register (read only)
x	0	1	1	Line control register
x	1	0	0	Modem control register
x	1	0	1	Line status register
x	1	1	0	Modem status register
x	1	1	1	Scratch register
1	0	0	0	Divisor latch (LSB)
1	0	0	1	Divisor latch (MSB)

x = Don't care

Note that the serial port is accessed only when $\overline{CS0}$ is low.

The **Transmitter Holding Register** and **Receiver Buffer Register** are data registers that hold from five to eight bits of data. If fewer than eight data bits are transmitted, bit 0 is always the first serial data bit received and transmitted. Data registers are buffered twice to allow read and write operations to be executed at the same time the UART is converting parallel to serial and serial to parallel.

The **Line Control Register** controls the format of a data character. The contents of the LCR can be read precluding the need to store line characteristics in system memory. Table 3 contains the contents of the Line Control register.

Table 3 Line Control Register

Bit	Function	Logic 1	Logic 0
0	Word length select Bit 0		
1	Word length select Bit 1		
2	Stop bit select	1.5 or 2 stop bits	1 stop bit
3	Parity enable	Enabled	Disabled
4	Even parity select	Even parity	Odd parity
5	Stick parity	Enabled	Disabled
6	Set break	Enabled	Disabled
7	Divisor latch access bit	Access divisor latches	Access receiver latches

Bit 0-1 The number of bits in each serial character is programmed according to the following states.

LCR(1)	LCR(0)	Word length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

Bit 2 Specifies the number of stop bits in each character transmitted. If Bit 2 = 0, one stop bit is generated in the transmitted data. If Bit 2 = 1 when a 5-bit word is selected, 1.5 stop bits are generated. If Bit 2 = 1 when a 6-, 7- or 8-bit word is selected, two stop bits are generated. A programmed receiver checks for two stop bits.

Bit 3 When high, generates and checks a parity bit between the last data word bit and stop bit.

Bit 4 When parity is enabled (Bit 3 = 1), and Bit 4 = 0, odd parity is selected. When parity is enabled and Bit 4 = 1, even parity is selected.

Bit 5 When parity is enabled and Bit 5 = 1, a parity bit is transmitted and received in the opposite state from the state indicated by Bit 4. Parity can therefore be forced to a known state and the receiver can check the parity bit in a known state.

Bit 6 When set to 1, serial output is forced to the spacing (logic 0) state. The break is disabled when this bit is set to 0. Bit 6 acts only on serial output and has no effect on the transmitting logic. Bit 6 enables the CPU to alert a terminal in a computer system. If the following sequence is used, erroneous or extraneous characters are not transmitted because of the break.

1. Load an all zeros pad character in response to Line Status register Bit 5.

2. Set break in response to the next Line Status register Bit 5.

3. Wait for the transmitter to become idle (Line Status register Bit 6), and clear break when normal transmission must be restored.

Bit 7 Must be set high to access the Divisor latches DLL and DLM of the Baud rate generator during a read or write operation. This bit must be input low to access the Receiver buffer, the Transmitter holding, or the Interrupt enable registers.

The **Line Status Register** is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of the serial port interface. Refer to Table 4 for bit definitions.

Table 4 Line Status Register

Bit	Function	Logic 1	Logic 0
0	Data ready	Ready	Not ready
1	Overrun error	Error	No error
2	Parity error	Error	No error
3	Framing error	Error	No error
4	Break interrupt Break	No break	
5	Transmitter holding register empty	Empty	Not empty
6	Transmitter empty	Empty	Not empty
7	Not used		

Bit 0 Indicates that the Receiver Buffer register has been loaded with a received character (including Break) and that the CPU can access this data. This bit is set high when an incoming character is received and transferred into the Receiver Buffer register. When the CPU reads the data in the Receiver Buffer register, Bit 0 is reset low.

Bits 1-4 are the error conditions that produce a Receiver Line Status interrupt (priority 1 interrupt in the Interrupt Identification register). This interrupt is enabled by setting the Interrupt Enable register Bit 2 to 1.

Bits 1-4 are cleared when the Line Status register is read.

Bits 1-3 Three error flags provide the status of an error condition detected in the receiver circuitry: Overrun error, Framing error, and Parity error. Error flags are set high by an error condition when stop bits are received. The absence of an error condition in the next character received does not reset the error flags. The flags reflect the last character only if no overrun occurred.

Bit 1 Overrun error means that the Receiver Buffer register was not read by the CPU before the next character was transferred into the Receiver Buffer register, overwriting the previous character. This bit is reset when the CPU reads the contents of the Line Status register.

Bit 2 A parity error means that the last character received had a parity error based on the programmed and calculated parity of the received character (Line Control register Bit 4). This bit is set high when a parity error is detected, and reset low when the CPU reads the contents of the Line Status register.

Bit 3 A framing error means that the last character received had incorrect (low) stop bits (caused when the required stop bit is absent or by a stop bit too short to be detected). This bit is high when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). This bit is reset low when the CPU reads the contents of the Line Status register.

Bit 4 This bit indicates that the last character received was a break character. A break character is defined as an invalid but complete data character, including parity and stop bits. This bit is set high when the received data input is held in the spacing (logic 0) state for a longer time than a full word transmission time (start bit + data bits + parity + stop bits). Bit 4 is reset when the CPU reads the contents of the Line Status register.

Bit 5 This bit indicates that the Transmitter Holding register is empty and can receive another character. If the interrupt is enabled (Interrupt Enable register Bit 1), this bit when active causes an interrupt. The interrupt is cleared when the Interrupt Identification register is read.

Bit 5 is set high when a character is transferred from the Transmitter Holding register into the Transmitter Shift register. This bit is reset low when the CPU loads the Transmitter Holding register. Bit 5 is NOT reset when the CPU reads the Line Status register.

Bit 6 This bit is set high when the Transmitter Holding register and the Transmitter Shift register are both empty. When a character is loaded into the Transmitter Holding register, this bit is set low and remains low until the character is transferred out of SOUT (Serial output pin). Bit 6 is NOT reset when the CPU reads the Line Status register.

Bit 7 This bit is always zero.

The **Modem Control Register** controls the interface with the modem or data set. This register can be read or written. The $\overline{RTS}$ and $\overline{DTR}$ outputs are by the respective control bits in this register. A high input asserts a low at the output pins. Table 5 contains Modem Control register bit definitions.

Table 5 Modem Control Register

Bit	Function
0	Data terminal ready (DTR)
1	Request to send (RTS)
2	0
3	Interrupt enable
4	Loop
5	0
6	0
7	0

Bit 0 When set to 1, the Data terminal ready output is forced to a logic 0. When this bit is reset to a logic 0, the Data terminal ready output is forced to a logic 1.

Bit 1 When set to 1, the Request to send output is forced to a logic 0. When this bit is reset to a logic 0, the Request to send output is forced to a logic 1.

Bit 3 When set high, INT output is enabled.

Bit 4 This bit provides a local loopback feature to perform diagnostic testing of the channel. When set high, SOUT is set to the marking state (logic 1), and the receiver data input Serial Input (SIN) is disconnected. The output of the Transmitter Shift register is looped back into the Receiver Shift register input. The three modem control inputs are disconnected. Modem control outputs are connected to the four modem control inputs internally. Modem control output pins are forced to the high (inactive state).

In the diagnostic mode, data transmitted is received immediately so the processor can verify the transmit and receive data paths of the selected serial port.

Bits 5-7 Permanently set to logic 0.

The **Modem Status Register** provides the CPU with the status of the modem input lines from the modem or peripheral devices. The CPU can read the serial port modem signal inputs by accessing the data bus interface of the MCS16C451. Four bits in this register indicate if the modem inputs have changed since the last read of the Modem status register. These bits are set high when a control input from the modem changes state. When the CPU reads the Modem Status register, these bits are reset low.

The $\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$ and $\overline{DCD}$ signals are the modem input lines for the channel. Bits 4 through 7 are status indications of these lines. If the modem status interrupt in the Interrupt Enable register Bit 3 is enabled, a change of state in a modem input signals is reflected by the modem status bits in the IIR register and an interrupt is generated. The Modem Status register is a priority 4 interrupt. Refer to Table 6 for bit definitions. Note that the state of the status bit is an inverted version of the actual input pin.

Table 6 Modem Status Register

Bit	Function
0	Delta clear to send
1	Delta data set ready
2	Trailing edge of ring indicator
3	Delta data carrier detect
4	Clear to send
5	Data set ready
6	Ring indicator
7	Data carrier detect

Bit 0 Indicates that Bit 4 input to the serial port interface has changed state since the last time it was read by the CPU.

Bit 1 Indicates that Bit 5 input to the serial port interface has changed state since the last time it was read by the CPU.

Bit 2 Indicates that Bit 6 input to the serial port interface has changed state since the last time it was read by the CPU. Low to high transitions on Bit 6 do not activate this bit.

Bit 3 Indicates that Bit 7 input to the serial port interface has changed state since the last time it was read by the CPU.

Bit 4 This bit is the status of clear-to-send input from the modem. This input tells the serial port that the modem is ready to receive data from he transmitter output of the serial port. If the serial port interface is in loop mode (Modem Control register Bit 4 = 1), this bit is equivalent to Modem Control register Bit 1 (request to send).

Bit 5 This bit is the status of the data-set-ready input from the modem to the serial port. This input tells the CPU that the modem is ready to provide received data to the serial port receiver circuitry. If the channel is in loop mode (Modem Control register Bit 4 = 1), this bit is equivalent to Modem Control register Bit (data terminal ready).

Bit 6 Indicates the status of the $\overline{RI}$ pin. If the channel is in loop mode (Modem Control register Bit 4 = 1), this bit is not connected in the Modem Control register.

Bit 7 Indicates the status of receiver line detect signal input.

Modem status inputs reflect the modem input lines with any change of status. Reading the Modem Status register clears the delta modem status indications but does not affect the status bits. The status bits reflect the state of the input pins regardless of mask control signals. If bits 0-3 are true, and a state change occurs during a read operation, the state change is no reflected in the Modem Status register. If bits 0-3 are false, the state change is indicated after the read.

Setting status bits is inhibited for the Line Status register and Modem Status register during status read operations. If a status condition is generated during a CPU read, the status bit is not set until the trailing edge of the read.

If a status bit is set during a read operation, and the same status condition occurs, that status bit is cleared at the trailing edge of the read instead of being set again.

The MCS16C451 serial port interface contains a programmable Baud Rate Generator that divides the clock from DC to 3.1 MHz. Any divisor from 1 to 2^{16-1} can be used. The output frequency of the baud generator is 16X the data rate [divisor # = clock + (baud rate x 16)]. The divisor is stored in a 16-bit binary format by two 8-bit divisor latch registers. These divisor latch registers must be loaded during initialization. A 16-bit baud counter is immediately loaded after either of the divisor latches is loaded to prevent long counts on initial load.

The MCS16C451 serial port receiver circuitry is programmable for 5, 6, 7 or 8 data bits per character. Word with less than eight bits are right justified, LSB = Data Bit 0, which is the first data bit received. Unused bits in a character less than eight bits are output low to the parallel output by the serial port.

Data received at the SIN (serial input) pin is shifted into the **Receiver Shift Register** by the clock (16X) provided at the XIN input. Based on the position of the start bit, this clock is synchronized to the incoming data. When a complete character is shifted into the Receiver Shift register, the assembled data bits are loaded in parallel into the **Receiver Buffer Register**. The Data Ready flag in the Line Status register is set.

The data received is buffered twice to permit continuous data reception without loss of data. As the Receiver Shift register is shifting a new character into the serial port, the Receiver Buffer register is holding a previously received character for the CPU. If data in the Receiver Buffer register is not read before complete reception of the next character, the data in the Receiver register goes low. The overrun condition is flagged by an Overrun error (Bit 1 of the Line Status register). Table 7 contains Receiver Buffer Register bit definitions.

Table 7 Receiver Buffer Register

Bit	Function
0	Data Bit 0
1	Data Bit 1
2	Data Bit 2
3	Data Bit 3
4	Data Bit 4
5	Data Bit 5
6	Data Bit 6
7	Data Bit 7

The Transmitter Holding Register holds parallel data from the data bus until the Transmitter Shift register is empty and ready to accept a new character. The receiver word length and transmitter and number of stop bit are the same. If the character has less than eight bits, unused bits are ignored by the transmitter at the microprocessor data bus. Table 8 contains the bit definitions of the Transmitter Holding register.

Table 8 Transmitter Holding Register

Bit	Function
0	Data Bit 0
1	Data Bit 1
2	Data Bit 2
3	Data Bit 3
4	Data Bit 4
5	Data Bit 5
6	Data Bit 6
7	Data Bit 7

Bit 0 The first serial data bit transmitted.

Bit 5 of the Line Status register reflects the status of the Transmitter Holding register. It shows if both the Transmitter Holding register and Transmitter shift register are empty.

The **Scratch Register** is an 8-bit Read/Write register. This register does not affect either channel in the **MCS16C451**. It is used by programmers to hold data temporarily. Table 9 contains bit definitions.

Table 9 Scratch Register

Bit	Function
0	Data Bit 0
1	Data Bit 1
2	Data Bit 2
3	Data Bit 3
4	Data Bit 4
5	Data Bit 5
6	Data Bit 6
7	Data Bit 7

The **Interrupt Identification Register** has the interrupt capability to interface to current microprocessors. The serial port interface prioritizes interrupts into four levels to minimize software overhead during data character transfer. The four levels of interrupt conditions include

Priority 1	Receiver Line Status
Priority 2	Received Data Ready
Priority 3	Transmitter Holding Register Empty
Priority 4	Modem Status

The Interrupt Identification register stores information that an interrupt is pending and the type of interrupt. When addressed during chip select time, this register indicates the highest priority interrupt pending. No other interrupts are acknowledged until the CPU services this interrupt. Table 10 contains Interrupt Identification register bit definitions. Table 11 contains IIR interrupt identification, set and reset information.

Table 10 Interrupt Identification Register

Bit	Function
0	Hardwired priority or polled environment
1-2	Identifies highest priority pending
3-7	0

Bit 0 Used as either a hardwired prioritized or polled environment. Indicates if an interrupt is pending. When this bit is low, an interrupt is pending and the register contents can be used as a pointer to the appropriate interrupt service routine. When this bit is high, no interrupt is pending.

Bits 1-2 Identify the highest priority interrupt pending.

Bits 3-7 Must be set to 0.

Table 11 IIR Interrupt ID, Set and Reset

Interrupt Identification				Interrupt Set and Reset Functions		
Bit2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
x	x	1		None	None	
1	1	0	1	Receiver line status	OE, PE FE, or BI	LSR Read
1	0	0	2	Received data available	Received data available	RBR Read
0	1	0	3	LSR(5)	LSR(5)	IIR Read if THRE is the interrupt source or THR write
0	0	0	4	Modem status	$\overline{CTS}$, $\overline{DSR}$. $\overline{RI}$, $\overline{RSLD}$	MSR Read

x = not defined

The **Interrupt Enable Register** is a write register that enables the four serial port interrupts independently. The interrupts activate the interrupt output. All interrupts are disabled by resetting Bits 0-3 of this register. Interrupts are enabled by setting the appropriate bits of this register high. When interrupts are disabled, the Interrupt Identification register and the active (high) INTR signal is inhibited. All other system functions operate normally, including the setting of the Line Status register and the Modem Status register. Table 12 contains Interrupt Enable register bit definitions.

Table 12 Interrupt Enable Register

Bit	Function
0	Received Data Available interrupt
1	Transmitter holding register empty interrupt
2	Receiver line status interrupt
3	Modem Status interrupt
4-7	Must be set to logic 0

Bit 0 Received Data Available interrupt.
1 = Enables
0 = Disables

Bit 1 Transmitter holding register empty interrupt.

1 = Enables
0 = Disables

Bit 2 Receiver line status interrupt.
1 = Enables
0 = Disables

Bit 3 Modem Status interrupt.
1 = Enables
0 = Disables

Bits 4-7 Must be set to logic 0.

Transmitting

The serial port interface transmitting function includes the Transmitter Holding register, Transmitter Shift register, and the associated control logic. Bits 5 and 6 in the Line Status Register indicate the status of the Transmitter Holding register and the Transmitter Shift register. To transmit a 5- to 8-bit word, the word is written to the Transmitter Holding register through D0-D7. The microprocessor performs a write operation only if it is transmitted.

When the transmitter is idle, Bit 5 of the Line Status register is high. This bit is set high when the word is automatically transferred from the Transmitter Holding register to the Transmitter Shift register when the start bit is transmitted.

When the transmitter is idle, Bits 5 and 6 of the Line Status register are high. The first word written causes Bit 5 to be reset to zero. After the transfer, Bit 5 return high. Bit 6 remains low while the data word is transmitted. If a second character is transmitted to the Transmitter Holding register, Bit 5 of the Line Status register is reset low. Because the data word cannot be transferred from the Transmitter Holding register to the Transmitter Shift register until its empty, Bit 5 of the Line Status register remains low until the word is completely transmitted. When the last word is transmitted out of the Transmitter Shift register, Bit 6 of the Line Status register is set high. Bit 5 of the Line Status register is set high one transfer time later.

Receiving

Serial asynchronous data is input into SIN (Serial Input pin). The idle state of the line providing the input into the SIN pin is high. Start bit detection circuitry continually searches for a high to low transition. When a transition is detected, a counter is reset. Count is the 16X clock to 7 1/2, which is the center of the start bit. If the SIN signal is still low at the mid-bit sample of the start bit, the start bit is considered valid. By verifying the start bit, the receiver is prevented from assembling a false data character caused by a low going noise spike on the Serial Input pin.

The Line Control register determines the number of data bits in a character, the number of stop bits, if parity is used, and the polarity of parity. The Line Status register provides status for the receiver to the Receiver Buffer register. The data received (indicated by Bit 0 of the Line Status register) is set high. The CPU reads the Receiver Buffer register through D0-D7. This read resets Bit 0 of the Line Status register. If D0-D7 are not read before a new character transfer from the Receiver Status register to the Receiver Buffer register, the overrun error status bit is set (Line Status register Bit 1). The parity check looks for even or odd parity on the parity bit which precedes the first stop bit. The parity error is set in Line Status register Bit 2 if an error is detected. If the stop bit is not high, a framing error is indicated by Line Status register Bit 3.

The center of the start bit is defined as clock count 7 1/2. If the data received by the Serial Input pin is a symmetrical square wave, the center of the data cells occurs within +/- 3.125% of the mid-point. This is a 46.875% error margin. The start bit can begin as much as one 16X clock cycle before it is detected.

Baud Rate Generator

The Baud Rate generator generates clocking for the UART function and provides standard

ANSI/CCITT bit rates. An external clock into CLK provides the oscillator driving the Baud Rate generator.

The Divisor Latch registers DLL and DLM, and external frequency determine the data rate. The bit rate is selected by programming the two divisor latches. When DLL is set to 1,and DLM is set to 0, the divisor divides by 1 (provides maximum baud rate for a given input frequency at the CLK input).

The Baud Rate generator can use three different frequencies, 1.8432 MHz, 2.4576 MHz, or 3.072 MHz, to provide standard baud rates. With these frequencies, standard bit rates from 50 to 38.5 kbps are available. Refer to Tables 13, 14, and 15 standard baud rates with these frequencies.

Table 13 Baud Rates for 1.8432 MHz Clock

Baud Rate	Divisor	Percent Error
50	2304	-
75	1536	-
110	1047	0.026
134.5	857	0.058
150	768	-
300	384	-
600	192	-
1200	96	-
1800	64	-
2000	58	0.69
2400	48	-
3600	32	-
4800	24	-
7200	16	-
9600	12	-
19200	6	-
38400	3	-
56000	2	2.86

Table 14 Baud Rates for 2.4576 MHz Clock

Baud Rate	Divisor	Percent Error
50	3072	-
75	2048	-
110	1396	0.026
134.5	1142	0.0007
150	1024	-
300	512	-
600	256	-
1200	128	-
1800	85	0.392
2000	77	0.260
2400	64	-
3600	43	0.775
4800	32	-
7200	21	1.587
9600	16	-
19200	8	-
38400	4	-

Table 15 Baud Rates for 3.072 MHz Clock

Baud Rate	Divisor	Percent Error
50	3840	-
75	2560	-
110	1745	0.026
134.5	1428	0.034
150	1280	-
300	640	-
600	320	-
1200	160	-
1800	107	0.312
2000	96	-
2400	80	-
3600	53	0.628
4800	40	-
7200	27	1.23
9600	20	-
19200	10	-
38400	5	-

Resetting

The $\overline{\text{RESET}}$ input must be held low for 500 ns to reset the MCS16C451 circuits to an idle mode until initialization. A low state on the $\overline{\text{RESET}}$ signal causes the following events.

1. Initializes the transmitter and receiver internal clock counters.

2. Clears the Line Status register except Bits 5 and 6 which are set. Also clears the Modem Control register. All discrete lines, memory elements and logic associated with these registers are also cleared or turned off. The Line Control register, Divisor latches, Receiver Buffer register and Transmitter Buffer register are not affected.

After the rest condition is removed, the MCS16C451 remains idle until programmed. A hardware reset sets Bits 5 and 6 of the Line Status register. When interrupts are enabled, Bit 5 activates the interrupt. Refer to Table 16 for summary of reset effects.

Table 16 Reset Summary

Register/Signal	Reset Control	Reset
Interrupt Enable reg	Reset	All bits low (0-3 forced and 4-7 permanent)
Interrupt Identification reg	Reset	Bit 0 is high, Bits 1-2 low
Line Control reg	Reset	All bits low
Modem Control reg	Reset	All bits low
Line Status reg	Reset	Bits 0-4 and 7 are low, Bits 5-6 high
Modem Status reg	Reset	Bits 0-3 low, Bits 4-7 input signal
Serial Output (SOUT)	Reset	High
Interrupt (RCVR errors)	Read LSR/Reset	Low
Interrupt (RCVR data ready)	Read RBR/Reset	Low
Interrupt (LSR(5)	Read IIR/Write THR/Reset	Low
Interrupt (Modem Status changes	Read MSR/Reset	Low
$\overline{\text{OUT2}}$		Reset High
$\overline{\text{RTS}}$		Reset High
$\overline{\text{DTR}}$		Reset High
$\overline{\text{OUT1}}$		Reset High

Programming

Each serial port is programmed by the following control registers:

- Bit Rate Select Register DLL (Division Latch LSB)
- Bit Rate Select Register DLM (Division Latch MSB)
- Line Control Register
- Interrupt Enable Register
- Modem Control Register

The control word define the character length, number of stop bits, parity, baud rate and modem interface. The control register can be written in any order, but the IER must be written last because it controls interrupt enables. After the serial port is programmed and operational, these registers can be updated whenever the serial port is NOT transmitting or receiving data.

Software Reset

A software reset returns the serial port to a completely known state without performing a system reset. A software reset is accomplished by writing to the Line Control register, Divisor latches, and Modem Control register. The Line Status register and Receiver Buffer register must be read before enabling interrupts to clear out residual data or status bits which can be invalid for subsequent operations.

Parallel Port Interface

The MCS16C451 parallel port interface provides compatibility for the device and a Centronics type printer. When the $\overline{CS2}$ signal is low, the parallel port is selected. Table 17 lists the registers associated with the parallel port interface.

The microprocessor reads information on the parallel bus through Read Data register. The read and write functions of a register are controlled by the state of the read pin ($\overline{IOR}$) and write pin ($\overline{IOW}$).

The microprocessor reads the status of the printer in the five most significant bits of the Read Status register. Table 18 contains the bit definitions for this register.

Table 17 Parallel Port Interface Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Read Status	$\overline{BUSY}$	$\overline{ACK}$	PE	SLCT	$\overline{ERROR}$	1	1	1
Read Control	1	1	1	IRQENB	SLIN	$\overline{INIT}$	AUTOFD	STROBE
Write Control	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Write Control	1	1	1	IRQENB	SLIN	$\overline{INIT}$	AUTOFD	STROBE

Table 18 Read Status Register

Bit	Function
0	1
1	1
2	1
3	Error
4	Printer select
5	Paper Empty
6	Acknowledge (handshake function)
7	Printer busy

The Read Control Register is for reading the state of the control lines. The Write Control Register sets the state of the control lines. Table 19 contains the bit definitions for the Write Control Register.

Table 19 Write Control Register

Bit	Function
0	Strobe to inform the printer of the presence of a valid byte on the parallel bus
1	Autofeed the paper
2	Initialize the printer
3	Select IN
4	Interrupt enable
5	Must be set to 1
6	Must be set to 1
7	Must be set to 1

The Microprocessor can write a byte to the parallel bus through the Write Data Register.

Decoder

The parallel port address decoder selects registers according to the states of the signals listed in Table 20.

Table 20 Address Decoder Register Selection

Control Signals					
$\overline{IOR}$	$\overline{IOW}$	$\overline{CSPA}$	A1	A0	Register Selected
0	1	0	0	0	Read Data register
0	1	0	0	1	Read Status register
0	1	0	1	0	Read Control register
0	1	0	1	1	Invalid
1	0	0	0	0	Write Data register
1	0	0	0	1	Invalid
1	0	0	1	0	Write Control register
1	0	0	1	1	Invalid

Interrupt Control Logic

The serial and parallel ports generate their own interrupts to the CPU. The $\overline{IRQ5}$ or $\overline{IRQ7}$ signal from the parallel port controls the parallel port interrupt mechanism. The serial port generates the $\overline{IRQ3}$ or $\overline{IRQ4}$ signal for interrupt service.

The MCS16C451 supports PC/XT and AT systems with both parallel port and serial port interrupts. For the parallel port, interrupts are tristate outputs. For the serial port, interrupts are tristate outputs.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage	V_{CC}	3.0	7.0	V
Power Dissipation (@ 5.25 V)	W_d	—	1	W
Supply Current (@ 5.25 V)	I_{DD}	20	50	mA
Standby Current	I_{DDSB}	—	100	μA
Input Voltage	V_I	0.0	5.5	V
Output Voltage	V_O	0.0	5.5	V
Operating Temperature	T_{op}	0	70	°C
Storage Temperature	T_{stg}	−50	150	°C
ESD	V_{esd}	3000	—	V

NOTE: Exposing the device to stress above these limits can cause permanent damage. The device is not meant to be oeprated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

DC CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = +5 V ±10%, Unless Otherwise Specified)

Parameter	Symbol	Min	Max	Unit
Input Low Voltage, V_{CC} = 5 V ±0.5 V	V_{IL}	—	0.8	V
Input High Voltage, V_{CC} = 5 V ±0.5 V	V_{IH}	2.0	—	V
Input Low Current, V_{in} = 0.0 V	I_{IL}	—	−10	μA
Input High Current, V_{in} = V_{CC}	I_{IH}	—	10	μA
Output Leakage Current, V_{CC} = 5 V ±0.5 V	I_{OZ}	—	±10	μA
Output Low Voltage, V_{CC} = 5 ±0.5 V	V_{OL}	—	0.4	V
Output High Voltage, V_{CC} = 5 ±0.5 V	V_{OH}	2.4	—	V

CAPACITANCE (T_A = +25°C, V_{CC} = 5 V)

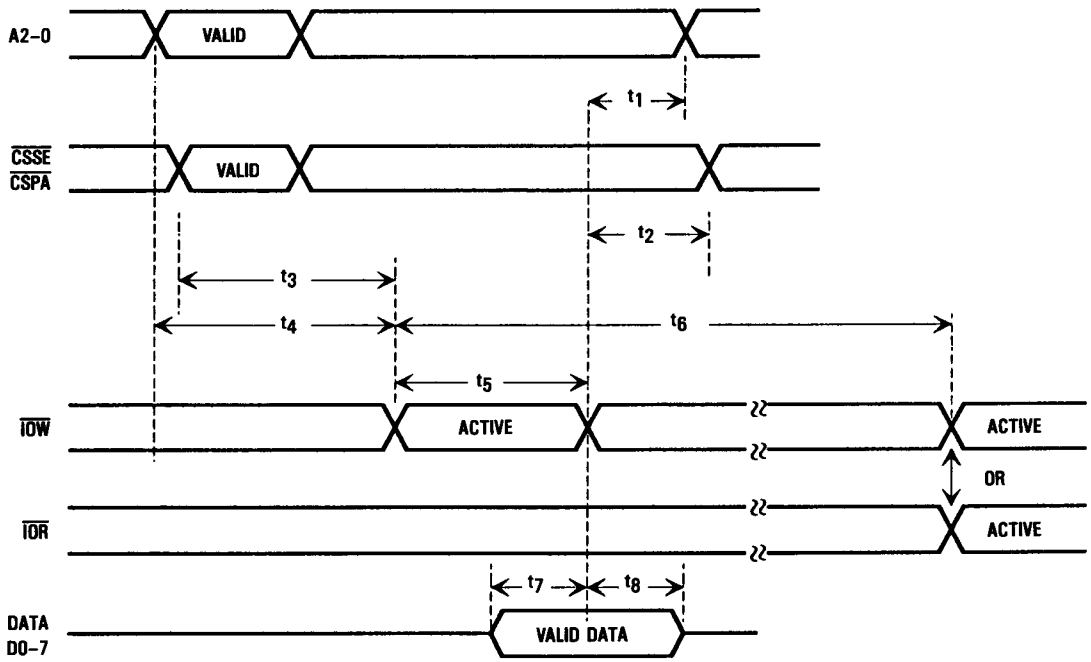
Parameter	Symbol	Min	Max	Unit
Input Capacitance, f_c = 1 MHz (Unmeasured Pins at GND)	C_I	—	10	pF
I/O Capacitance	C_{IO}	—	10	pF

AC CHARACTERISTICS

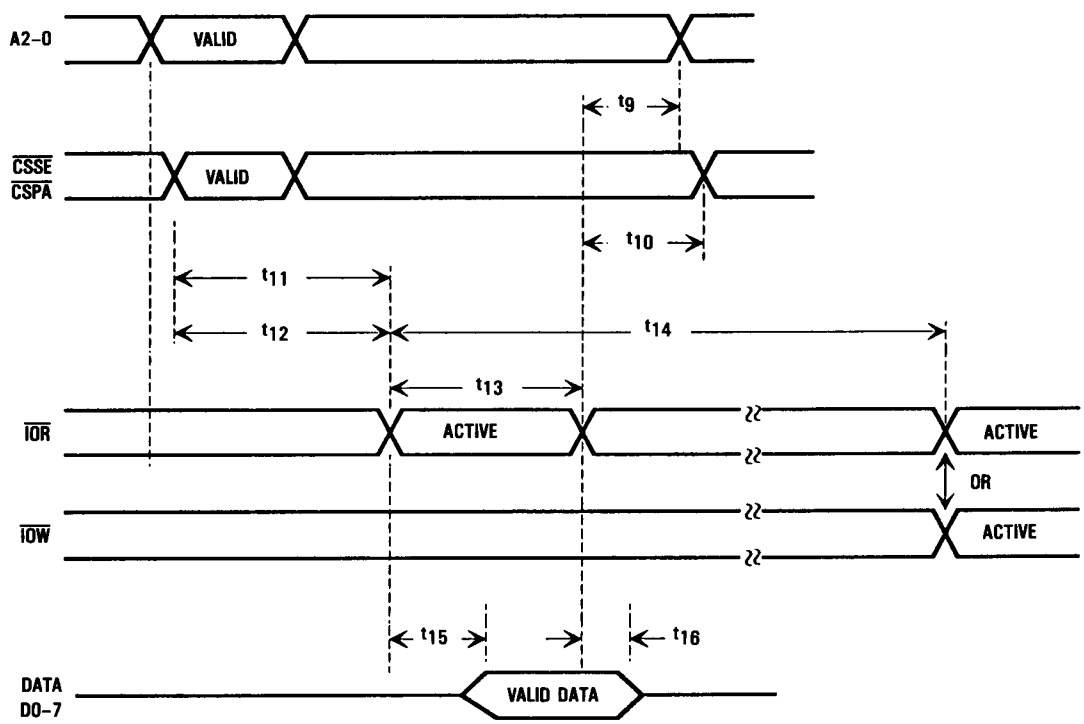
Parameter	Symbol	Min	Max	Unit
Address Hold Time from $\overline{IOW}$	t_1	20	—	ns
Chip Select Hold Time from $\overline{IOW}$	t_2	20	—	ns
$\overline{IOW}$ Delay from Select	t_3	50	—	ns
$\overline{IOW}$ Delay from Address	t_4	60	—	ns
$\overline{IOW}$ Strobe Width	t_5	100	—	ns
Write Cycle	t_6	360	—	ns
Data Setup Time	t_7	40	—	ns
Data Hold Time	t_8	40	—	ns
Address Hold Time from $\overline{IOR}$	t_9	20	—	ns
Chip select Hold Time from $\overline{IOR}$	t_{20}	20	—	ns
$\overline{IOR}$ Delay from Chip Select	t_{11}	50	—	ns
$\overline{IOR}$ Delay from Address	t_{12}	60	—	ns
$\overline{IOR}$ Strobe Width	t_{13}	125	—	ns
Read Cycle	t_{14}	360	—	ns
Serial Port Delay from $\overline{IOR}$ to Data (@ 100 pF Loading)	t_{15}	—	175	ns
Parallel Port Delay from $\overline{IOR}$ to Data (@100 pF Loading)		—	75	ns
Serial Port $\overline{IOR}$ to Floating Data Delay (@ 100 pF Loading)	t_{16}	0	100	ns
Parallel Port $\overline{IOR}$ to Floating Data Delay (@ 100 pF Loading)		0	35	ns
Delay from Stop to Set Interrupt (Receiver Clock Cycles)	t_{17}	—	1	
Delay from $\overline{IOR}$ (RD RBR or RD LSR) to Reset Interrupt (100 pF Load)	t_{18}	—	1	ns
Delay from Initial INTR Reset to Transmit Start (Baud Out Cycles)	t_{19}	24	40	
Delay from Stop to Interrupt (THRE) (Baud Out Cycles)	t_{20}	8	8	
Delay from $\overline{IOW}$ (WR THR) to Reset Interrupt (100 pF Load)	t_{21}	—	175	ns
Delay from Initial Write to Interrupt (Baud Out Cycles)	t_{22}	16	24	
Delay from $\overline{IOR}$ (RD IIR) to Reset Interrupt (THRE) (100 pF Load)	t_{23}	—	250	ns
Delay from $\overline{IOW}$ (WR MOR) to Output (100 pF Load)	t_{24}	—	200	ns
Delay to Set Interrupt from Modem Input (100 pF Load)	t_{25}	—	250	ns
Delay to Reset Interrupt from $\overline{IOR}$ (RD MSR) (100 pF Load)	t_{26}	—	250	ns
Parallel Port Delay of Valid Data from Parallel Port Data Register and Control Register to $\overline{IOW}$	t_{27}	—	45	ns
Parallel Port Delay from Interrupt to ACK	t_{28}	—	25	ns

TIMING DIAGRAMS

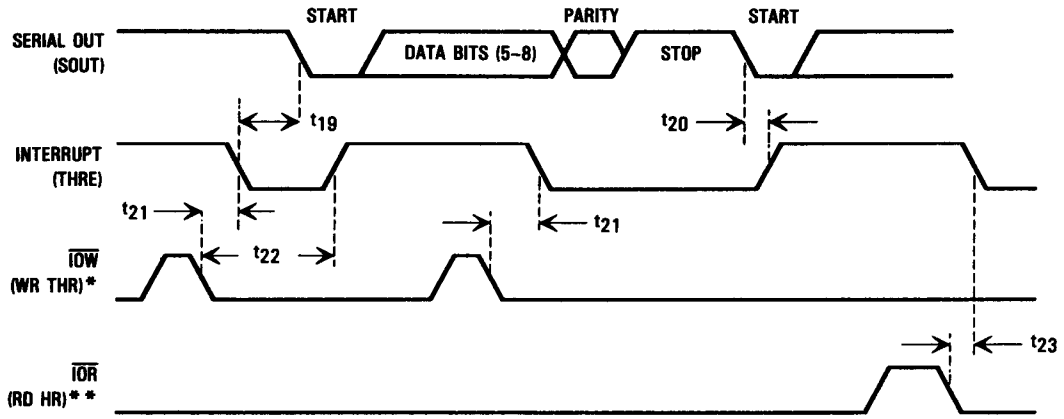
Write Cycle Timing



Read Cycle Timing

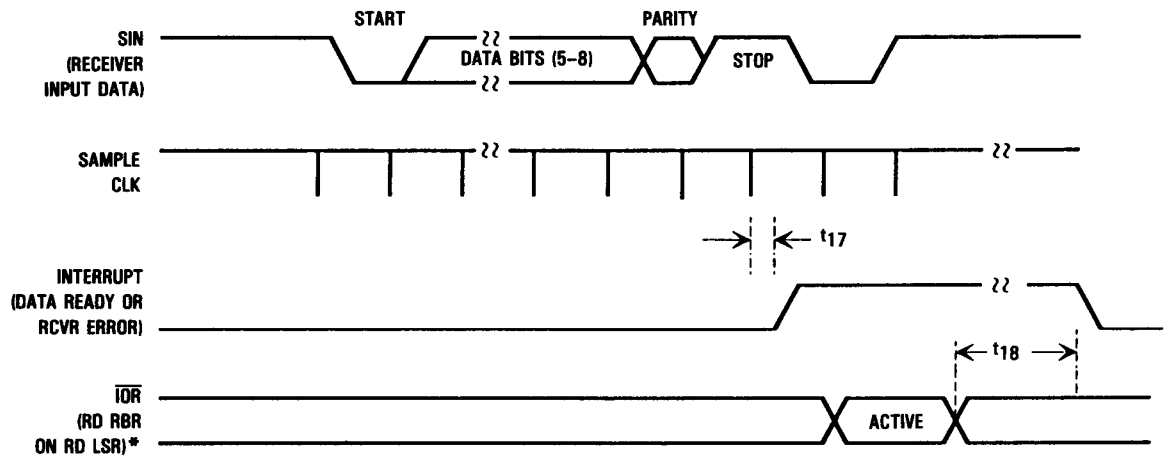


Transmitter Timing



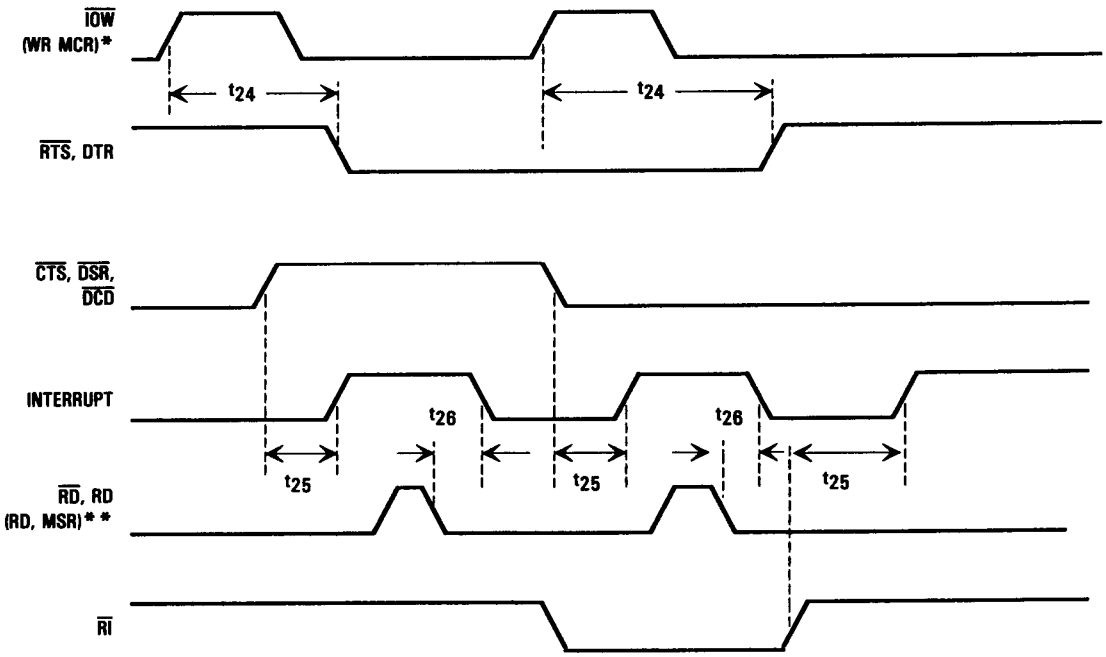
*See Write Cycle Timing.
**See Read Cycle Timing.

Receiver Timing



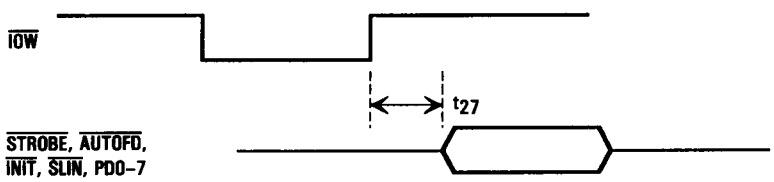
*See Read Cycle Timing.

Modem Controls Timing

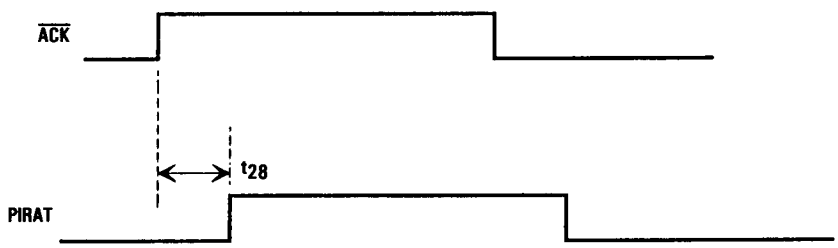


*See Write Cycle Timing.
**See Read Cycle Timing.

Parallel Port Data Register and Control Register Timing



Parallel Port Interrupt Timing



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