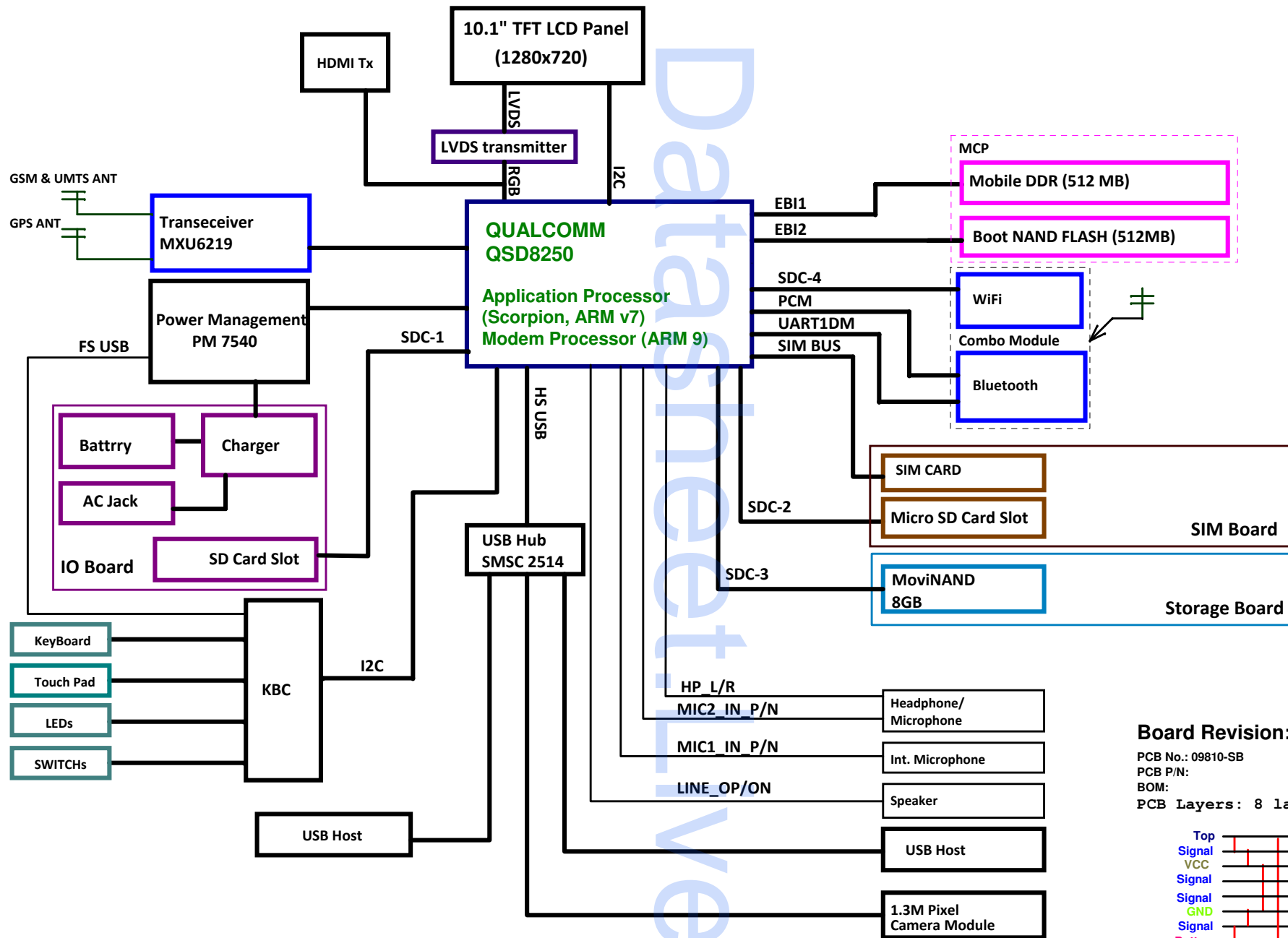
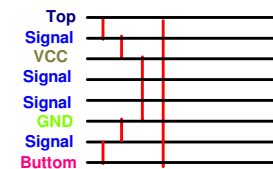


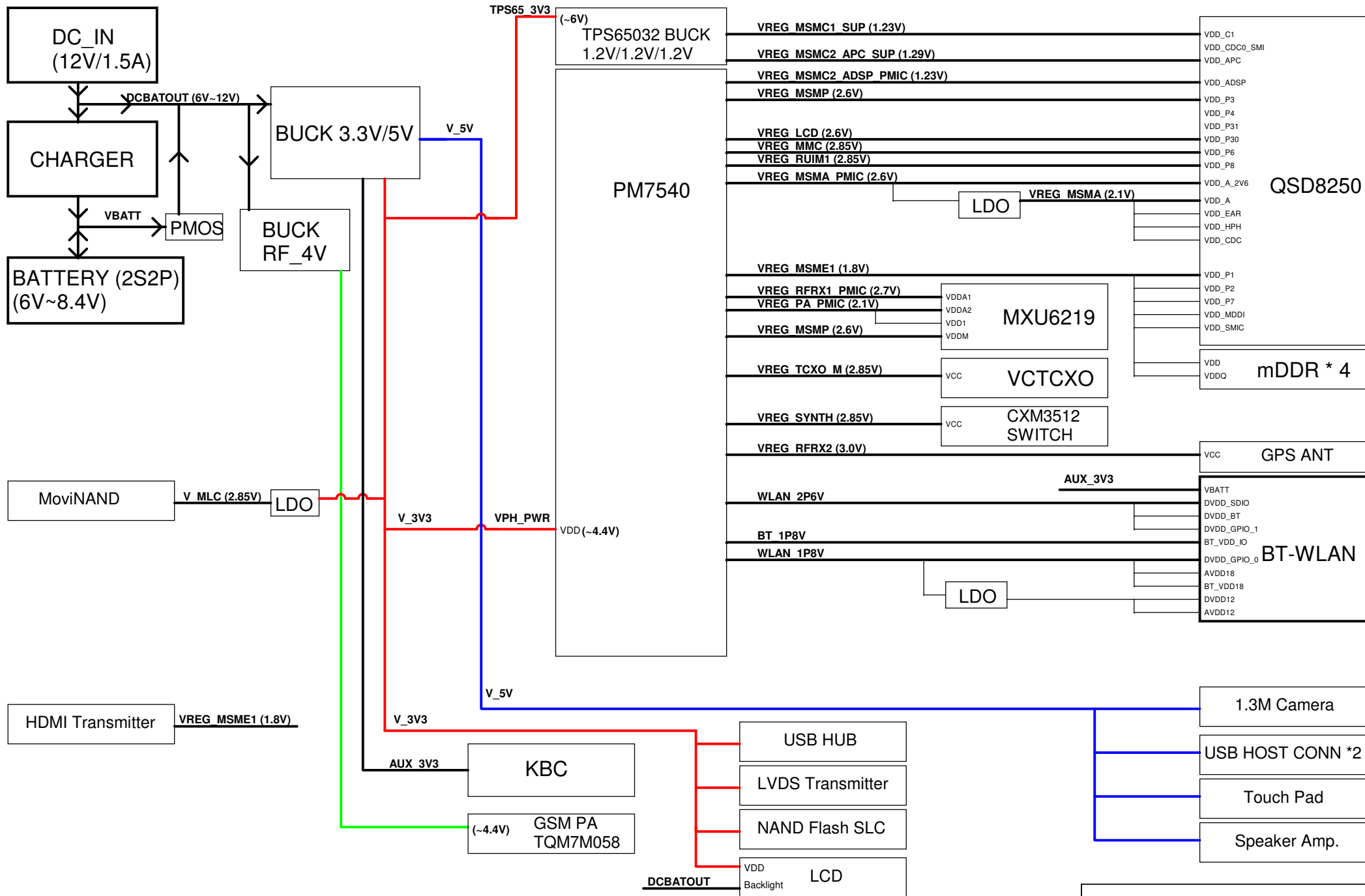
T-note System Block Diagram

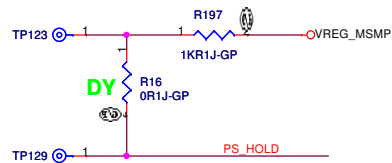
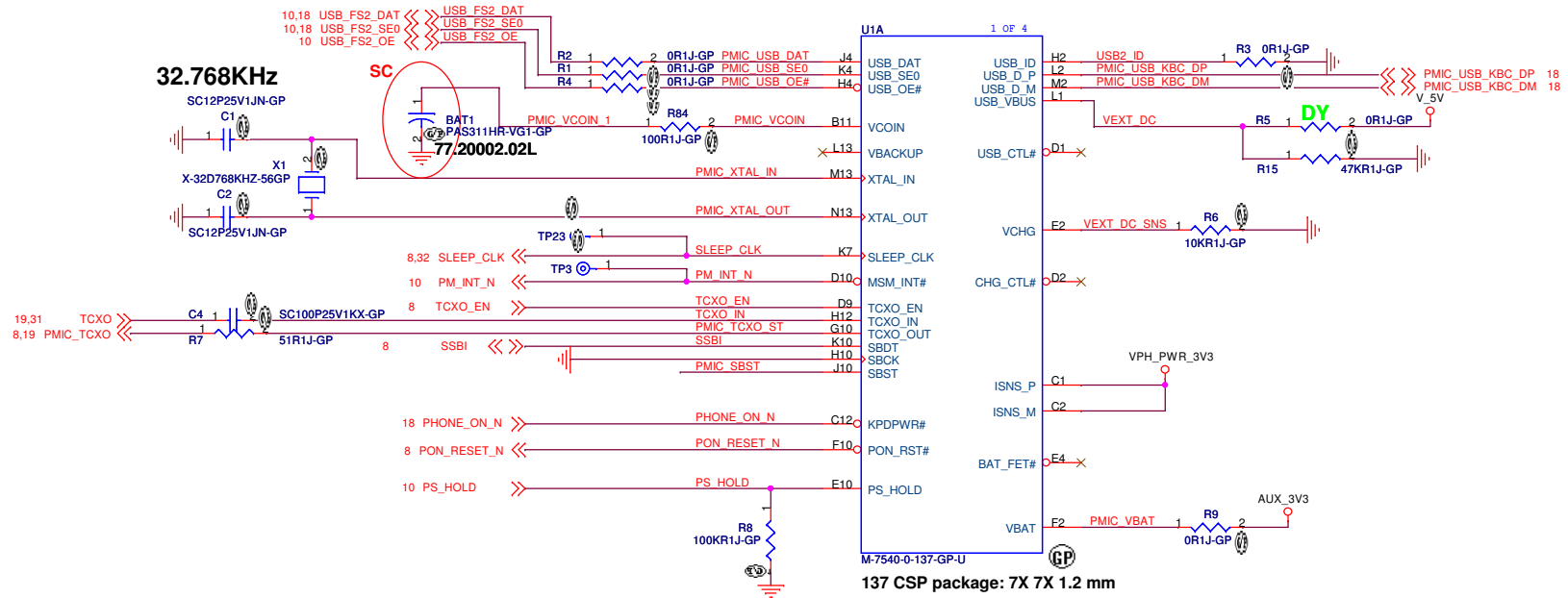


Board Revision:

PCB No.: 09810-SB
 PCB P/N:
 BOM:
 PCB Layers: 8 layers HDI



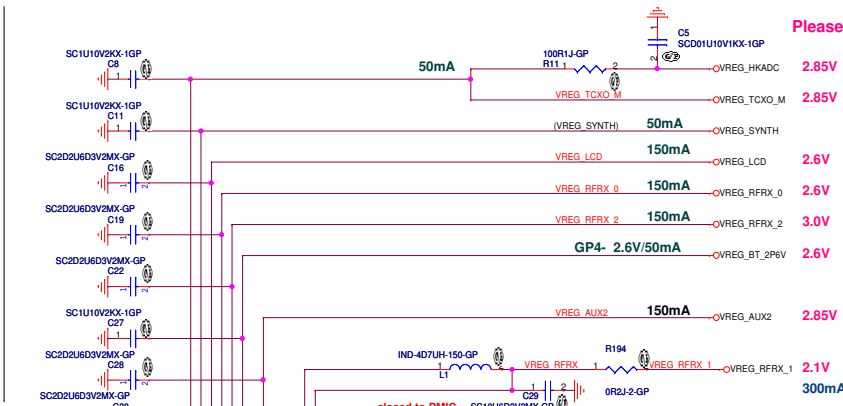
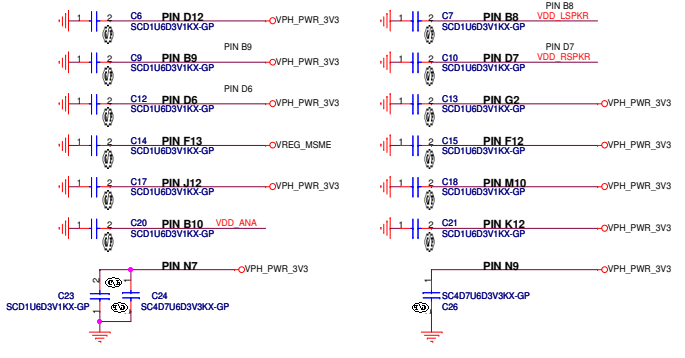




Put TP123 and TP129 out of shielding can
TP123 connect with TP129 at fixture side

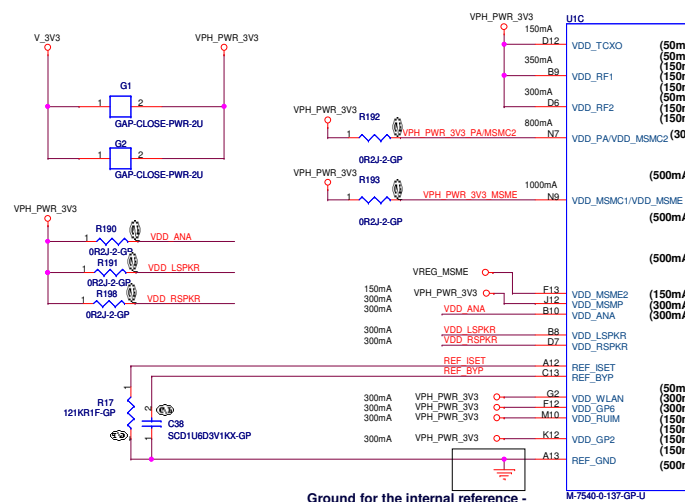
To configure PMIC for SSBI mode.
PMIC_SBST must be connected to VREG_MSMP
PMIC_SBCK must be connected to GND

Input Capacitors

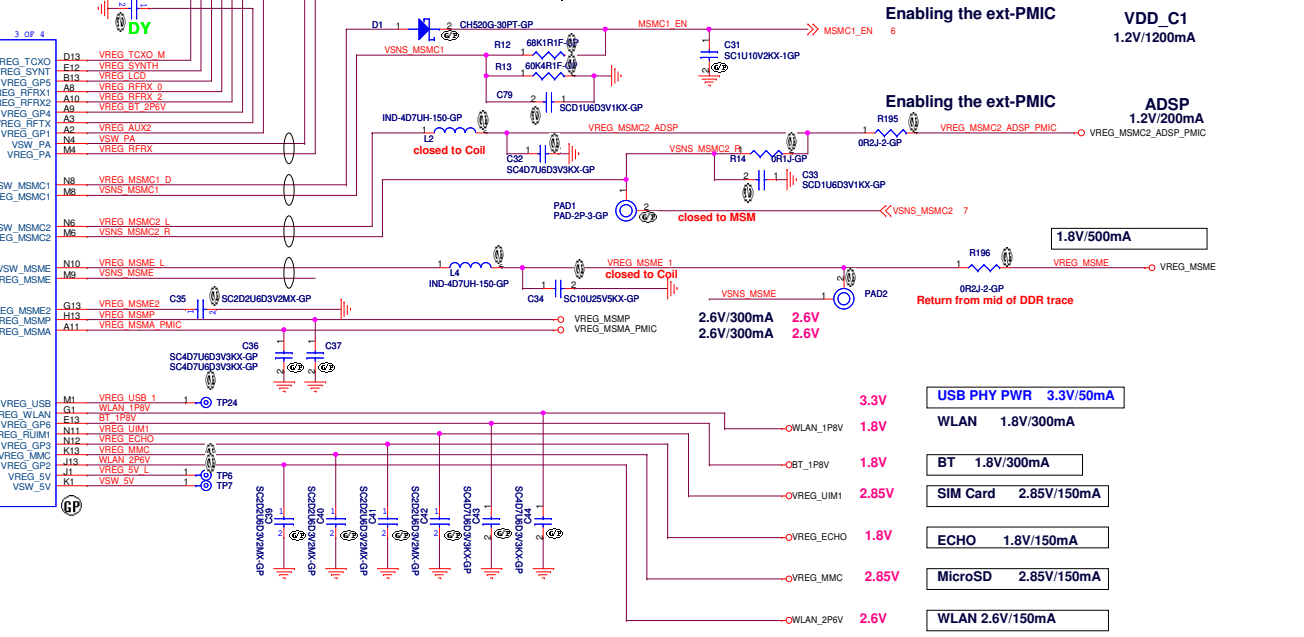


Please Refer to These Power Levels

QSD HKADC	2.85V	CDMA PA Min. Typ. Max. +3.2 +3.4 +4.2
RF	2.85V	
RF	2.6V	
LCD Interface	2.6V	GSM PA VBATT_A -> V_PA_BATT
RF	2.6V	
RF	3.0V	
BT_IO-2.6V	2.6V	EFuse blow
RF	2.85V	
RF	2.1V	



Ground for the internal reference - connect as directly as possible to the handset's reference ground.



VDD_C1	1.2V/1200mA
ADSP	1.2V/200mA
VREG_MSME	1.8V/500mA
USB PHY PWR	3.3V/50mA
WLAN	1.8V/300mA
BT	1.8V/300mA
SIM Card	2.85V/150mA
ECHO	1.8V/150mA
MicroSD	2.85V/150mA
WLAN	2.6V/150mA

Type/name	1	2	Default conditions	3	Voltage range	Intended use
SMPS - Boost	5 V (500 mA)	Off, 5,000 V			3.000 to 6.100 V	USB-OTG host, while LEDs, camera flash
SMPS - Buck						
MSMC1 (500 mA)	On, 1,200 V				0.750 to 3.050 V	MSM core #1; DVS available
MSMC2 (500 mA)	On, 1,200 V				0.750 to 3.050 V	MSM core #2; DVS available
MSME (500 mA)	On, 1,800 V				0.750 to 3.050 V	Devices on EBI #1 bus
PA (300 mA)	Off, 1,800 V				0.750 to 3.050 V	Power amplifier(s); DVS available
Linear - 300 mA						
MSMA 4	On, 2,600 V				1.500 to 3.050 V	MSM analog circuits
MSMP 6	On, 2,600 V				1.500 to 3.050 V	MSM pad voltage and other IC digital I/Os
WLAN	Off, 2,850 V				1.500 to 3.050 V	802.11 wireless LAN Bluetooth
GP6 (BT)	Off, 2,850 V				1.500 to 3.050 V	Bluetooth
Linear - 150mA						
MMIC	Off, 2,850 V				1.500 to 3.050 V	Mtimedia or SD circuits
MSME2	On, 1,500 V				0.750 to 1.525 V	Devices on EBI #2 bus
RFRX1	Off, 2,850 V				1.500 to 3.050 V	First of two RF receiver circuit supplies
RFRX2	Off, 2,850 V				1.500 to 3.050 V	Second of two RF receiver circuit supplies
RFTX	Off, 2,850 V				1.500 to 3.050 V	RF transmitter circuits
RUIM1	Off, 2,850 V				1.500 to 3.050 V	RUIM module #1
GP1 (CAM)	Off, 2,850 V				1.500 to 3.050 V	Camera circuits
GP2 (MD0)	Off, 2,850 V				1.500 to 3.050 V	MDDI circuits
GP3 (RUIM2)	Off, 2,850 V				1.500 to 3.050 V	RUIM module #2
GP5 (AUX2)	Off, 2,850 V				1.500 to 3.050 V	Auxiliary #2 analog circuits
Linear - 50 mA						
SVN1	Off, 2,850 V				1.500 to 3.050 V	Tx VCO and PLL circuits
TCXO	On, 2,850 V				1.500 to 3.050 V	VCCTXO and Rx VCO and PLL circuits
USB	Off, 3,300 V				3.000 V to 6.100 V	Internal USB transceiver; not used off-chip
GP4 (AUX1)	Off, 2,850 V				1.500 to 3.050 V	Auxiliary #1 analog circuits
Linear - MIC bias						
MIC bias	Off, 2,000 V				1.73, 1.80, 1.93, 2.00 V	Microphone bias

WLAN/BT Power
 1.2V : 1.2V +/-5% (ripple Vpp<10mV) 50mA
 1.8V : 1.8V +/-5% (ripple Vpp<10mV) 80mA
 VBATT : 3.2-4.2 (Recommend 3.3V-3.6V, ripple Vpp<10mV) 200mA
 SDIO & Interface : Need to meet SDIO High signal level & IO level of BT

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Title: **PM7540 (System Power)**

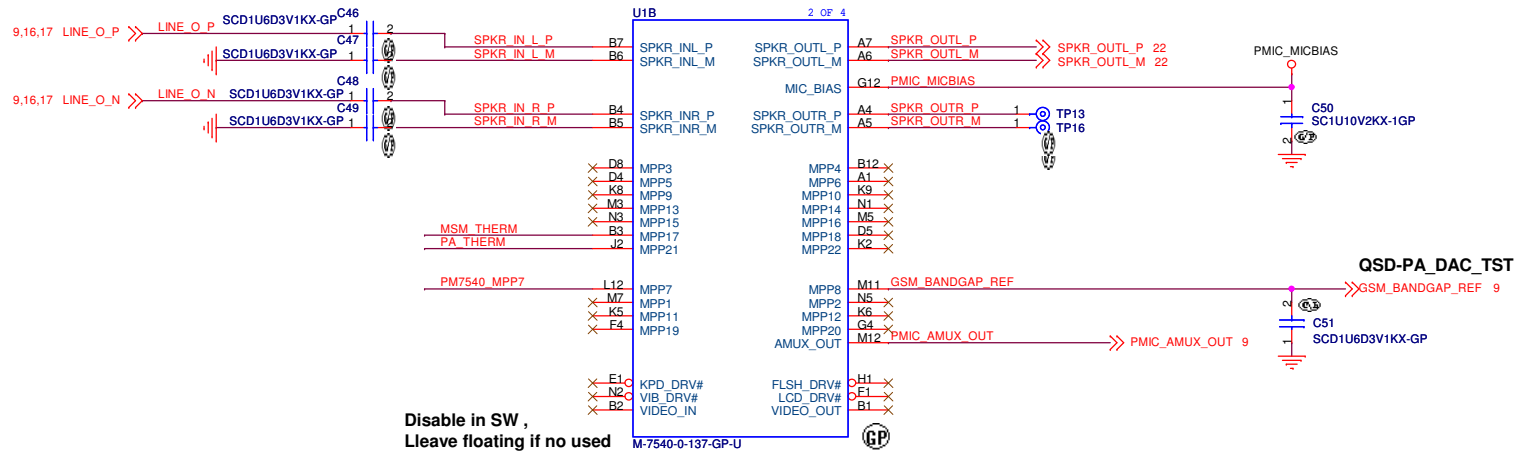
Size: C Document Number

Date: Tuesday, June 30, 2009

Sheet: 4 of 34

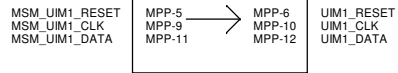
Rev: SC

PM7540 ADC/AMP



Disable in SW,
Leave floating if not used

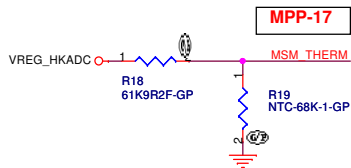
SIM Driver



MSM Side		RUIM side	
MPP-1	AMUX_IN1	MPP-2	AMUX_IN2
MPP-3	CBL0PWR_N	MPP-4	CBL1PWR_N
MPP-5	RUIM_M_RST	MPP-6	RUIM_RST
MPP-7	GP1_DRV_N	MPP-8	REF_OUT
MPP-9	RUIM_M_CLK	MPP-10	RUIM_CLK
MPP-11	RUIM_M_IO	MPP-12	RUIM_IO

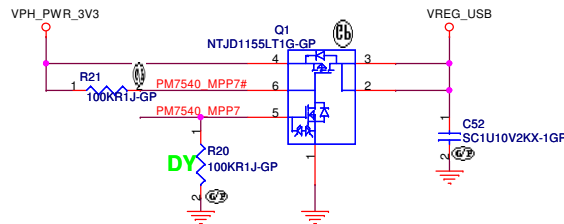
Pairs intend to be used as RUIM level translator:
MPP-5/6, MPP-9/10, MPP-11/12

MSM Thermistor

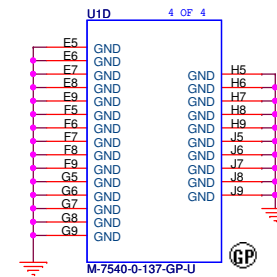


Note: Place close to MSM and SDRAM

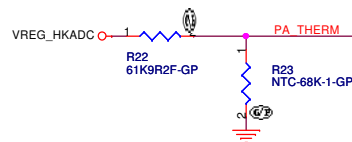
QSD8K USB PHY Power



PM7540 GND



PA Thermistor

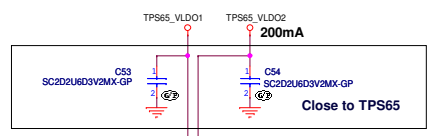
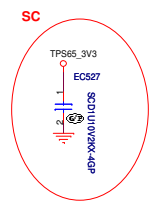
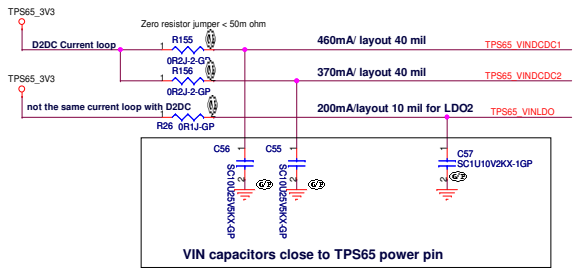


Note: Place close to PA

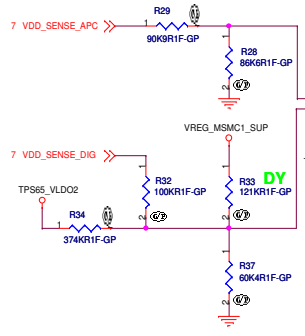
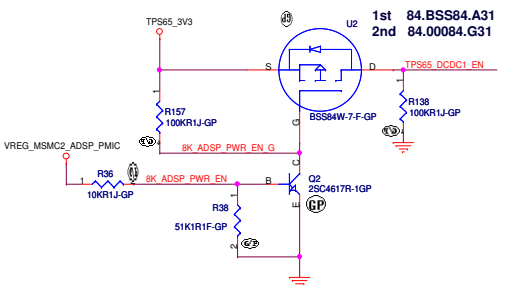
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
PM7540 (Audio, Power, MGT)	
Title Size A3	Document Number T-note
Date: Tuesday, June 30, 2009	Rev SC
Sheet 5 of 34	

ADSP Power

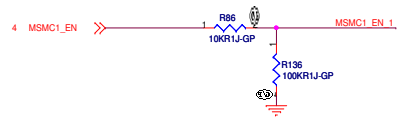
Digital Core Power



DCDC-1 : Enable Logic

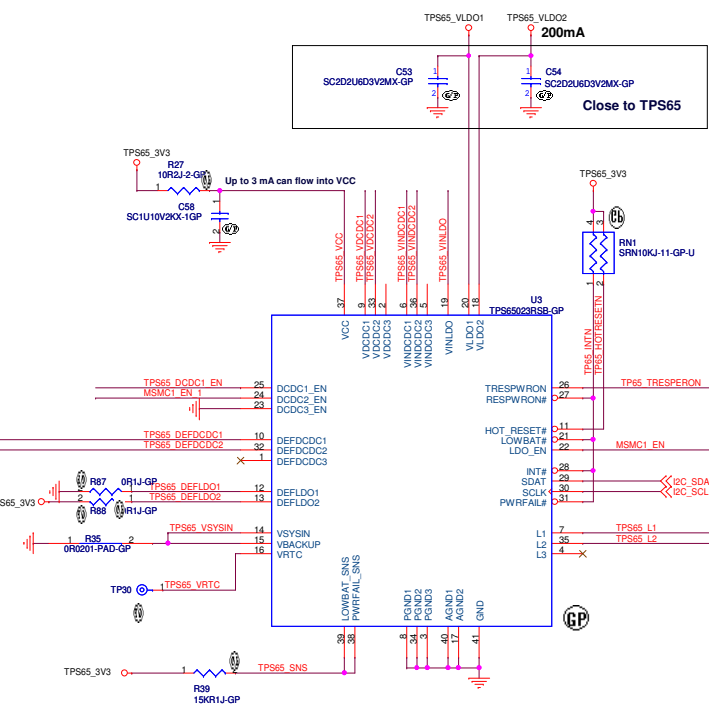
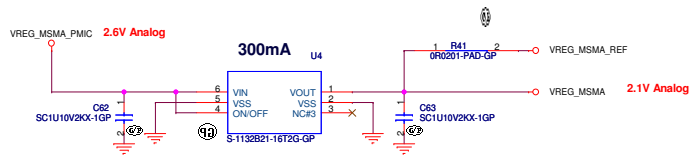


DCDC-2 : Enable



MSMA Power

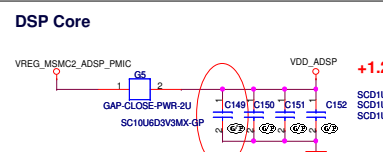
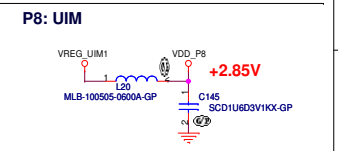
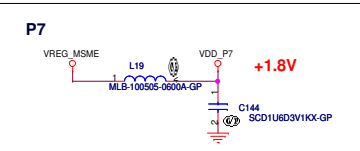
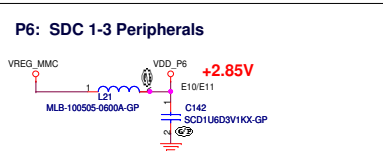
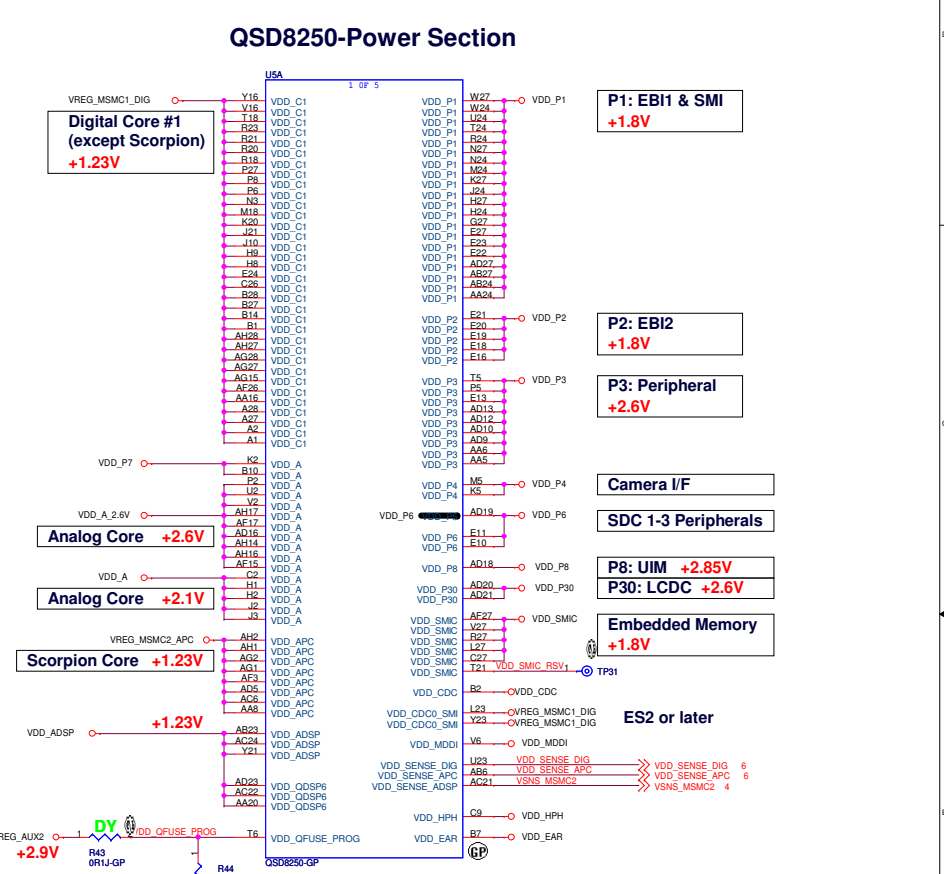
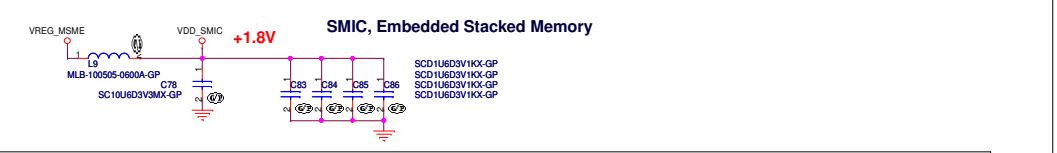
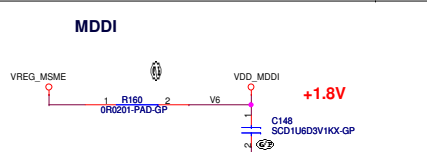
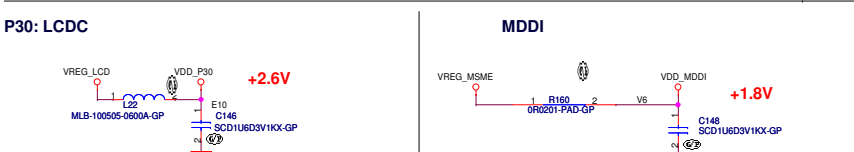
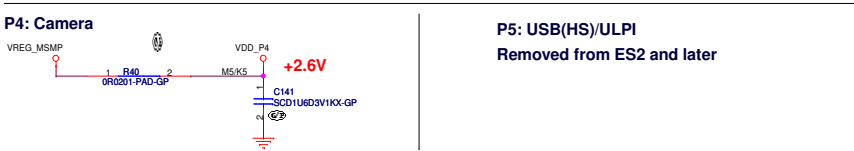
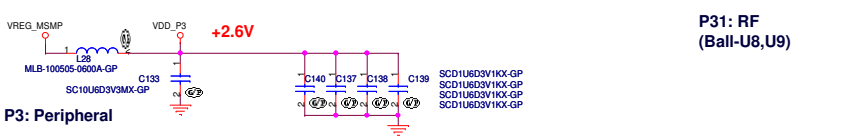
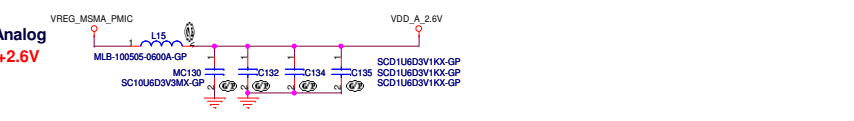
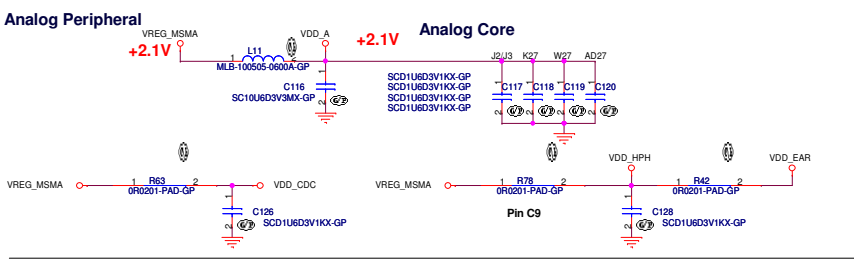
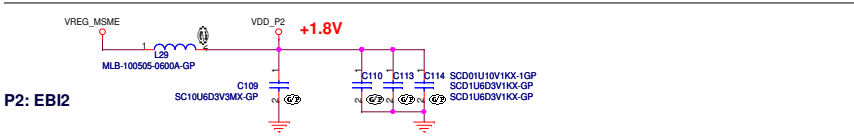
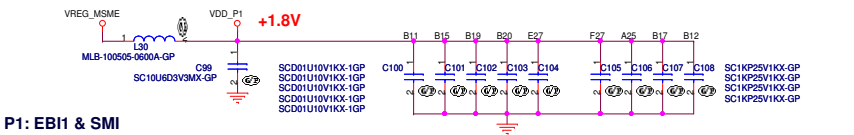
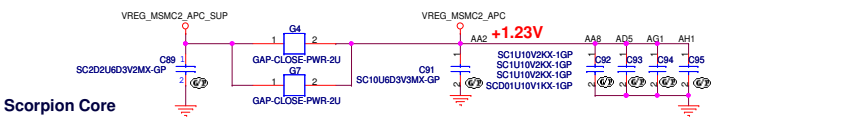
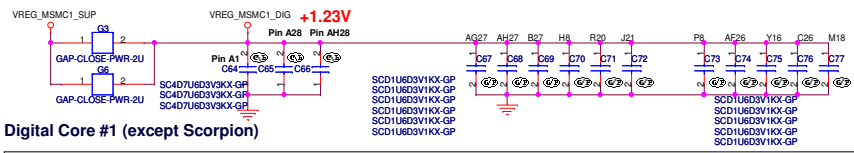
+2.1V (only for ES2 or later)



Voltage will strat at 1.225V. Need to program to desired value

APC Power (VDDAPC) 1.29V/1500mA

Digital Core Power (VDDC1) 1.2V/1200mA



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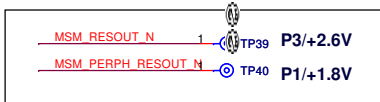
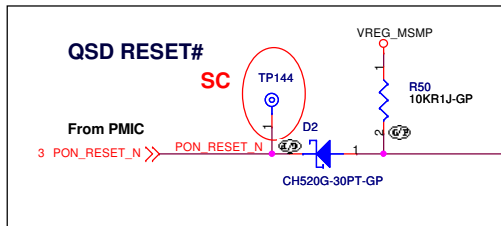
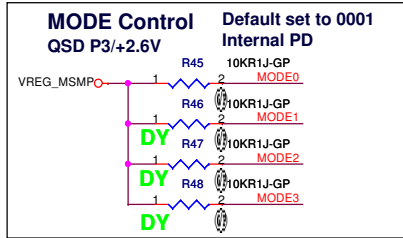
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Size: C Document Number

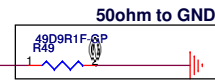
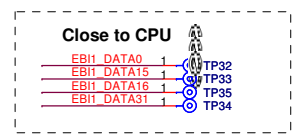
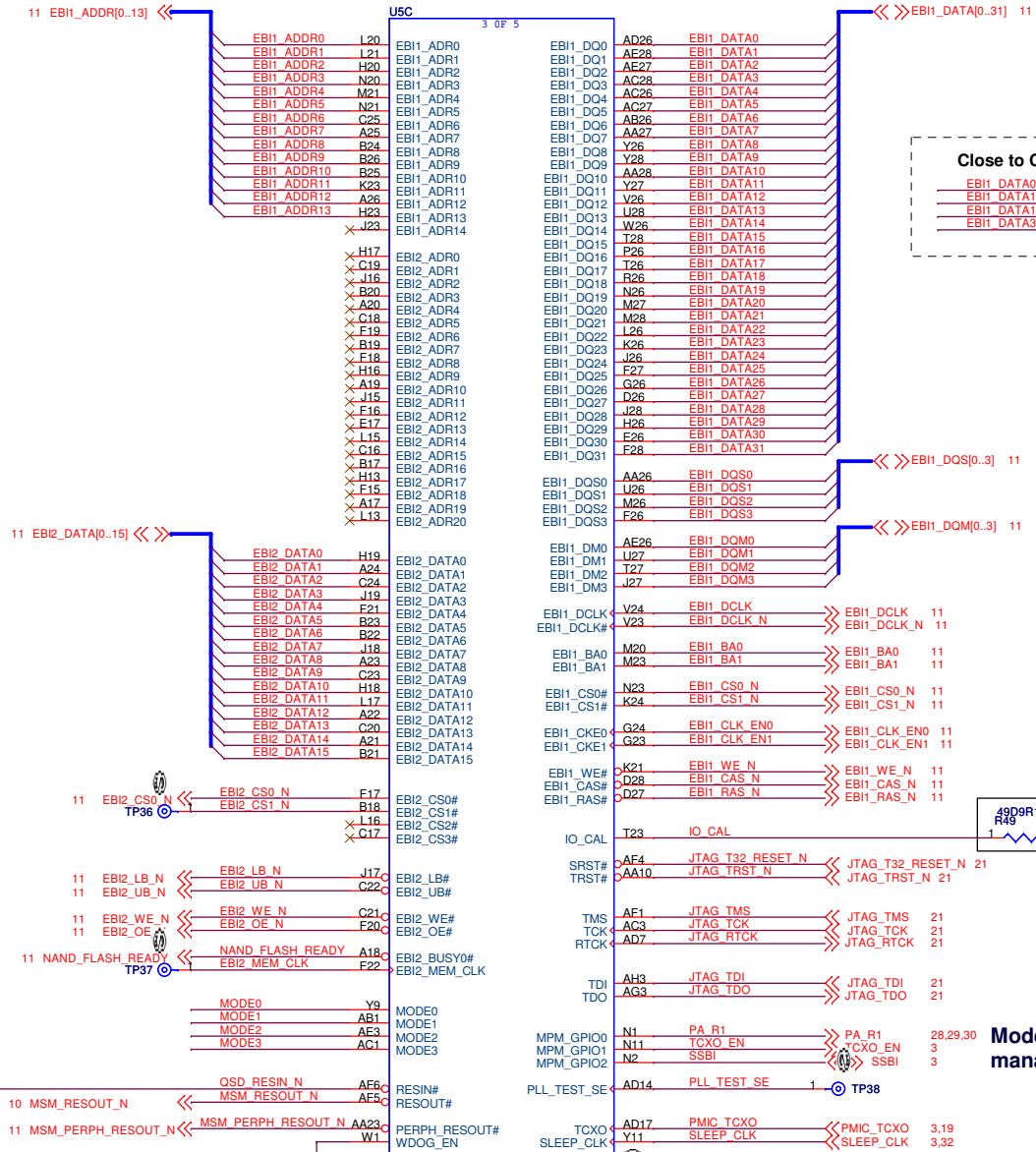
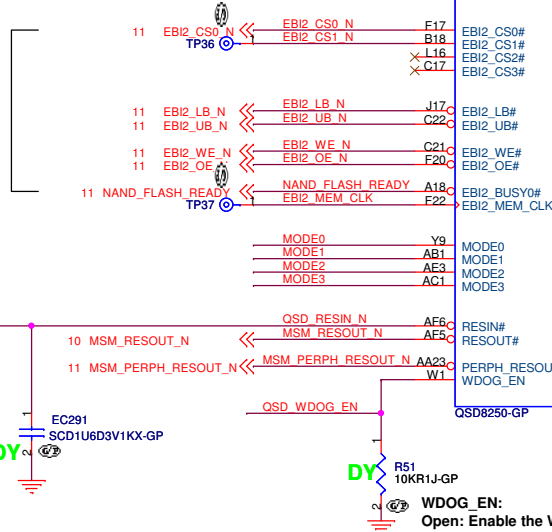
Date: Tuesday, June 30, 2009

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Rev: SC



NAND Flash Command



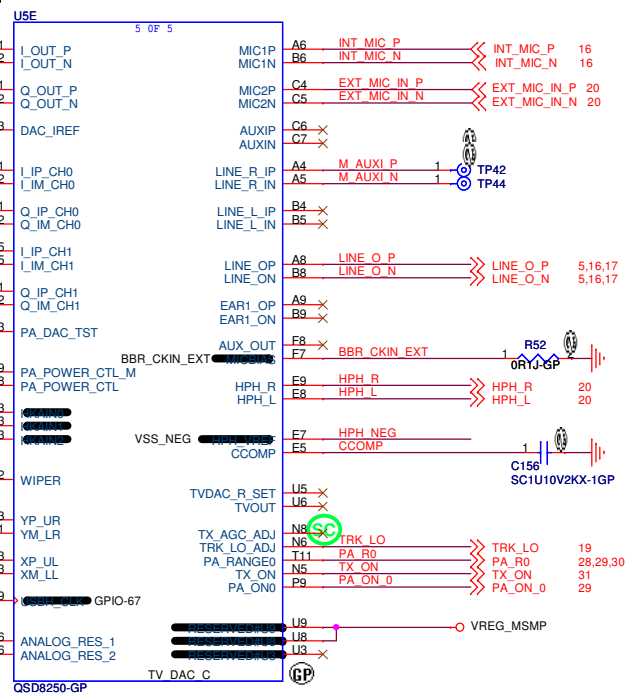
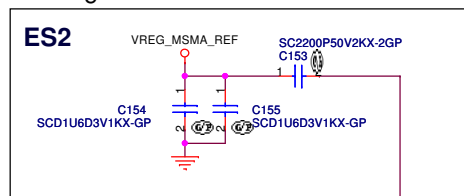
JTAG

Modem power manager

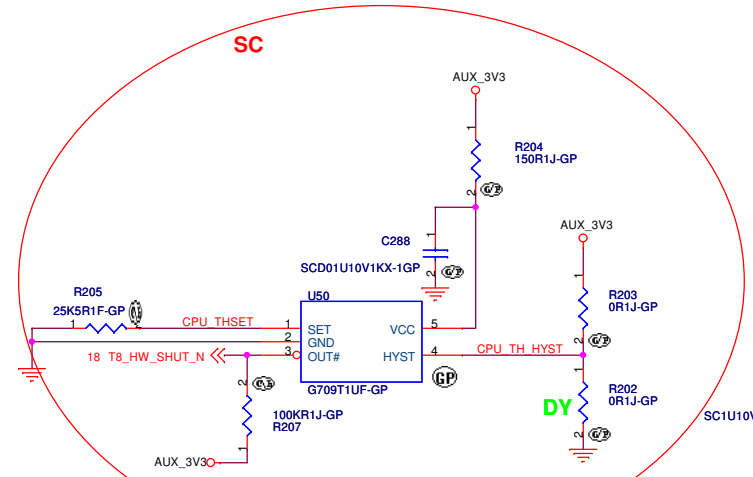
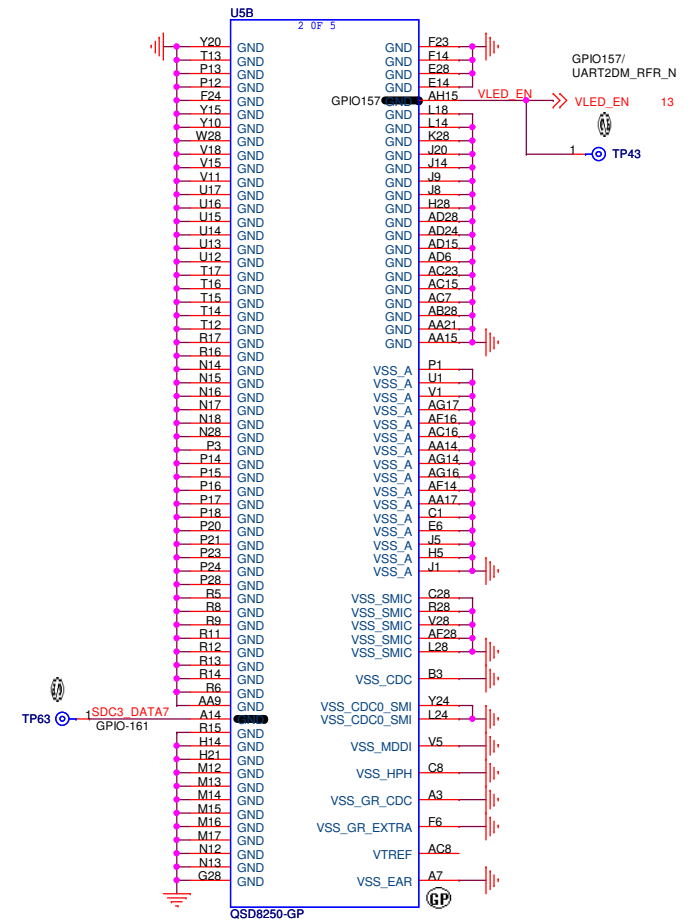
WDOG_EN:
Open: Enable the WDOG (internal pull up to VDD_P)
PD: Disable the WDOG

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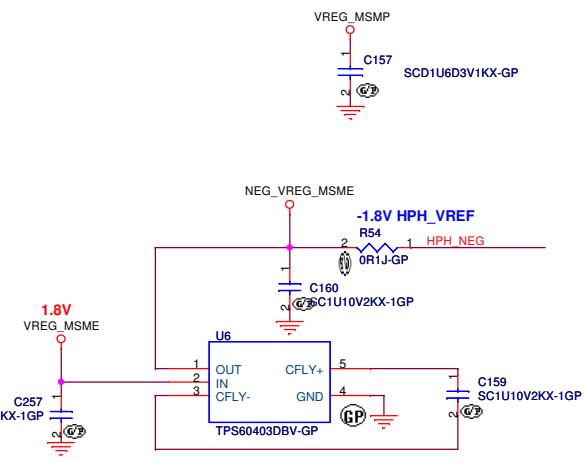
Title		QSD8250 (EBI-1/2)	
Size	Document Number	Rev	
A3	T-note	SC	
Date:	Tuesday, June 30, 2009	Sheet	8 of 34



QSD8250-GND Section



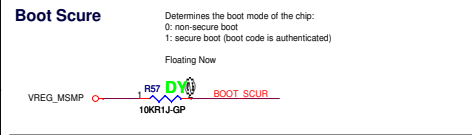
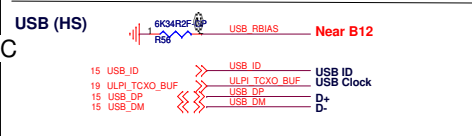
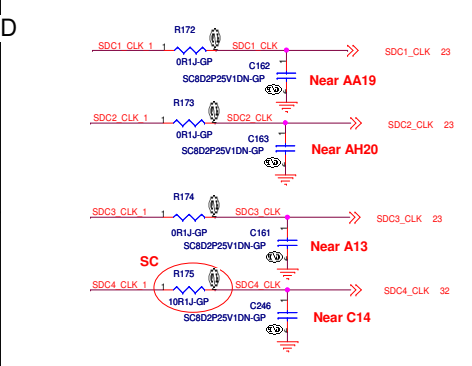
P31: RF (Ball-U8,U9)



QSD (GPIO, MDDI)

QSD 8650 71.Q8650.00U
QSD 8250 71.Q8250.00U

SDC



WakeUP and Higher Voltage GPIO
ES2 GPIO # 21, 24, 28, 35, 36, 37, 38, 39, 40, 41, 42, 45, 49, 51, 53, 64, 66, 68, 69, 83, 86, 90, 92, 94, 139, 141, 145, 152, 153



TPS65023
The TPS65023 has a 7-bit address: 1001000, other addresses are available upon contact with the factory.

HDMI Transmitter
The SDA/SCL programming address is 0x72 or 0x7A based on whether the PD/AD pin is pulled high (I2C address = 0x7A) or pulled low (I2C address = 0x72). The ADV7520 Programming Guide provides the information necessary for programming the transmitter.

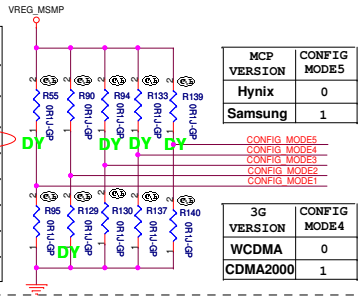
HW MB VERSION

default is INPUT P/L

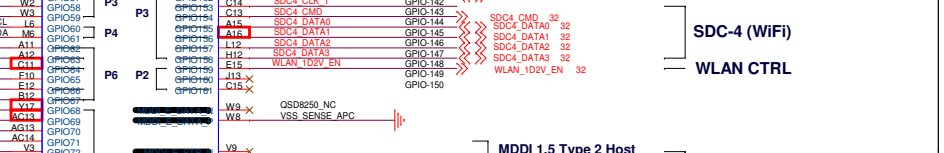
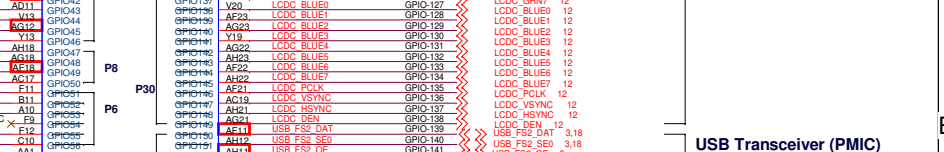
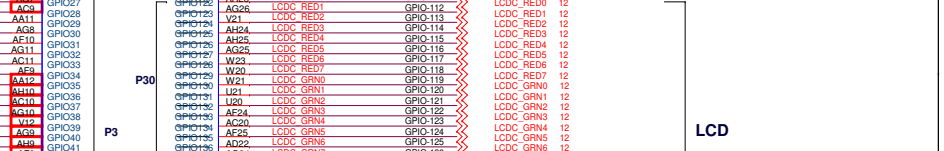
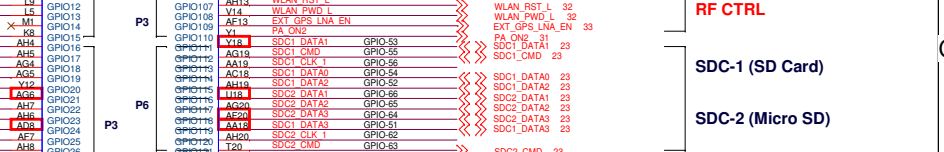
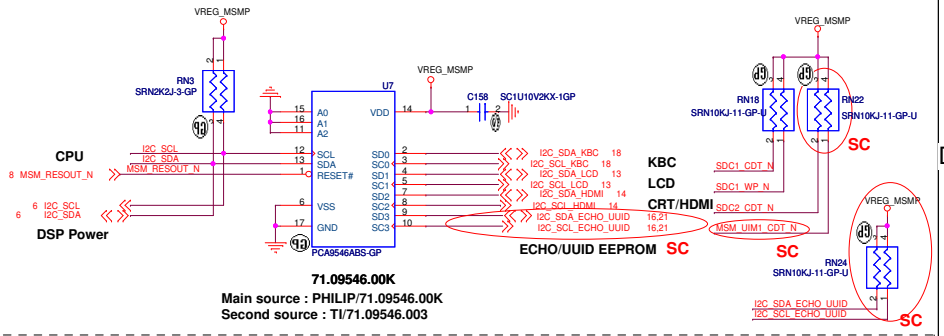
MB VERSION	CONFIG MODE1	CONFIG MODE2	CONFIG MODE3
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SB	0	0	1
SC	0	1	0
-1	0	1	1
-2	1	0	0
-3	1	0	1
-4	1	1	0
-5	1	1	1

MCP VERSION	CONFIG MODE5
Hynix	0
Samsung	1

3G VERSION	CONFIG MODE4
WCDMA	0
CDMA2000	1



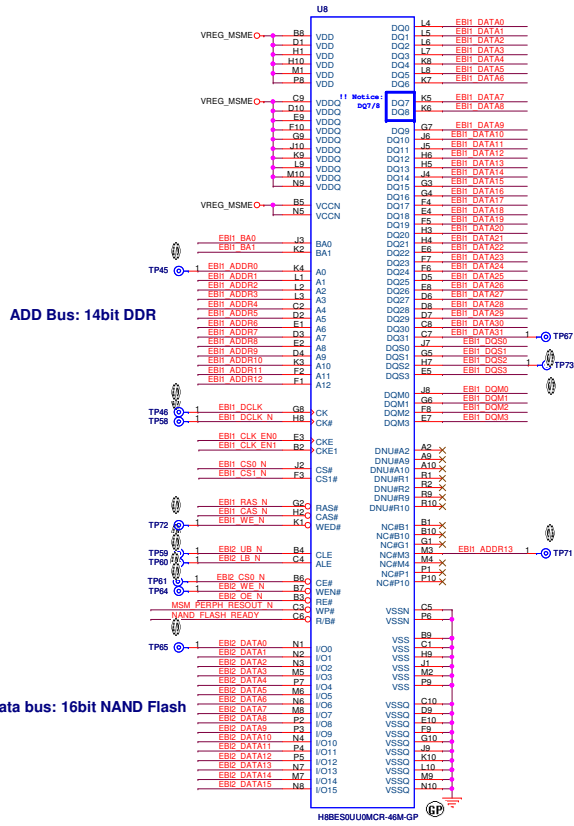
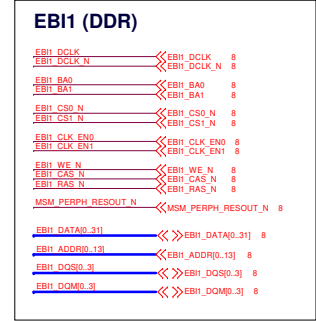
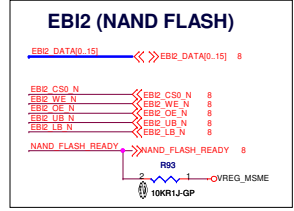
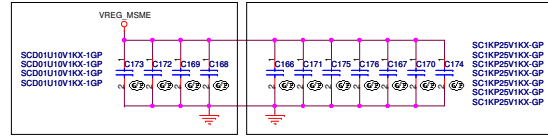
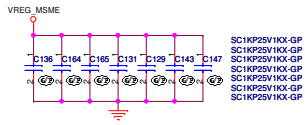
I2C Level Shifter



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Title	QSD8250 (GPIO)	Rev	SC
Size	Document Number	T-Note	
Customer			
Date	Tuesday, June 30, 2009	Sheet	10 of 34

Memory MCP DDR SDRAM & NAND Flash



Data Bus: 32bit DDR

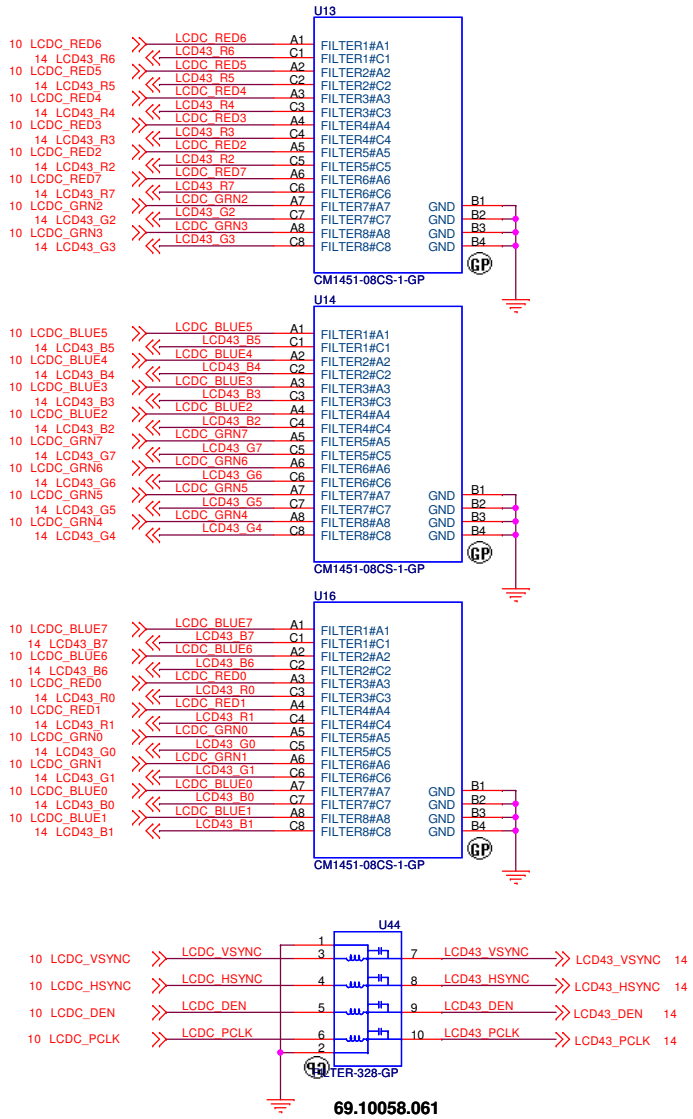
ADD Bus: 14bit DDR

Data bus: 16bit NAND Flash

P/N: 72.H8BES.B0U
Hynix H8BES00UMCR-46M-GP (MCP4G+4G)
4Gb (256Mb x16) NAND Flash
+ 4Gb (64Mb x32 2/CS 2KE) mobile DDR

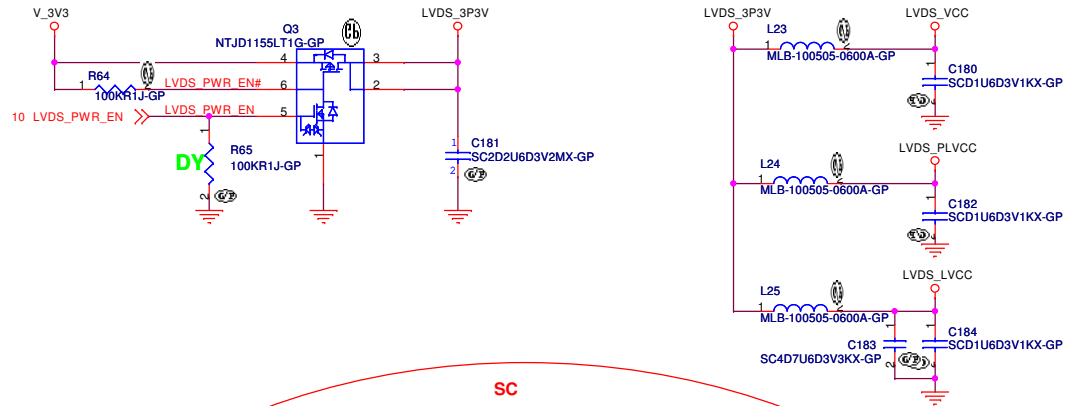
LCD I/F FILTER

(Close to CPU)

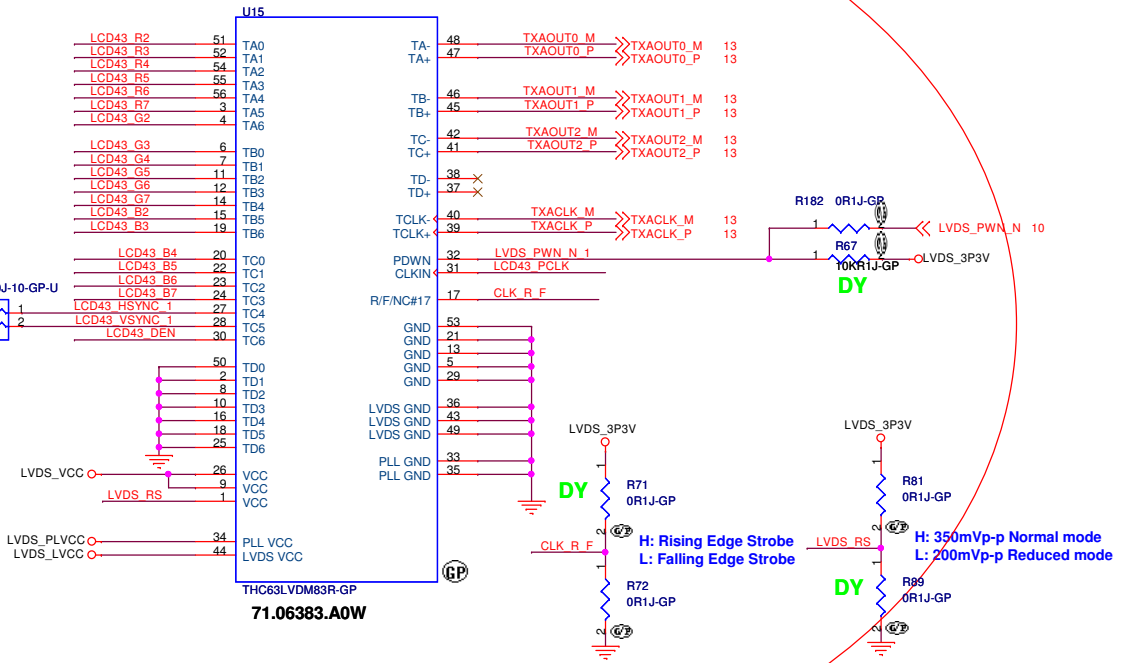


LVDS Transmitter

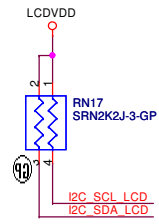
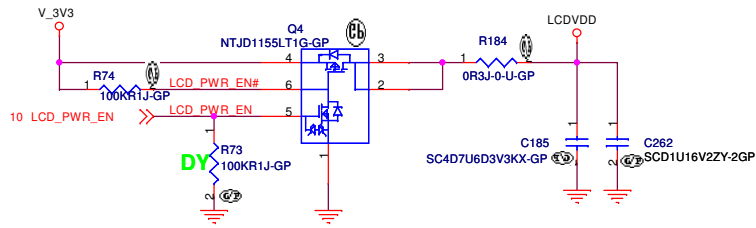
3.3V Power Switch for LVDS Transmitter (3.3V/50mA)



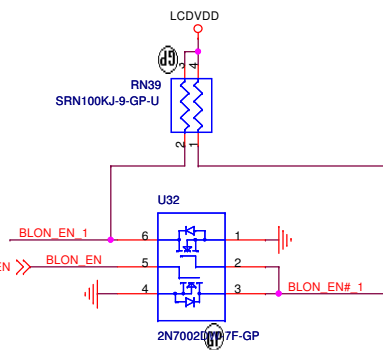
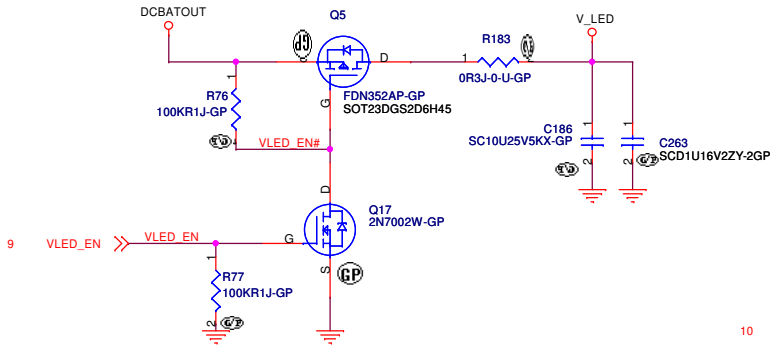
Change to THC63LVDM83R-GP



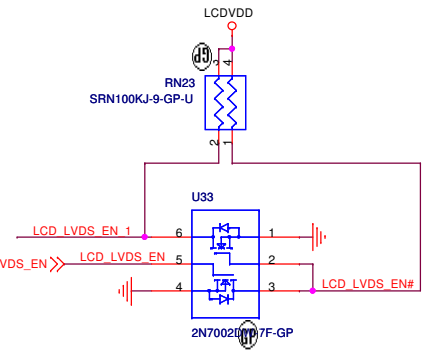
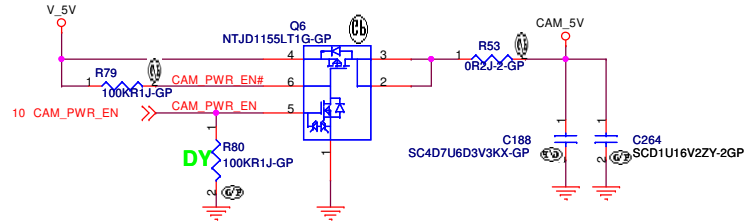
3.3V for LCD Panel (3.3V/210mA)



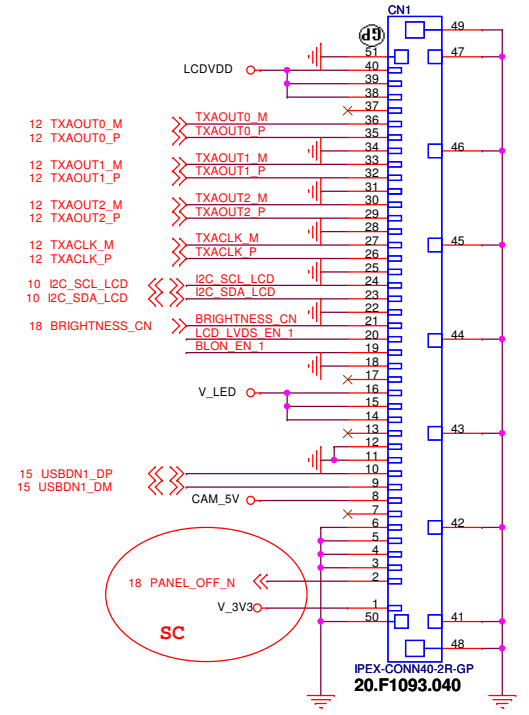
DCBATOUT for LCD Backlight (6V~12V/333mA~167mA)



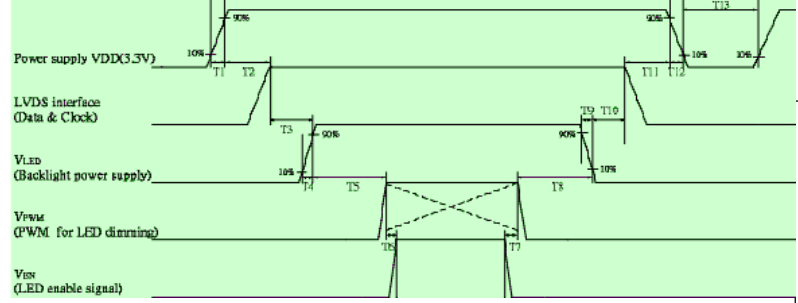
5V for Camera (5V/50mA)



LCD/Camera Connector

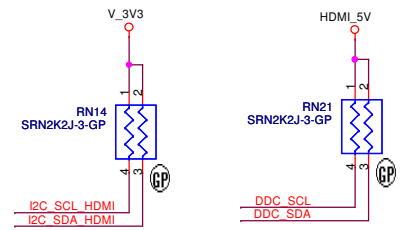
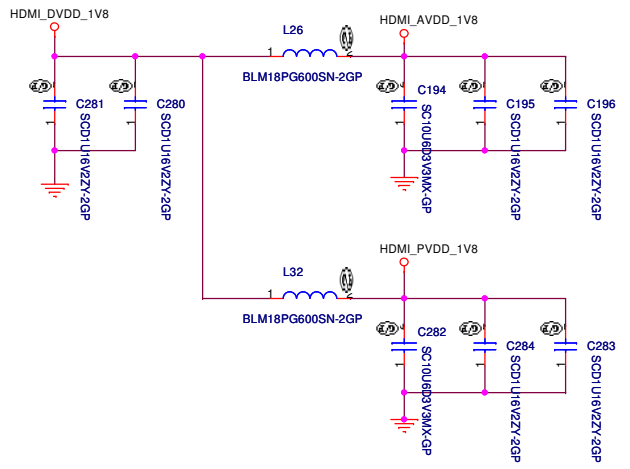
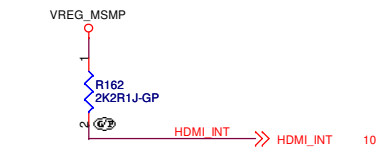
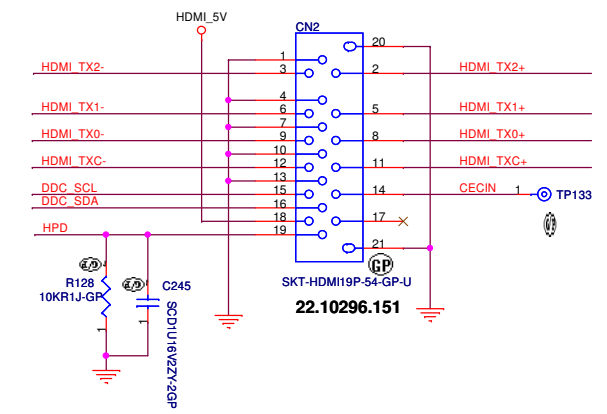
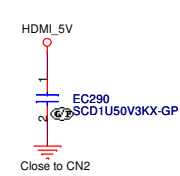
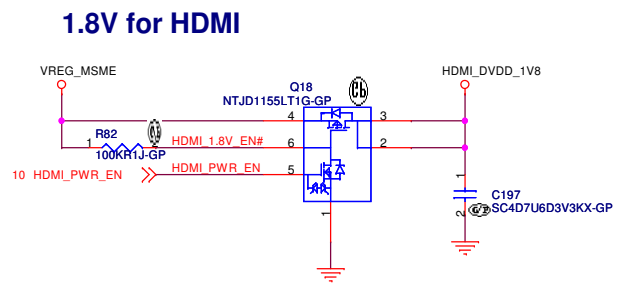
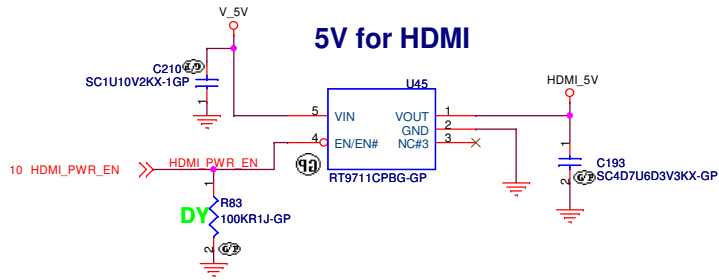
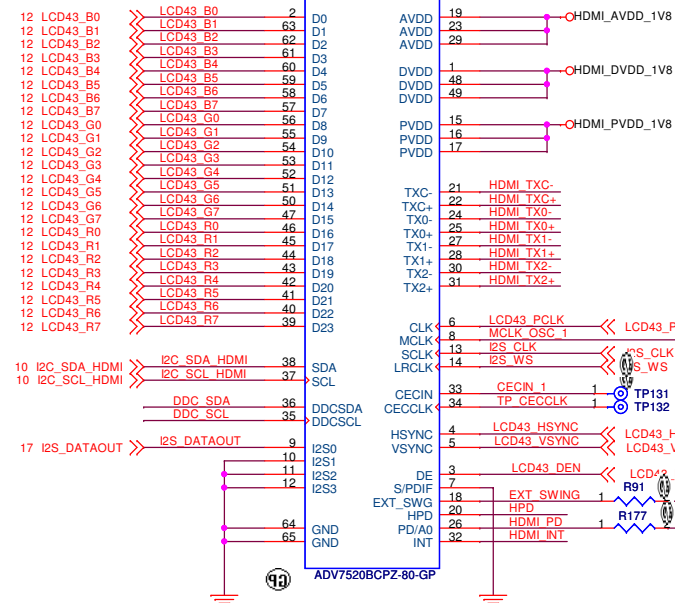


B101EW01 V2 (1280x720)



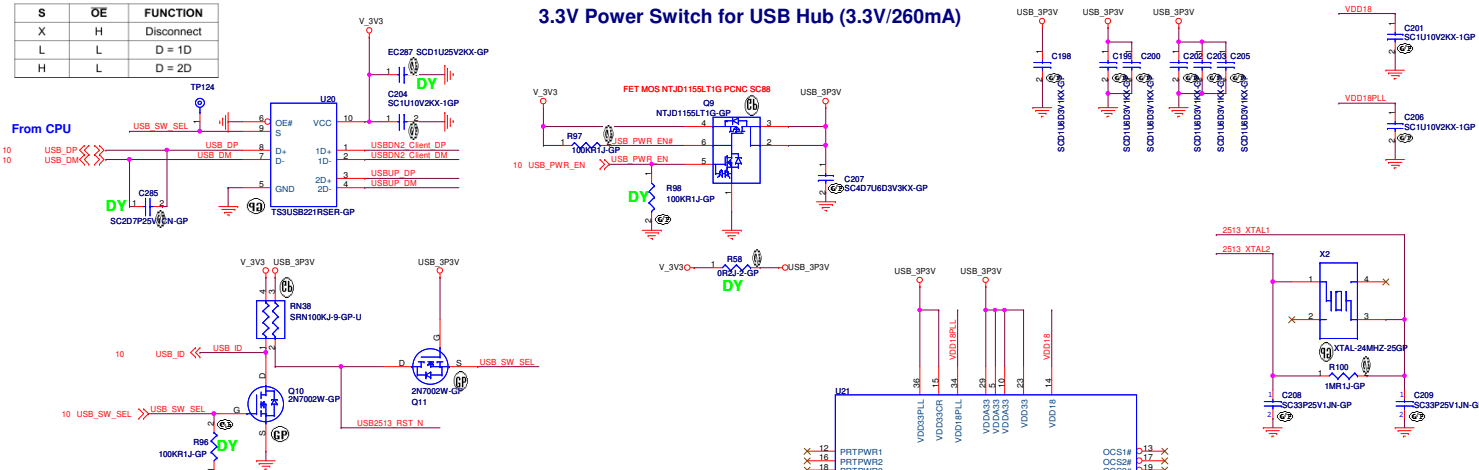
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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hstchih, Taipei Hsien 221, Taiwan, R.O.C.

Title LCD, Camera		Rev SC
Size A3	Document Number T-Note	
Date: Saturday, July 04, 2009	Sheet 13 of 34	

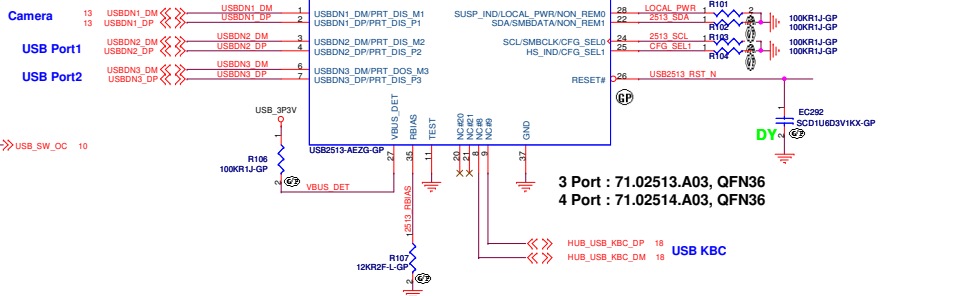


S	OE	FUNCTION
X	H	Disconnect
L	L	D = 1D
H	L	D = 2D

3.3V Power Switch for USB Hub (3.3V/260mA)



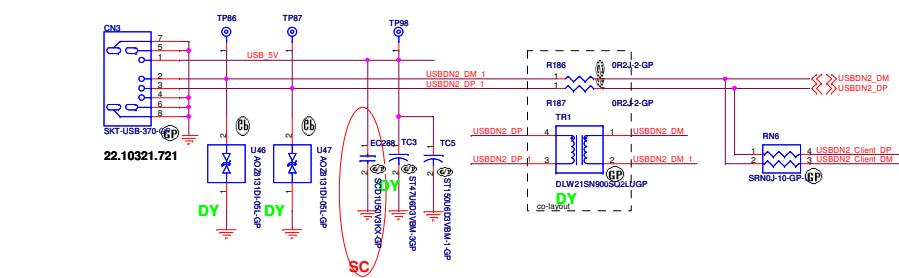
USB_SW_SEL	USB_ID	USB Mode
L	Floating	Client
H	L	Host



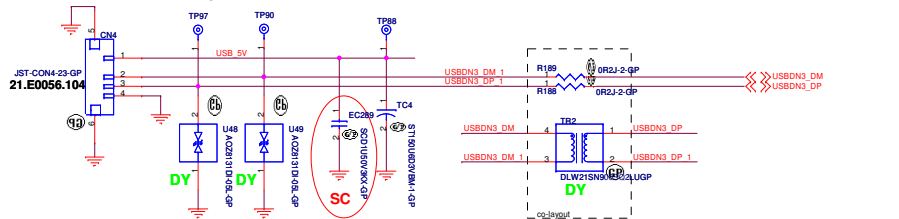
3 Port : 71.02513.A03, QFN36
4 Port : 71.02514.A03, QFN36

HUB_USB_KBC_DP 18 USB KBC
HUB_USB_KBC_DM 18

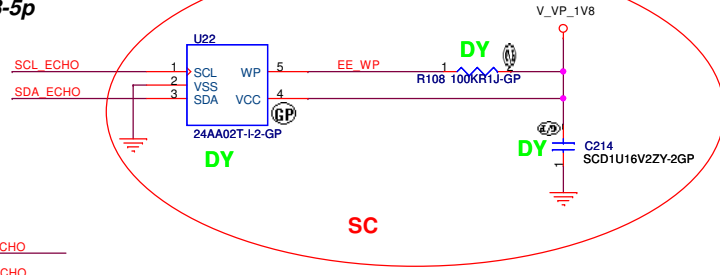
USB Host and Client



USB Host Only

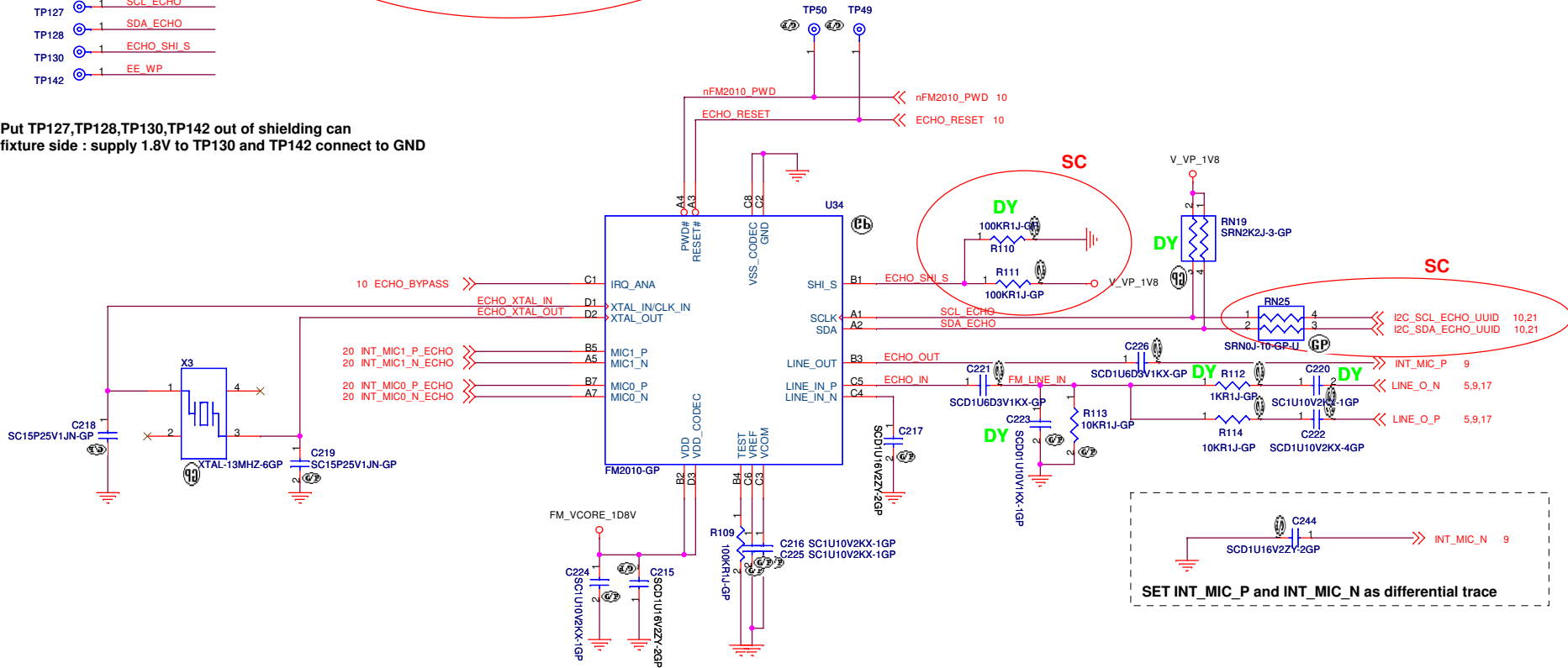


**Microchip EEPROM 2Kbit
24LC02B SOT-23-5p**



- TP127 ① SCL ECHO
- TP128 ① SDA ECHO
- TP130 ① ECHO_SHI_S
- TP142 ① EE_WP

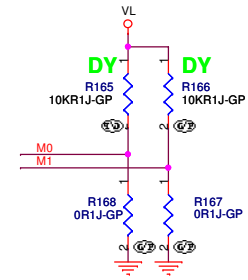
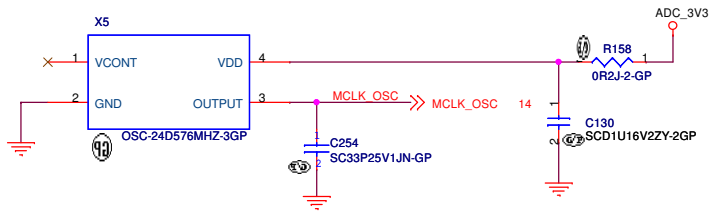
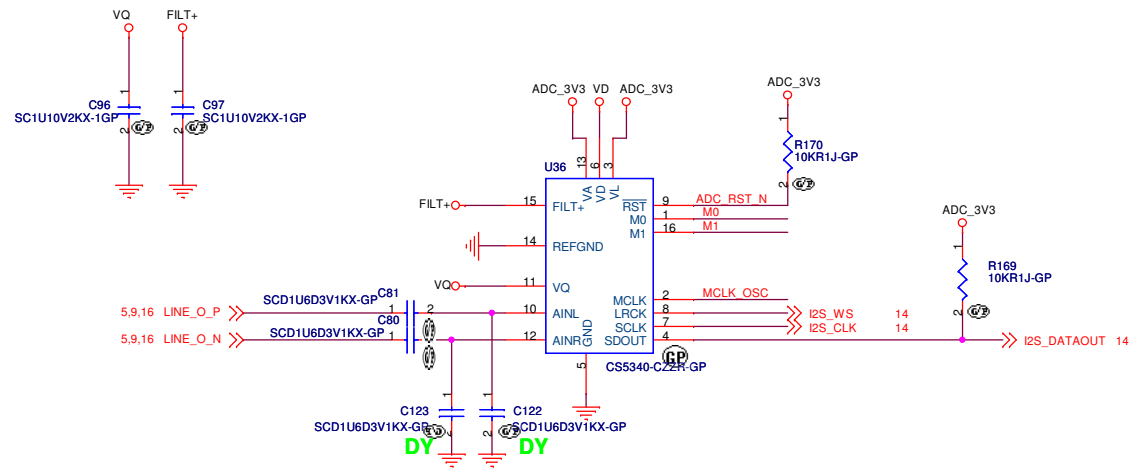
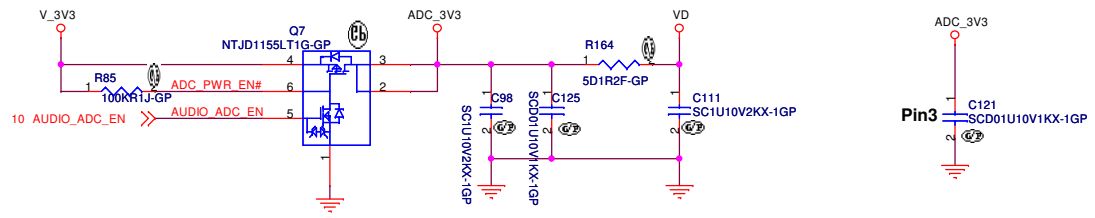
Put TP127,TP128,TP130,TP142 out of shielding can
fixture side : supply 1.8V to TP130 and TP142 connect to GND



SET INT_MIC_P and INT_MIC_N as differential trace

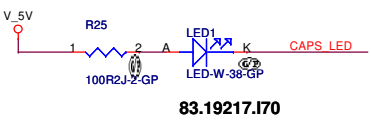
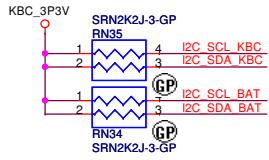
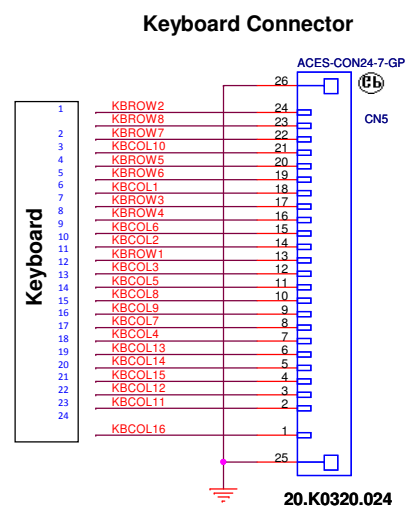
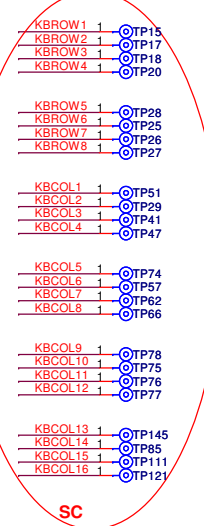
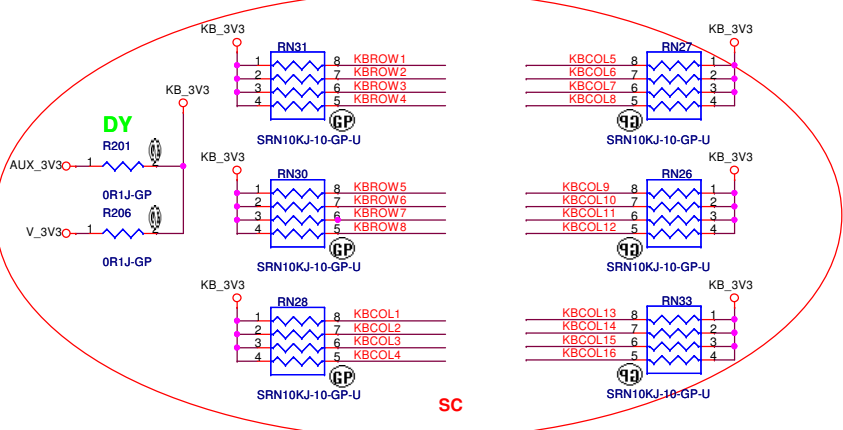
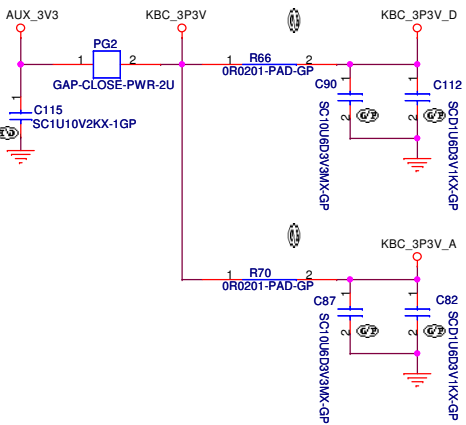
SHI_S --> Low for EEPROM
--> HI for I2C

TEST == Low(normal mode, not test mode)
RESET == High(no reset held low)
PWD == High(normal mode,not power down)
IRQ_ANA == Low(normal mode, not bypass)

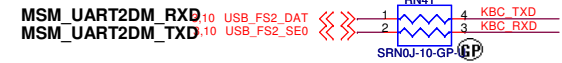
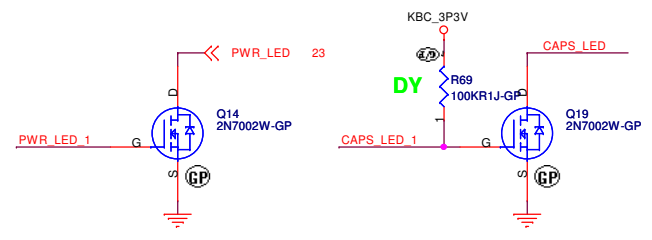


M1	M0	Mode
0	0	48KHz Master mode
0	1	96KHz Master mode
1	0	192KHz Master mode
1	1	Auto detect speed Slave mode

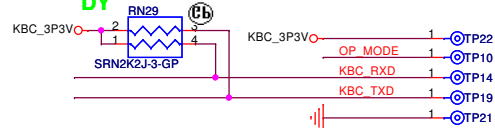
3.3V for KBC



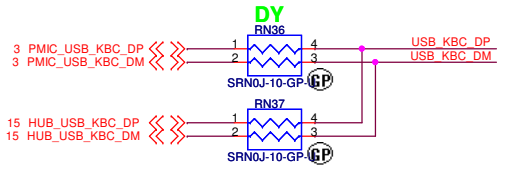
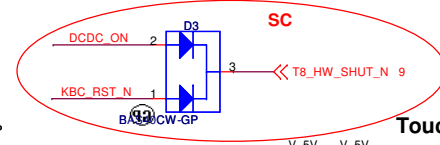
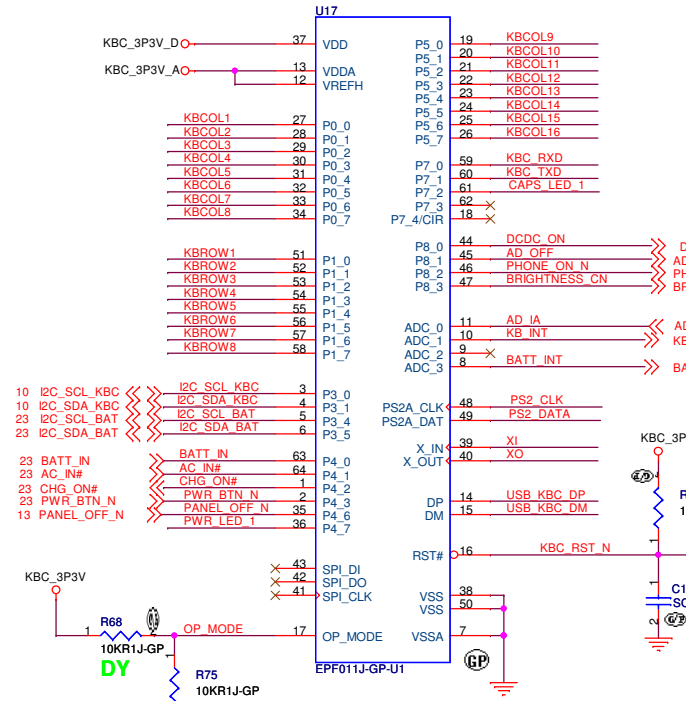
83.19217.I70



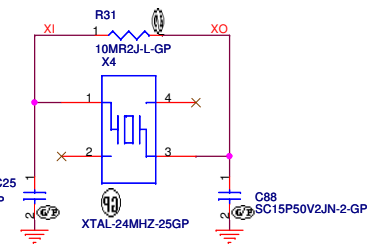
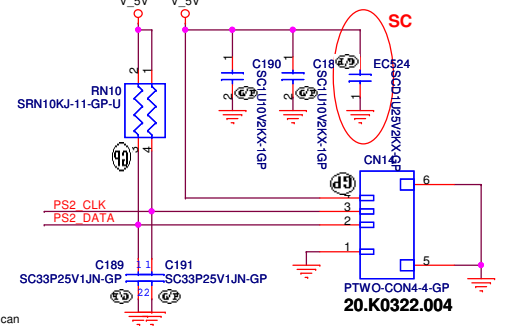
Test PAD for Debugging



Put TP14,TP19,TP10, out of shielding can



TouchPad Connector



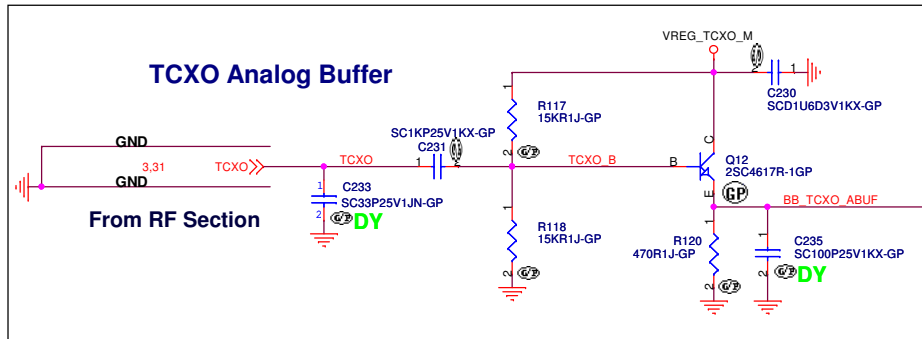
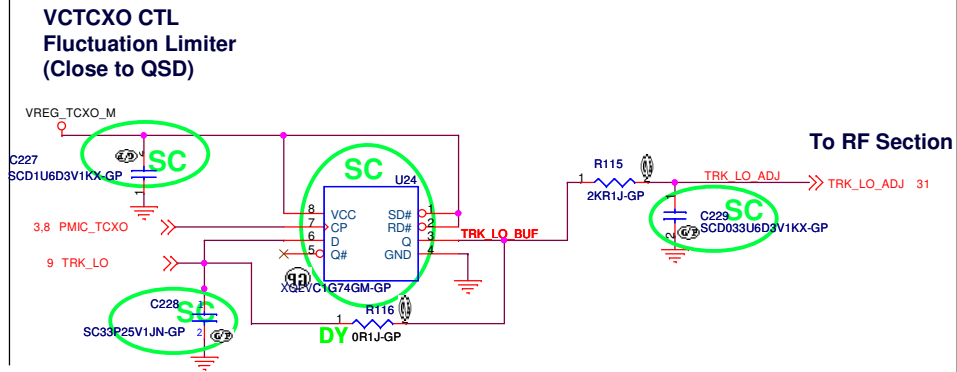
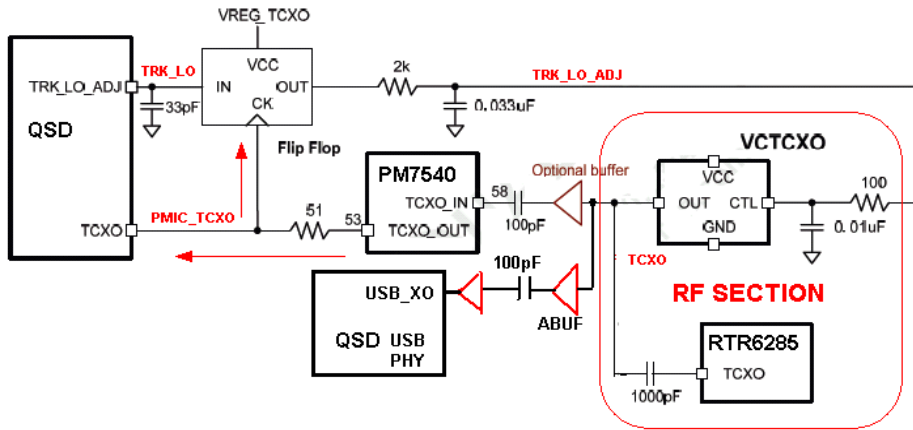
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Haichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **KBC, Keyboard con., T/P**

Rev: **SC**

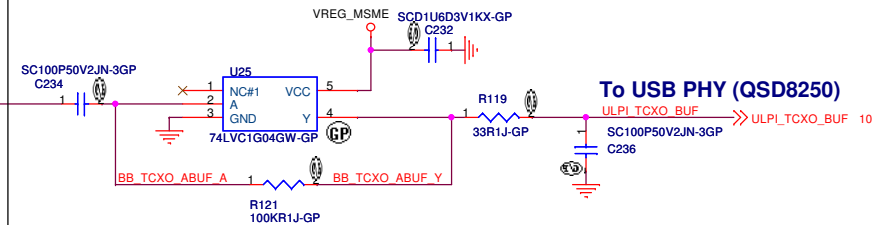
Date: Tuesday, June 30, 2009 Sheet 18 of 34

VCTCXO CTL

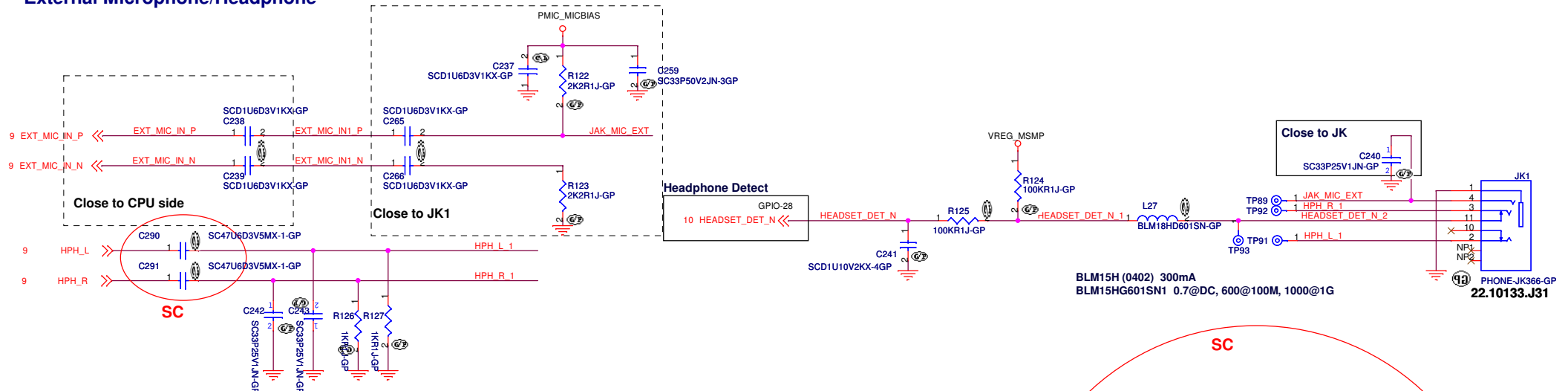


TCXO Buffer for USB_XO of QSD USB PHY

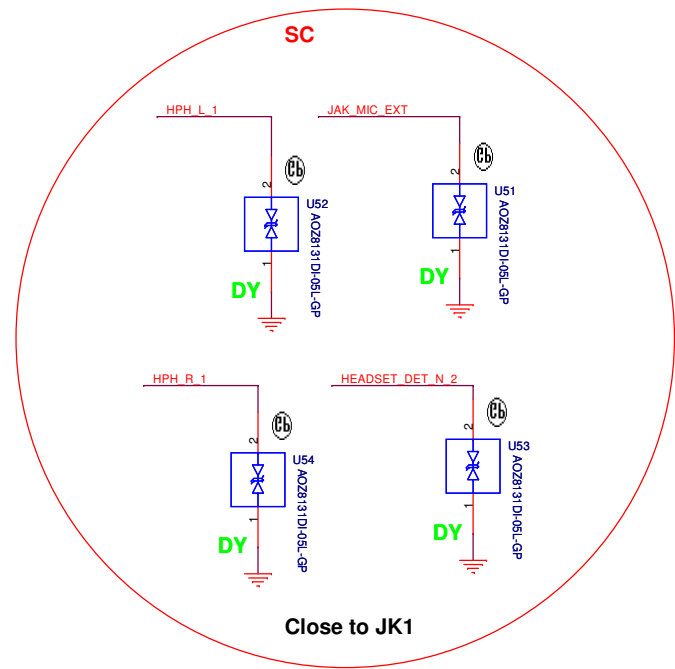
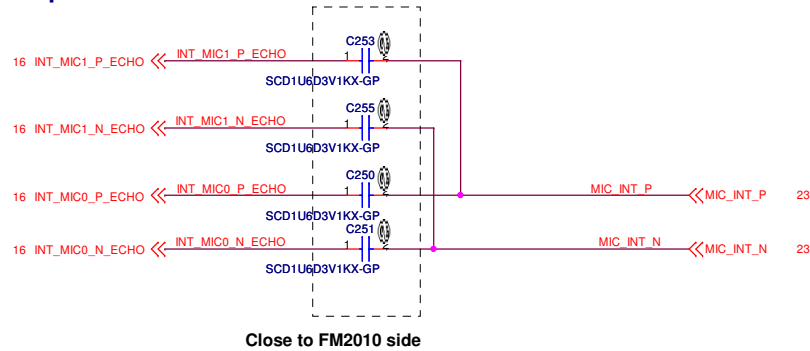
Modified from VREG_TCXO_M to VREG_MSME



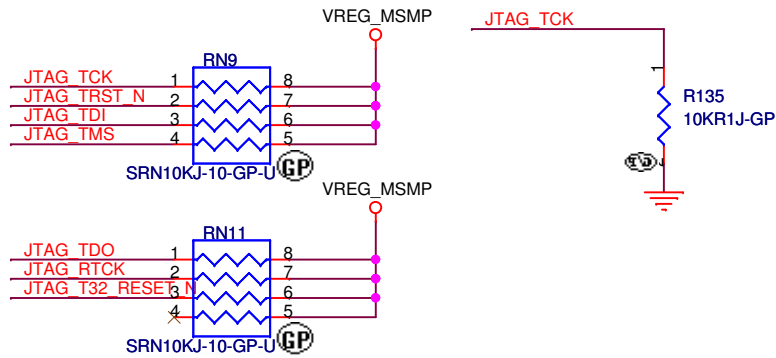
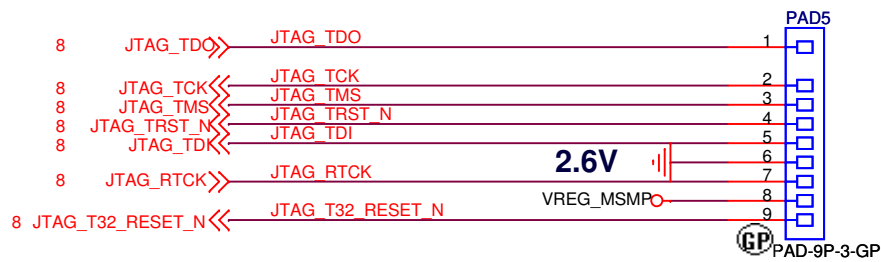
External Microphone/Headphone



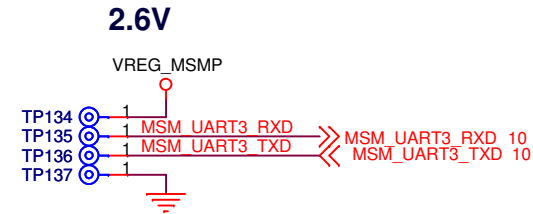
Internal Microphone



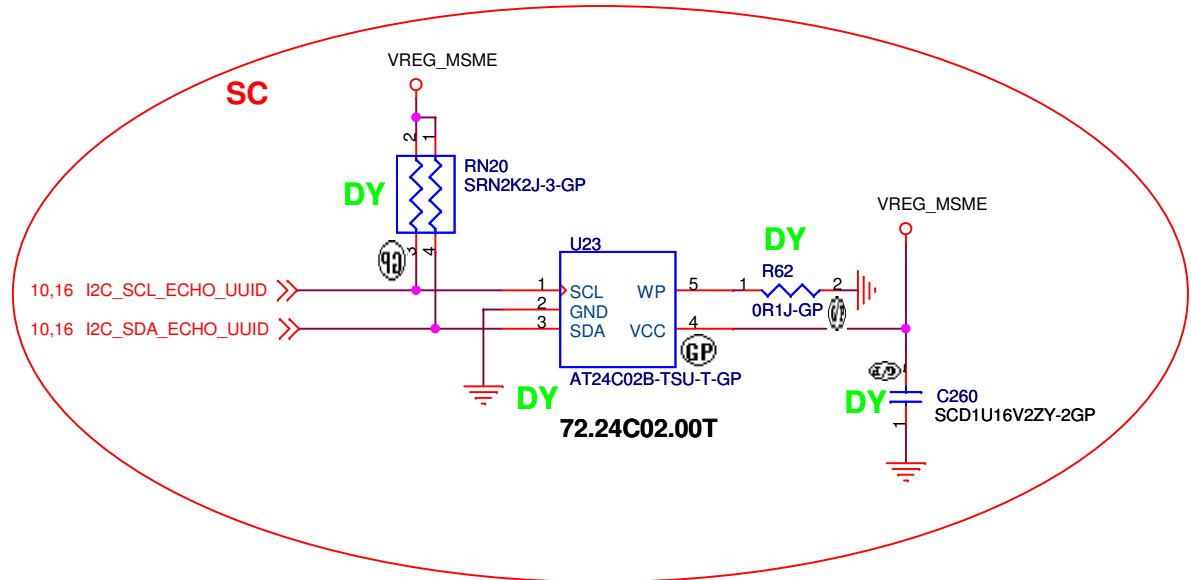
JTAG



UART-3

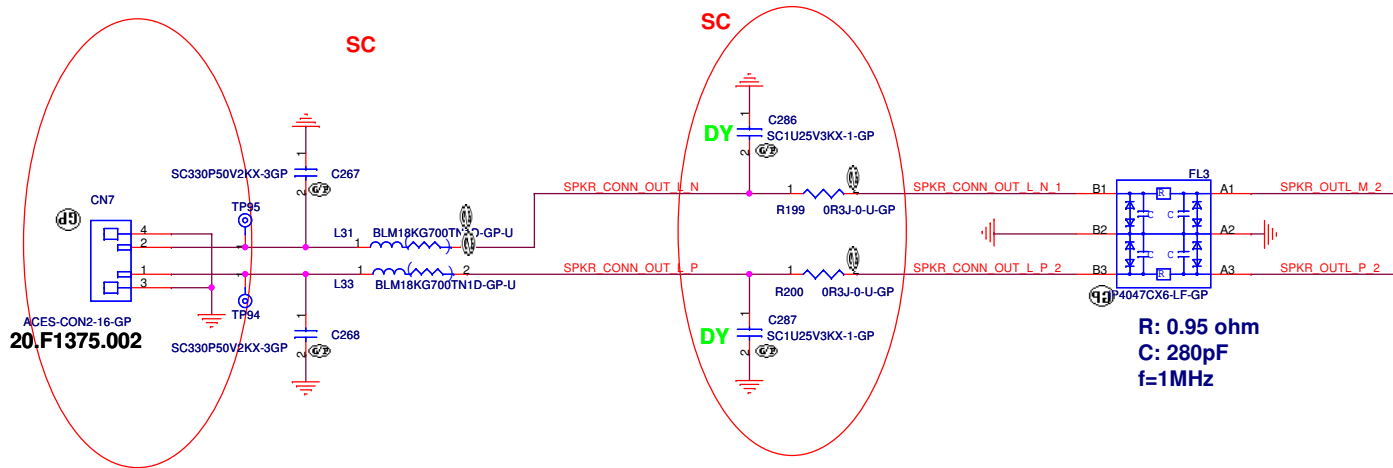
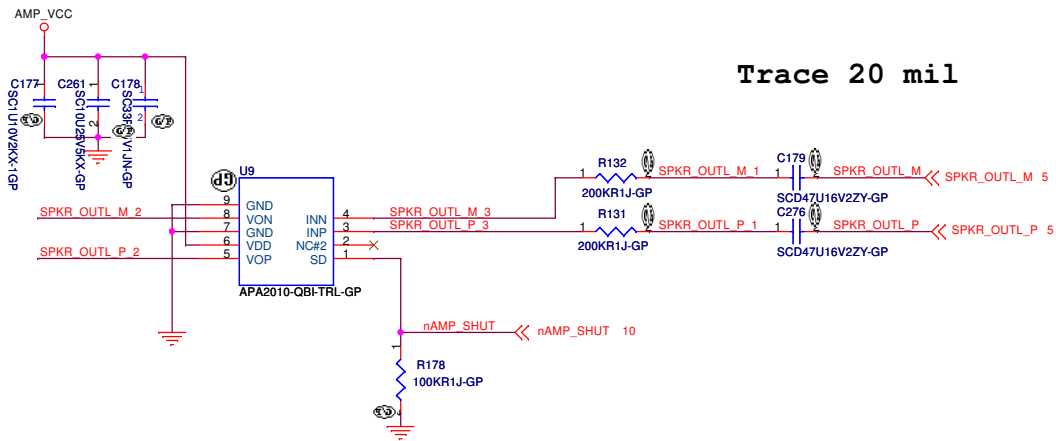
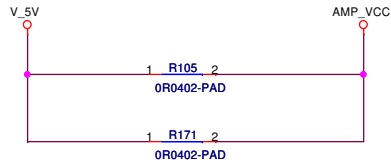


Put TP134,TP135,TP136,TP137 out of shielding can

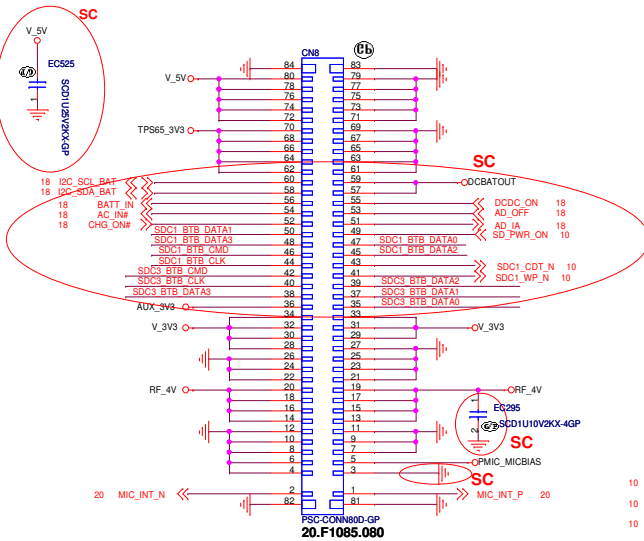


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 Taipei Hsien 221, Taiwan, R.O.C.

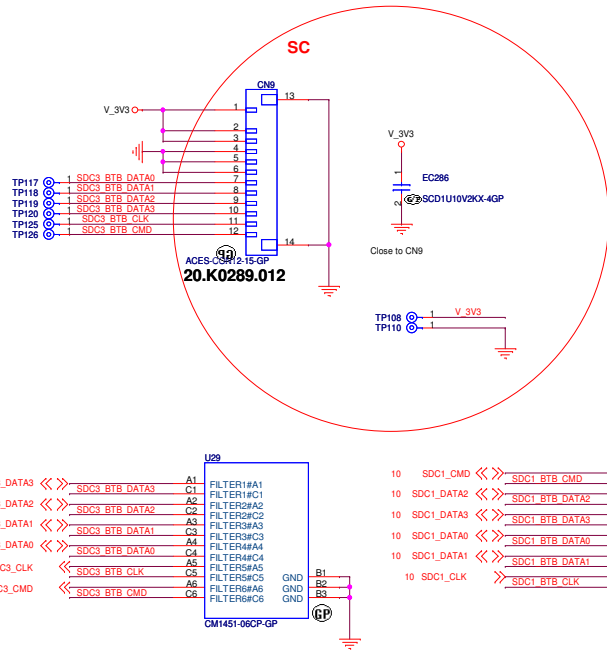
Title			Debug Port		
Size	Document Number		Rev		
A4			T-Note		SC
Date:	Tuesday, June 30, 2009	Sheet	21	of	34



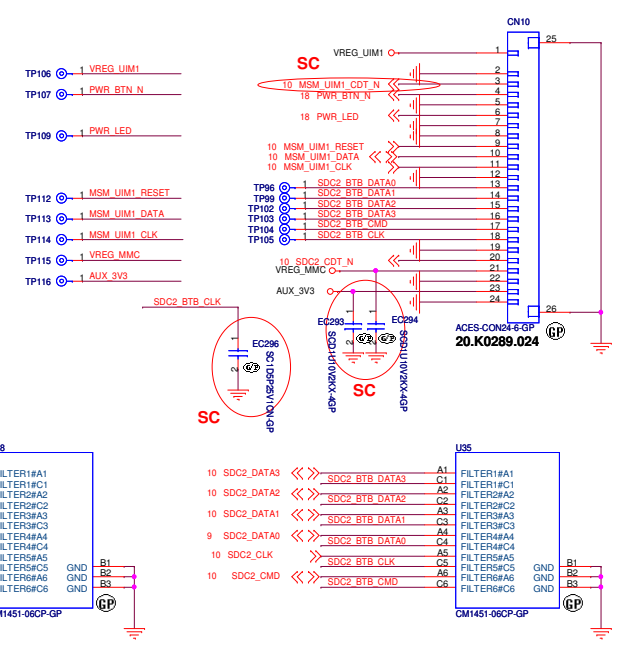
BTB Connector: IO Board <-> MB Board



FPC Connector: Flash Board <-> MB Board

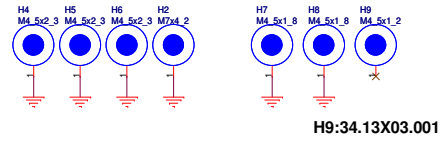


FPC Connector: SIM Board <-> MB Board

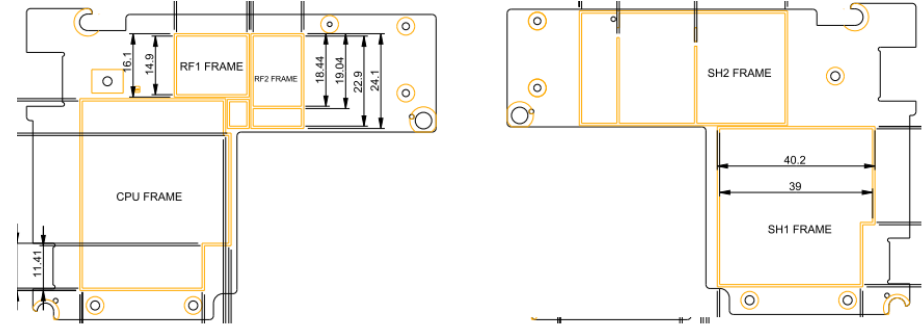
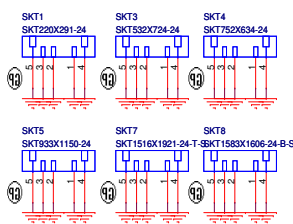


Shielding Can

Screw Hole



Shielding Can



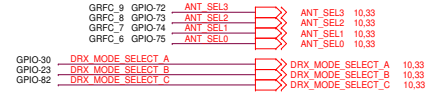
frame	p/n	cover	p/n
RF1	33.13X04.001	RF1_COVER	34.13X09.001
RF2	33.13X05.001	RF2_COVER	34.13X10.001
CPU	33.13X09.001	CPU_COVER	34.13X11.001
SH2	33.13X07.001	SH2_COVER	34.13X08.001
SH1	33.13X06.001	SH1_COVER	34.13X07.001

RF Interface (MXU)

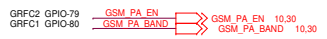
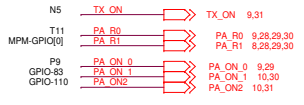
SSBDI



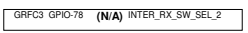
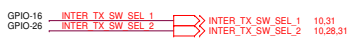
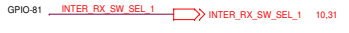
ANT SEL



PA CTRL



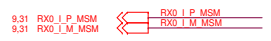
RF CTRL



GPS

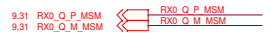


RX0 IQ

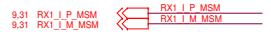


RX0 IQ
To QSD RF RX
(Analog)

RX0 IQ
To QSD RF RX
(Analog)

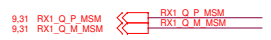


RX1 IQ

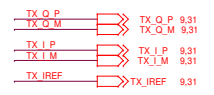


RX1 IQ
To QSD RF RX
(Analog)

RX1 IQ
To QSD RF RX
(Analog)



TX IQ



TX IQ
From QSD TXDAC
(Analog)

VCTCXO

VCTCXO ADJ



Covered by GND traces and planes

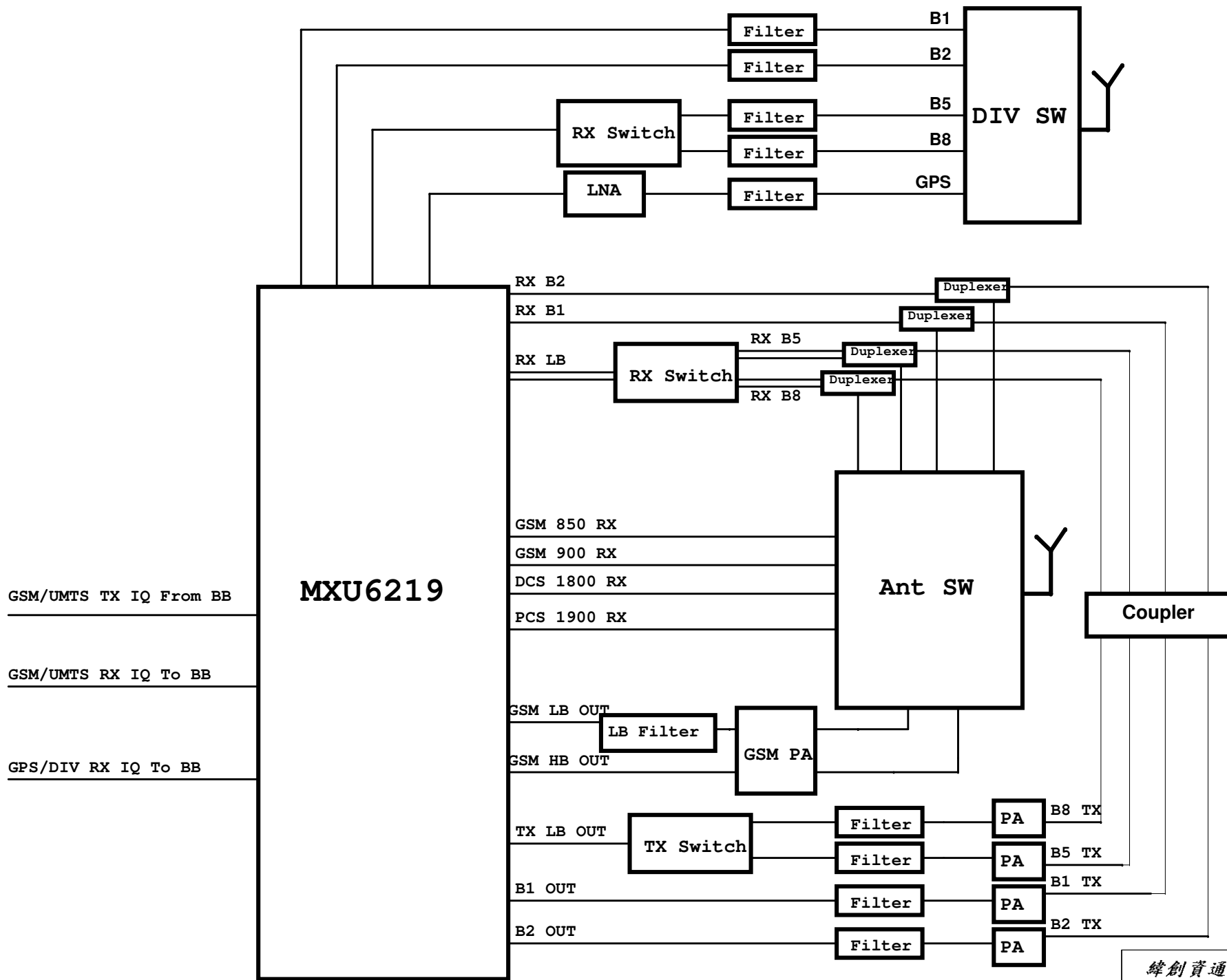
T-Note RF

Table of Content

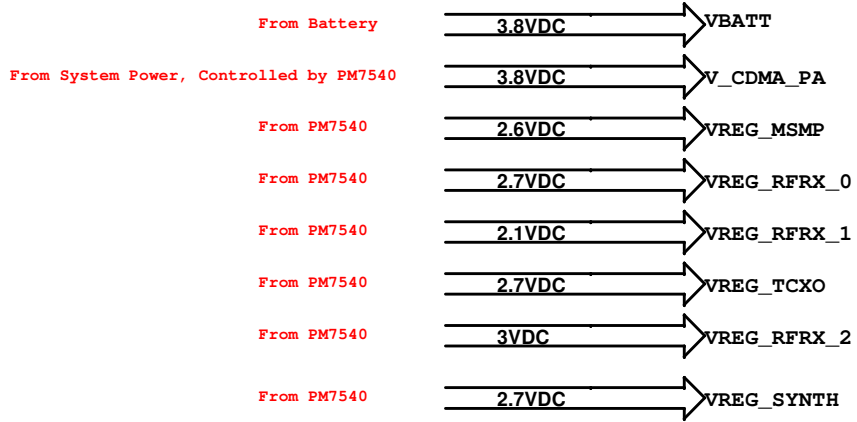
Sheet #	Content
RF01	RF VERSION SHEET
RF02	RF BLOCK DIAGRAM
RF03	RF POWER DIAGRAM
RF04	WCDMA B8 & RX CHAIN
RF05	WCDMA B1/2 PAs & DUPLX
RF06	WCDMA B5 PA AND GSM PA
RF07	MXU6219
RF08	SWB-A23 BT+WLAN
RF09	ANT SW & ANT DIVERSITY

Change Notes

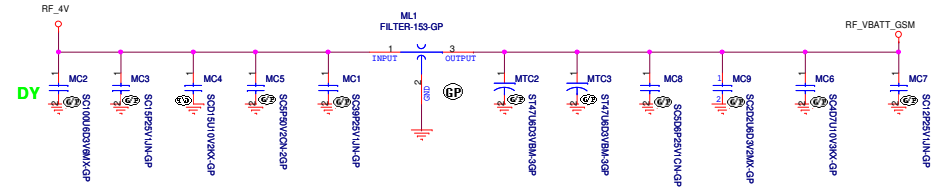
緯創資通		Wistron Corporation	
		<small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
Title			
VERSION SHEET			
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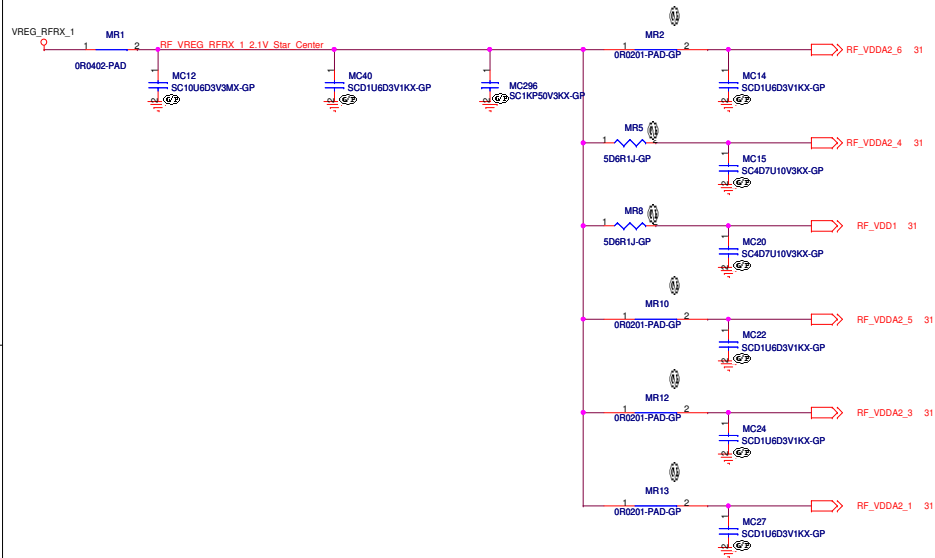
POWER DIAGRAM



VBATT for GSM AP



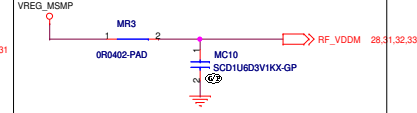
+2.1VDC



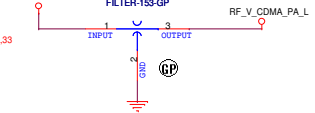
VREG_TCXO_M



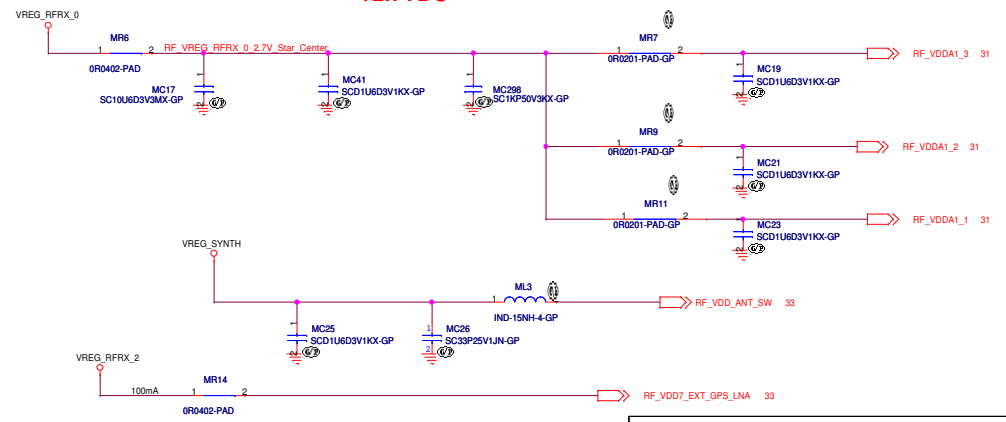
+2.6VDC



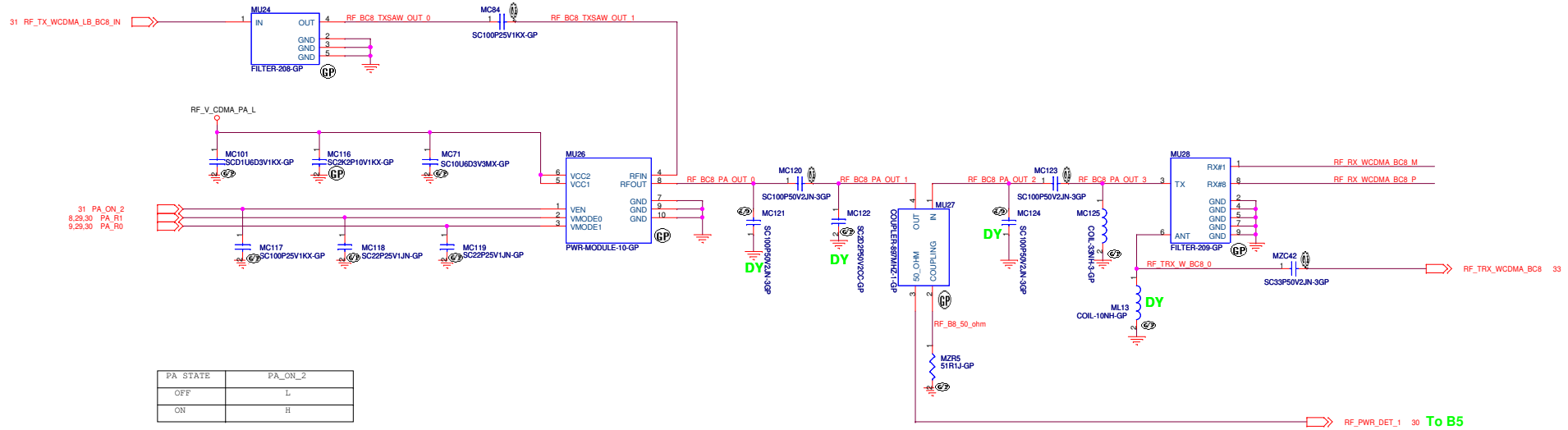
V_CDMA_PA



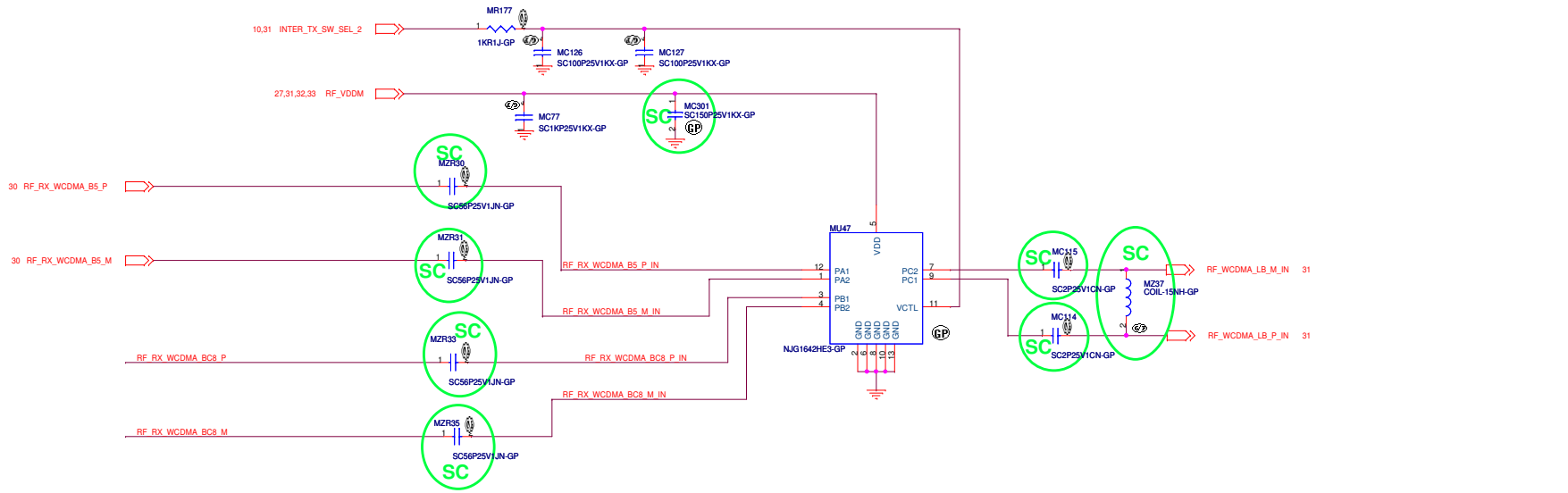
+2.7VDC



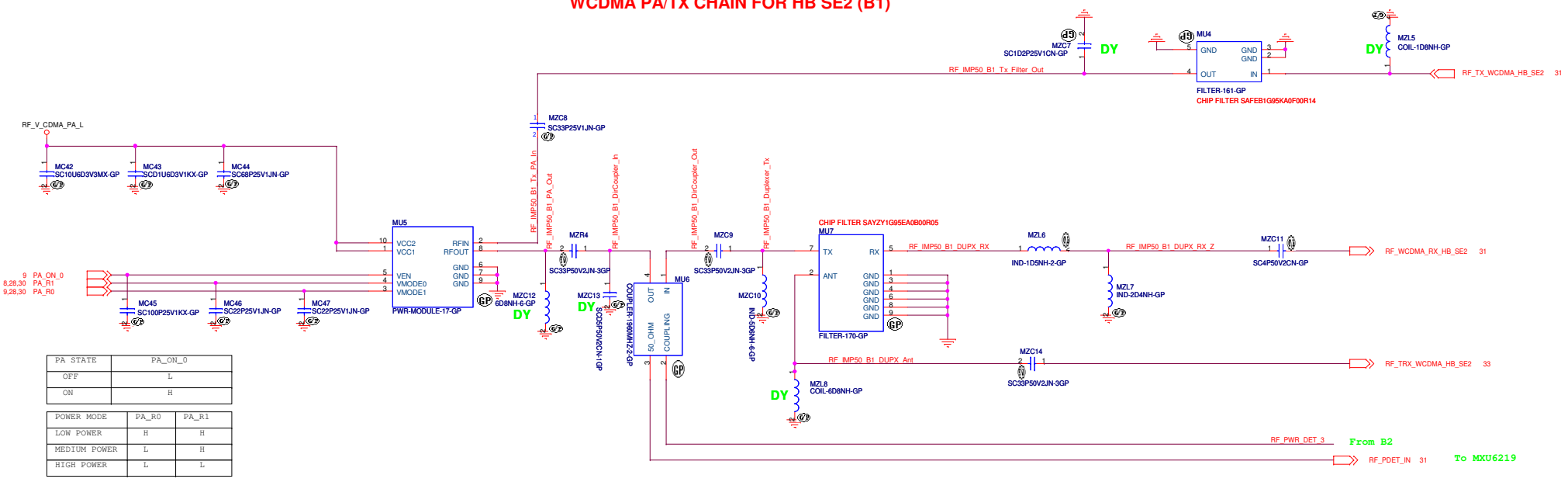
UMTS PA/TX CHAIN FOR LB (BC8)



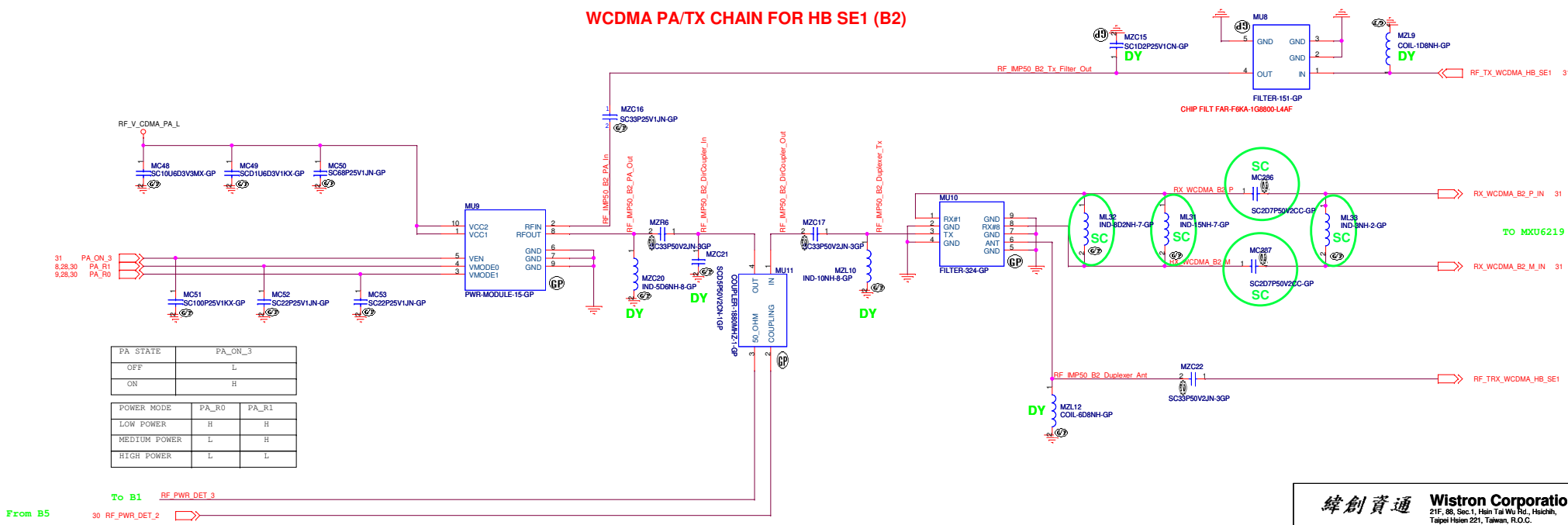
RX INTERSTAGE CHAIN



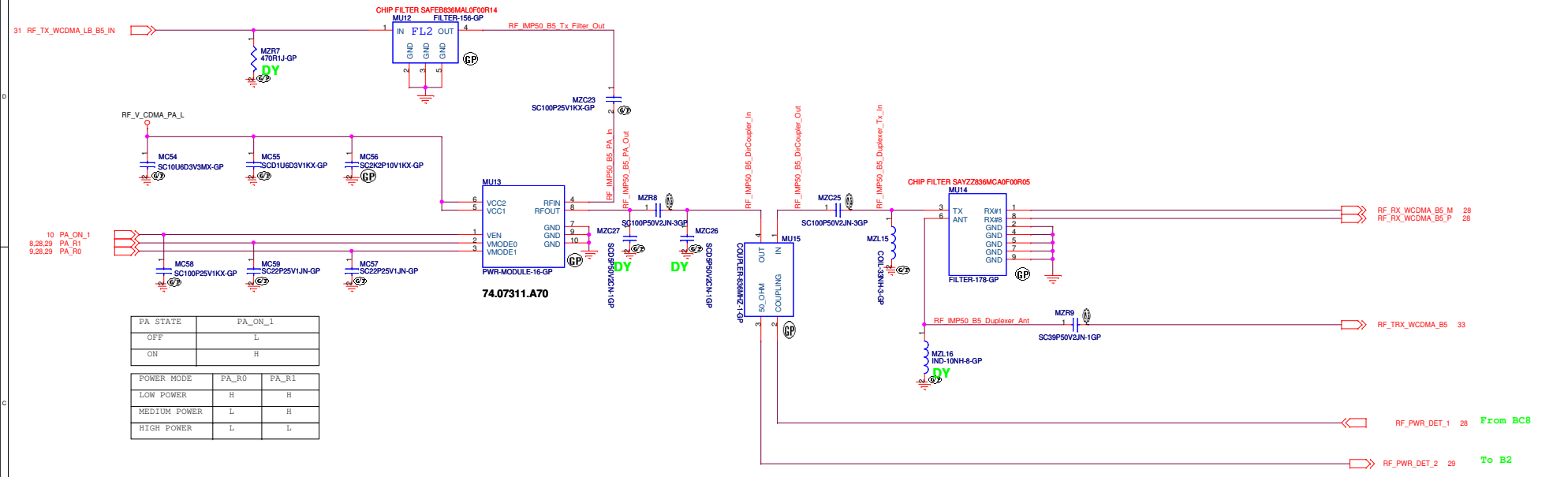
WCDMA PA/TX CHAIN FOR HB SE2 (B1)



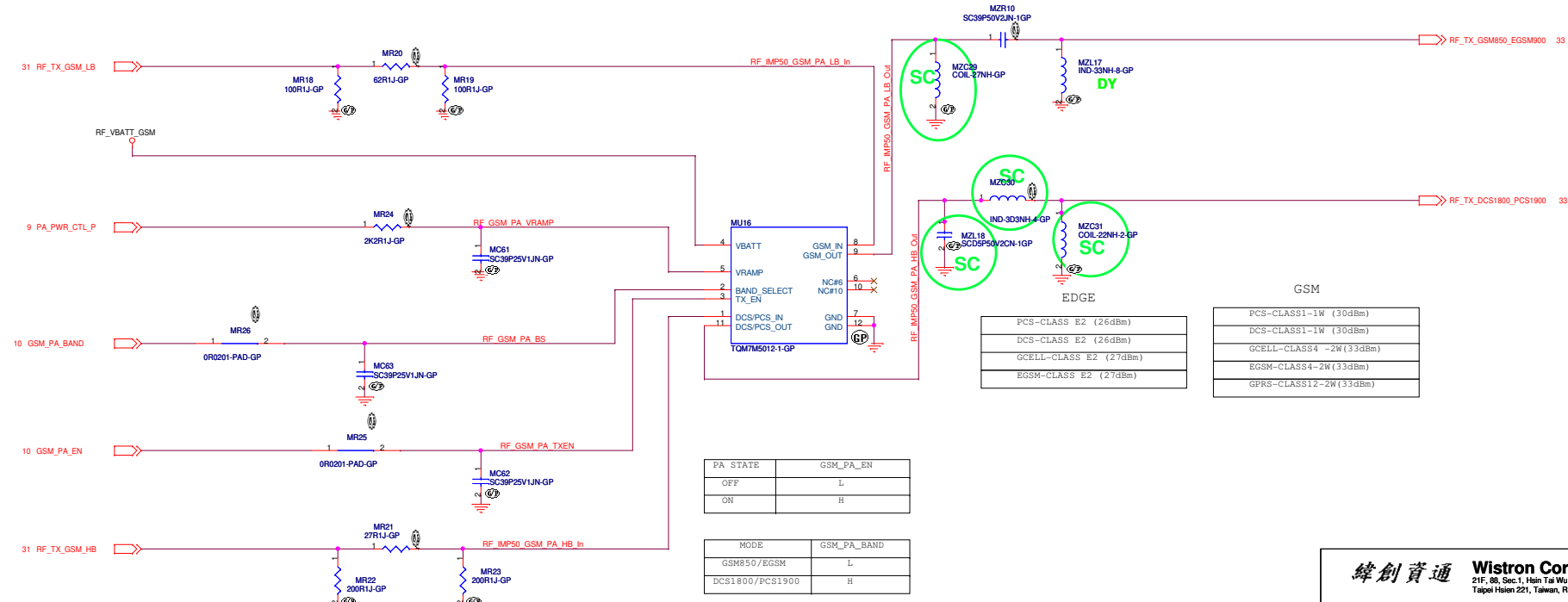
WCDMA PA/TX CHAIN FOR HB SE1 (B2)



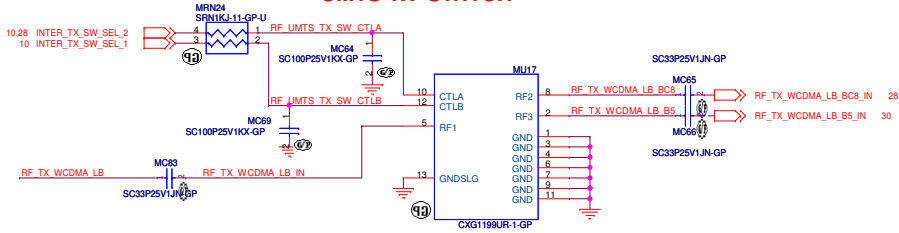
WCDMA 800 (B5/6) - PA/TX CHAIN



GSM QUAD-BAND PA

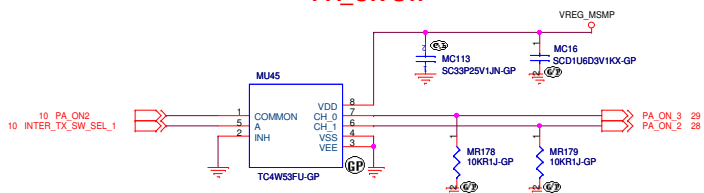


UMTS TX SWITCH

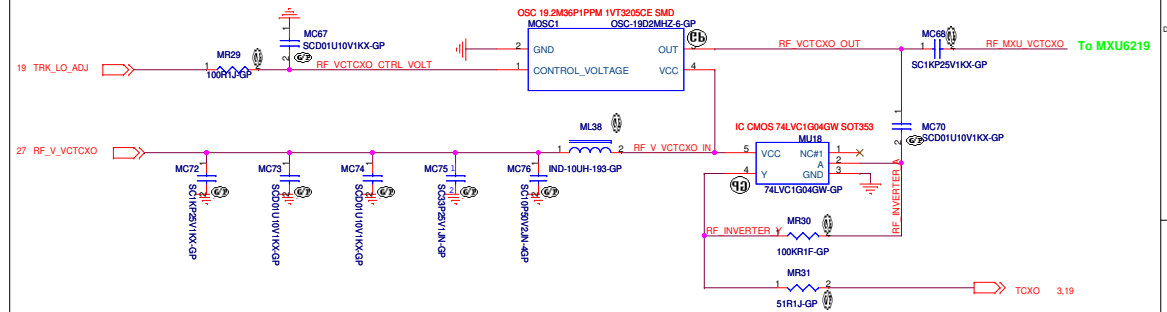


TX MODE	INTER_TX_SW_SEL_2	INTER_TX_SW_SEL_1
RF_TX_WCDMA_LB_B5	H	L
RF_TX_WCDMA_LB_BCS	L	H

PA_ON SW

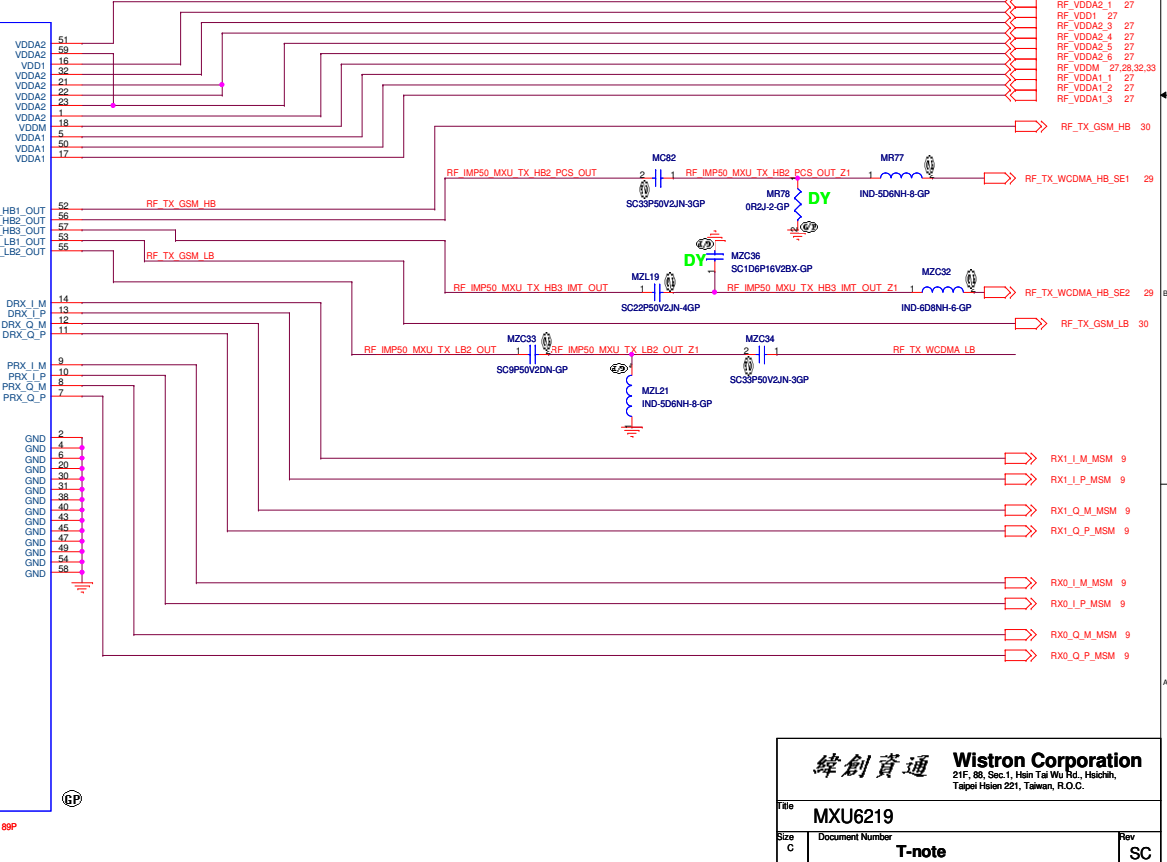
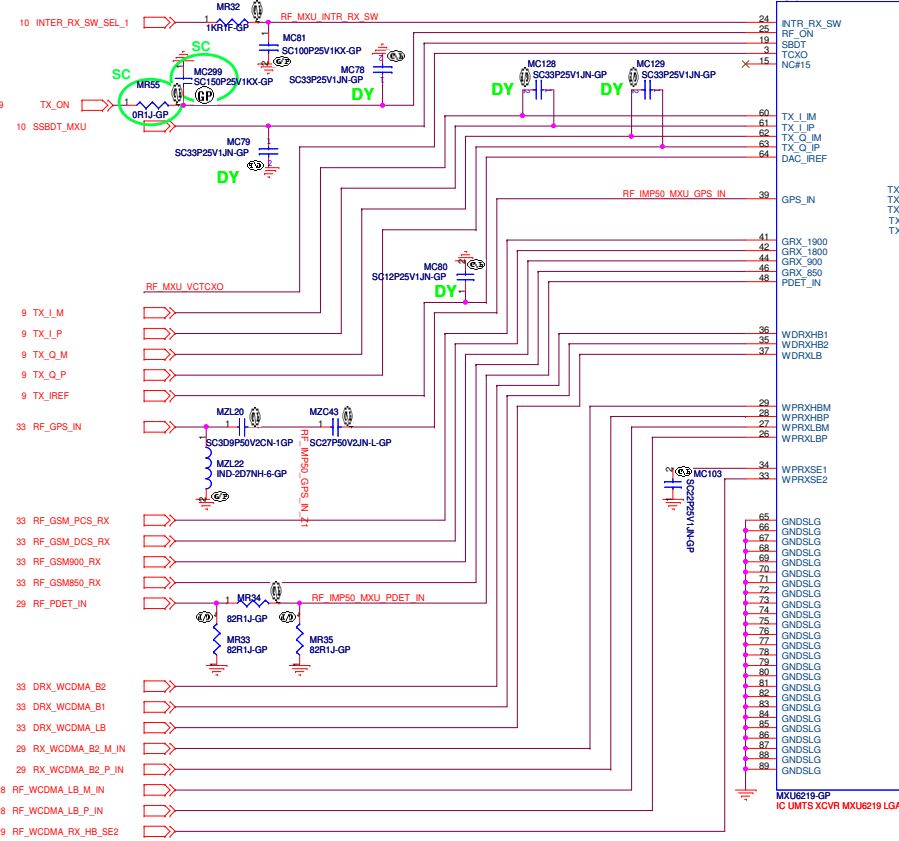


VCTCXO



MXU6219

RX INTERSTAGE CHAIN



20090617:
1. Page7: Change C149 to 0603 10uF 6.3v
2. Page3: Change BAT1 to PAS311HR-VG1-GP
3. Page12. Change U15 to THC63LVDM83R-GP
4. Page18. Change Keyboard matrix pull high power plan to V_3V3
5. Page10. Change R175 from 0 ohm to 10ohm
6. Page15. Add TP143 for USB_SW_EN
7. Page8. Add TP144 for PON_RESET_N
8. Page10/16/21. Modify I2C of ECHO_UUID circuit

20090618:
1. Page16: Dummy R110, Mount R111
2. Page9. Add Thermal sensor circuit
RF:
MZR32,MZR36=>Dummy
U24: Change Part Number
MZ37: New addition

20090619:
EE:
1. Page22. Change C247,C248 to 0402 size.
2. Page9. Add R207
3. Page18. modify KB pull high power plan
RF:
1. Change part number of MU41.

20090621:
EE:
1. Page22. Change C247,C248 to 330pF.
2. Page23. Change CN9 to 20.K0315.012

20090622:
EE:
1. Page22. Change C247,C248 to 33pF.
2. Page23. Change CN9 to 20.K0315.012
3. Page22. Add L31,L33,C267,C268
4. Page9. Modify and Setting thermal sensor circuit to DY

20090623:
EE:
1. Page22. Del C247,C248
2. Page9. Change R205 to 0201 size
RF:
1. Page32. Add MU30 circuit
2. Page 32. Add MR65,DY MR61, Del TP8,TP9,TP47

20090624:
EMI:
1. Page23. Add EC293,EC294,EC295,EC286
2. Page20. Del D14,D15,D16,D17, Add U51,U52,U53,U54
EE:
1. Page12. Change U15 to THC63LVDM83C-GP
2. Page12. Add R81,R89
Audio:
1. Page20. Add C290,C291
RF:
1. Change part number of MU41.
2. Delete MZR32 and MZR36.
3. Change part number of MZR30, MZR31, MZR33,MZR35.
4. Change part number of MZC29,
5. Change part number of ML33

20090625:
EE:
1. Page23. Add TP108,TP110
2. Page12. Change U15 back to THC63LVDM83R-GP
RF:
1. Dummy U5.N8 (Page 9)
2. Change size of C228, C228 and C229(Page 19)
3. Add MC301 (Page 28)
4. Add MR55 and MC299 (Page 31)

20090626:
EE:
1. Page 23. Modify CN8 Pin define for SD3
2. Page10. Add MSM_MSM_UIM1_CDT_N for SIM CD pin
3. Page13. Add Modify CN1 pin define for MR sensor
4. Page18. Add D3 and Mount U50 circuit
5. Page18. Del ERC1~ERC6 and add TP
EMI:
1. Page23. Add EC296
RF:
1. Page31. Change MR55 to 0 ohm, Dummy MC299

20090629:
EMI:
1. Add EC524,EC525,EC526,EC527
ME:
1. Update CN9 Symbol

20090629:
Audio:
1. Add RN24
EE:
1. Del SKT2,SKT6

20090630:
RF:
1. Page31. Mount MC29
EE:

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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