

DATA SHEET

Datasheet.Live

NE5517/NE5517A

Dual operational transconductance
amplifier

Product data
Supersedes data of 1994 Aug 31
File under Integrated Circuits, IC11 Data Handbook

2001 Aug 03

Dual operational transconductance amplifier

NE5517/NE5517A

DESCRIPTION

The NE5517 contains two current-controlled transconductance amplifiers, each with a differential input and push-pull output. The NE5517 offers significant design and performance advantages over similar devices for all types of programmable gain applications. Circuit performance is enhanced through the use of linearizing diodes at the inputs which enable a 10 dB signal-to-noise improvement referenced to 0.5% THD. The NE5517 is suited for a wide variety of industrial and consumer applications and is recommended as the preferred circuit in the Dolby™ HX (Headroom Extension) system.

Constant impedance buffers on the chip allow general use of the NE5517. These buffers are made of Darlington transistor and a biasing network which changes bias current in dependence of I_{ABC} .

Therefore, changes of output offset voltages are almost eliminated. This is an advantage of the NE5517 compared to LM13600. With the LM13600, a burst in the bias current I_{ABC} guides to an audible offset voltage change at the output. With the constant impedance buffers of the NE5517 this effect can be avoided and makes this circuit preferable for high quality audio applications.

FEATURES

- Constant impedance buffers
- ΔV_{BE} of buffer is constant with amplifier I_{BIAS} change
- Pin compatible with LM13600
- Excellent matching between amplifiers
- Linearizing diodes
- High output signal-to-noise ratio

APPLICATIONS

- Multiplexers
- Timers
- Electronic music synthesizers
- Dolby™ HX Systems
- Current-controlled amplifiers, filters
- Current-controlled oscillators, impedances

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70 °C	NE5517N	SOT38-4
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70 °C	NE5517AN	SOT38-4
16-Pin Small Outline (SO) Package	0 to +70 °C	NE5517D	SOT109-1

PIN CONFIGURATION

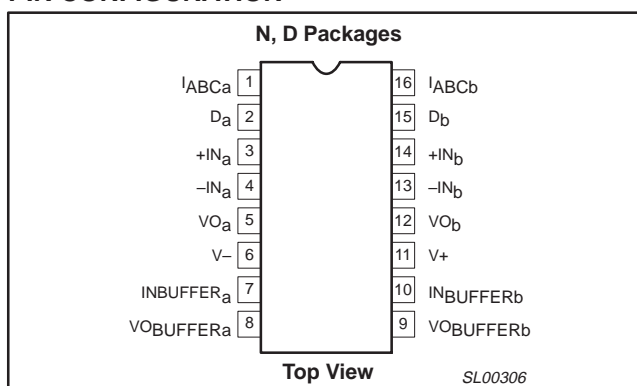


Figure 1. Pin Configuration

PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	I_{ABCa}	Amplifier bias input A
2	D_a	Diode bias A
3	$+IN_a$	Non-inverting input A
4	$-IN_a$	Inverting input A
5	VO_a	Output A
6	$V-$	Negative supply
7	$IN_{BUFFERa}$	Buffer input A
8	$VO_{BUFFERa}$	Buffer output A
9	$VO_{BUFFERb}$	Buffer output B
10	$IN_{BUFFERb}$	Buffer input B
11	$V+$	Positive supply
12	VO_b	Output B
13	$-IN_b$	Inverting input B
14	$+IN_b$	Non-inverting input B
15	D_b	Diode bias B
16	I_{ABCb}	Amplifier bias input B

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CIRCUIT SCHEMATIC

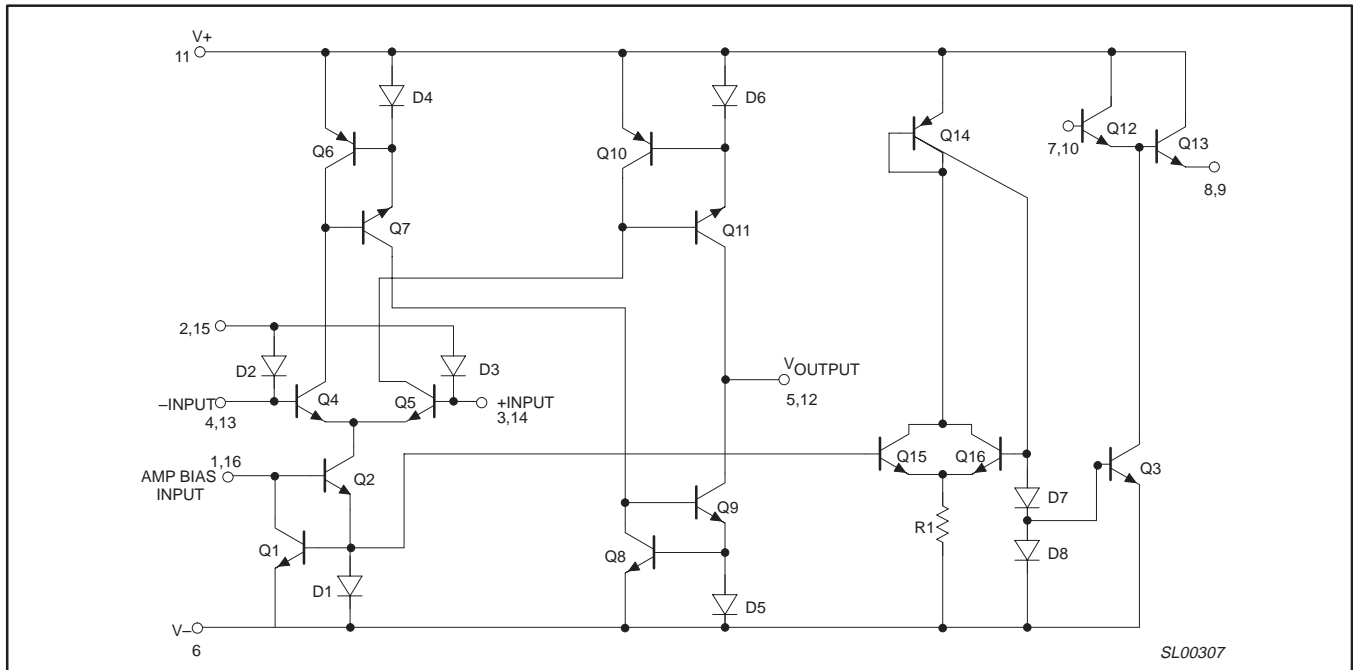


Figure 2. Circuit Schematic

CONNECTION DIAGRAM

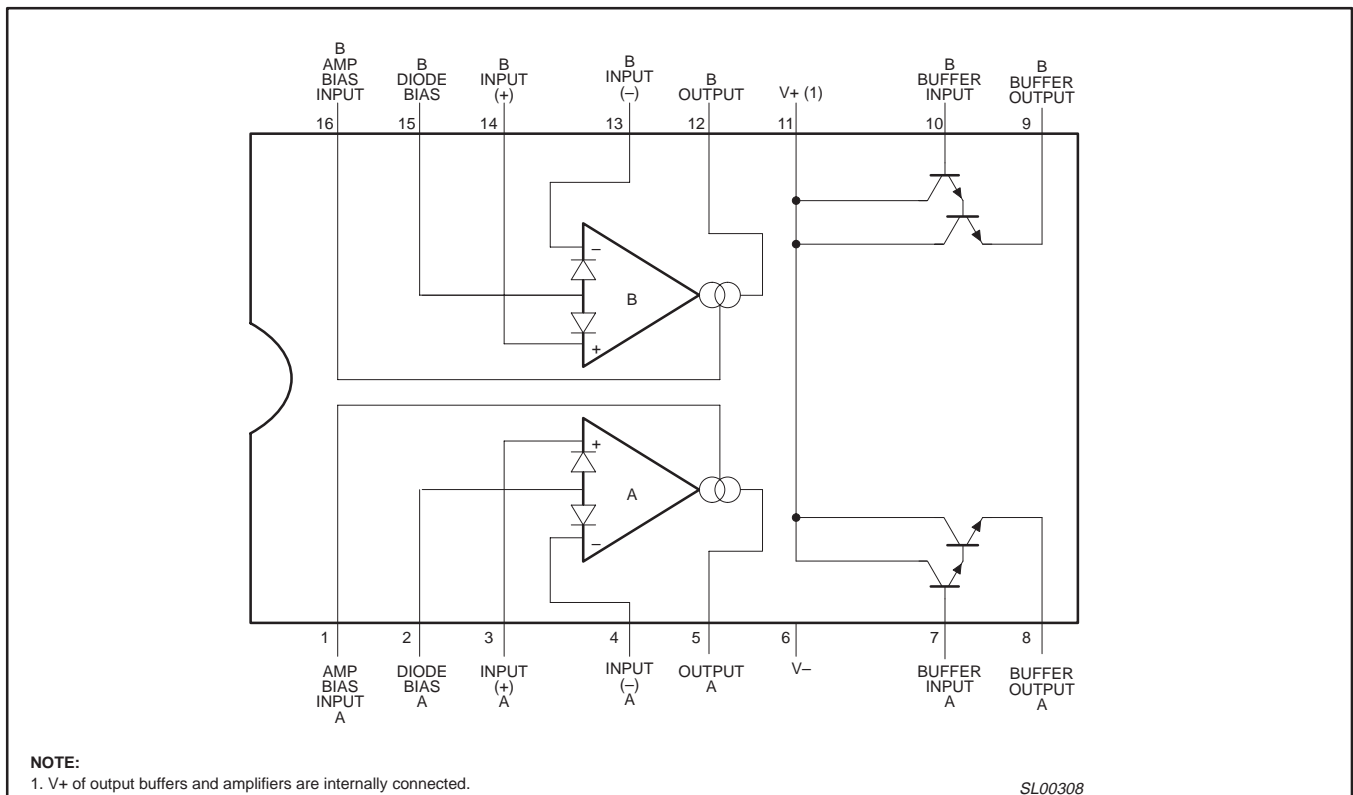


Figure 3. Connection Diagram

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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage ¹ NE5517 NE5517A	36 V_{DC} or ± 18 44 V_{DC} or ± 22	V V
P_D	Power dissipation, $T_{amb} = 25\text{ }^\circ\text{C}$ (still air) ² NE5517N, NE5517AN NE5517D	1500 1125	mW mW
V_{IN}	Differential input voltage	± 5	V
I_D	Diode bias current	2	mA
I_{ABC}	Amplifier bias current	2	mA
I_{SC}	Output short-circuit duration	Indefinite	
I_{OUT}	Buffer output current ³	20	mA
T_{amb}	Operating temperature range NE5517N, NE5517AN	0 $^\circ\text{C}$ to +70 $^\circ\text{C}$	$^\circ\text{C}$
V_{DC}	DC input voltage	$+V_S$ to $-V_S$	
T_{stg}	Storage temperature range	-65 $^\circ\text{C}$ to +150 $^\circ\text{C}$	$^\circ\text{C}$
T_{sld}	Lead soldering temperature (10 sec max)	230	$^\circ\text{C}$

NOTES:

- For selections to a supply voltage above $\pm 22\text{ V}$, contact factory
- The following derating factors should be applied above 25 $^\circ\text{C}$
N package at 12.0 mW/ $^\circ\text{C}$
D package at 9.0 mW/ $^\circ\text{C}$
- Buffer output current should be limited so as to not exceed package dissipation.

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DC ELECTRICAL CHARACTERISTICS¹

SYMBOL	PARAMETER	TEST CONDITIONS	NE5517			NE5517A			UNIT	
			Min	Typ	Max	Min	Typ	Max		
V _{OS}	Input offset voltage	Over temperature range I _{ABC} 5 μA		0.4	5		0.4	2	mV	
				0.3	5		0.3	2	mV	
	ΔV _{OS} /ΔT	Avg. TC of input offset voltage		7			7		μV/°C	
	V _{OS} including diodes	Diode bias current (I _D) = 500 μA		0.5	5		0.5	2	mV	
V _{OS}	Input offset change	5 μA ≤ I _{ABC} ≤ 500 μA		0.1			0.1	3	mV	
I _{OS}	Input offset current			0.1	0.6		0.1	0.6	μA	
				0.001			0.001		μA/°C	
I _{BIAS}	Input bias current	Over temperature range		0.4	5		0.4	5	μA	
				1	8		1	7	μA	
	ΔI _B /ΔT	Avg. TC of input current		0.01			0.01		μA/°C	
g _M	Forward transconductance	Over temperature range	6700	9600	1300	7700	9600	1200	μmho	
			5400			4000				μmho
	g _M tracking			0.3			0.3		dB	
I _{OUT}	Peak output current	R _L = 0, I _{ABC} = 5 μA		5		3	5	7	μA	
		R _L = 0, I _{ABC} = 500 μA	350	500	650	350	500	650	μA	
		R _L = 0	300			300			μA	
V _{OUT}	Peak output voltage	Positive	R _L = ∞, 5 μA ≤ I _{ABC} ≤ 500 μA	+12	+14.2		+12	+14.2	V	
		Negative	R _L = ∞, 5 μA ≤ I _{ABC} ≤ 500 μA	-12	-14.4		-12	-14.4	V	
I _{CC}	Supply current	I _{ABC} = 500 μA, both channels		2.6	4		2.6	4	mA	
	V _{OS} sensitivity	Positive Negative	ΔV _{OS} /ΔV+		20	150		20	150	μV/V
				20	150		20	150	μV/V	
CMRR	Common-mode rejection ratio			80	110		80	110	dB	
				±12	±13.5		±12	±13.5	V	
	Crosstalk	Referred to input ² 20 Hz < f < 20 kHz		100			100		dB	
I _{IN}	Differential input current	I _{ABC} = 0, input = ±4 V		0.02	100		0.02	10	nA	
					0.2	100		0.2	5	nA
R _{IN}	Input resistance		10	26		10	26	kΩ		
B _W	Open-loop bandwidth			2			2		MHz	
SR	Slew rate	Unity gain compensated		50			50		V/μs	
I _N BUFFER	Buffer input current	5		0.4	5		0.4	5	μA	
V _O BUFFER	Peak buffer output voltage	5	10			10			V	
	ΔV _{BE} of buffer	Refer to Buffer V _{BE} test circuit ³		0.5	5		0.5	5	mV	

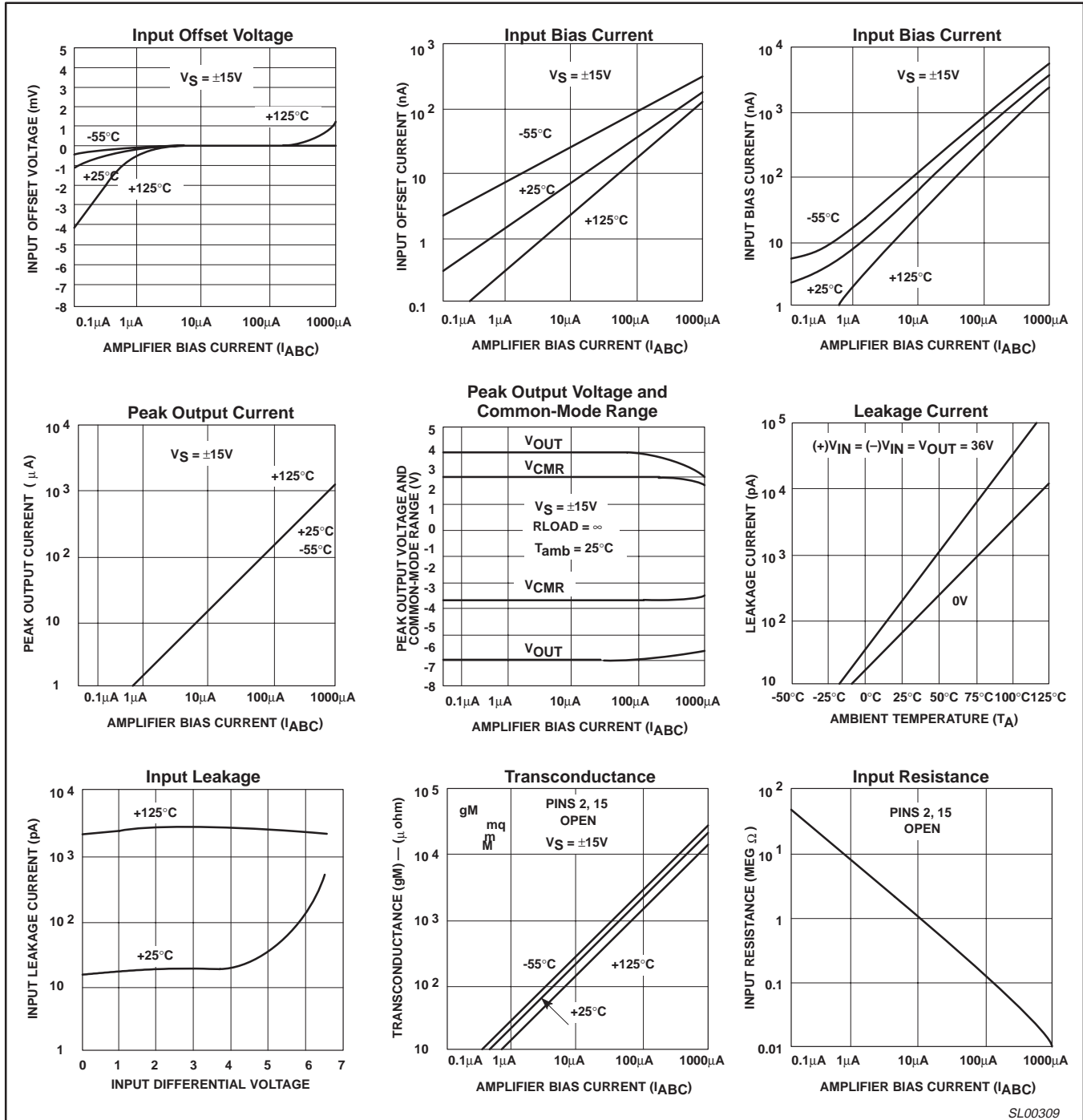
NOTES:

- These specifications apply for V_S = ±15 V, T_{amb} = 25 °C, amplifier bias current (I_{ABC}) = 500 μA, Pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.
- These specifications apply for V_S = ±15 V, I_{ABC} = 500 μA, R_{OUT} = 5 kΩ connected from the buffer output to -V_S and the input of the buffer is connected to the transconductance amplifier output.
- V_S = ±15, R_{OUT} = 5 kΩ connected from Buffer output to -V_S and 5 μA ≤ I_{ABC} ≤ 500 μA.

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TYPICAL PERFORMANCE CHARACTERISTICS



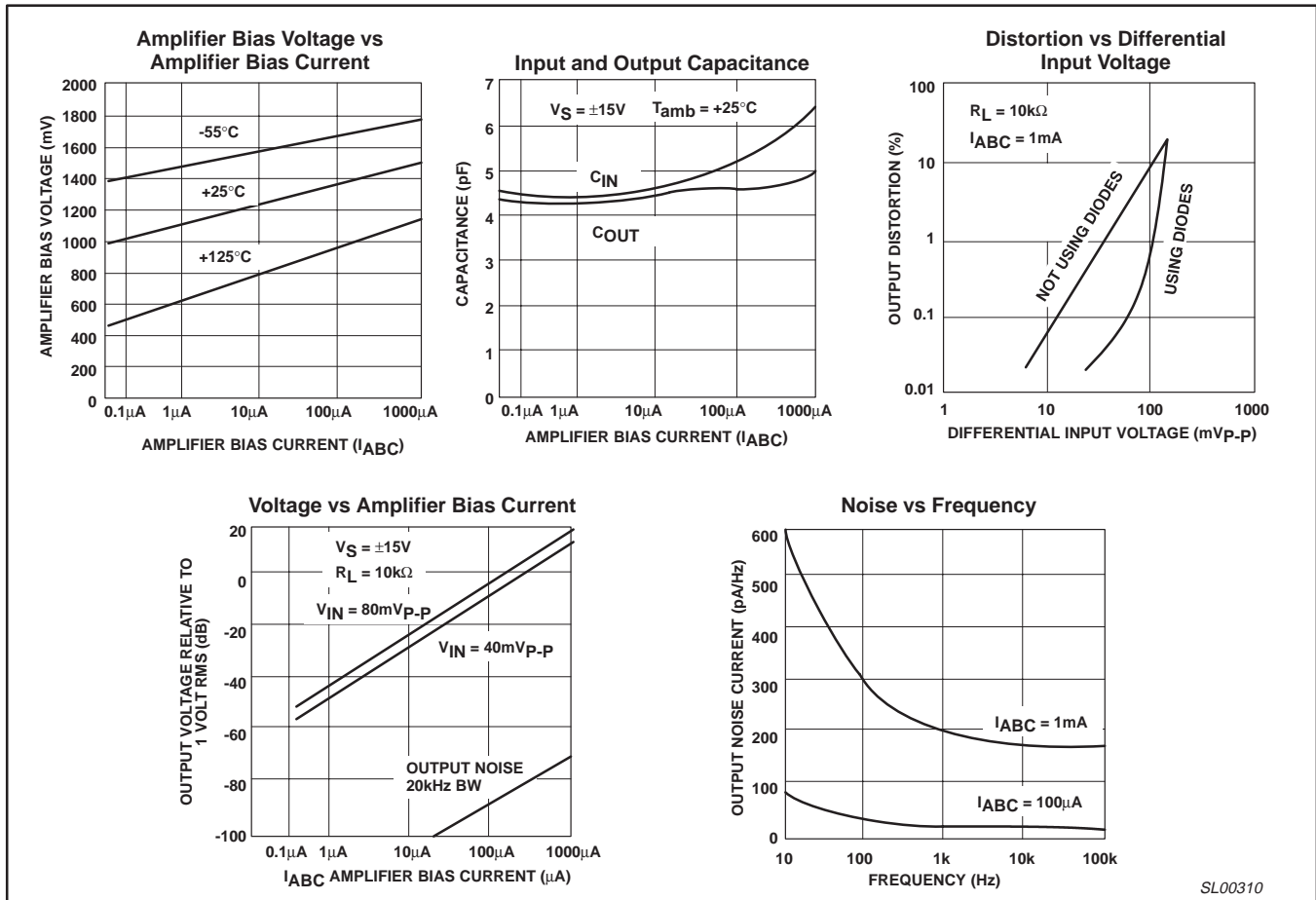
SL00309

Figure 4. Typical Performance Characteristics

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TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



SL00310

Figure 5. Typical Performance Characteristics (cont.)

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TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

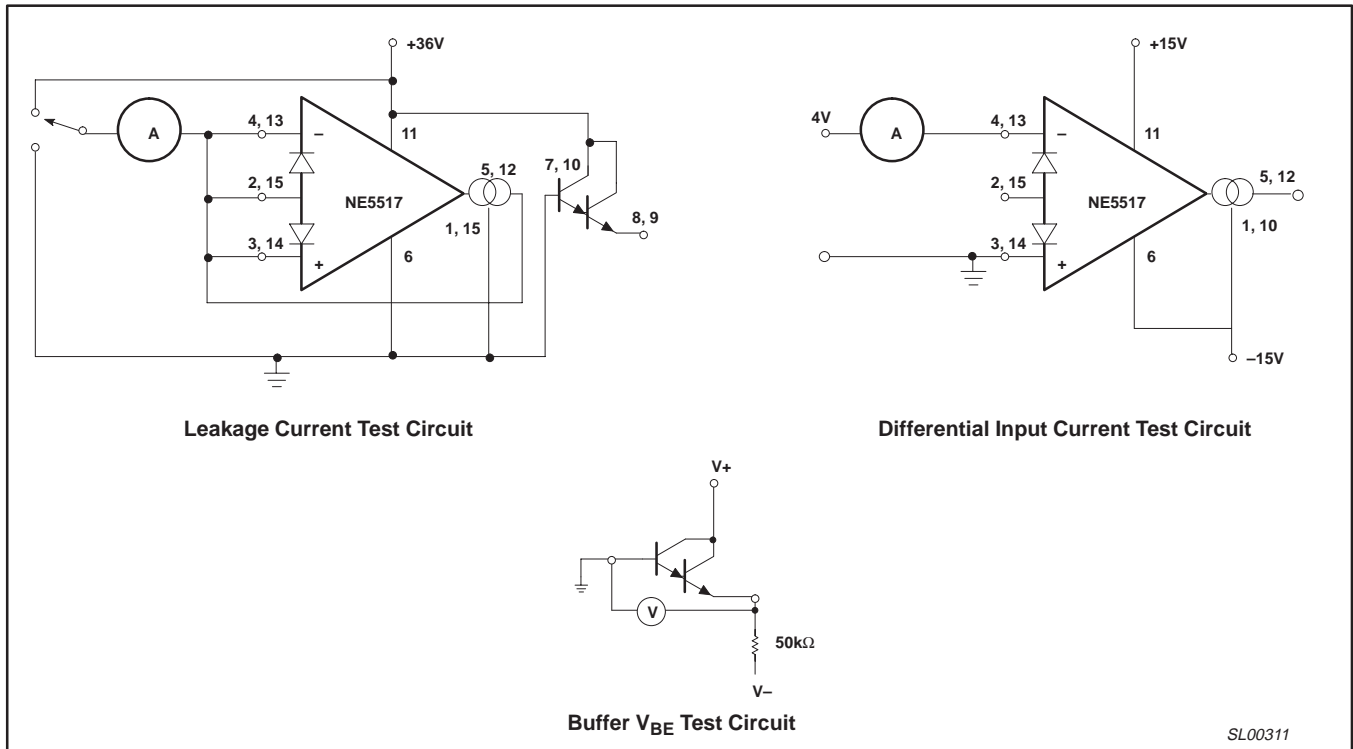


Figure 6. Typical Performance Characteristics (cont.)

APPLICATIONS

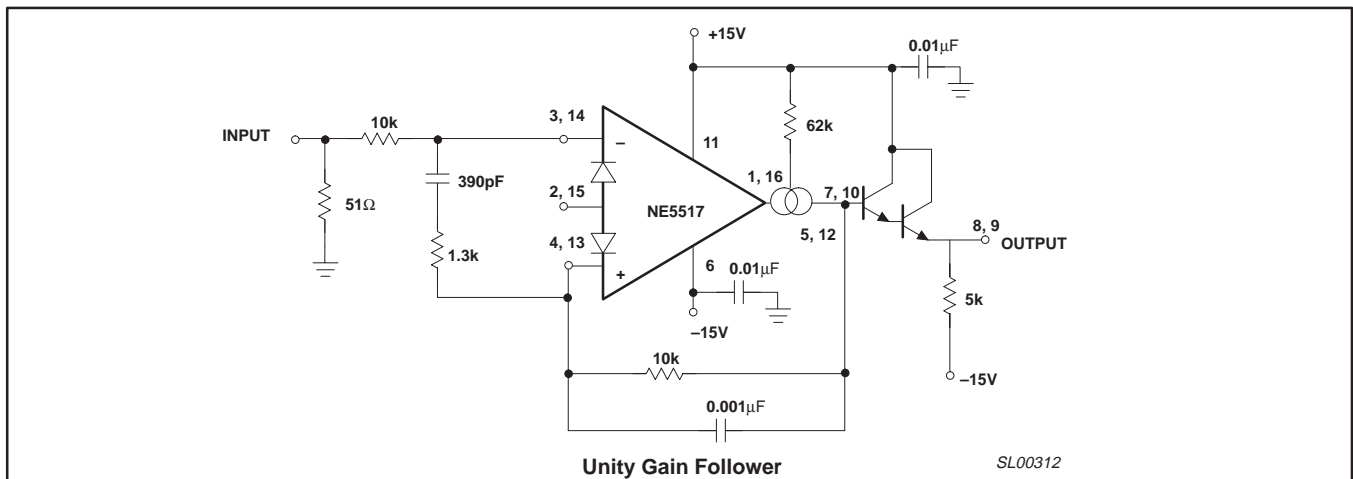


Figure 7. Applications

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CIRCUIT DESCRIPTION

The circuit schematic diagram of one-half of the NE5517, a dual operational transconductance amplifier with linearizing diodes and impedance buffers, is shown in Figure 8.

1. Transconductance Amplifier

The transistor pair, Q₄ and Q₅, forms a transconductance stage. The ratio of their collector currents (I₄ and I₅, respectively) is defined by the differential input voltage, V_{IN}, which is shown in equation 1.

$$V_{IN} = \frac{KT}{q} \ln \frac{I_5}{I_4} \quad (1)$$

Where V_{IN} is the difference of the two input voltages

$$KT \approx 26 \text{ mV at room temperature (300 °K)}.$$

Transistors Q₁, Q₂ and diode D₁ form a current mirror which focuses the sum of current I₄ and I₅ to be equal to amplifier bias current I_B:

$$I_4 + I_5 = I_B \quad (2)$$

If V_{IN} is small, the ratio of I₅ and I₄ will approach unity and the Taylor series of ln function can be approximated as

$$\frac{KT}{q} \ln \frac{I_5}{I_4} \approx \frac{KT}{q} \frac{I_5 - I_4}{I_4} \quad (3)$$

and I₄ ≈ I₅ ≈ I_B

$$\frac{KT}{q} \ln \frac{I_5}{I_4} \approx \frac{KT}{q} \frac{I_5 - I_4}{1/2 I_B} = \frac{2KT}{q} \frac{I_5 - I_4}{I_B} = V_{IN}^{(4)}$$

$$I_5 - I_4 = V_{IN} \frac{(I_B^q)}{2KT}$$

The remaining transistors (Q₆ to Q₁₁) and diodes (D₄ to D₆) form three current mirrors that produce an output current equal to I₅ minus I₄. Thus:

$$V_{IN} \left(I_B \frac{q}{2KT} \right) = I_O \quad (5)$$

The term $\frac{(I_B^q)}{2KT}$ is then the transconductance of the amplifier and is proportional to I_B.

2. Linearizing Diodes

For V_{IN} greater than a few millivolts, equation 3 becomes invalid and the transconductance increases non-linearly. Figure 9 shows how the internal diodes can linearize the transfer function of the operational amplifier. Assume D₂ and D₃ are biased with current sources and the input signal current is I_S. Since

I₄ + I₅ = I_B and I₅ - I₄ = I_O, that is:

$$I_4 = (I_B - I_O), I_5 = (I_B + I_O)$$

For the diodes and the input transistors that have identical geometries and are subject to similar voltages and temperatures, the following equation is true:

$$\frac{I_O}{I_S} \ln \frac{\frac{I_D}{2} + I_S}{\frac{I_D}{2} - I_S} = \frac{KT}{q} \ln \frac{1/2(I_B + I_O)}{1/2(I_B - I_O)} \quad (6)$$

$$I_O = I_S \frac{2I_D}{I_D} \text{ for } |I_S| < \frac{I_D}{2}$$

The only limitation is that the signal current should not exceed I_D.

3. Impedance Buffer

The upper limit of transconductance is defined by the maximum value of I_B (2 mA). The lowest value of I_B for which the amplifier will function therefore determines the overall dynamic range. At low values of I_B, a buffer with very low input bias current is desired. A Darlington amplifier with constant-current source (Q₁₄, Q₁₅, Q₁₆, D₇, D₈, and R₁) suits the need.

APPLICATIONS**Voltage-Controlled Amplifier**

In Figure 10, the voltage divider R₂, R₃ divides the input-voltage into small values (mV range) so the amplifier operates in a linear manner.

It is:

$$I_{OUT} = -V_{IN} \cdot \frac{R_3}{R_2 + R_3} \cdot g_M;$$

$$V_{OUT} = I_{OUT} \cdot R_L;$$

$$A = \frac{V_{OUT}}{V_{IN}} = \frac{R_3}{R_2 + R_3} \cdot g_M \cdot R_L$$

$$(3) g_M = 19.2 I_{ABC}$$

$$(g_M \text{ in } \mu\text{mhos for } I_{ABC} \text{ in mA})$$

Since g_M is directly proportional to I_{ABC}, the amplification is controlled by the voltage V_C in a simple way.

When V_C is taken relative to -V_{CC} the following formula is valid:

$$I_{ABC} = \frac{(V_C - 1.2V)}{R_1}$$

The 1.2 V is the voltage across two base-emitter baths in the current mirrors. This circuit is the base for many applications of the NE5517.

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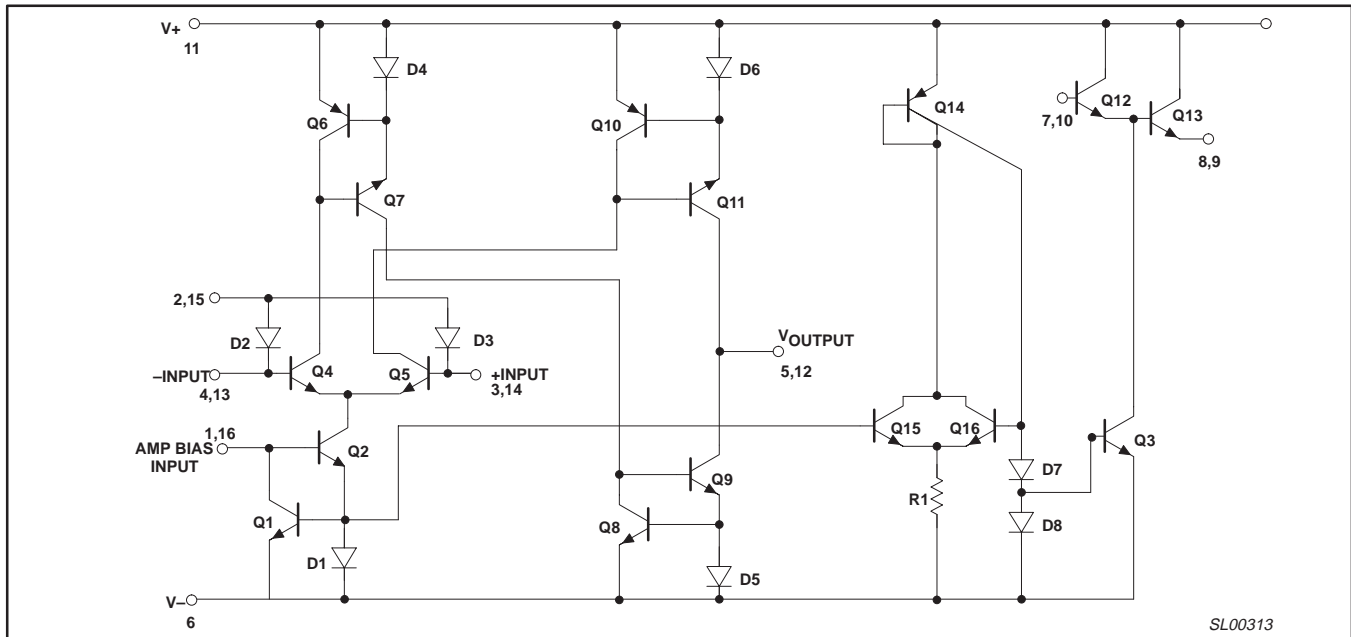


Figure 8. Circuit Diagram of NE5517

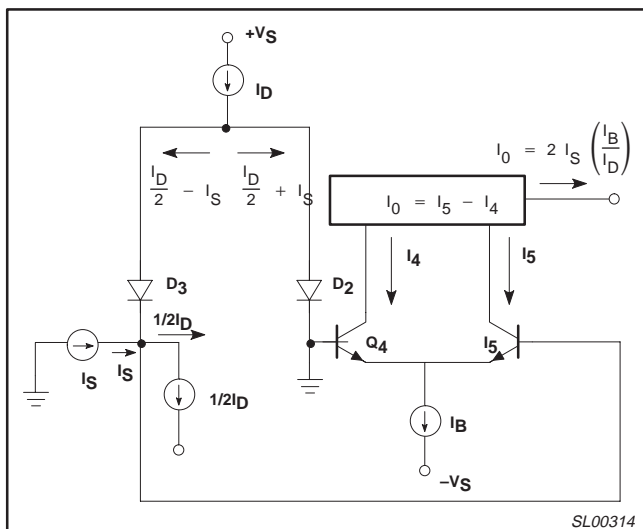


Figure 9. Linearizing Diode

Stereo Amplifier With Gain Control

Figure 11 shows a stereo amplifier with variable gain via a control input. Excellent tracking of typical 0.3 dB is easy to achieve. With the potentiometer, R_P , the offset can be adjusted. For AC-coupled amplifiers, the potentiometer may be replaced with two 510 Ω resistors.

Modulators

Because the transconductance of an OTA (Operational Transconductance Amplifier) is directly proportional to I_{ABC} , the amplification of a signal can be controlled easily. The output current is the product from transconductance \times input voltage. The circuit is effective up to approximately 200 kHz. Modulation of 99% is easy to achieve.

Voltage-Controlled Resistor (VCR)

Because an OTA is capable of producing an output current proportional to the input voltage, a voltage variable resistor can be made. Figure 13 shows how this is done. A voltage presented at the R_X terminals forces a voltage at the input. This voltage is multiplied by g_M and thereby forces a current through the R_X terminals:

$$R_X = \frac{R + R_A}{g_M + R_A}$$

where g_M is approximately 19.21 μ MHOs at room temperature. Figure 14 shows a Voltage Controlled Resistor using linearizing diodes. This improves the noise performance of the resistor.

Voltage-Controlled Filters

Figure 15 shows a Voltage Controlled Low-Pass Filter. The circuit is a unity gain buffer until X_C/g_M is equal to R/R_A . Then, the frequency response rolls off at a 6dB per octave with the -3 dB point being defined by the given equations. Operating in the same manner, a Voltage Controlled High-Pass Filter is shown in Figure 16. Higher order filters can be made using additional amplifiers as shown in Figures 17 and 18.

Voltage-Controlled Oscillators

Figure 19 shows a voltage-controlled triangle-square wave generator. With the indicated values a range from 2 Hz to 200 kHz is possible by varying I_{ABC} from 1 mA to 10 μ A.

The output amplitude is determined by $I_{OUT} \times R_{OUT}$.

Please notice the differential input voltage is not allowed to be above 5 V.

With a slight modification of this circuit you can get the sawtooth pulse generator, as shown in Figure 20.

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APPLICATION HINTS

To hold the transconductance g_M within the linear range, I_{ABC} should be chosen not greater than 1 mA. The current mirror ratio should be as accurate as possible over the entire current range. A current mirror with only two transistors is not recommended. A suitable current mirror can be built with a PNP transistor array which causes excellent matching and thermal coupling among the

transistors. The output current range of the DAC normally reaches from 0 to -2 mA. In this application, however, the current range is set through R_{REF} (10 k Ω) to 0 to -1 mA.

$$I_{DACMAX} = 2 \cdot \frac{V_{REF}}{R_{REF}} = 2 \cdot \frac{-5V}{10k\Omega} = 1mA$$

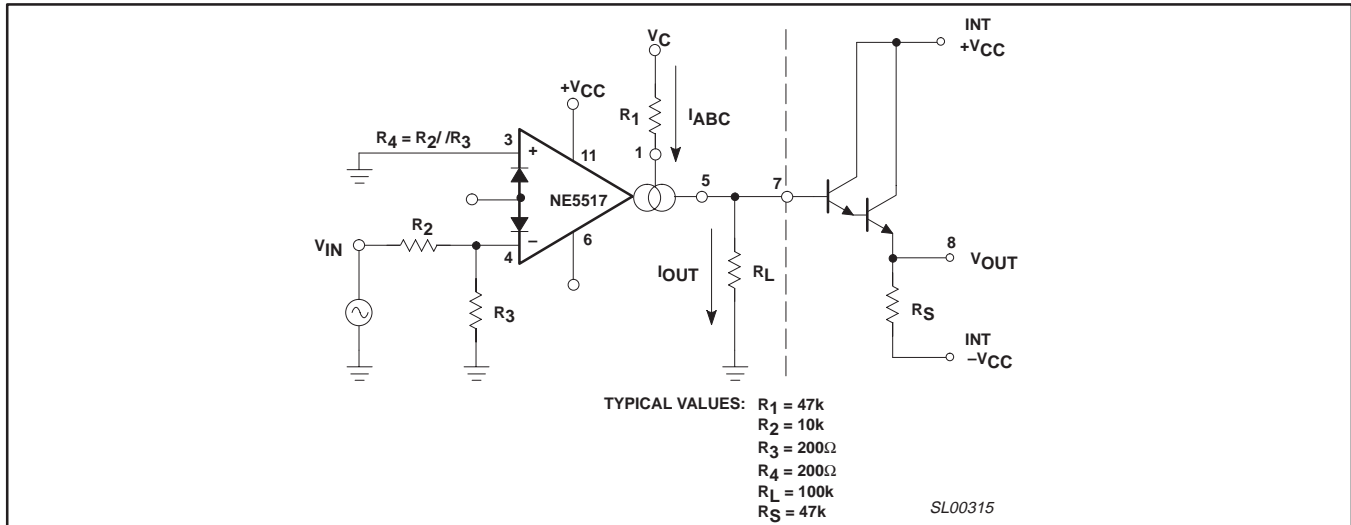


Figure 10.

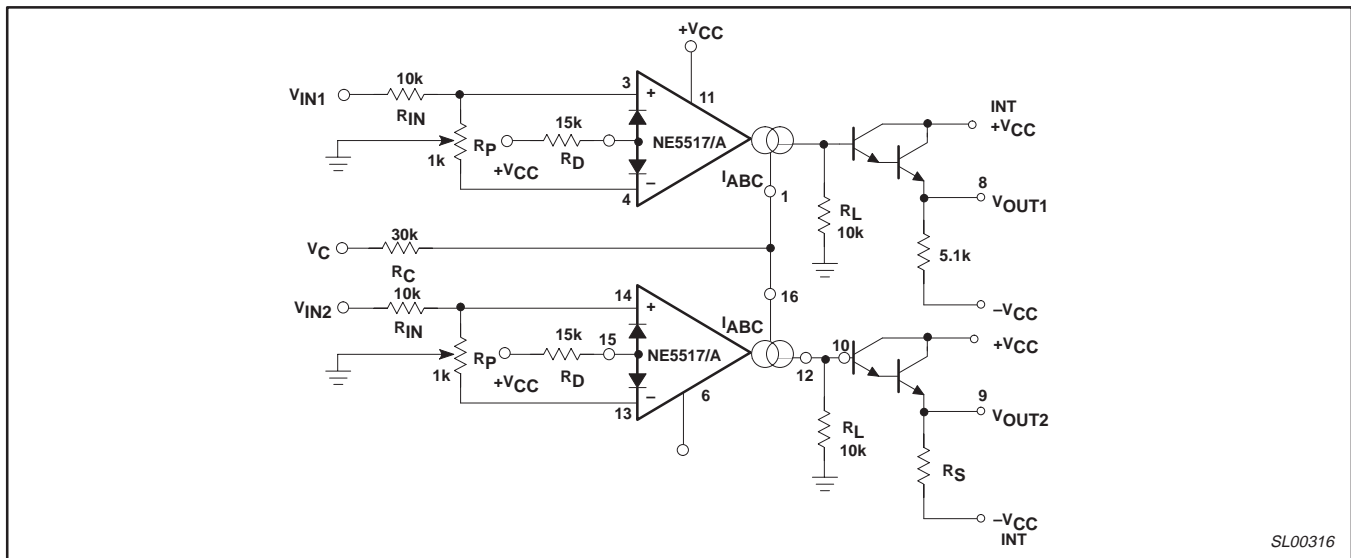


Figure 11. Gain-Controlled Stereo Amplifier

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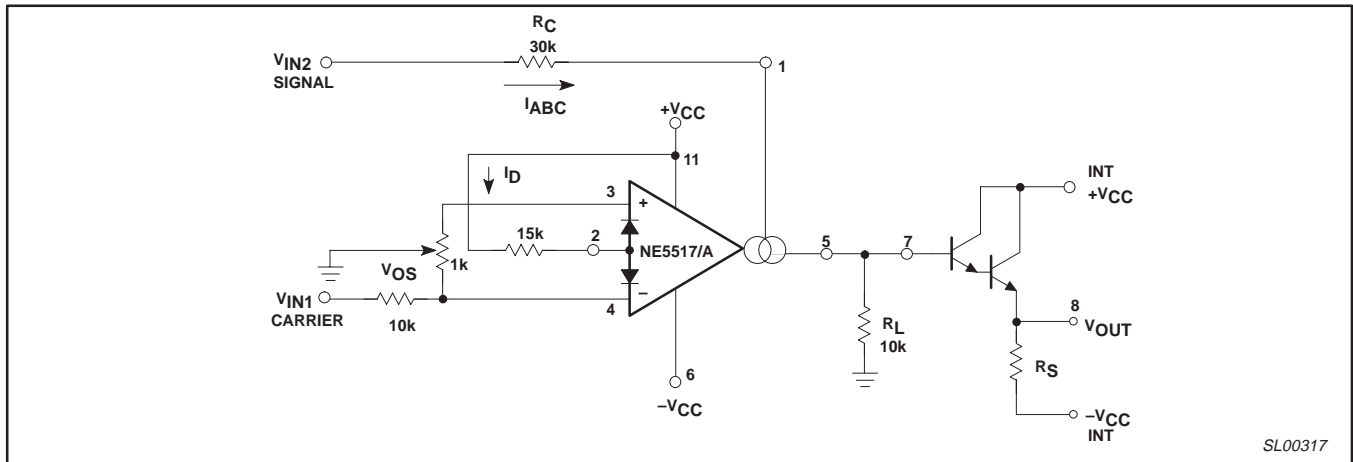


Figure 12. Amplitude Modulator

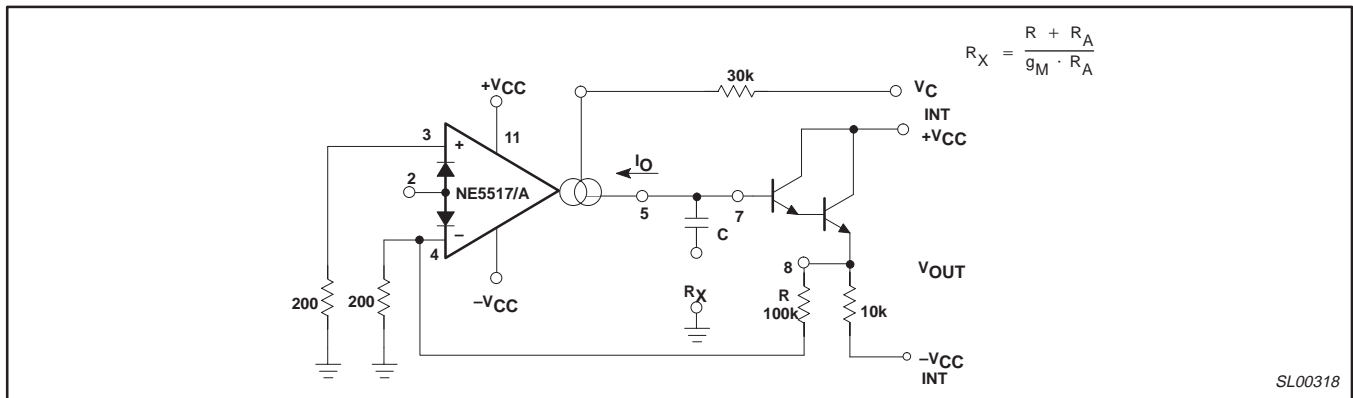


Figure 13. VCR

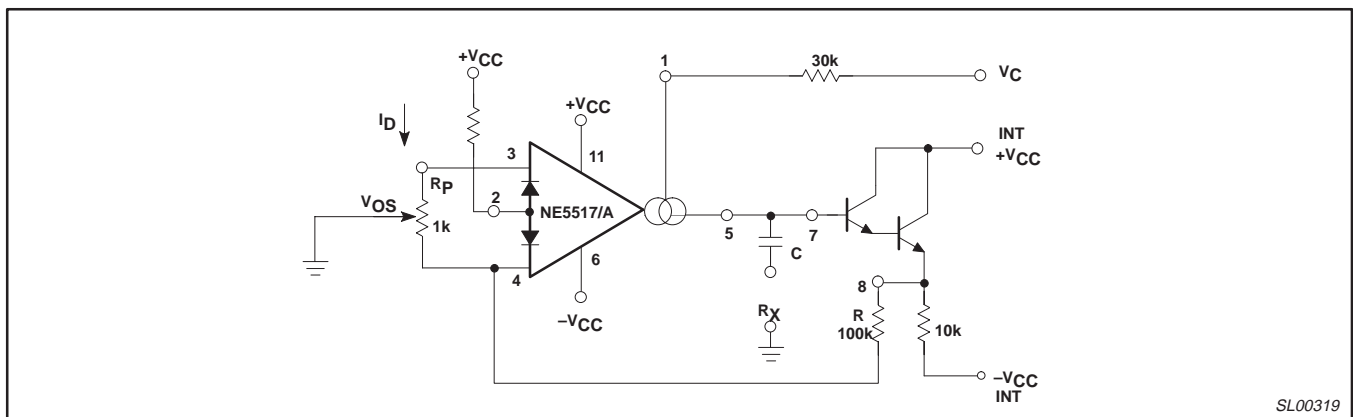


Figure 14. VCR with Linearizing Diodes

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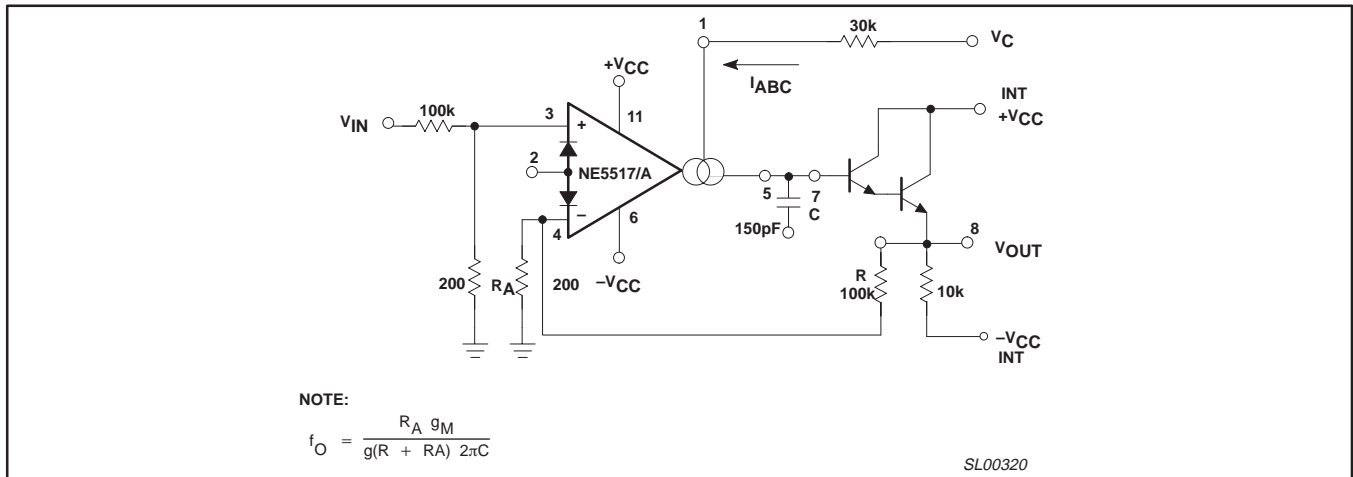


Figure 15. Voltage-Controlled Low-Pass Filter

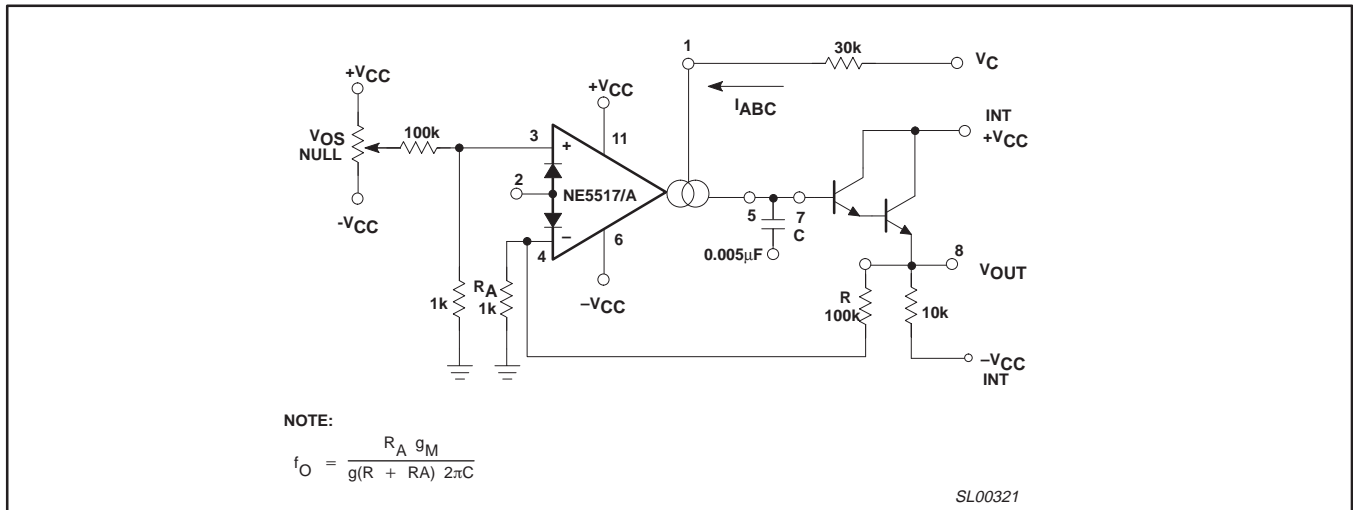


Figure 16. Voltage-Controlled High-Pass Filter

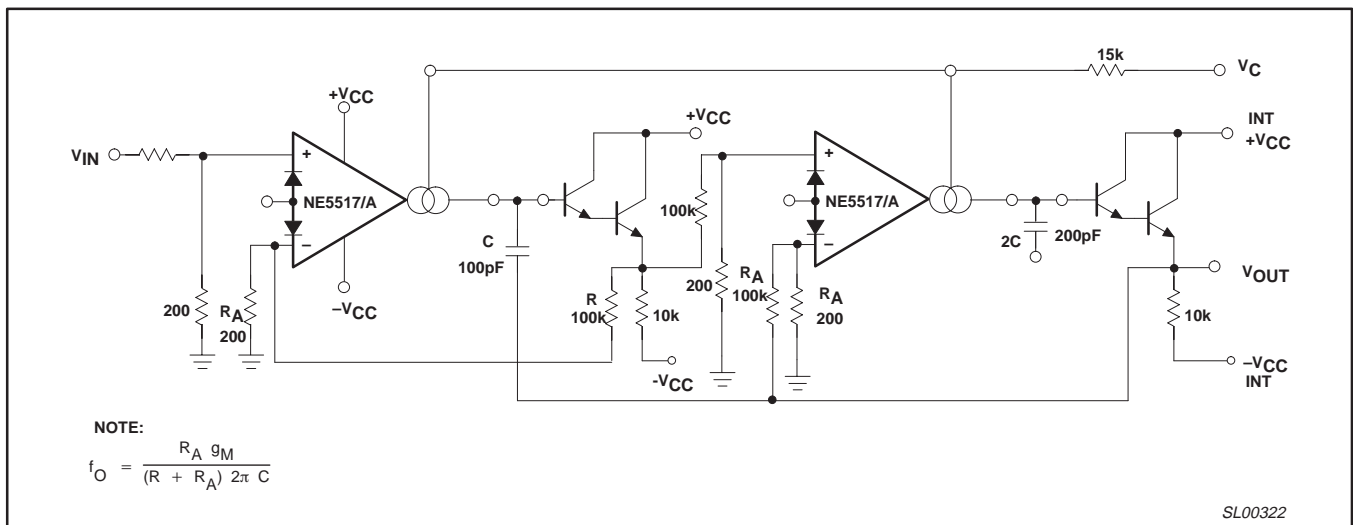


Figure 17. Butterworth Filter – 2nd Order

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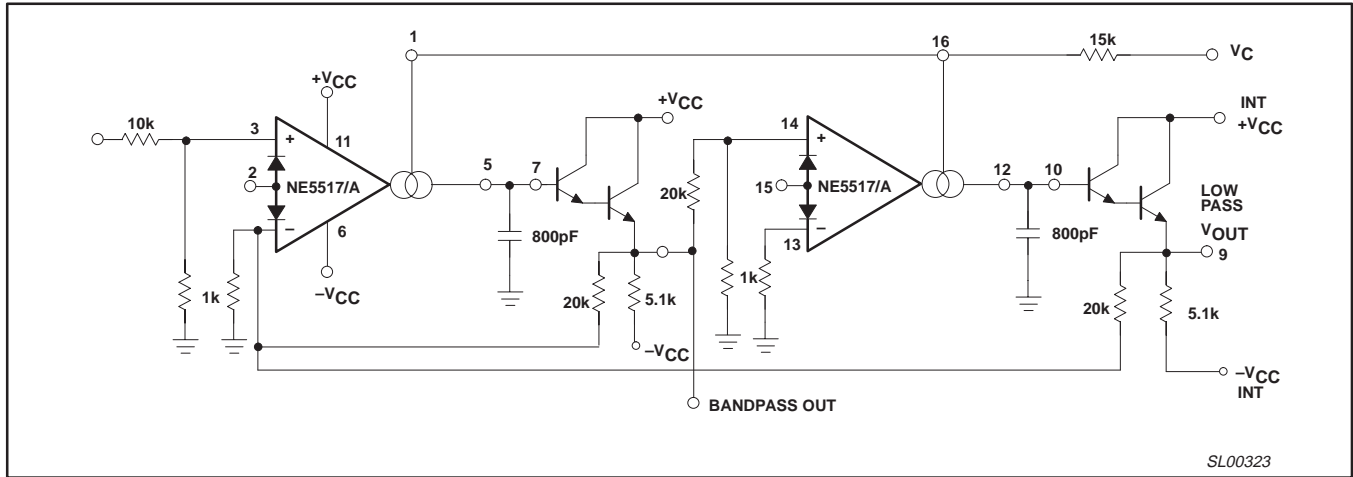


Figure 18. State Variable Filter

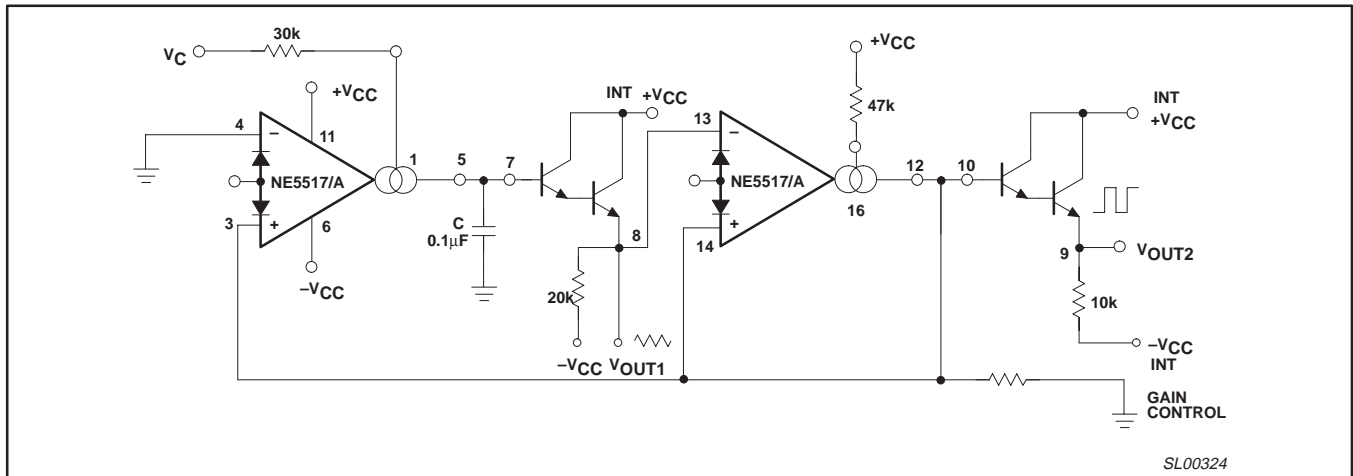


Figure 19. Triangle-Square Wave Generator (VCO)

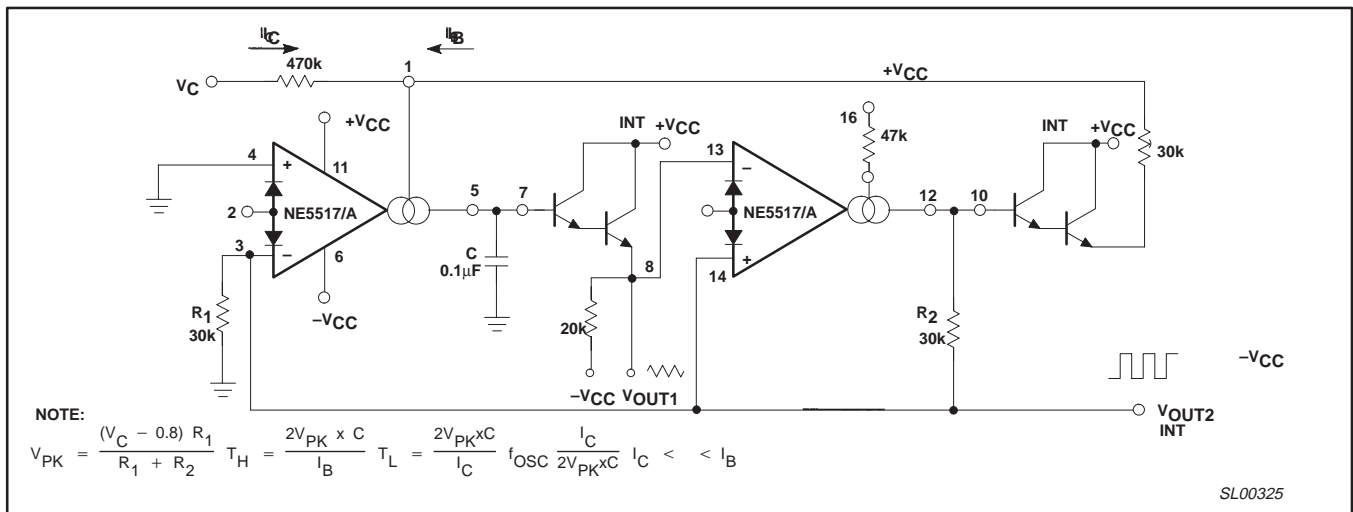


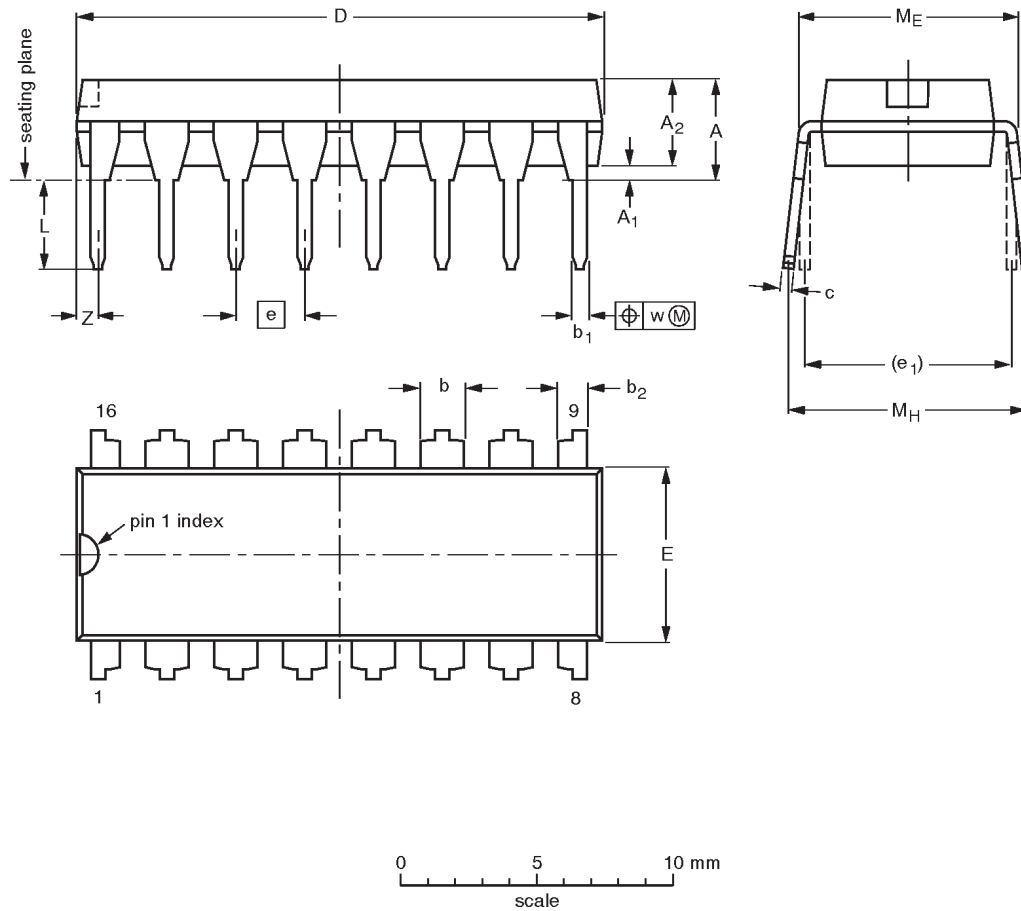
Figure 20. Sawtooth Pulse VCO

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DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	b ₂	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

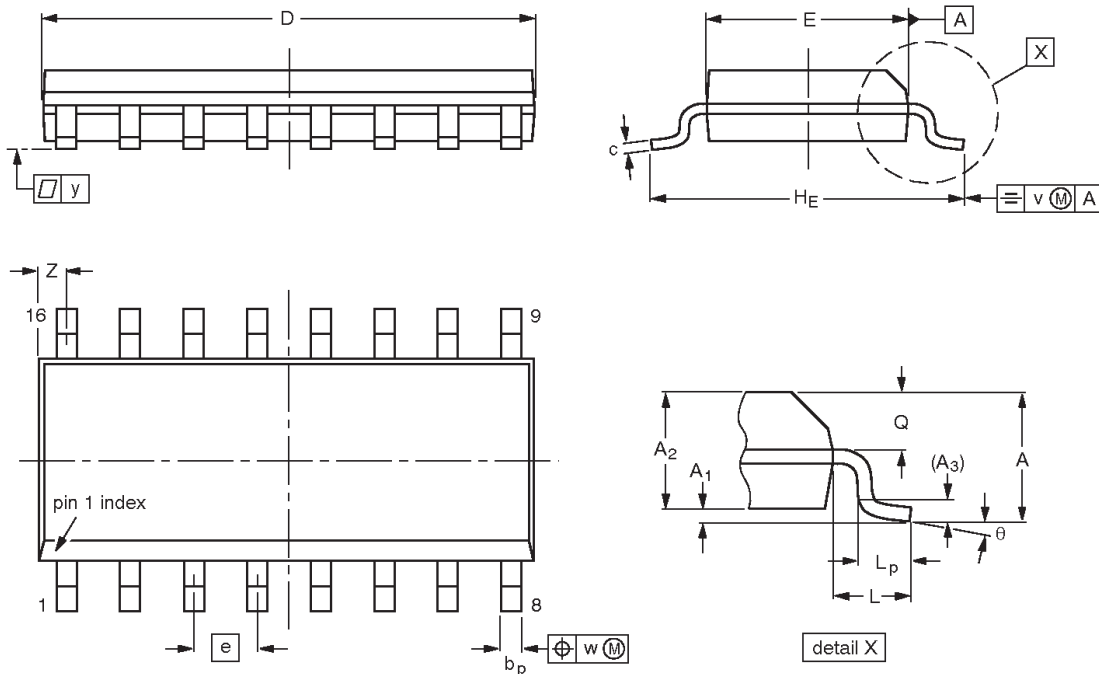
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						92-11-17 95-01-14

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SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07	MS-012				97-05-22- 99-12-27

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NOTES

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Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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