National Semiconductor

MICROCIRCUIT DATA SHEET

MNLM124A-X REV 1A3

Original Creation Date: 07/07/95
Last Update Date: 12/04/01
Last Major Revision Date: 05/21/01

LOW POWER QUAD OPERATIONAL AMPLIFIER

General Description

The LM124A consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124A can be directly operated off of the standard +5Vdc power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15Vdc power supplies.

Industry Part Number

LM124A

NS Part Numbers

LM124AE/883
LM124AJ/883
LM124AW/883
LM124AWG/883

Prime Die

LM1902

Controlling Document

SEE FEATURES SECTION

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Internally frequency compensated for unity gain.
- Large DC voltage gain. 100dB
- Wide bandwidth (unity gain) 1MHz
  (temperature compensated)
- Wide power supply range:
  Single supply 3V or 32V
  or dual supply ±1.5V to ±16V
- Very low supply current drain (700uA) - essentially independent of supply voltage.
- Low input baising current 45nA
  (temperature compensated)
- Low input offset voltage 2mV
  and offset current 5nA
- Input common-mode voltage range includes ground.
- Differential input voltage range equal to the power supply voltage.
- Large output voltage swing. 0V to V+ - 1.5V

CONTROLLING DOCUMENTS:

LM124AE/883	77043022A
LM124AJ/883	7704302CA
LM124AWG/883	7704302XA

(Absolute Maximum Ratings)

(Note 1)

Supply Voltage V+		32Vdc or ±16Vdc
Differential Input Voltage		32Vdc
Input Voltage		-0.3Vdc to +32Vdc
Input Current (Note 4)		
Vin < -0.3Vdc		50mA
Power Dissipation (Note 2)		
CERDIP		1260mW
CERPACK		700mW
LCC		1350mW
CERAMIC SOIC		700mW
Output Short-Circuit to GND (Note 3)		
(One Amplifier)		
V+ ≤ 15Vdc and TA = 25 C		Continuous
Operating Temperature Range		-55 C ≤ Ta ≤ +125 C
Maximum Junction Temperature		150 C
Storage Temperature Range		-65 C ≤ Ta ≤ +150 C
Lead Temperature		
Soldering, (10 seconds)		260 C
Thermal Resistance		
ThetaJA		
CERDIP	(Still Air)	103 C/W
	(500LF/Min Air flow)	51 C/W
CERPACK	(Still Air)	176 C/W
	(500LF/Min Air flow)	116 C/W
LCC	(Still Air)	91 C/W
	(500LF/Min Air flow)	66 C/W
CERAMIC SOIC	(Still Air)	176 C/W
	(500LF/Min Air flow)	116 C/W
ThetaJC		
CERDIP		19 C/W
CERPACK		18 C/W
LCC		24 C/W
CERAMIC SOIC		18 C/W
Package Weight (Typical)		
CERDIP		TBD
CERPACK		TBD
LCC		TBD
CERAMIC SOIC		410mg
ESD Tolerance (Note 5)		250V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Rating indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Short circuits from the output to V+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40mA independent of the magnitude of V+. At values of supply voltage in excess of +15Vdc, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 4: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3Vdc (at 25 C).

Note 5: Human body model, 1.5K Ohms in series with 100pF.

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: All voltages referenced to device ground.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Icc	Power Supply Current	V+ = 5V				1.2	mA	1, 2, 3
		V+ = 30V				3.0	mA	1
						4.0	mA	2, 3
Isink	Output Sink Current	V+ = 15V, Vout = 200mV, +Vin = 0mV, -Vin = +65mV			12		uA	1
		V+ = 15V, Vout = 2V, +Vin = 0mV, -Vin = +65mV			10		mA	1
					5		mA	2, 3
Isource	Output Source Current	V+ = 15V, Vout = 2V, +Vin = 0mV, -Vin = -65mV				-20	mA	1
						-10	mA	2, 3
Ios	Short Circuit Current	V+ = 5V, Vout = 0V			-60		mA	1
Vio	Input Offset Voltage	V+ = 30V, Vcm = 0V			-2	2	mV	1
					-4	4	mV	2, 3
		V+ = 30V, Vcm = 28.5V			-2	2	mV	1
		V+ = 30V, Vcm = 28V			-4	4	mV	2, 3
		V+ = 5V, Vcm = 0V			-2	2	mV	1
					-4	4	mV	2, 3
CMRR	Common Mode Rejection Ratio	V+ = 30V, Vin = 0V to 28.5V			70		dB	1
±Iib	Input Bias Current	V+ = 5V, Vcm = 0V			-50	10	nA	1
±Iib	Input Bias Current	V+ = 5V, Vcm = 0V			-100	10	nA	2, 3
Iio	Input Offset Current	V+ = 5V, Vcm = 0V			-10	10	nA	1
					-30	30	nA	2, 3
PSRR	Power Supply Rejection Ratio	V+ = 5V to 30V, Vcm = 0V			65		dB	1
Vcm	Common Mode Voltage	V+ = 30V	1			28.5	V	1
			1			28	V	2, 3
Avs	Large Signal Gain	V+ = 15V, Rl = 2K Ohms, Vo = 1V to 11V	2		50		V/mV	4
			2		25		V/mV	5, 6

Electrical Characteristics

DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: All voltages referenced to device ground.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Voh	Output Voltage High	V+ = 30V, Rl = 2K Ohms			26		V	4, 5, 6
		V+ = 30V, Rl = 10K Ohms			27		V	4, 5, 6
Vol	Output Voltage Low	V+ = 30V, Rl = 10K Ohms				40	mV	4, 5, 6
		V+ = 30V, Isink = 1uA				40	mV	4
						100	mV	5, 6
		V+ = 5V, Rl = 10K Ohms				20	mV	4, 5, 6
	Channel Separation Amp to Amp Coupling	1KHz, 20KHz	3		80		dB	4

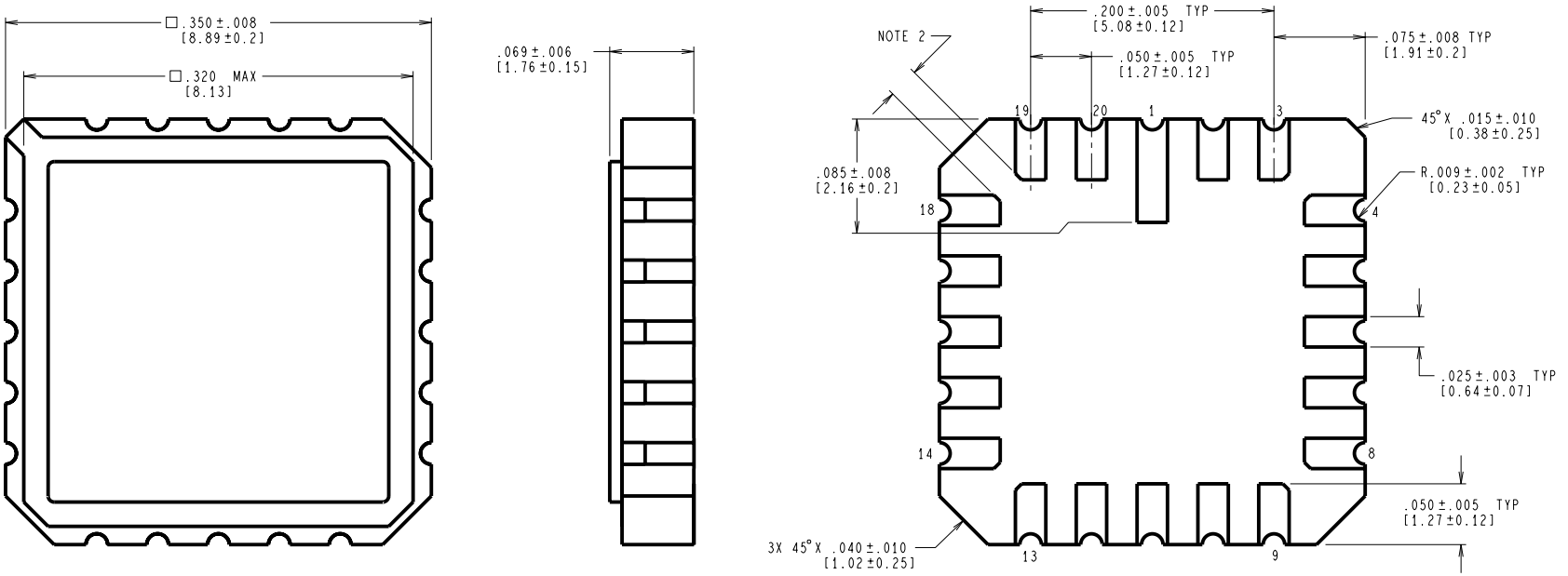
Note 1: Guaranteed by Vio tests .
Note 2: Datalog reading in K=V/mV (For Teredyne program only).
Note 3: Guaranteed, not tested

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
05275HRA4	CERPACK (W), 14 LEAD (B/I CKT)
05819HRA2	LDLESS CHIP CARRIER,TYPE C,20 TERMINAL(B/I CKT)
09173HRA2	CERDIP (J), 14 LEAD (B/I CKT)
E20ARE	LCC (E), TYPE C, 20 TERMINAL(P/P DWG)
J14ARH	CERDIP (J), 14 LEAD (P/P DWG)
P000254B	CERAMIC SOIC (WG), 14 LEAD (PINOUT)
P000288A	CERDIP (J), 14 LEAD (PINOUT)
P000318B	LCC (E), 20 LEAD (PINOUT)
P000474A	CERPACK (W), 14 LEAD (PIN OUT)
W14BRN	CERPACK (W), 14 LEAD (P/P DWG)
WG14ARC	CERAMIC SOIC (WG), 14LD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
E	REVISE AND REDRAW.	10005	02/10/94	DEG/



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH TO BE ONE OF THE FOLLOWING:

   a. 50 MICROINCHES/12.7 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICROINCHES/1.27-8.89 MICROMETERS NICKEL.

   b. SOLDER DIP.
   SOLDER THICKNESS PER LATEST REVISION OF MIL-STD-1835.

2. CORNER PADS MAY HAVE A 45°X.020IN/0.51mm MAXIMUM CHAMFER TO ACCOMPLISH THE .015IN/0.38mm DIMENSION.

4. REFERENCE JEDEC REGISTRATION MS-004, VARIATION CB, DATED 7/90.

MIL/AERO
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: Dwayne Grady	02/10/94
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION INCH [MM]

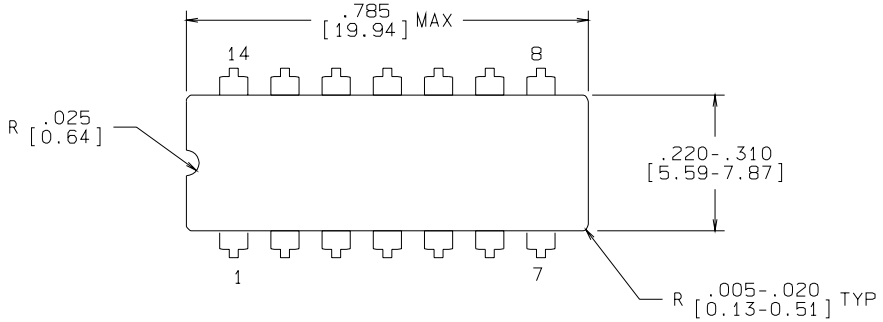
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

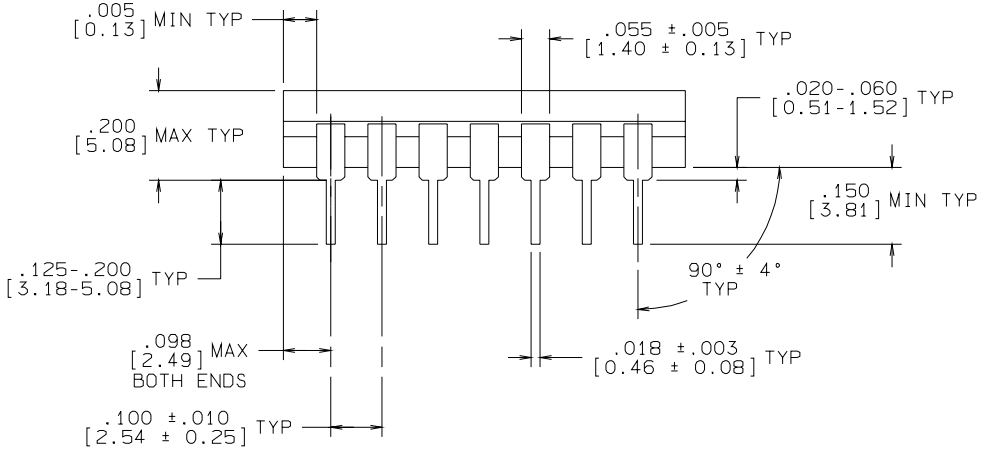
LEADLESS CHIP CARRIER, TYPE C, 20 TERMINAL

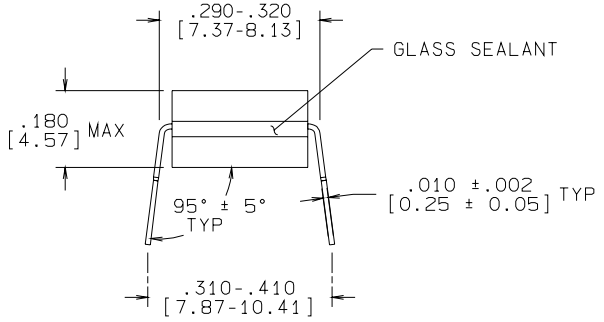
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-E20A	E

DO NOT SCALE DRAWING | SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
H	REVISE PER CURRENT STD; REDRAW	10001	09/15/93	TL/







CONTROLLING DIMENSION: INCH

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AB, DATED 04/1981.

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

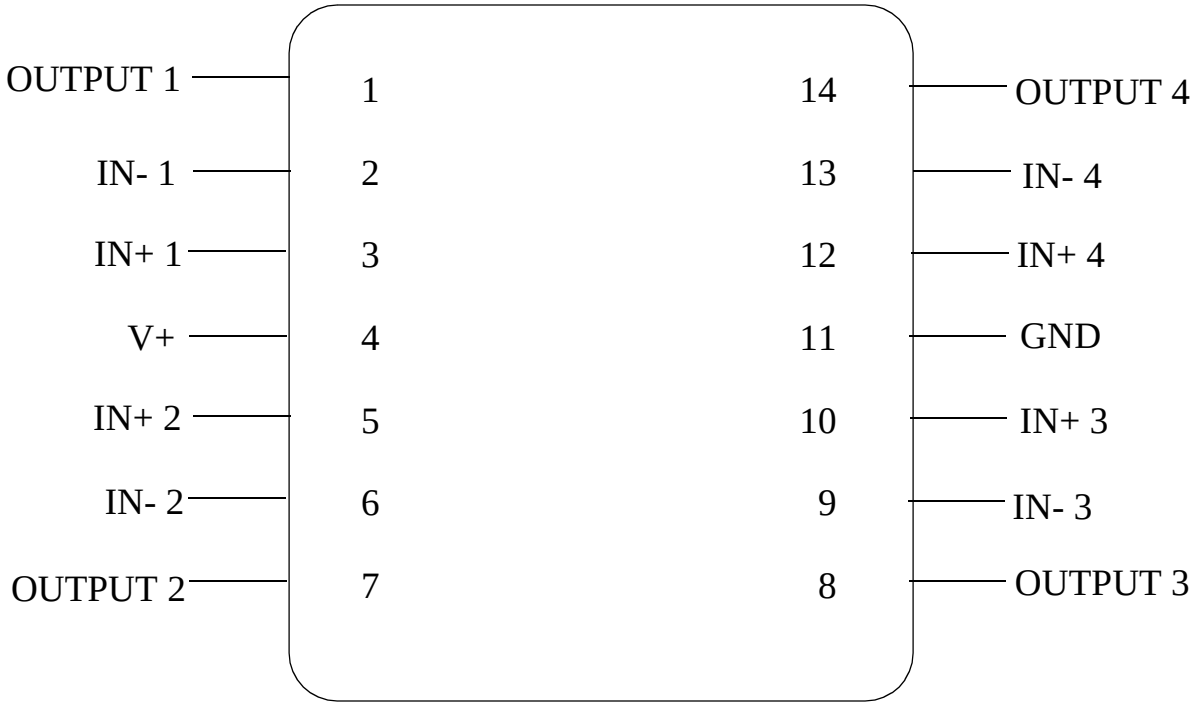
INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 14 LEAD,

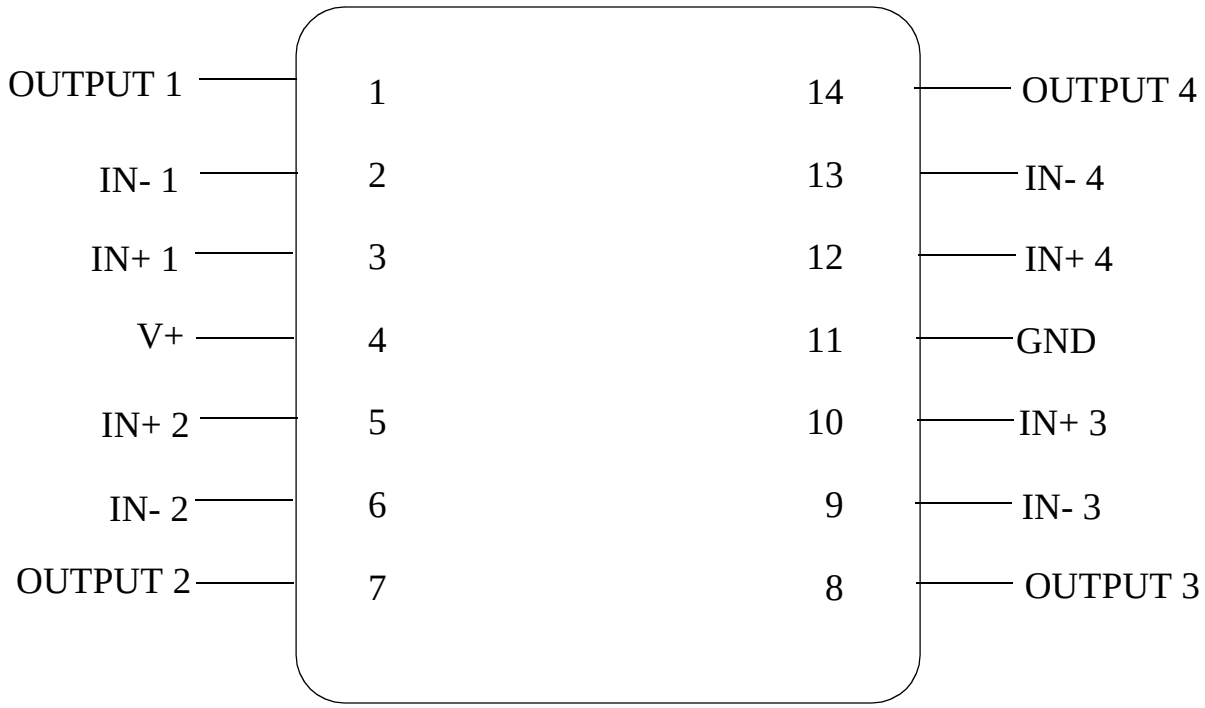
SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J14A	H

DO NOT SCALE DRAWING | SHEET 1 OF 1



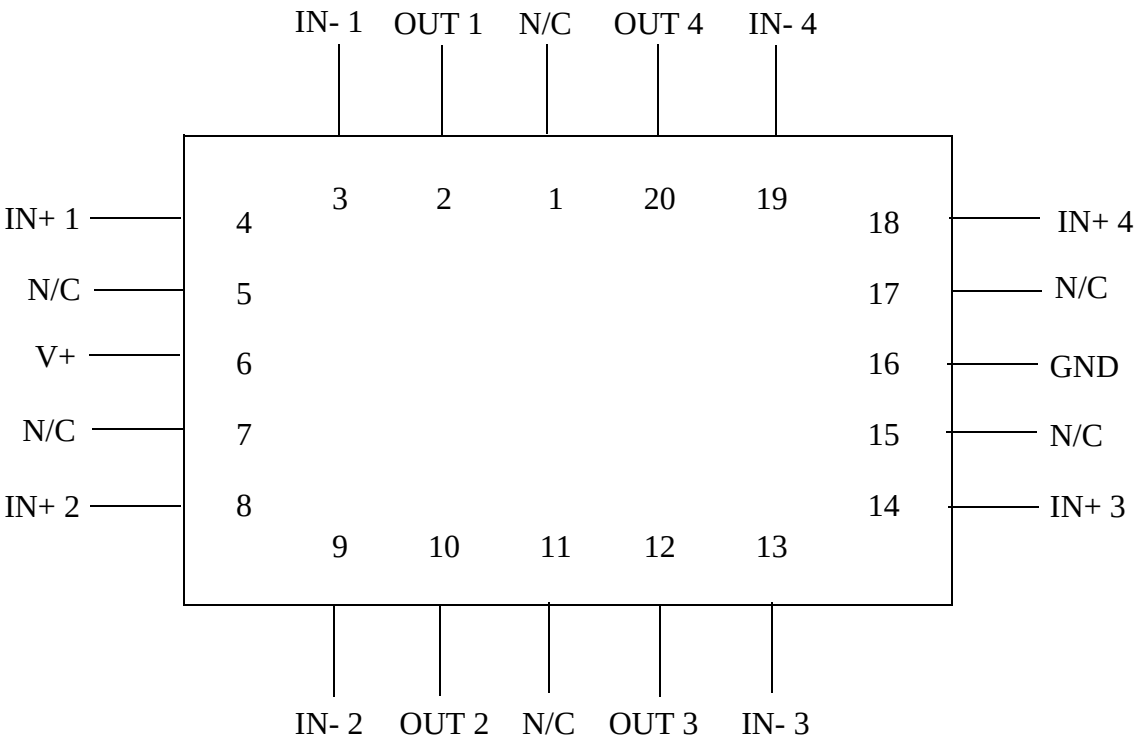
LM124AWG, LM124WG
14 - LEAD CERAMIC SOIC
CONNECTION DIAGRAM
TOP VIEW
P000254B

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM124AJ, LM124J
14 - LEAD DIP
CONNECTION DIAGRAM
TOP VIEW
P000288A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM124AE, LM124E

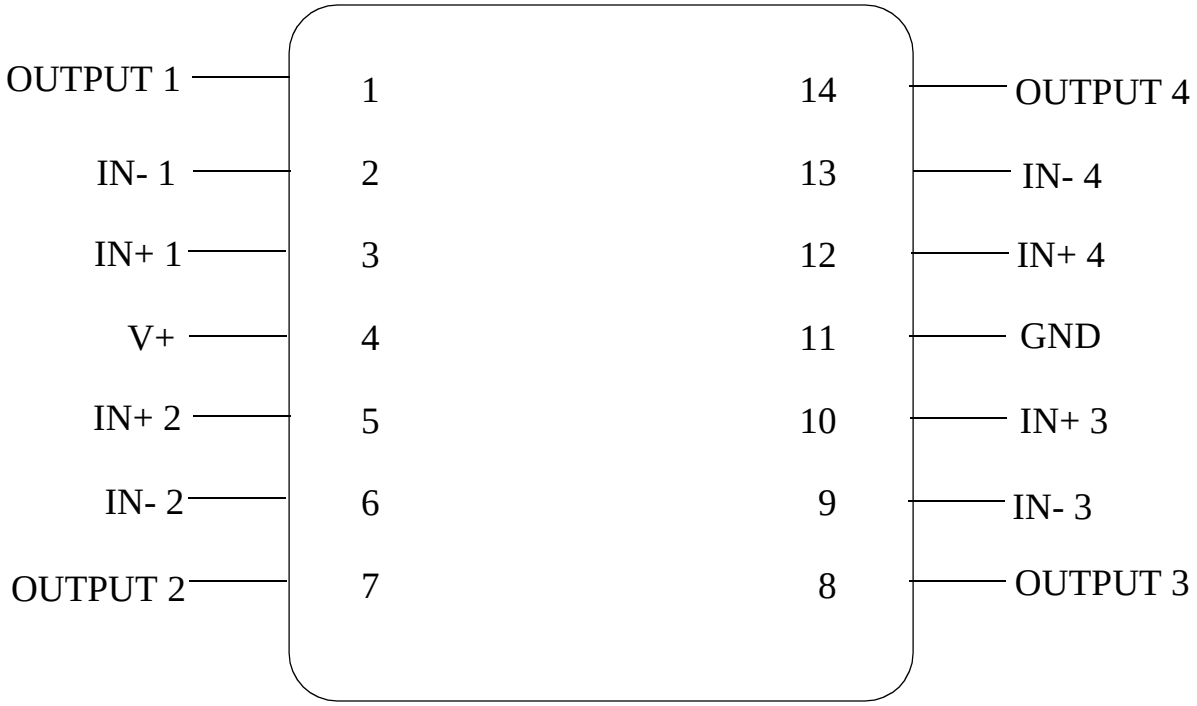
20 - LEAD LCC

CONNECTION DIAGRAM

TOP VIEW

P000318B

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM124AW, LM124W

14 - LEAD CERAMIC CERPACK

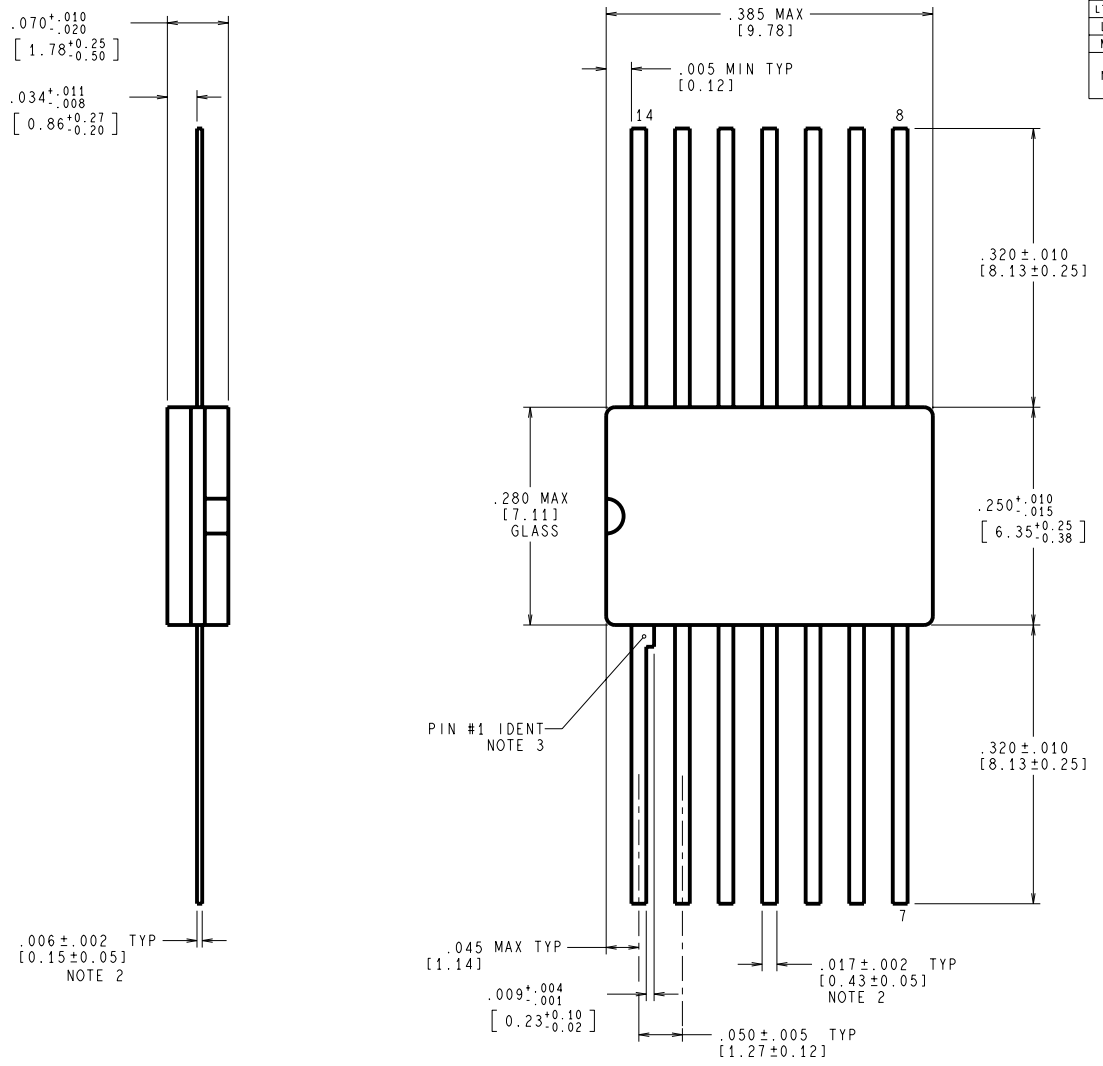
CONNECTION DIAGRAM

TOP VIEW

P000474A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE AND REDRAW PER NEW STANDARD.	10513	07/26/94	DEG/AEP
M	.017±.002 WAS .017±.020.	10655	10/21/94	DEG/CD
N	L/F THKS .006±.002 WAS .005±.001; UPDATE NOTES 1 & 2; REMOVE NOTE 4; UPDATE MILAERO STAMP; DUAL DIM'S WERE INCHES ONLY.	11005	06/08/95	MS/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-I-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. MAXIMUM LIMIT MAY BE INCREASED BY .003 INCHES/ 0.08 MILLIMETERS AFTER LEAD FINISH APPLIED.
3. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-I-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN D.E.Grady	07/26/94
DFTG. CHK.	
ENGR. CHK.	

PROJECTION INCH [MM]

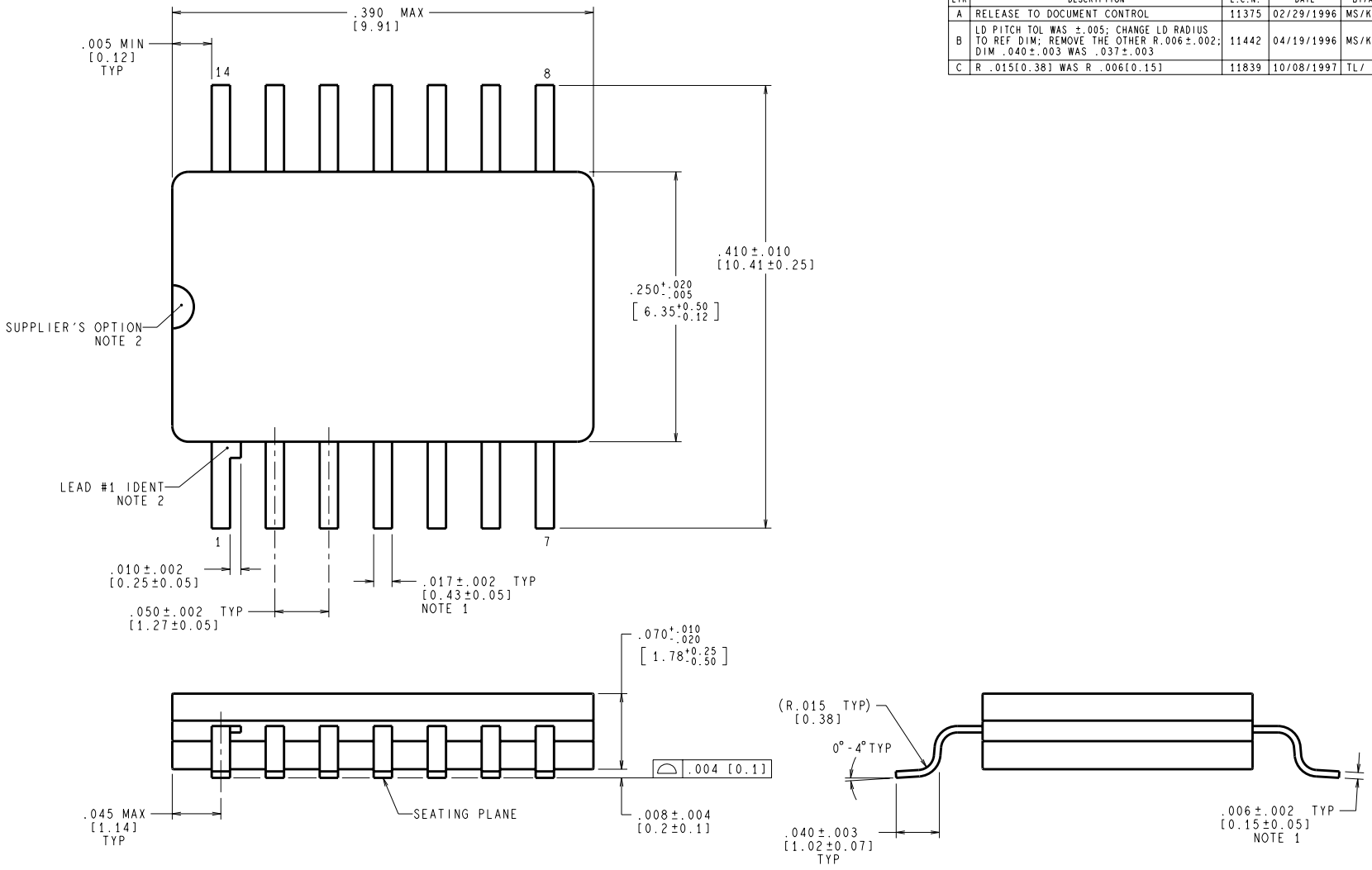
National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 14 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-W14B	N

DO NOT SCALE DRAWING | SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11375	02/29/1996	MS/KH
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002; DIM .040±.003 WAS .037±.003	11442	04/19/1996	MS/KH
C	R .015[0.38] WAS R .006[0.15]	11839	10/08/1997	TL/



NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
2. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
3. NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: MARTA SUCHY	02/29/96
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 14 LEAD, GULL WING

PROJECTION — INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	(SC)MKT-WG14A	C

DO NOT SCALE DRAWING — SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0002729	08/24/98	Barbara Lopez	Update MDS: MNLM124A-X Rev. 0BL to MNLM124A-X Rev. 0A0. Added WG Package to MDS. Added all required graphics and thermal data.
0B1	M0003007	12/15/98	Rose Malone	Update MDS: MNLM124A-X Rev. 0A0 to MNLM124A-X Rev. 0B1. Updated Burn-In graphics for all packages. Updated Pinout for E packag. Added Package Weight section.
0B2	M0003115	05/24/01	Rose Malone	Update MDS: MNLM124A-X, Rev. 0B1 to 0B2.
1A2	M0003808	12/04/01	Rose Malone	Update MDS: MNLM124A-X, Rev. 0B2 to MNLM124A-X, Rev. 1A2. Moved Controlling Document infomation to Features Section. Updated Absolute Maximum Ratings Section. CHANGED Electrical Section: Isink Conditions FROM: V+ = 15V, Vout = 200V, TO: V+ = 15V, Vout = 200V, +Vin = 0mV, -Vin = +65mV AND: V+ = 15V, Vout = 2V, TO: V+ = 15V, Vout = 2V, +Vin = 0mV, -Vin = +65mV. Isource Condition FROM: V+ = 15V, Vout = 2V, TO: V+ = 15V, Vout = 2V, +Vin = 0V, -Vin = -65mV.
1A3	M0003952	12/04/01	Rose Malone	Updated MDS: MNLM124A-X, Rev. 1A2 to MNLM124A-X, Rev. 1A3. Updated Graphics Section B/I Ckt 05275HRA3 to 05275HRA4 and Added Pin Out dwg for W pkg. P000474A