

TPS23754EVM-383 EVM: Evaluation Module for TPS23754

This User's Guide describes the TPS23754 EVM (TPS23754EVM-383). TPS23754EVM-383 contains evaluation and reference circuitry for the TPS23754. The TPS23754 is an IEEE 802.3at compliant powered device (PD) controller and power supply controller optimized for isolated converter topologies. TPS23754EVM-383 is targeted at 25W, active clamp, forward converter applications.

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1 Description

TPS23754EVM-383 will allow reference circuitry evaluation of the TPS23754. It contains input and output power connectors and an array of on board test points for circuit evaluation. A synchronous flyback, 5V, 25W EVM is also available, see [SLVU301](#).

1.1 Features

- Efficient, general market design
 - Self driven, synchronous rectified secondary
 - 25w output power from power over ethernet (POE), 30W output power from a 48V adapter
 - Operates from either POE or external adaptors (48V)
 - 12V output voltage

1.2 Applications

- Voice over Internet Protocol – IP telephones
- Wireless LAN – Wireless Access Points
- Security – Wired IP cameras

2 Electrical Specifications

Table 1. TPS23754EVM-383 Electrical and Performance Specifications

Parameter	Condition	Min	Typ	Max	Units
Power Interface					
Input voltage	Applied to the power pins of connectors J1 or J3	0		57	V
Operating Voltage	After start up	30		57	V
Input UVLO	Rising input voltage			36	V
	Falling input voltage	30			
Detection voltage	At device terminals	1.6		10	V
Classification voltage	At device terminals	10		23	V
Classification current	Rclass = 63.4 Ω	36		44	mA
Inrush current-limit		100		180	mA
Operating current-limit		850		1100	mA
DC/DC Converter					
Output voltage	$33\text{ V} \leq V_{in} \leq 57\text{ V}$, $I_{LOAD} \leq I_{LOAD}(\text{max})$				V
Output current	$33\text{ V} \leq V_{in} \leq 57\text{ V}$			2.5	Amps
Output ripple voltage, peak-to-peak	$V_{in} = 44\text{ V}$, $I_{LOAD} = 2.5\text{ A}$		100		mV
Efficiency, end-to-end	$V_{in} = 44\text{ V}$, $I_{LOAD} = 2.5\text{ A}$		87%		
Switching frequency		225		275	kHz

3 Schematic

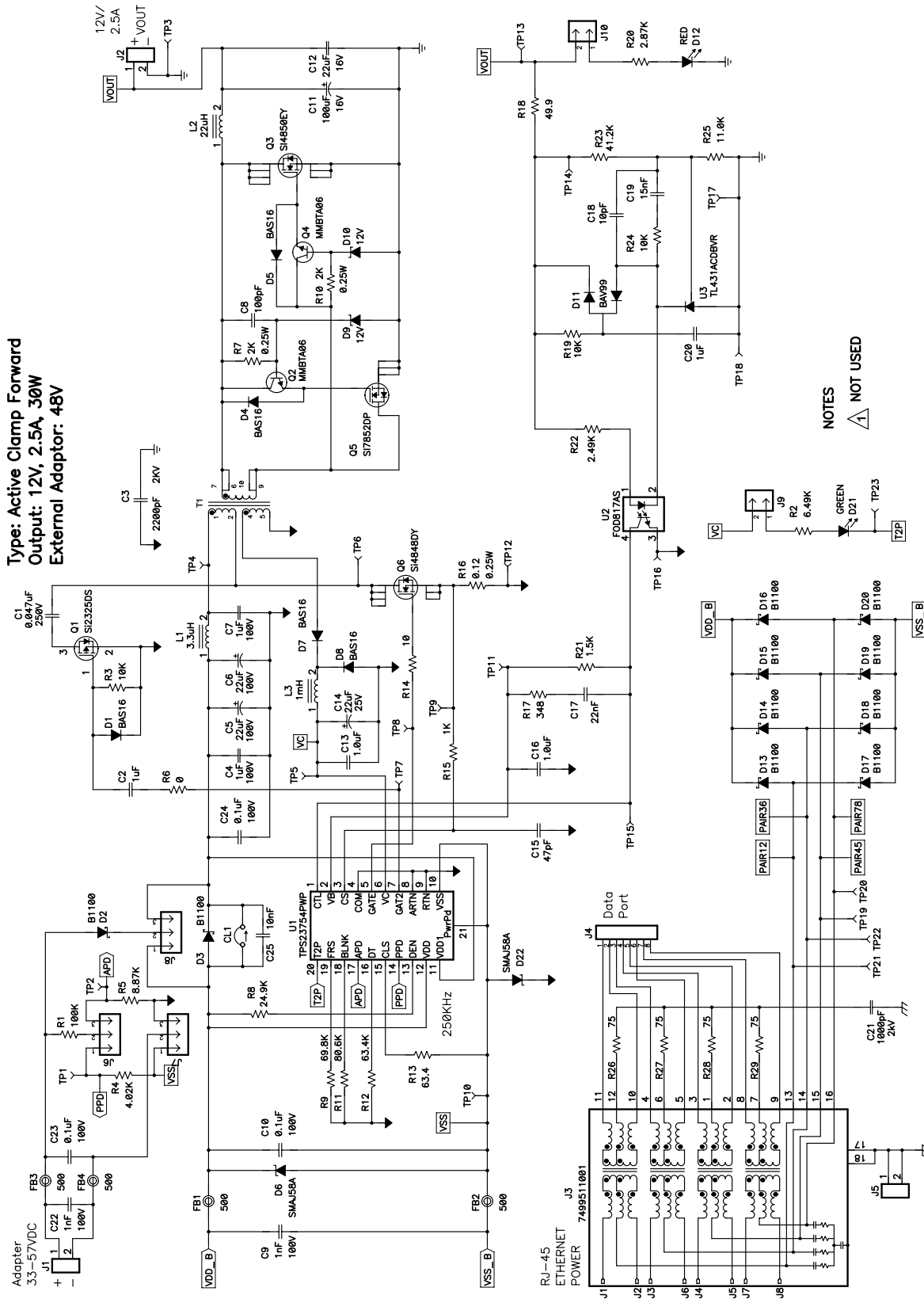


Figure 1. TPS23754EVM-383 Schematic

4 General Configuration and Description

4.1 Physical Access

Table 2 lists the TPS23754EVM-383 connector functionality and Table 3 describes the test point availability.

Table 2. Connector Functionality

Connector	Label	Description
J1	ADAPTER	External adapter input. J7 (low side) and J8 (high side) can select whether the adapter is at the PD controller input (VDD to VSS) or at the converter input (VDD1 to RTN). J6 is used to select PPD or APD function.
J2	VOUT	Output voltage connector
J3	DATA + PoE POWER	Ethernet power input connector. Contains Ethernet transformer and cable terminations
J4	DATA PORT	Ethernet data port connector
J5	EGND	Earth GND connection

Table 3. Test Points

Test Point	Color	Label	Description
TP3, TP17, TP18	BLK	GND	Secondary side (output) grounds (GND)
TP5	RED	VC	DC/DC converter bias supply
TP6	ORG	DRAIN	Drain terminal of the primary side switching MOSFET
TP10	BLK	VSS	POE input, low side
TP12, TP16	BLK	RTN	DC/DC converter return
TP14	ORG	LOOP	Can be used with TP13 for overall feedback loop measurements.
TP13	RED	VOUT	DC/DC converter output voltage.
TP15	WHT	CTL	Control loop input to the pulse width modulator
TP9	WHT	RCS	DC/DC converter primary side switching MOSFET current sense (resistor side).
TP11	RED	VB	Bias voltage regulator
TP8	WHT	GATE	Gate drive for the primary side switching MOSFET
TP7	WHT	GAT2	Gate drive for the primary side active clamp MOSFET
TP4	RED	PVDD1	Transformer primary high side.
TP23	WHT	T2P	Type 2 PSE output from TPS23754
TP1	WHT	PPD	Connected to PPD pin of TPS23754
TP2	WHT	APD	Connected to APD pin of TPS23754
TP20	RED	P78	Pair 7,8
TP21	ORG	P12	Pair 1,2
TP19	ORG	P45	Pair 4,5
TP22	RED	P36	Pair 3,6
D21	GRN	T2P	Type 2 PSE indicator. Remove the shunt on J9 to inhibit the T2P indicator.
D12	RED	POWER ON	Output power indicator. Remove the shunt on J10 to inhibit the output power indicator.
CL1	N/A	CL1	Provides a connection between VDD and VDD1 shorting out D3. Removing the short at CL1 allows certain power source priority schemes to be tested.

5 Test Setup

Figure 2 shows a typical test setup for TPS23754EVM-383. Input voltage can be applied as described in Table 2.

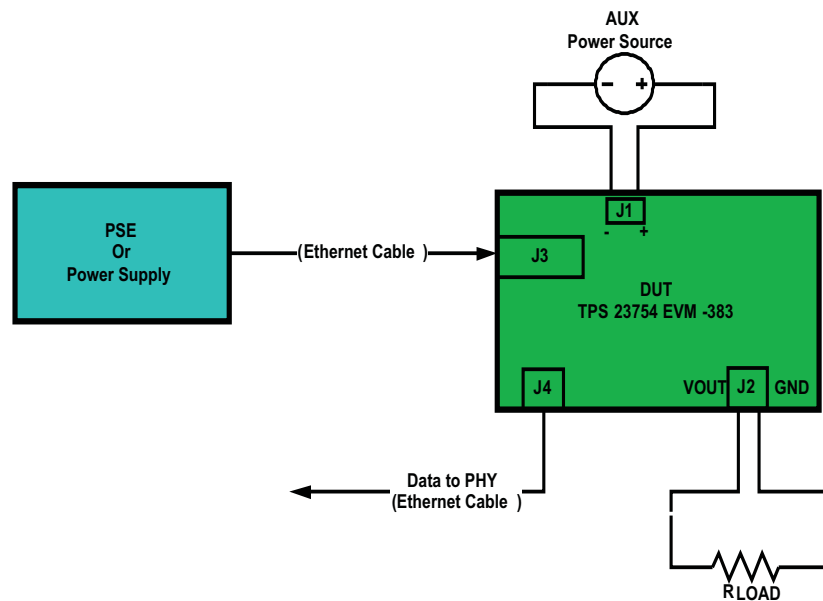


Figure 2. Typical TPS23754EVM-383 Test Setup

6 TPS23754EVM-383 Typical Performance Data

6.1 12V DC/DC Efficiency

Figure 3 illustrates three different 48VDC input efficiency plots:

1. PoE, 48V from J3
2. Converter only 48V
3. Adapter 48V from J1

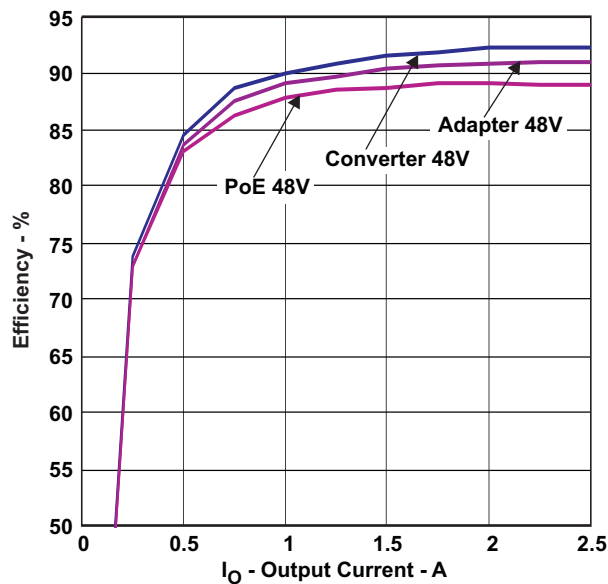


Figure 3. TPS23754EVM-383 Efficiency With 12V Output

6.2 TPS23754EVM-383 Conducted Emissions

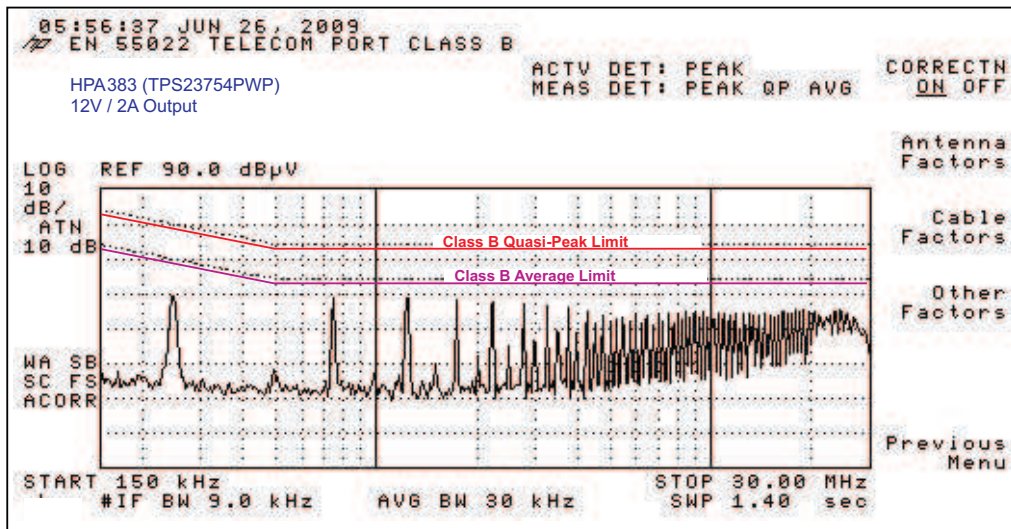


Figure 4. TPS23754EVM-383 Conducted Emissions

7 EVM Assembly Drawings and Layout Guidelines

7.1 PCB Drawings

The following figure shows component placement and layout.

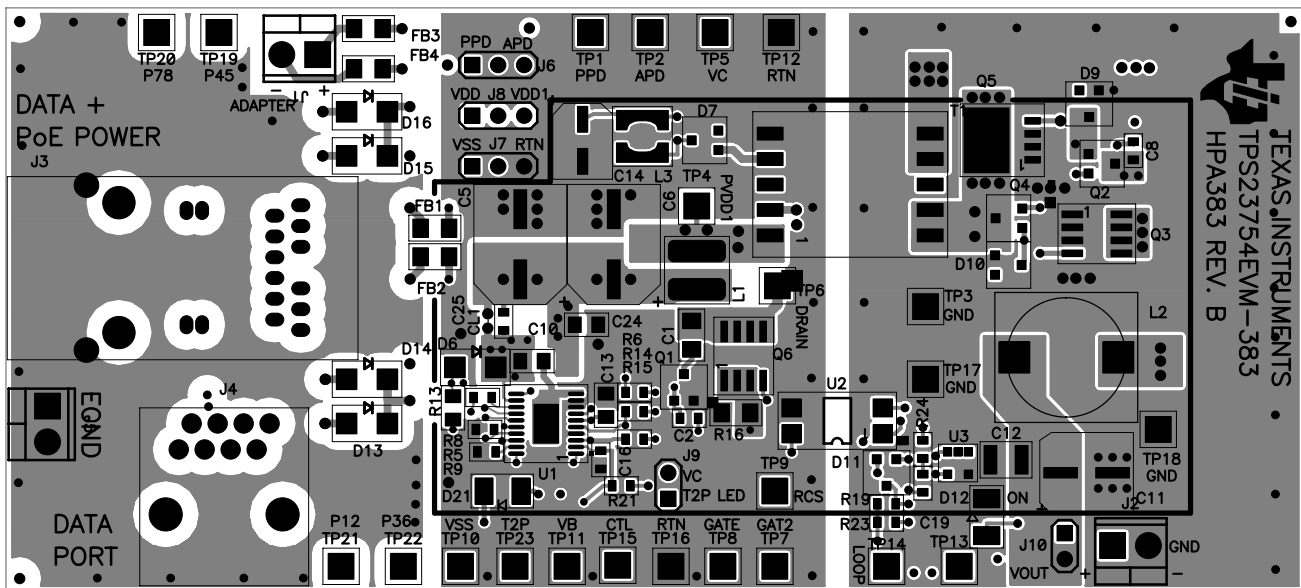


Figure 5. Top Side Layout/Routing

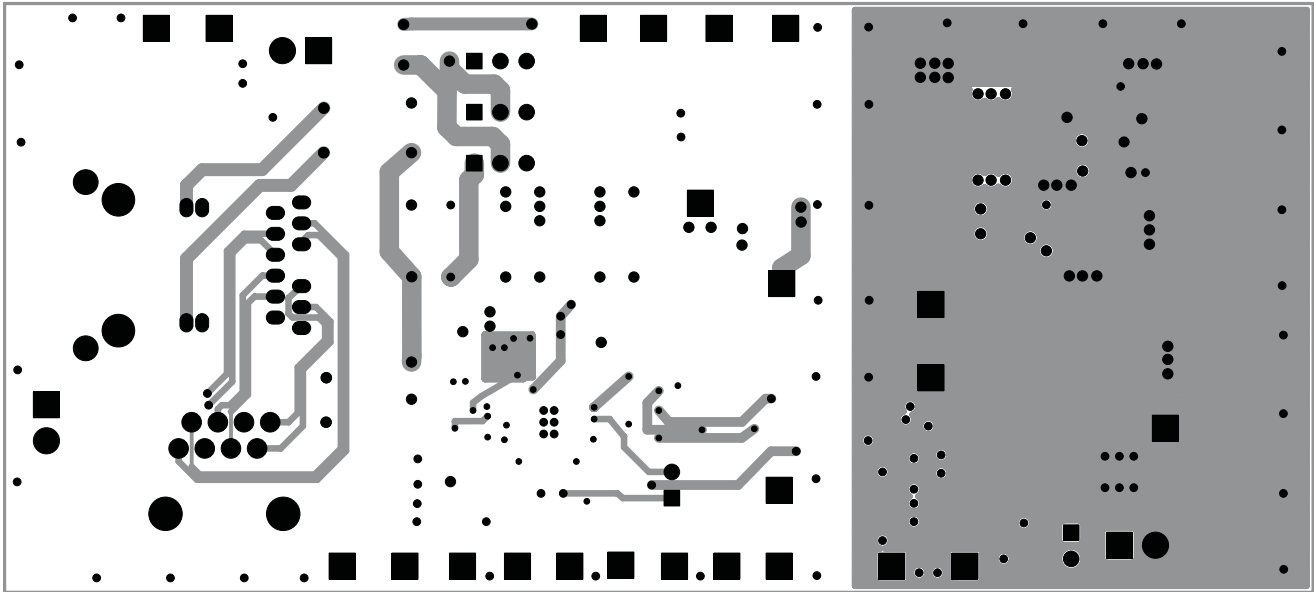


Figure 6. Layer Two Routing

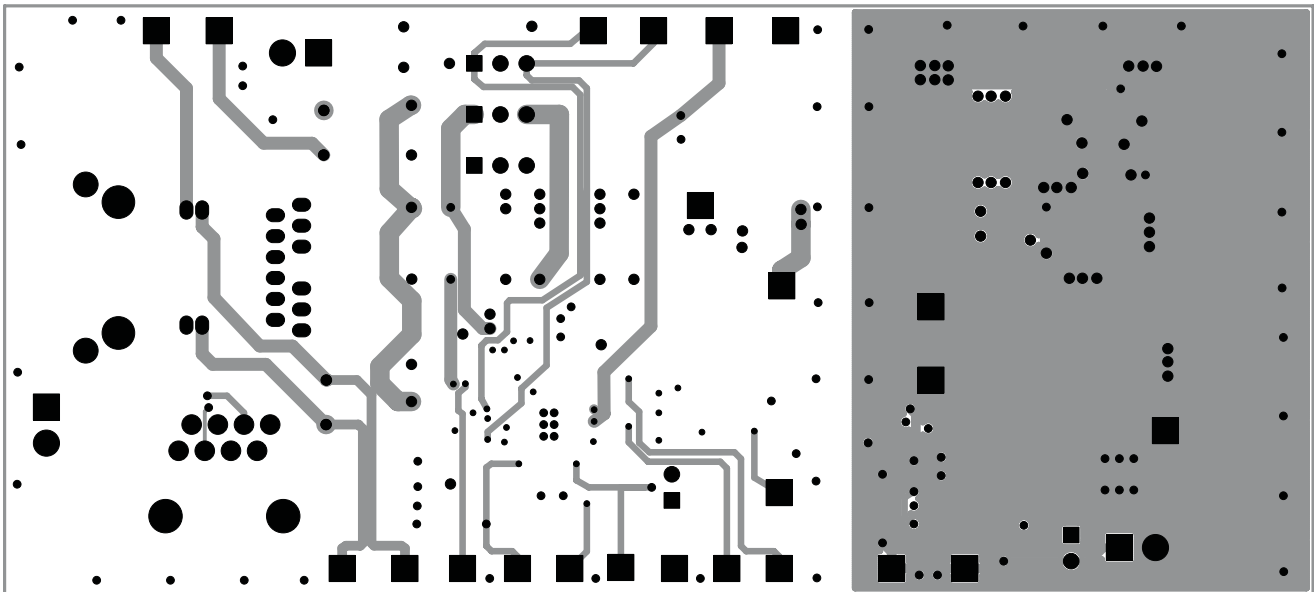


Figure 7. Layer Three Routing

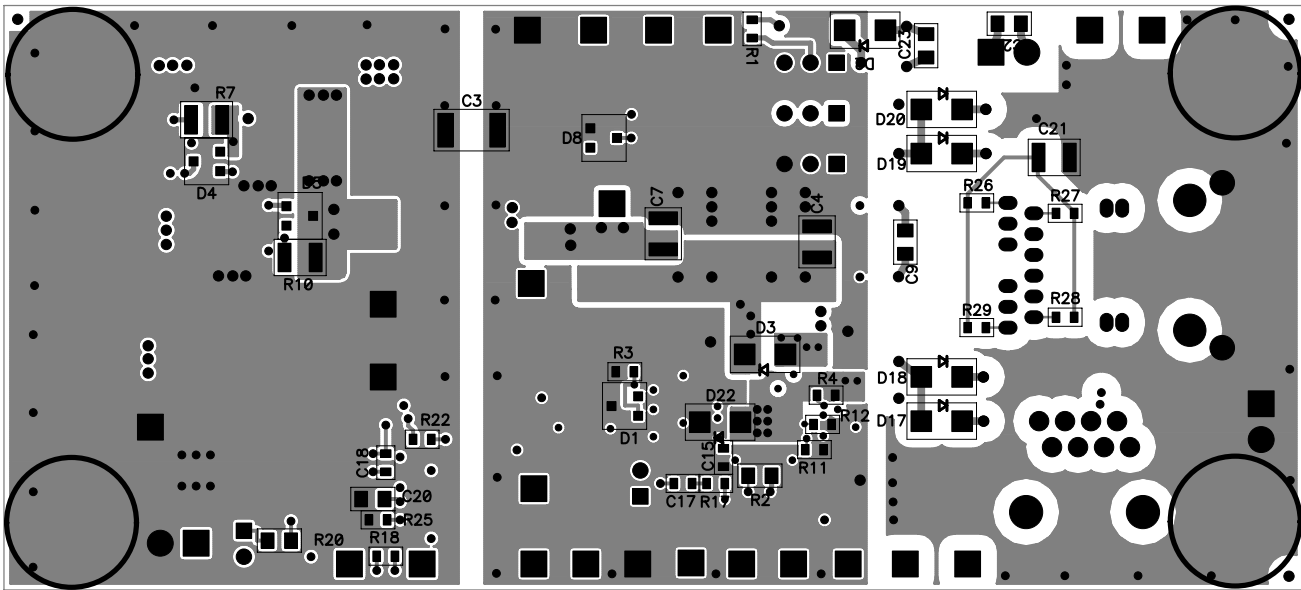


Figure 8. Bottom Side Placement/Routing

7.2 Layout Guidelines

The layout of the PoE front end should follow power and EMI/ESD best practice guidelines. A basic set of recommendations include:

- Parts placement must be driven by power flow in a point-to-point manner; RJ-45, Ethernet transformer, diode bridges, TVS and 0.1- μ F capacitor, and TPS23754 converter input bulk capacitor.
- All leads should be as short as possible with wide power traces and paired signal and return.
- There should not be any crossovers of signals from one part of the flow to another.
- Spacing consistent with safety standards like IEC60950 must be observed between the 48-V input voltage rails and between the input and an isolated converter output.
- The TPS23754 should be located over split, local ground planes referenced to VSS for the PoE input and to RTN for the converter. Whereas the PoE side may operate without a ground plane, the converter side must have one. Logic ground and power layers should not be present under the Ethernet input or the converter primary side.
- Large copper fills and traces should be used on SMT power-dissipating devices, and wide traces or overlay copper fills should be used in the power path.

The DC/DC Converter layout can benefit from basic rules such as:

- Pair signals to reduce emissions and noise, especially the paths that carry high-current pulses which include the power semiconductors and magnetics.
- Minimize trace length of high current, power semiconductors, and magnetic components.
- Where possible, use vertical pairing.
- Use the ground plane for the switching currents carefully.
- Keep the high-current and high-voltage switching away from low-level sensing circuits including those outside the power supply.
- Pay special attention to spacing around the high-voltage sections of the converter.

7.3 EMI Containment

- Use compact loops for dv/dt and di/dt circuit paths (power loops and gate drives)
- Use minimal, yet thermally adequate, copper areas for heat sinking of components tied to switching nodes (minimize exposed radiating surface).
- Use copper ground planes (possible stitching) and top layer copper floods (surround circuitry with ground floods)
- Use 4 layer PCB if economically feasible (for better grounding)
- Minimize the amount of copper area associated with input traces (to minimize radiated pickup)
- Hide copper associated with switching nodes under shielded magnetics where possible
- Heat sink the “quiet side” of components instead of the “switching side” where possible (like the output side of inductor)
- Use Bob Smith terminations, Bob Smith EFT capacitor, and Bob Smith plane
- Use Bob Smith plane as ground shield on input side of PCB (creating a phantom or literal earth ground)
- Use LC filter at DC/DC input
- Dampen high frequency ringing on all switching nodes if present (allow for possible snubbers)
- Control rise times with gate drive resistors and possibly snubbers
- Switching frequency considerations
- Use of EMI bridge capacitor across isolation boundary (isolated topologies)
- Observe the polarity dot on inductors (embed noisy end)
- Use of ferrite beads on input (allow for possible use of beads or 0 ohm resistors)
- Maintain physical separation between input-related circuitry and power circuitry (use ferrite beads as boundary line)
- Balance efficiency vs. Acceptable noise margin
- Possible use of common-mode inductors
- Possible use of integrated RJ-45 jacks (shielded with internal transformer and Bob Smith terminations)
- End-product enclosure considerations (shielding)

8 Bill of Materials
Table 4. TPS23754EVM-383 Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
1	C1	0.047 μ F	Capacitor, Ceramic, 250V, X7R, 10%	1206	Std	Std
3	C10, C23, C24	0.1 μ F	Capacitor, Ceramic, 100V, X7R, 10%	0805	Std	Std
1	C11	100 μ F	Capacitor, Aluminum, 16V, 20%, FK Series	0.217 \times 0.169	EEVFK1C101P	Panasonic
1	C12	22 μ F	Capacitor, Ceramic, 16-V, X7R, 20%	1210	C3225X7R1C226MT	TDK
1	C13	1.0 μ F	Capacitor, Ceramic, 25V, X7R, 10%	0805	Std	Std
1	C14	22 μ F	Capacitor, Aluminum, 25V, 20%	5 \times 5.8mm	EEVFK1E220R	Panasonic
1	C15	47 pF	Capacitor, Ceramic, 50V, X7R, 10%	0603	Std	Std
1	C16	1.0 μ F	Capacitor, Ceramic, 16V, X7R, 10%	0603	Std	Std
1	C17	22 nF	Capacitor, Ceramic, 50V, X7R, 10%	0603	Std	Std
1	C18	10 pF	Capacitor, Ceramic, 50V, C0G, 5%	0603	Std	Std
1	C19	15 nF	Capacitor, Ceramic, 50V, X7R, 10%	0603	Std	Std
1	C2	1 μ F	Capacitor, Ceramic, 16V, X7R, 20%	0603	C1608X7R1C105M	TDK
1	C20	1 μ F	Capacitor, Ceramic, 16V, X7R, 10%	0805	Std	Std
1	C21	1000 pF	Capacitor, Ceramic, 2kV, X7R, 10%	1210	Std	TDK
1	C25	10 nF	Capacitor, Ceramic, 100V, X7R, 10%	0603	Std	Std
1	C3	2200 pF	Capacitor, Ceramic, 2KV, X7R, 10%	1812	C4532X7R3D222K	TDK
2	C4, C7	1 μ F	Capacitor, Ceramic, 100V, X7R, 10%	1210	Std	Std
2	C5, C6	22 μ F	Capacitor, Aluminum, 100V, \pm 20%	8 \times 10.2mm	EEVFK2A220P	Panasonic
1	C8	100 pF	Capacitor, Ceramic, 50V, X7R, 10%	0603	C1608X7R1H101K	TDK
2	C9, C22	1 nF	Capacitor, Ceramic, 100V, X7R, 10%	0805	Std	Std
1	CL1	NA	Current Loop, 0.025 holes	0.120 \times 0.075 inch	NA	NA
5	D1, D4, D5, D7, D8	BAS16	Diode, Switching, 75V, 200mA	SOT23	BAS16LT1	Vishay-Liteon
1	D11	BAV99	Diode, Dual Ultra Fast, Series, 200-mA, 70-V	SOT23	BAV99	Fairchild
1	D12	RED	Diode, LED, RED, 2.0-V, 850-mcd, SM	1210	LTST-C930KRKT	LITE-ON INC
10	D2, D3, D13–D20	B1100	Diode, Schottky, 1A, 100V	SMA	B1100	Diodes, Inc
1	D21	GREEN	Diode, LED, GRN, 2.0-V, 650-mcd, SM	1210	LTST-C930KGKT	LITE-ON INC
2	D6, D22	SMAJ58A	Diode, TVS, 58-V, 1W	SMA	SMAJ58A	Diodes Inc.
2	D9, D10	12V	Diode, Zener, 12-V	SOT23	BZX84C12LT1	ON Semiconductor
4	FB1–FB4,	500	Bead, Ferrite, 2000mA, 60m-ohm	1206	MI1206L501R-10	Steward
3	J1, J2, J5	ED1514	Terminal Block, 2-pin, 6-A, 3.5mm	0.27 \times 0.25	ED1514	OST
1	J3	7499511001	Connector, RJ45, PoE+ Enabled, 1000 Base-T	0.670 \times 1.300 inch	7499511001	Wuerth Electronics
1	J4	5556416-1	Connector, Jack Modular, Vertical, Pos.	0.655 \times 0.615 inch	5556416-1	AMP

Table 4. TPS23754EVM-383 Bill of Materials (continued)

Count	RefDes	Value	Description	Size	Part Number	MFR
3	J6–J8	PTC36SAAN	Header, Male 3-pin, 100mil spacing, (36-pin strip)	0.100 inch × 3	PTC36SAAN	Sullins
2	J9, J10	PTC36SAAN	Header, Male 2-pin, 100mil spacing, (36-pin strip)	0.100 inch × 2	PTC36SAAN	Sullins
1	L1	3.3 µH	Inductor, SMT, 2.15A, 35 milliohm or 1.53A, 32 milliohm	5.1×5.1mm	744043003 or MSS5131-332MX	Würth or Coilcraft
1	L2	22 µH	Inductor, SMT, 4.1A, 43 milliohm or 3.8A, 33 milliohm	0.492 sq"	744770122 or P1173.223T	Würth or Pulse
1	L3	1 mH	Inductor, SMT, 100mA, 16.3 Ohms	0.169 × 0.169 inch	LPS4414-105MLC	Coilcraft
1	Q1	Si2325DS	MOSFET,P-ch, -150 V, 690-mA, 1.2 Ohms	SOT-23	Si2325DS	Vishay
2	Q2, Q4	MMBTA06	Bipolar, NPN, 80V, 500mA	SOT23	MMBTA06LT1	ON Semiconductor
1	Q3	Si4850EY	MOSFET, Nch, 60V, 8.5A, 22milliohm	SO8	Si4850EY	Vishay
1	Q5	Si7852DP	MOSFET, Nchan, 80V, 12A, 16-milliohm	PWRPAK-S08	Si7852DP	Vishay
1	Q6	Si4848DY	MOSFET, N-ch, 150V, 3.7A, 85 milliohm	SO8	Si4848DY	Vishay
1	R1	100K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R11	80.6K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R12	63.4K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R13	63.4	Resistor, Chip, 1/10W, 1%	0805	Std	Std
1	R14	10	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R15	1K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R16	0.12	Resistor, Chip, 1/4W, 1%	1206	ERJ-8RQFR12V	Panasonic ECG
1	R17	348	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R18	49.9	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R2	6.49K	Resistor, Chip, 1/10-W, 1%	0805	Std	Std
1	R20	2.87K	Resistor, Chip, 1/10-W, 1%	0805	Std	Std
1	R21	1.5K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R23	41.2K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R25	11.0K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
4	R26–R29	75	Resistor, Chip, 1/16W, 1%	0603	Std	Std
3	R3, R19, R24	10K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R4	4.02K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R22	2.49K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R5	8.87K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R6	0	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R7, R10	2K	Resistor, Chip, 1/4W, 5%	1210	Std	Std
1	R8	24.9K	Resistor, Chip, 1/16W, 1%	0603	Std	Std

Table 4. TPS23754EVM-383 Bill of Materials (continued)

Count	RefDes	Value	Description	Size	Part Number	MFR
1	R9	69.8K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	T1	750311320 or PA2649NL or 835-01064FC	Transformer, forward, 100 μ H, 12V, 2.5A	0.524 × 0.685 inch	750311320 or PA2649NL or 835-01064FC	Würth or Pulse or E&E Magnetics
7	TP1, TP2, TP7–TP9, TP15, TP23	5012	Test Point, White, Thru Hole	0.125 × 0.125 inch	5012	Keystone
6	TP3, TP10, TP12, TP16–TP18	5011	Test Point, Black, Thru Hole	0.125 × 0.125 inch	5011	Keystone
6	TP4, TP5, TP11, TP13, TP20, TP22	5010	Test Point, Red, Thru Hole	0.125 × 0.125 inch	5010	Keystone
4	TP6, TP14, TP19, TP21	5013	Test Point, Orange, Thru Hole	0.125 × 0.125 inch	5013	Keystone
1	U1	TPS23754PWP	IC, IEEE 802.3at PoE Interface and Isolated Converter Controller	PWP20	TPS23754PWP	TI
1	U2	FOD817AS	IC, Optocoupler, 6-V, 80-160% CTR	SMT-4PDIP	FOD817AS	Fairchild
1	U3	TL431ACDBVR	IC, Shunt Regulator, 2.49-V ref, 36-V, 10-mA, 1%	SOT23-5	TL431ACDBVR	TI
4			Bumpons		2566	SPC
5	—		Shunt, Black	100-mil	929950-00	3M

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 0 V to 57 V and the output voltage range of 10 V to 15 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 80°C. The EVM is designed to operate properly with certain components above 80°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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