

SN54ALS112A, SN74ALS112A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

SDAS199A – APRIL 1982 – REVISED DECEMBER 1994

- Fully Buffered to Offer Maximum Isolation From External Disturbance
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

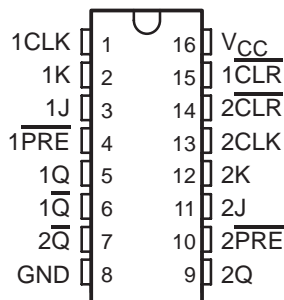
| TYPE | TYPICAL MAXIMUM CLOCK FREQUENCY (MHz) | TYPICAL POWER DISSIPATION PER FLIP-FLOP (mW) |
|----------|---------------------------------------|--|
| 'ALS112A | 50 | 6 |

description

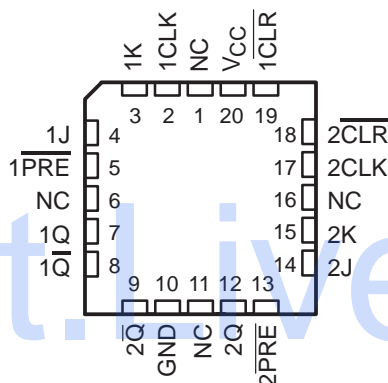
These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset (\overline{PRE}) or clear (\overline{CLR}) inputs sets or resets the outputs, regardless of the levels of the other inputs. When \overline{PRE} and \overline{CLR} are inactive (high), data at the J and K inputs meeting the setup-time requirements is transferred to the outputs on the negative-going edge of the clock pulse (CLK). Clock triggering occurs at a voltage level and is not directly related to the fall time of the clock pulse. Following the hold-time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54ALS112A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS112A is characterized for operation from 0°C to 70°C .

SN54ALS112A . . . J PACKAGE
SN74ALS112A . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS112A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each flip-flop)

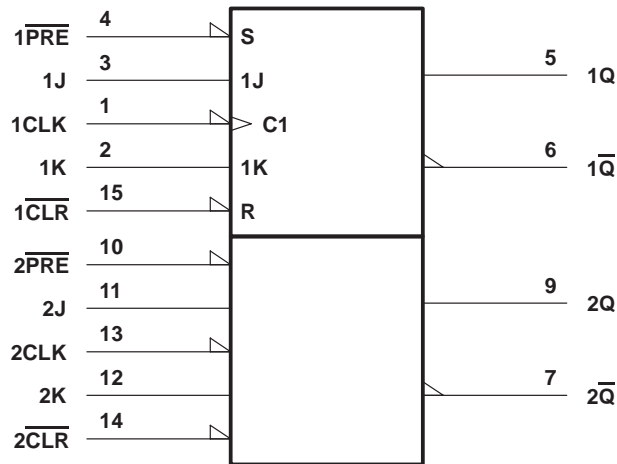
| INPUTS | | | | | OUTPUTS | |
|------------------|------------------|-----|---|---|----------------|------------------|
| \overline{PRE} | \overline{CLR} | CLK | J | K | Q | \overline{Q} |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H [†] | H [†] |
| H | H | ↓ | L | L | Q ₀ | \overline{Q}_0 |
| H | H | ↓ | H | L | H | L |
| H | H | ↓ | L | H | L | H |
| H | H | ↓ | H | H | Toggle | |
| H | H | H | X | X | Q ₀ | \overline{Q}_0 |

[†] The output levels in this configuration may not meet the minimum levels for V_{OH} . Furthermore, this configuration is nonstable; that is, it does not persist when either \overline{PRE} or \overline{CLR} returns to its inactive (high) level.

SN54ALS112A, SN74ALS112A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

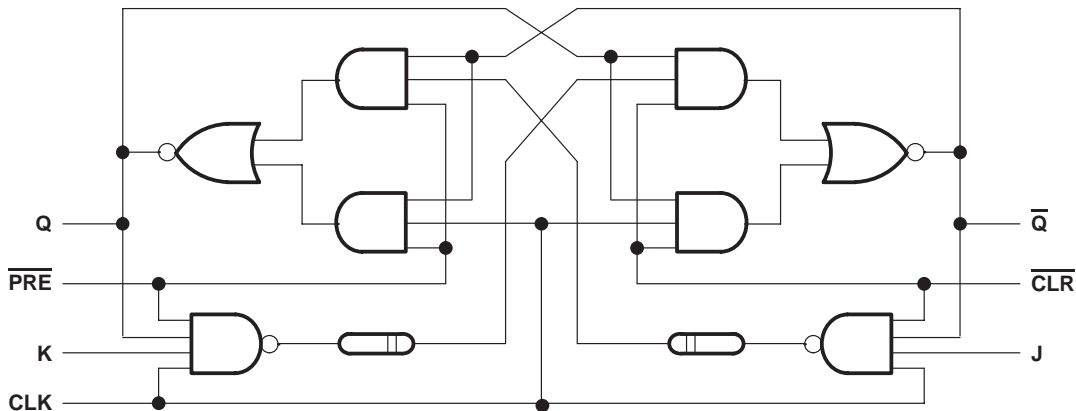
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

| | |
|---|----------------|
| Supply voltage, V_{CC} | 7 V |
| Input voltage, V_I | 7 V |
| Operating free-air temperature range, T_A : SN54ALS112A | -55°C to 125°C |
| SN74ALS112A | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SN54ALS112A, SN74ALS112A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

SDAS199A – APRIL 1982 – REVISED DECEMBER 1994

recommended operating conditions

| | | SN54ALS112A | | | SN74ALS112A | | | UNIT |
|-------------|--------------------------------|---|-----|------|-------------|-----|------|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | | 2 | | | V |
| V_{IL} | Low-level input voltage | | | 0.7 | | | 0.8 | V |
| I_{OH} | High-level output current | | | -0.4 | | | -0.4 | mA |
| I_{OL} | Low-level output current | | | 4 | | | 8 | mA |
| f_{clock} | Clock frequency | 0 | | 25 | 0 | | 30 | MHz |
| t_w | Pulse duration | \overline{PRE} or \overline{CLR} low | | 15 | 10 | | ns | |
| | | CLK high | | 20 | 16.5 | | | |
| | | CLK low | | 20 | 16.5 | | | |
| t_{su} | Setup time before CLK↓ | Data | | 25 | 22 | | ns | |
| | | \overline{PRE} or \overline{CLR} inactive | | 22 | 20 | | | |
| t_h | Hold time after CLK↓ | Data | | 0 | 0 | | ns | |
| T_A | Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54ALS112A | | SN74ALS112A | | UNIT |
|-----------------|--------------------------------------|--|---------------------------|-------------|------|-------------|------|---------------|
| | | | | MIN | TYP† | MAX | MIN | |
| V_{IK} | | $V_{CC} = 4.5\text{ V}$, | $I_I = -18\text{ mA}$ | | -1.5 | | -1.5 | V |
| V_{OH} | | $V_{CC} = 4.5\text{ V to } 5.5\text{ V}$, | $I_{OH} = -0.4\text{ mA}$ | $V_{CC}-2$ | | $V_{CC}-2$ | | V |
| V_{OL} | | $V_{CC} = 4.5\text{ V}$ | $I_{OL} = 4\text{ mA}$ | 0.25 | 0.4 | 0.25 | 0.4 | V |
| | | | $I_{OL} = 8\text{ mA}$ | | | 0.35 | 0.5 | |
| I_I | J, K, or CLK | $V_{CC} = 5.5\text{ V}$, | $V_I = 7\text{ V}$ | | 0.1 | | 0.1 | mA |
| | \overline{PRE} or \overline{CLR} | | | | 0.2 | | 0.2 | |
| I_{IH} | J, K, or CLK | $V_{CC} = 5.5\text{ V}$, | $V_I = 2.7\text{ V}$ | | 20 | | 20 | μA |
| | \overline{PRE} or \overline{CLR} | | | | 40 | | 40 | |
| I_{IL} | J, K, or CLK | $V_{CC} = 5.5\text{ V}$, | $V_I = 0.4\text{ V}$ | | -0.2 | | -0.2 | mA |
| | \overline{PRE} or \overline{CLR} | | | | -0.4 | | -0.4 | |
| $I_{O\ddagger}$ | | $V_{CC} = 5.5\text{ V}$, | $V_O = 2.25\text{ V}$ | -20 | -112 | -30 | -112 | mA |
| I_{CC} | | $V_{CC} = 5.5\text{ V}$, | See Note 1 | 2.5 | 4.5 | 2.5 | 4.5 | mA |

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

NOTE 1: I_{CC} is measured with J, K, CLK, and \overline{PRE} grounded, then with J, K, CLK, and \overline{CLR} grounded.



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SDAS199A – APRIL 1982 – REVISED DECEMBER 1994

switching characteristics (see Figure 1)

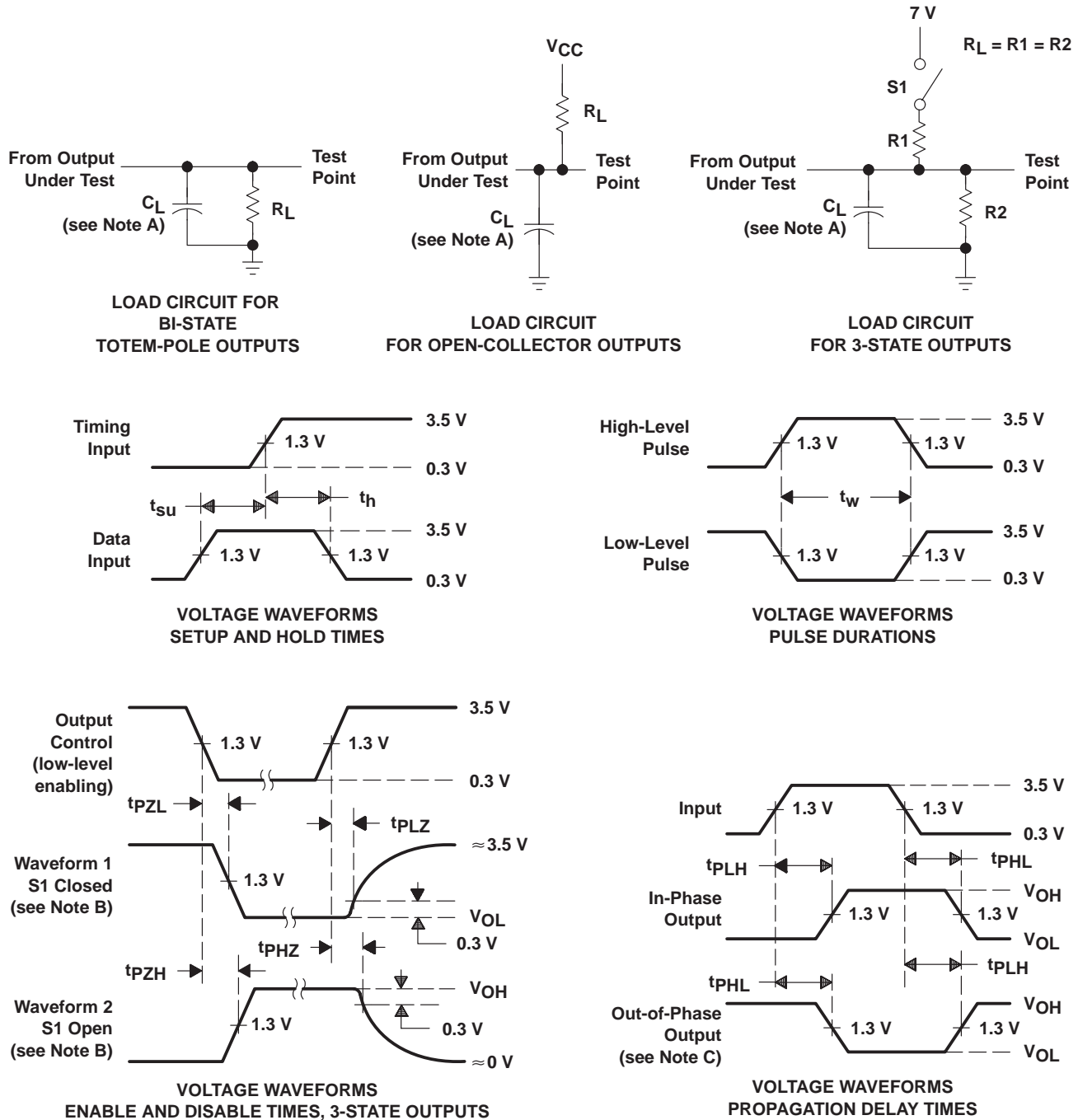
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX† | | | | UNIT |
|------------------|--|----------------------------|---|-----|-------------|-----|------|
| | | | SN54ALS112A | | SN74ALS112A | | |
| | | | MIN | MAX | MIN | MAX | |
| f _{max} | | | 25 | | 30 | | MHz |
| t _{PLH} | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ | Q or $\overline{\text{Q}}$ | 3 | 26 | 3 | 15 | ns |
| t _{PHL} | | | 4 | 23 | 4 | 18 | |
| t _{PLH} | CLK | Q or $\overline{\text{Q}}$ | 3 | 23 | 3 | 15 | ns |
| t _{PHL} | | | 5 | 24 | 5 | 19 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

SN54ALS112A, SN74ALS112A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

SDAS199A – APRIL 1982 – REVISED DECEMBER 1994

PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 84000022A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| 8400002EA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| 8400002FA | OBSOLETE | CFP | W | 16 | | TBD | Call TI | Call TI |
| JM38510/37103B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| JM38510/37103BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| SN54ALS112AJ | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| SN74ALS112AD | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALS112ADE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALS112ADG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALS112ADR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALS112ADRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALS112ADRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALS112AN | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74ALS112AN3 | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI |
| SN74ALS112ANE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74ALS112ANSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALS112ANSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALS112ANSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SNJ54ALS112AFK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| SNJ54ALS112AJ | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 SNPB | N / A for Pkg Type |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ALS112ADR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74ALS112ANSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ALS112ADR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74ALS112ANSR | SO | NS | 16 | 2000 | 346.0 | 346.0 | 33.0 |

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F16)

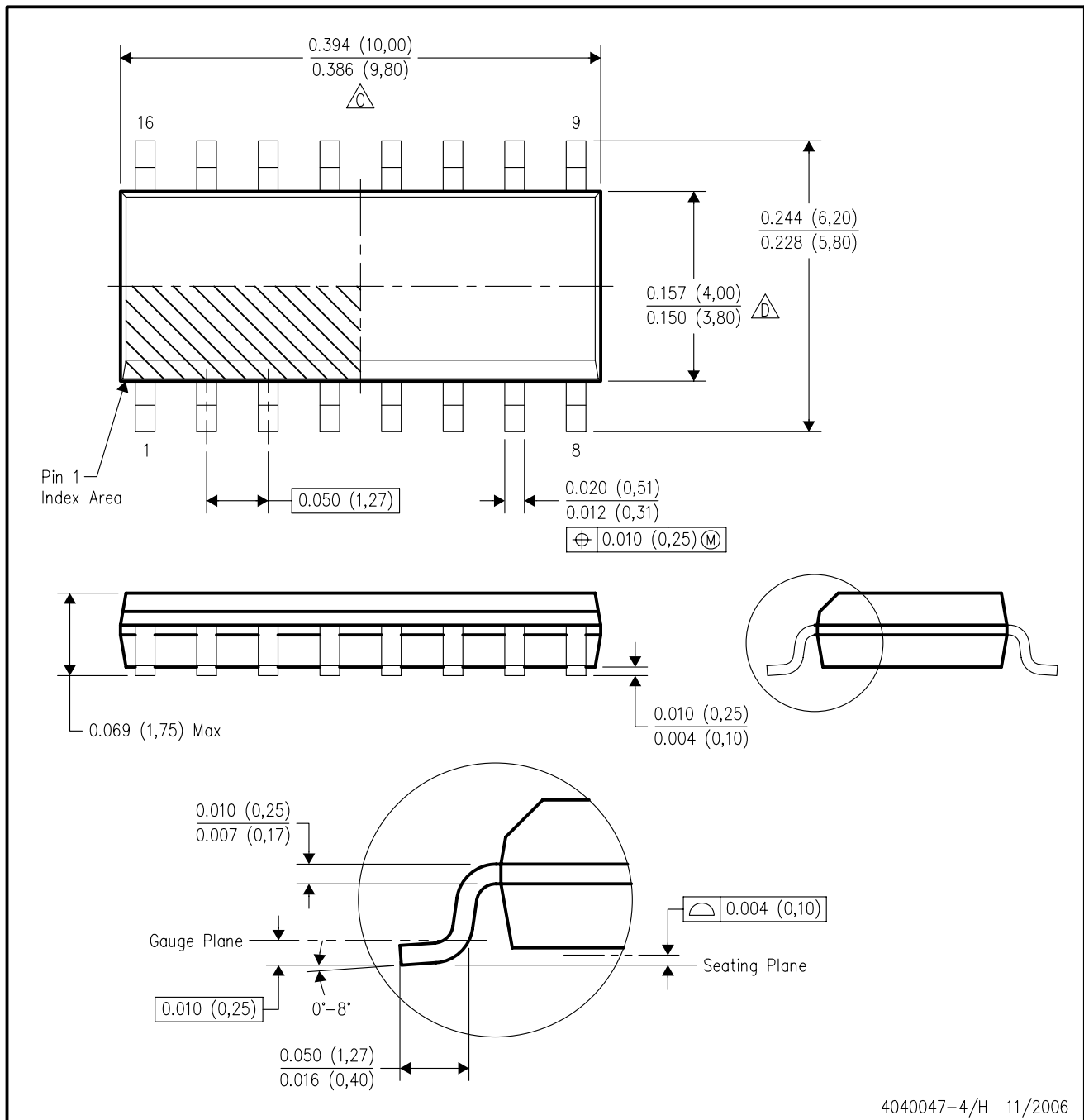
CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



4040047-4/H 11/2006

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AC.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

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