MILITARY SPECIFICATION

SEMICONDUCTOR DEVICES, THYRISTOR, REVERSE BLOCKING, SILICON,
TYPES 2N1792 2N1793, 2N1795, 2N1797, 2N1798, 2N1799, 2N1800, 2N1805,
2N1806, 2N1910, 2N1911, 2N1913, 2N1915, 2N1916, 2N2031,
JAN, JANTX, AND JANTXV

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for silicon thyristors. Three levels of product assurance are provided for each device type as specified in MIL-S-19500.

1.2 Physical dimensions. See figures 1 (TO-94) and 2 (TO-83).

1.3 Maximum ratings.

$I_{T(AV)}$ 1/	I_{TSM} 2/	$-V_{GM}$	V_{GM}	I_{GM}	P_{GM}	$P_{G(AV)}$	Stud torque	Operating altitude	T_{op} (case temperature)	T_{STG} and T_J	$R_{\theta JC}$
Adc	A(pk)(1 cycle)	v(pk)	v(pk)	A(pk)	W	W	lb-in	mm.H_g	°C	°C	°C/W
50	1000	5	10	2	5	0.5	150	15	-40 to +125	-40 to +150	0.4

1/ This average on-state current is for a maximum allowable case temperture of 83°C and 180 electrical degrees of half sine wave conduction. For other operating conditions see figure 3.

2/ Surge rating is nonrecurrent and applies only with device in the conducting state.

1.3.1 Individual ratings.

Types	$V_{D(RMS)}$	V_{RRM} 1/	V_{DRM} 1/	V_{RSM} 2/
	V_{RMS}	V(pk)	V(pk)	V(pk)
2N2031	35	50	50	75
2N1792, 2N1910	35	50	50	75
2N1793, 2N1911	70	100	100	150
2N1795, 2N1913	140	200	200	300
2N1797, 2N1915	210	300	300	400
2N1798, 2N1916	280	400	400	500
2N1799, 2N1805	350	500	500	650
2N1800, 2N1806	420	600	600	720

1/ Values apply for zero or negative gate voltage (V_G).

2/ Transient inverse voltage, nonrecurrent, t = 5.0 ms max.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Naval Electronic Systems Command, ATTN: ELEX 8111, Washington, DC 20360 by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

FSC 5961

1.4 Primary electrical characteristics at T_A = 25°C (unless otherwise specified).

Limits	V_{TM} 1/	I_H 1/	dv/dt 1/	V_{GT} 1/	I_{GT} 1/	t_q 1/ T_C = 100°C
	v(pk)	mAdc	V/µs	Vdc	mAdc	µs
Min	---	---	200	0.25 2/	5	---
Max	2.1	40	---	3.0	70 3/	40

1/ See conditions column for the applicable group A test.

2/ This value also applies at T_A = +125°C.

3/ This value also applies at T_A = -40°C.

2. APPLICABLE DOCUMENTS

2.1 Government specifications and standards. Unless otherwise specified, the following specifications and standards, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-S-19500 - Semiconductor Devices, General Specification for.

STANDARD

MILITARY

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Copies of specifications, standards, drawings, and publications required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting officer.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this specification shall take precedence.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-S-19500, and as specified herein.

3.2 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein shall be as specified in MIL-S-19500.

3.3 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-S-19500, and figures 1 and 2 herein.

3.4 Marking. Marking shall be in accordance with MIL-S-19500, except that the country of origin may be omitted at the option of the manufacturer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection shall be in accordance with MIL-S-19500, and as specified herein.

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-S-19500, and as specified herein.

4.3 Screening (JANTX, and JANTXV levels only). Screening shall be in accordance with MIL-S-19500 (table II) and as specified herein. The following electrical measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table II of MIL-S-19500)	Measurements JANTX and JANTXV levels
3	T_{Low} = -40°C; T_{high} = +150°C
4	2500 G (leads removed or secured)
9	Not required
10	Not required
11	I_{RRM1}, I_{DRM1}, V_{GT1}, and V_{TM}
12	Test condition A (ac blocking voltage); T_C = 125°C; V_{RM} = V_{RRM} (see 1.3.1), V_{DM} = V_{DRM} (see 1.3.1); R_{GK} = ∞
13	Subgroup 2 of table 1 herein, ΔI_{DRM1} = 100% of initial value or 1 mA(pk), whichever is greater. ΔI_{RRM1} = 100% of initial value or 1 mA(pk), whichever is greater.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-S-19500, and as specified herein. All testing shall be conducted on devices prior to attachment of external leads or terminals. After attachment of leads or terminals, the tests of subgroups 1 and 2 of table I shall be performed prior to shipment.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-S-19500, and table I herein. End point electrical measurements shall be in accordance with the applicable steps of table IV herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table IVb of MIL-S-19500, and table II herein. Electrical measurements shall be in accordance with the applicable steps of table IV herein. Subgroups 3 and 6 of table II shall be performed on a sample from the sublot containing the highest voltage rated devices in the lot.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table V of MIL-S-19500, and table III herein. Electrical measurements shall be in accordance with the applicable steps of table IV herein. Subgroups 5 and 6 of table III shall be performed on a sample from the sublot containing the highest voltage rated devices in the lot to accept that type and all lower voltage rated devices. In the event subsequent lots contain a higher voltage type, that type shall be subjected to the tests of subgroups 5 and 6 prior to the acceptance of the lot.

4.5 Methods of inspection. Methods of inspection shall be as specified in appropriate tables and as follows:

4.5.1 Intermittent life test. The thyristors shall be operated in a single phase circuit as shown on figure 4 with 175 ±5 degree conduction angle. Cell stud temperature shall be maintained at 80° ±5°C as measured with a thermocouple rigidly attached to a cell hex. Peak input voltage from a 60 Hz sinusoidal blocking voltage power supply shall be equal to rated blocking voltage. Average forward current shall be 50 amperes per cell from the 60 Hz sinusoidal forward current supply. The blocking voltage supply shall be phase delayed 90 electrical degrees with respect to the forward current supply in order to impose both forward and reverse blocking duty on the cells under test. The forward current supply consists of a low voltage transformer with a means of adjusting the secondary voltage. The blocking voltage supply consists of a high voltage transformer with a synchronous switch connected in series with one of the secondary transformer leads. The synchronous switch is set to conduct for 170 ±5 electrical degrees conduction during the interval when terminal A is negative with respect to terminal C. A minimum of 2 and a maximum of 5 electrical degrees off time shall be allowed after forward current conduction before blocking voltage is applied by the synchronous switch. The gate firing pulses shall be delivered from a firing circuit with an open circuit voltage of 7.0 ±3.0 volts and a short circuit current of 1.2 ±0.8 amperes. The gate pulse average power input shall not exceed 0.5 watt. The gate firing supply shall be in phase with the cell forward current supply.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-S-19500.

6. NOTES

6.1 Notes. The notes specified in MIL-S-19500 are applicable to this specification.

6.2 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

Custodians:
Army - ER
Navy - EC
Air Force - 17

Review activities:
Army - AR, MI
Air Force - 11, 19, 85, 99
DLA - ES
NASA - NA

User activities:
Army - SM
Navy - AS, CG, MC, OS, SH

Agent:
DLA - ES

Preparing activity:
Navy - EC

(Project 5961-0810)

TABLE I. Group A inspection.

Inspection	MIL-STD-750 Method	Conditions	LTPD JANTX JANTXV	Symbol	Limits Min	Limits Max	Unit
Subgroup 1			5				
Visual and mechanical inspections	2071						
Subgroup 2			5				
Reverse blocking current	4211	AC method, bias condition D, f = 60 Hz, $V_{RM} = V_{RRM}$ (see 1.3.1)		I_{RRM1}	---	5	mA(pk)
Forward blocking current	4206	AC method, bias condition D, f = 60 Hz, $V_{DM} = V_{DRM}$ (see 1.3.1)		I_{DRM1}	---	5	mA(pk)
Gate-trigger voltage and gate-trigger current	4221	V_2 = 6.0 Vdc, R_L = 10 ohms, R_e = 25 ohms maximum		V_{GT1} I_{GT1}	0.25 5	3.0 70	Vdc mAdc
Forward "on" voltage	4226	I_{TM} = 220 A(pk) (pulse), Pulse width = 8.3 ms maximum, Duty cycle = 2% maximum		V_{TM}	---	2.1	V(pk)
Holding current	4201	V_{AA} = 22.5 Vdc, I_{F1} = 5 Adc, I_{F2} = 500 mAdc, bias condition D, Gate-trigger source voltage = 6 Vdc, R_2 = 50 ohms		I_H	---	40	mAdc
Reverse gate current	4219	V_G = -5.0 Vdc		I_G	---	-300	mAdc
Subgroup 3			5				
High-temperature reverse blocking current	4211	AC method, T_C = 125°C, bias condition D, f = 60 Hz, $V_{RM} = V_{RRM}$ (see 1.3.1)		I_{RRM2}	---	15	mA(pk)
High-temperature forward blocking current	4206	AC method, T_C = 125°C, bias condition D, $V_{DM} = V_{DRM}$ (see 1.3.1)		I_{DRM2}	---	15	mA(pk)
Gate-trigger voltage	4221	T_C = 125°C, R_e = 25 ohms maximum, R_L = 500 ohms, $V_2 = V_{DRM}$ (see 1.3.1)		V_{GT2}	0.25	---	Vdc
Low-temperature reverse blocking current	4211	AC method, T_C = -40°C, bias condition D, f = 60 Hz, $V_{RM} = V_{RRM}$ (see 1.3.1)		I_{RRM3}	---	5	mA(pk)
Low-temperature forward blocking current	4206	AC method, T_C = -40°C, bias condition D, $V_{DM} = V_{DRM}$ (see 1.3.1)		I_{DRM3}	---	5	mA(pk)
Low-temperature gate-trigger voltage and gate-trigger current	4221	V_2 = 6.0 Vdc, R_L = 10 ohms, R_e = 25 ohms maximum, T_C = -40°C		V_{GT3} I_{GT2}	0.25 ---	3.0 130	Vdc mAdc

TABLE I. Group A inspection -Continued.

Inspection	MIL-STD-750 Method	Conditions	LTPD JANTX JANTXV	Symbol	Limits Min	Limits Max	Unit
Subgroups 4 & 5							
Not applicable							
Subgroup 6			10				
Surge current	4066	I_{TSM} = 1000 A(pk) (1/2 sine wave), 10 surges at 1 per minute, I_O = 0, V_{RM} = V_{RRM} (see 1.3.1), T_C = 125°C, surge duration = 7 ms minimum					
Electrical measurements		See table IV, steps 1, 2, 3, and 4					
Subgroup 7			10				
Expotential rate of voltage rise	4231	T_C = 125°C, bias condition D, C = .05 µF, R_L = 100 ohms, repetition rate = 60 pps, test duration = 15 s, dv/dt = 200 V/µs		V_D			
2N1910, 2N1792, 2N2031		V_{AA} = 50 Vdc			45	---	Vdc
2N1911, 2N1793		V_{AA} = 100 Vdc			95	---	Vdc
2N1913, 2N1795		V_{AA} = 200 Vdc			190	---	Vdc
2N1915, 2N1797		V_{AA} = 300 Vdc			280	---	Vdc
2N1916, 2N1798		V_{AA} = 400 Vdc			370	---	Vdc
2N1805, 2N1799		V_{AA} = 500 Vdc			470	---	Vdc
2N1805, 2N1800		V_{AA} = 600 Vdc			570	---	Vdc
Circuit-commutated turn-off time	4224	T_C = 100°C, I_{TM} = 50 A(pk), t_{on} = 100 ±50 µs, di/dt = 25 A/µs maximum, V_{RM} = V_{RRM} maximum (see 1.3.1) rev. voltage @ t_1 = 15 V minimum, repetition rate = 60 pps maximum, dv/dt = 20 V/µs, V_{DM} = V_{DRM} (see 1.3.1), gate bias condition, gate source voltage = 0, gate source resistance = 100 ohms maximum		t_q	---	40	µs
Gate-controlled turn-on time (2N2031 only)	4223	V_{AA} = 6 Vdc, I_{TM} = 2A(pk), V_{GG} = 6 Vdc, t_{p1} = 11 µs maximum, R_e = 25 ohms maximum, Forward current pulse = 4A/µs $\leq \frac{di}{dt} \leq$ 200A/µs		t_{on}	---	15	µs

TABLE II. Group B inspection.

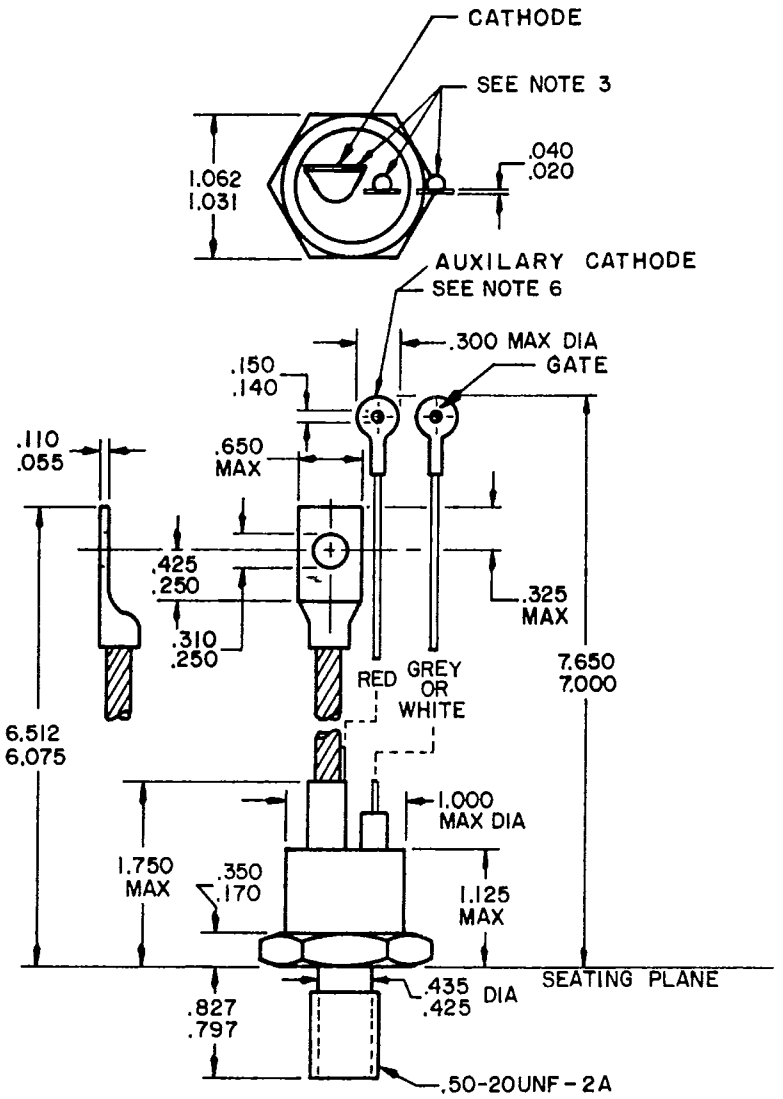
Inspection	MIL-STD-750		LTPD
	Method	Conditions	
Subgroup 1			15
Resistance to solvents	1022		
Subgroup 2			10
Thermal shock (temperature cycling)	1051	Test condition F_1, except T_{Low} = -40°C	
Hermetic seal Fine leak Gross leak	1071		
Electrical measurements		See table IV, steps 1, 2, 3, and 4	
Subgroup 3			5
Blocking life	---	Test conditions per MIL-STD-750, method 1040, test condition A (ac blocking voltage); T_C = 125°C; $V_{RM} = V_{RRM}$ (see 1.3.1), $V_{DM} = V_{DRM}$ (see 1.3.1); $R_{GK} = \infty$	
Electrical measurement		See table IV, steps 1, 2, 3, and 4	
Subgroup 4			
Decap internal visual design verification	2075		1 device /0 failure for each lot
Subgroup 5			20
Thermal resistance	4081	I_{T1} = 50 Adc, T_2 = 125°C maximum, I_{T2} = lowest level which assures complete turn on (approximately 1 Adc), $R_{\theta JC}$ = 0.4 °C/W maximum	
Subgroup 6			10
High-temperature life (non operating)	1032	T_A = 150°C, t = 340 hours	
Electrical measurements		See table IV, steps 1, 2, 3, and 4	

TABLE III. Group C inspection.

Inspection	MIL-STD-750		LTPD
	Method	Conditions	
Subgroup 1			15
Physical dimensions	2066	See figures 1 and 2	
Subgroup 2			10
Thermal shock (glass strain)	1056	Test condition B	
Terminal strength stud torque	2036	Test condition D2 torque = 150 lb-in, t = 15 seconds minimum	
Hermetic seal Fine leak Gross leak	1071		
Moisture resistance	1021	Omit initial conditioning	
External visual	2071		
Electrical measurements		See table IV, steps 1, 2, 3, and 4	
Subgroup 3			10
Shock	2016	5 blows each Y_1, Y_2, Z_1, axes; 500 G, 1.0 ms.	
Vibration, variable frequency	2056	10 G, 100 to 1000 Hz, leads secured or removed	
Constant acceleration	2006	2500 G, orientations X_1, Y_1, Z_1	
Electrical measurements		See table IV, steps 1, 2, 3, and 4	
Subgroup 4			15
Salt atmosphere (corrosion)	1041		
Subgroup 5			15
Barometric pressure (reduced)	1001	15 mm Hg, $V_{RM} = V_{RRM}$ (see 1.3.1), $V_{DM} = V_{DRM}$ (see 1.3.1), t = 60 s	
Subgroup 6			$\lambda = 10$
Intermittent operation life	1036	t_{on} = 50 minutes, t_{off} = 10 minutes, see paragraph 4.5.1	
Electrical measurements		See table IV, steps 1, 2, 3, and 4	

TABLE IV. Group A, B, and C.

Step	Inspection	MIL-STD-750		Symbol	Limits		Unit
		Method	Conditions		Min	Max	
1.	Reverse blocking current	4211	AC method, bias condition D, f = 60 Hz, $V_{RM} = V_{RRM}$ (see 1.3.1)	I_{RRMI}	---	5	mA(pk)
2.	Forward blocking current	4206	AC method, bias condition D, f = 60 Hz, $V_{DM} = V_{DRM}$ (see 1.3.1)	I_{DRM1}	---	5	mA(pk)
3.	Gate-trigger voltage and gate-trigger current	4221	V_2 = 6.0 Vdc, R_L = 10 ohms, R_e = 25 ohms maximum	V_{GT1} I_{GT1}	0.25 5	3.0 70	Vdc mAdc
4.	Forward "on" voltage	4226	I_{TM} = 220 A(pk) (pulse), Pulse width = 8.3 ms maximum, Duty cycle = 2% maximum	V_{TM}	---	2.1	V(pk)

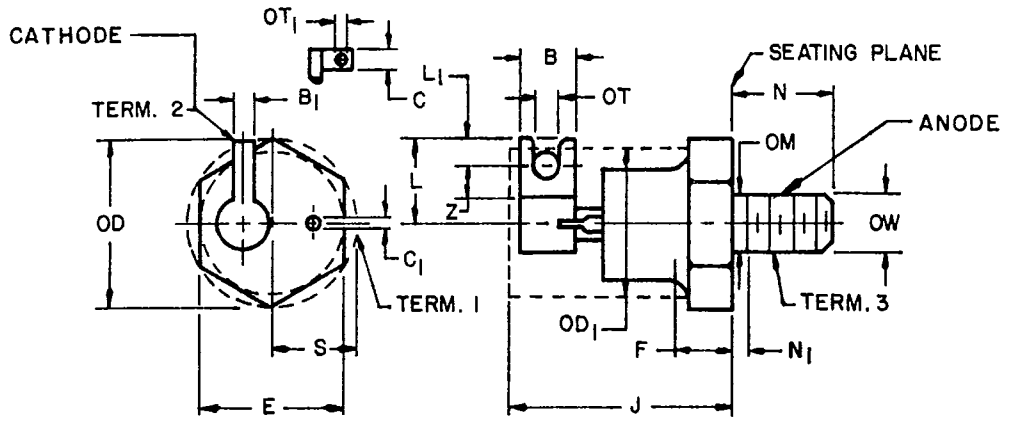


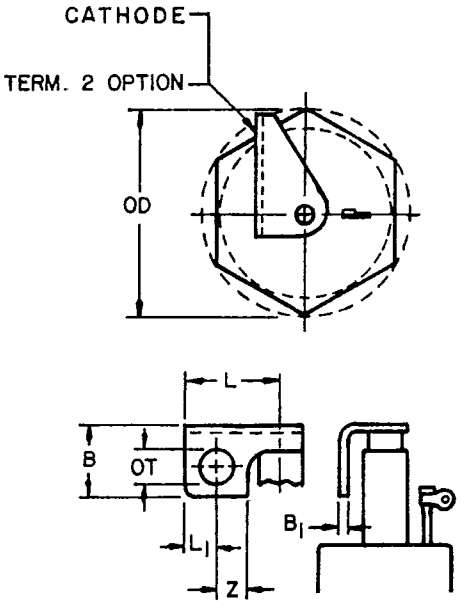
INCHES	MM
.020	.51
.040	1.02
.055	1.40
.110	2.79
.140	3.56
.150	3.81
.170	4.32
.250	6.35
.300	7.62
.310	7.87
.325	8.26
.350	8.89
.425	10.80
.435	11.05
.50	12.70
.650	16.51
.797	20.24
.827	21.01
1.000	25.40
1.031	26.19
1.062	26.97
1.125	28.58
1.750	44.45
6.075	154.31
6.512	165.40
7.000	177.80
7.650	194.31

NOTES:

1. Complete threads to extend within 2.50 (63.50 mm) threads of seating plane.
2. Maximum pitch diameter of plated threads shall be basic pitch diameter .4675 (11.87 mm) Ref. (Screw Thread Standards for Federal Services) FED-STD-H28, P1.
3. Angular orientation of these terminals is undefined. Square or radiu · and of terminal is optional.
4. A chamber or undercut on one or both ends of hex portions is optional.
5. Dimensions are in inches.
6. This auxiliary cathode lead may be cut off if not required for shielding of stray signals which might trigger the thyristor.
7. Metric equivalents are given for general information only and are based upon 1 inch = 25.4 mm.

FIGURE 1. Dimensions of controlled rectifier, types 2N1805, 2N1806, 2N1910, 2N1911, 2N1913, 2N1915, 2N1916, and 2N2031, TO-94 outline.





SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
B	.360	.480	9.14	12.19	1
B1	.059	.115	1.49	2.92	1
C	.115	.160	2.92	4.06	1
C1	.012	.050	.30	1.27	1
OD	---	1.227	---	31.16	
OD1	---	1.031	---	26.19	2
E	1.031	1.062	26.19	26.97	
F	.170	.400	4.32	10.16	3
J	---	1.810	---	45.97	2
L	---	.650	---	16.51	2
L1	.180	---	4.57	---	
OM	.425	.499	10.80	12.67	4, 7
N	.797	.827	20.24	21.00	
N1	---	.125	---	3.18	4
S	---	.575	---	14.60	2
OT	.180	.260	4.57	6.60	
OT1	.060	.080	1.52	2.03	
OW	.4619	.4675	11.73	11.87	5
Z	.180	---	4.57	---	6

NOTES:

1. Contour and orientation of fixed terminal lugs are undefined.
2. The body and terminals of the device, with the exception of the extended lug length S and L, lies within the cylinder defined by OD1 and length J.
3. A chamfer (or undercut) on one or both ends of the hexagonal portions is optional.
4. Length of incomplete or undercut threads.
5. Pitch diameter of .50-20 UNF 2-A (coated) threads (USA B1. 1-1960).
6. Minimum flat.
7. Complete threads to extend to within 2.50 threads of head.
8. Angular orientation of terminals 1 and 2 is undefined.

FIGURE 2. Dimensions of thyristor types 2N1792, 2N1793, 2N1795, 2N1797, 2N1798, 2N1799, 2N1800, TO-83 outline.

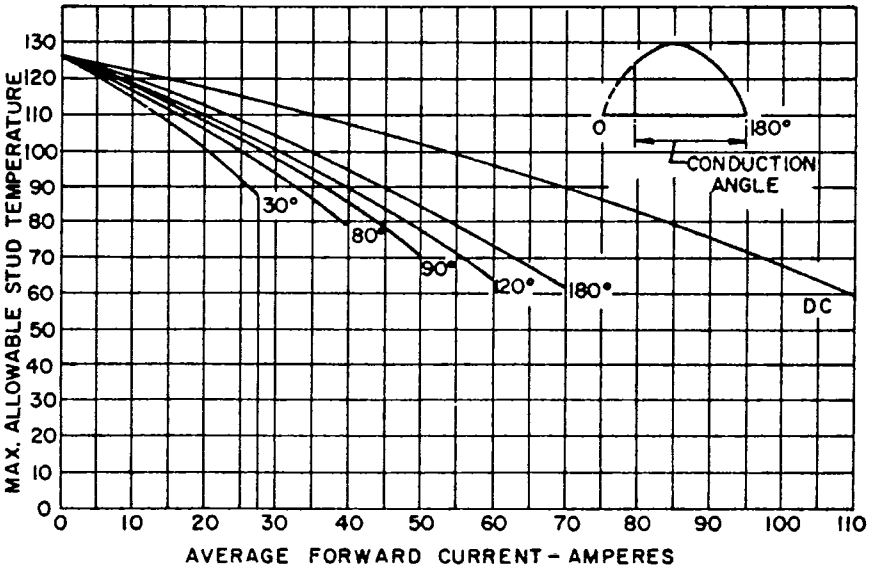


FIGURE 3. Maximum allowable stud temperature.

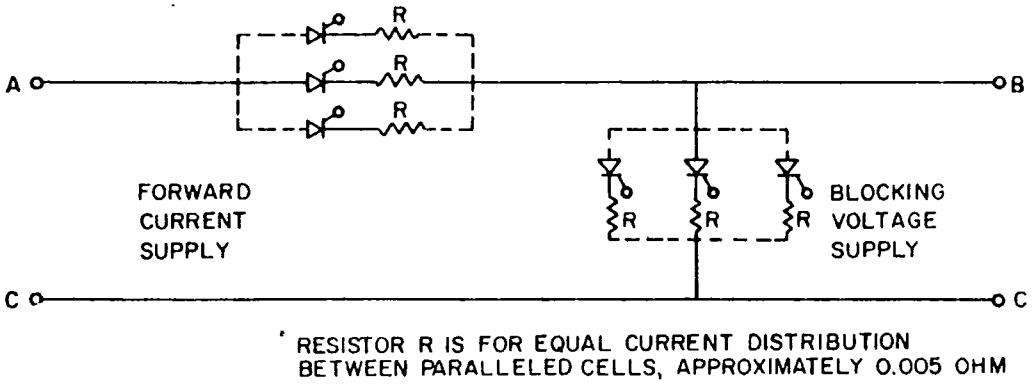


FIGURE 4. Basic test circuit for intermittent life test.

☆U.S. GOVERNMENT PRINTING OFFICE: 1982—505-022/2736