

# CERAMIC SMD CRYSTAL CLOCK OSCILLATOR



7.0 x 5.0 x 1.8mm

ABFM SERIES



RoHS  
Compliant

## FEATURES:

- Based on a proprietary analog multiplier
- Tri-State Output
- Ultra low Phase Noise
- 125MHz, 156.25MHz, 187.5MHz, and 212.5MHz applications
- 2.5V to 3.3V +/- 10% operation
- Ceramic SMD, low profile package

## APPLICATIONS:

- Fiber Channel
- 12Gbit SERDES
- 10Gbit SERDES
- PCI Express

## STANDARD SPECIFICATIONS:

### PARAMETERS

|   |   |
|---|---|
| ABRACON P/N   | ABFM Series   |
| Frequency Range   | 30 MHz to 280 MHz (Contact ABRACON for frequencies out of the range)  |
| Operating Temperature                                   | 0°C to + 70°C (see options)   |
| Storage Temperature                                     | - 55°C to + 125°C   |
| Frequency Stability over Operating Temp. (ref to +25°C) | ± 50 ppm max. (see options)   |
| Supply Voltage (Vdd)                                    | 3.3V or 2.5V ±10% (see options)   |
| Jitter (12KHz - 20MHz)                                  | RMS phase jitter = 0.5pS max.<br>period jitter = 20pS peak to peak typical  |
| Low Phase Noise   | -130 dBc/Hz @ 1kHz Offset from 212.5 MHz<br>-140 dBc/Hz @ 10kHz Offset from 212.5 MHz<br>-145 dBc/Hz @ 100kHz Offset from 212.5 MHz |
| Aging (PPM/year)  | TBD Per Crystal   |

### PECL

|  |                                |
|--|--------------------------------|
| Supply Current (I <sub>DD</sub> ) [Fout = 212.50MHz] | 85mA max.                      |
| Output Clock Duty Cycle @ V <sub>DD</sub> -1.3V      | 45% min, 50% typical, 55% max. |
| Output High Voltage (V <sub>OH</sub> )               | V <sub>DD</sub> -1.025V min    |
| Output Low Voltage (V <sub>OL</sub> )                | V <sub>DD</sub> -1.620V max    |
| Clock Rise time (t <sub>r</sub> ) @ 20/80%           | 0.2nS typ, 0.5nS max           |
| Clock Fall time (t <sub>f</sub> ) @ 80/20%           | 0.2nS typ, 0.5nS max           |

### LVDS

|  |  |
|--|--|
| Supply Current (I <sub>DD</sub> ) [Fout = 212.50MHz]                           | 55mA typical, 60mA max                                 |
| Output Clock Duty Cycle @ 1.25V  | 45% min, 50% typical, 55% max                          |
| Output Differential Voltage (V <sub>OD</sub> )                                 | 247mV min, 355mV typical, 454mV max                    |
| VDD Magnitude Change (ΔV <sub>OD</sub> )                                       | -50mV min, 50mV max                                    |
| Output High Voltage (V <sub>OH</sub> )   | 1.4V typical, 1.6V max                                 |
| Output Low Voltage (V <sub>OL</sub> )  | 1.1V typical, 0.9V min                                 |
| Offset Voltage [R <sub>L</sub> = 100Ω]   | V <sub>OS</sub> = 1.125V min, 1.2V typical, 1.375V max |
| Offset Magnitude Voltage [R <sub>L</sub> = 100Ω]                               | ΔV <sub>OS</sub> = 0mV min, 3mV typical, 25mV max      |
| Power-off Leakage (I <sub>OXD</sub> ) [Vout=VDD or GND, VDD=0V]                | ±1 mA typical, ±10 μA max                              |
| Output Short Circuit Current (I <sub>OSD</sub> )                               | -5.7mA typ, -8mA max                                   |
| Differential Clock Rise Time (t <sub>r</sub> ) [R <sub>L</sub> =100Ω, CL=10pF] | 0.2ns min, 0.5ns typical, 0.7ns max                    |
| Differential Clock Fall Time (t <sub>f</sub> ) [R <sub>L</sub> =100Ω, CL=10pF] | 0.2ns min, 0.5ns typical, 0.7ns max                    |

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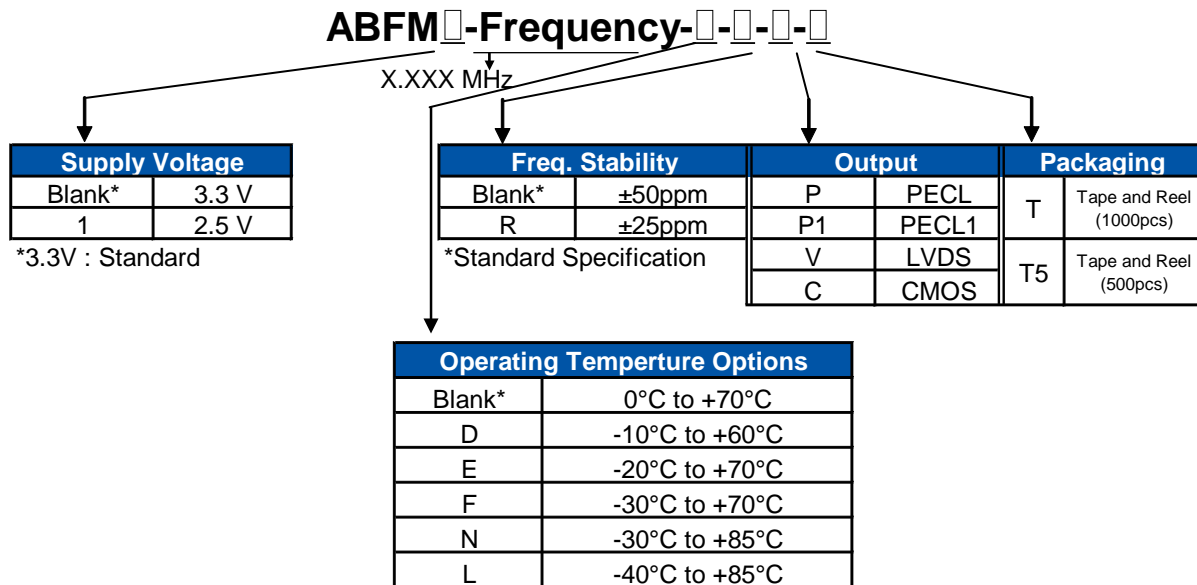


RoHS Compliant

## STANDARD SPECIFICATIONS:

| <b>CMOS</b>   |                               |
|---|-------------------------------|
| Supply Current ( $I_{DD}$ ) [at 100MHz, load 15pF]                    | 16mA typ, 20mA max            |
| Output Clock Duty Cycle @ 50% $V_{DD}$                                | 45% min, 50% typical, 55% max |
| Output High Voltage ( $V_{OH}$ ) [ $I_{OH} = -8.5mA$ ]                | 2.4V min                      |
| Output Low Voltage ( $V_{OL}$ ) [ $I_{OL} = 8.5mA$ ]                  | 0.4V max                      |
| Output Drive Current ( $I_{OSD}$ ) [ $V_{OL} = 0.4V, V_{OH} = 2.4V$ ] | 8.5mA typ                     |
| Output Clock Rise/Fall time [10% ~ 90% $V_{DD}$ w/10pF load]          | 1.2nS typical, 1.6nS max      |
| Output Clock Duty cycle [Measured @ 50% $V_{DD}$ ]                    | 45% min, 50% typical, 55% max |

## OPTIONS AND PART IDENTIFICATION (Left blank if standard):



\*Standard Specification  
Contact ABRACON for extended temperatures.

## PIN ASSIGNMENTS:

| PIN # | NAME           | DESCRIPTION              |
|-------|----------------|--------------------------|
| 1     | Tri-state      | Tri-state                |
| 2     | NC             | No Connect               |
| 3     | GND            | Ground                   |
| 4     | Q              | PECL, LVDS               |
| 5     | $\overline{Q}$ | Complimentary PECL, LVDS |
| 6     | $V_{DD}$       | VDD Connection           |

## TRI-STATE PIN OUT DESCRIPTION:

| OUTPUT TYPE OPTION |       | PIN 1 LOGIC LEVEL* | OUTPUT STATE |
|--------------------|-------|--------------------|--------------|
| P                  | PECL  | 1                  | Tri-state    |
|                    |       | 0 (Default)        | Enabled      |
| P1                 | PECL1 | 0                  | Tri-state    |
|                    |       | 1                  | Enabled      |
| V                  | LVDS  | 0                  | Tri-state    |
|                    |       | 1 (Default)        | Enabled      |
| C                  | CMOS  | 0                  | Tri-state    |
|                    |       | 1 (Default)        | Enabled      |

\*Connect to VDD from logic level "1", connect to ground for logic level "0".

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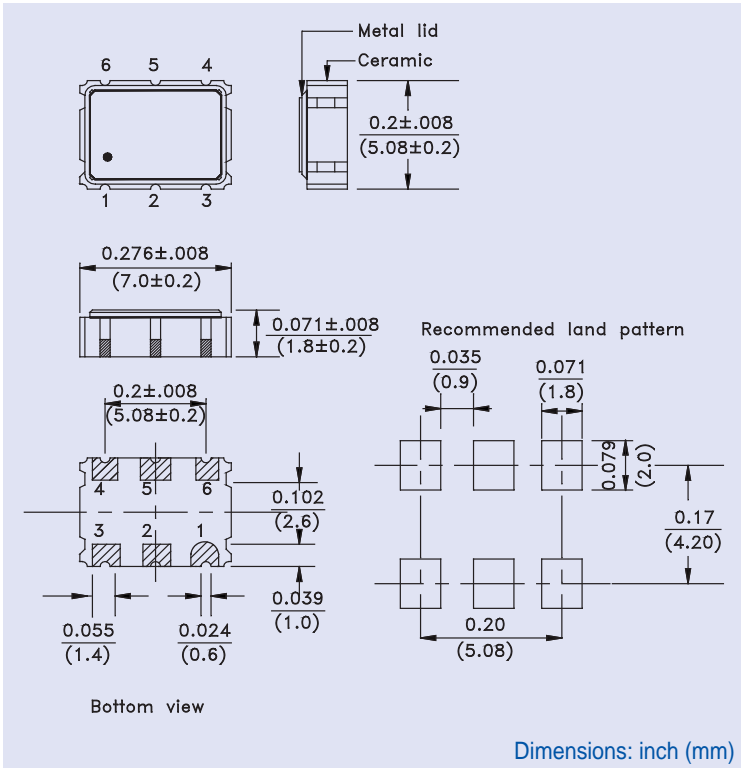


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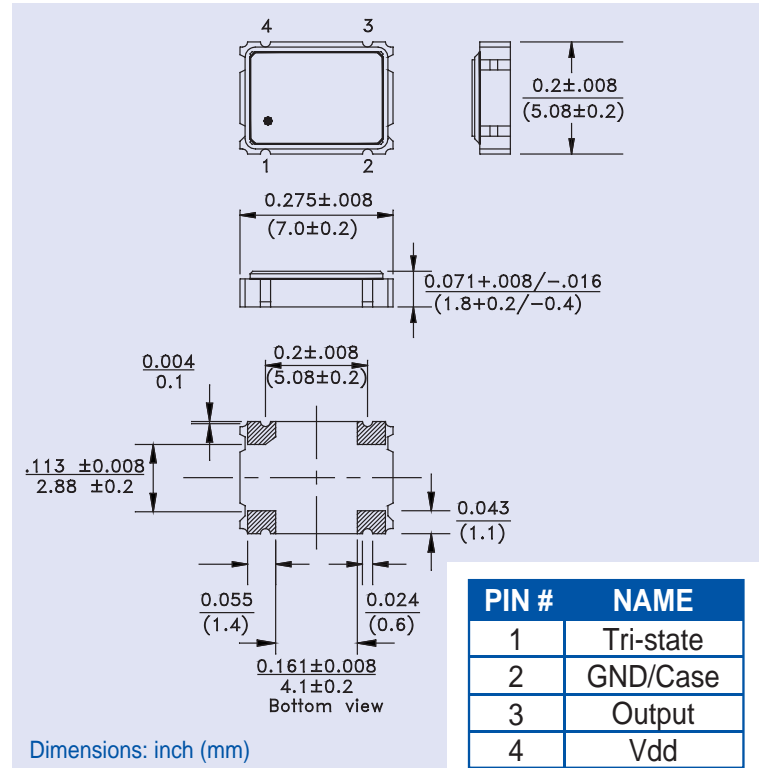


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## PECL & LVDS DRAWING:



## CMOS DRAWING:



## TAPE & REEL:

