

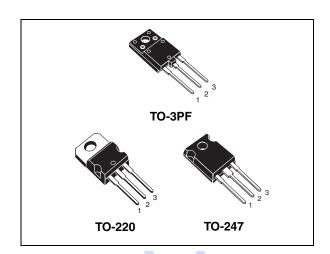
STFW6N120K3 STP6N120K3, STW6N120K3

N-channel 1200 V, 1.85 Ω, 5 A, TO-3PF, TO-220, TO-247 Zener-protected SuperMESH3[™] Power MOSFET

Features

Туре	V _{DSS}	R _{DS(on)} max	I _D	Pw
STFW6N120K3	1200 V	< 2.4 Ω	5 A	TBD
STP6N120K3	1200 V	< 2.4 Ω	5 A	150 W
STW6N120K3	1200 V	< 2.4 Ω	5 A	150 W

- 100% avalanche tested
- Extremely large avalanche performance
- Gate charge minimized
- Very low intrinsic capacitances
- Zener-protected



Application

Switching applications

Description

The new SuperMESH3™ series is obtained through the combination of a further fine tuning of ST's well established strip-based PowerMESH™ layout with optimized vertical structure. In addition to pushing on-resistance significantly down, special attention has been taken to ensure a very good dynamic performances coupled with a very large avalanche capability for the most demanding application.

Figure 1. Internal schematic diagram

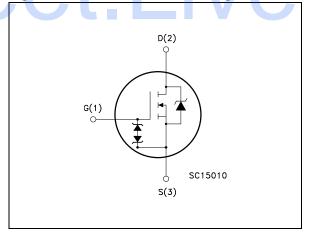


Table 1. Device summary

Order codes	Order codes Marking		Packaging
STFW6N120K3	6N120K3	TO-3PF	Tubes
STP6N120K3	6N120K3	TO-220	Tubes
STW6N120K3	6N120K3	TO-247	Tubes

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1 Electrical ratings

Table 2. Absolute maximum ratings

Cumbal	Symbol Parameter		Value		Unit
Symbol	Parameter	TO-3PF	TO-220	TO-247	Offic
V _{GS}	Gate- source voltage		30		V
I _D	Drain current (continuous) at T _C = 25 °C		5		Α
I _D	Drain current (continuous) at T _C = 100 °C		3.2		Α
I _{DM} ⁽¹⁾	Drain current (pulsed)	20			Α
P _{TOT}	Power dissipation at T _C = 25 °C	TBD	150	150	W
I _{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T _{JMAX})	TBD			Α
E _{AS}	Single pulse avalanche energy (starting $T_J = 25$ °C, $I_D = I_{AR}$, $V_{DD} = 50$ V)	TBD			mJ
dv/dt (2)	Peak diode recovery voltage slope	TBD			V/ns
V _{ESD(G-S)}	G-S ESD (HBM-C = 100 pF, R = 1.5 k Ω)	4000			V
V _{ISO}	Insulation withstand voltage (AC)	3500		V	
T _{stg}	Storage temperature -55 to 150		°C		
T _J	Operating junction temperature		-55 10 150		0

^{1.} Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	TO-3PF	TO-220	TO-247	Unit
R _{thj-case}	Thermal resistance junction-case	TBD 0.83		°C/W	
R _{thj-pcb}	Thermal resistance junction to pcb minimum footprint		°C/W		
R _{thj-amb}	Thermal resistance junction-ambient max	50	62.5	50	°C/W
T _J	Maximum lead temperature for soldering purpose	300			°C

^{2.} $I_{SD} \le 5A$, $di/dt = 100 A/\mu s$, $V_{Peak} < V_{(BR)DSS}$

2 Electrical characteristics

 $(T_C = 25 \, ^{\circ}C \text{ unless otherwise specified})$

Table 4. On / off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	$I_D = 1 \text{ mA}, V_{GS} = 0$	1200	-	-	V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, T_{J} = 125 °C	-	-	1 50	μ Α μ Α
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0$	-	-	± 10	μΑ
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 100 \mu A$	3	4	5	٧
R _{DS(on)}	Static drain-source on resistance	$V_{GS} = 10 \text{ V}, I_D = 2.5 \text{ A}$	-	1.85	2.4	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
9 _{fs} (1)	Forward transconductance	V _{DS} = 15 V, I _D = 2.5 A	-	TBD	-	S
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 100 \text{ V, f} = 1 \text{ MHz,}$ $V_{GS} = 0$	-	1050 70 1	-	pF pF pF
C _{O(tr)} (2)	Equivalent capacitance time related	$V_{GS} = 0$, $V_{DS} = 0$ to 960 V	-	TBD	-	pF
C _{O(er)} (3)	Equivalent capacitance energy related	$V_{GS} = 0$, $V_{DS} = 0$ to 960 V	-	TBD	-	pF
R _G	Intrinsic gate resistance	f = 1 MHz open drain	-	3	-	Ω
Qg	Total gate charge	$V_{DD} = 960 \text{ V}, I_D = 5 \text{ A},$		32		nC
Q_{gs}	Gate-source charge	V _{GS} = 10 V	-	TBD	-	nC
Q_{gd}	Gate-drain charge	(see Figure 3)		TBD		nC

^{1.} Pulsed: pulse duration = 300 μ s, duty cycle 1.5%.

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^{2.} C_{oss} eq. time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

^{3.} C_{oss} eq. energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times on/off

Symbol	Parameter	Test conditions	Min.	Тур.	Max	Unit
$\begin{array}{c} t_{\text{d(on)}} \\ t_{\text{r}} \\ t_{\text{d(off)}} \\ t_{\text{f}} \end{array}$	Turn-on delay time Rise time Turn-off-delay time Fall time	$V_{DD} = 600 \text{ V}, I_{D} = 2.5 \text{ A},$ $R_{G} = 4.7 \Omega, V_{GS} = 10 \text{ V}$ (see <i>Figure 2</i>)	,	TBD TBD TBD TBD	1	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD}	Source-drain current Source-drain current (pulsed)		-	-	5 20	A A
V _{SD} ⁽²⁾	Forward on voltage	$I_{SD} = 5 \text{ A}, V_{GS} = 0$	-		1.6	V
t _{rr} Q _{rr} I _{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 5 A, di/dt = 100 A/ μ s V_{DD} = 60 V T _J = 25 °C (see Figure 7)	1	TBD TBD TBD	1	ns nC A
t _{rr} Q _{rr} I _{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 5 A, di/dt = 100 A/ μ s V_{DD} = 60 V, T_{J} = 150 °C (see <i>Figure 7</i>)	-	TBD TBD TBD	-	ns nC A

^{1.} Pulse width limited by safe operating area

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
BV _{GSO}	Gate-source breakdown voltage	I _{GS} = ± 1 mA (open drain)	30	-	ı	V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

^{2.} Pulsed: Pulse duration = 300 μ s, duty cycle 1.5%

3 Test circuits

Figure 2. Switching times test circuit for resistive load

Figure 3. Gate charge test circuit

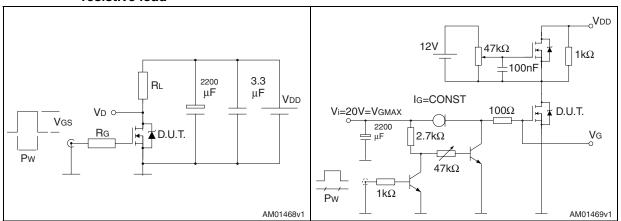


Figure 4. Test circuit for inductive load switching and diode recovery times

Figure 5. Unclamped inductive load test circuit

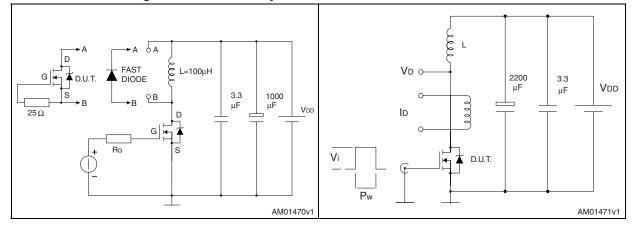
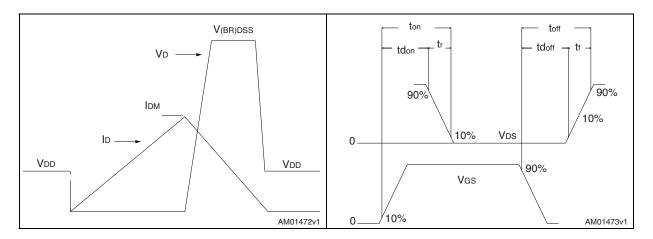


Figure 6. Unclamped inductive waveform

Figure 7. Switching time waveform



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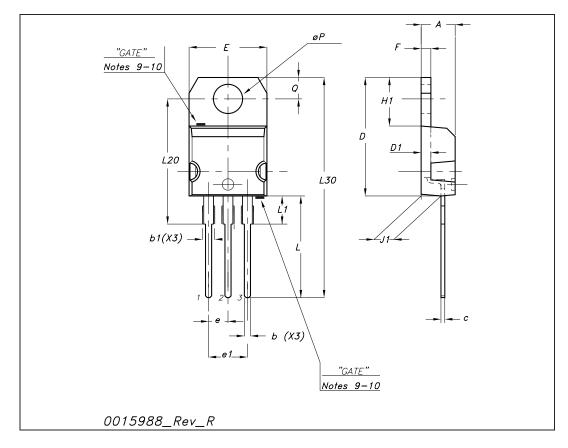
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.



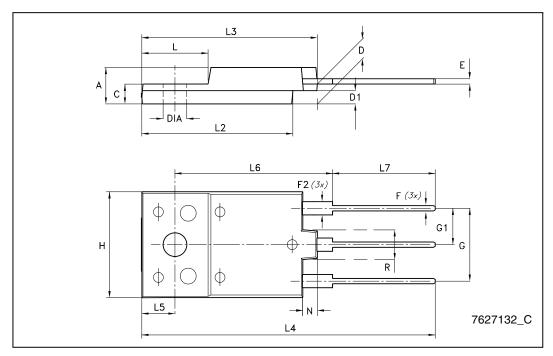
TO-220 mechanical data

Dim		mm			inch	
Dim	Min	Тур	Max	Min	Тур	Max
Α	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
С	0.48		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
е	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
ØP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



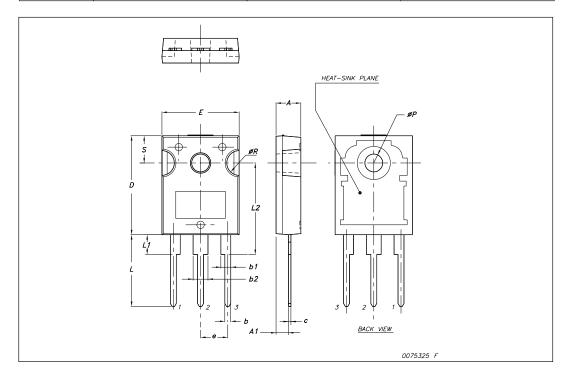
TO-3PF	mechan	ical data
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DIM.	mm.			
	min.	typ	max.	
Α	5.30		5.70	
С	2.80		3.20	
D	3.10		3.50	
D1	1.80		2.20	
E	0.80		1.10	
F	0.65		0.95	
F2	1.80		2.20	
G	10.30		11.50	
G1		5.45		
Н	15.30		15.70	
L	9.80	10	10.20	
L2	22.80		23.20	
L3	26.30		26.70	
L4	43.20		44.40	
L5	4.30		4.70	
L6	24.30		24.70	
L7	14.60		15	
N	1.80		2.20	
R	3.80		4.20	
Dia	3.40		3.80	



TO-247 mechanical data

Dim.	mm.		
	Min.	Тур	Max .
Α	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
С	0.40		0.80
D	19.85		20.15
Е	15.45		15.75
е		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
øΡ	3.55		3.65
øR	4.50		5.50
S		5.50	



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
15-Apr-2009	1	First release

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