DSP56301ADM

User's Manual

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DSP56301ADMUM/AD

Introduction

This document supports the DSP56301 Application Development Module (DSP56301ADM), including a description of its basic structure and operation, the equipment required to use it, the specifications of the key components, schematic diagrams, and a parts list. Section 1 is a Quick Start Guide. Section 2 provides detailed information about key components in the evaluation module. Appendix A has detailed schematics.Appendix B lists the Bill Of Materials (BOM) for the board. Detailed information is provided in the additional documents supplied with this kit.

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SECTION 1

QUICK START GUIDE

1.1 OVERVIEW

The Motorola Application Development System (ADS) is a tool used to design and test complex software applications and hardware products using a specific Motorola DSP chip. The related Application Development Modules (ADMs) contain the DSP chip and related hardware used for bench development and test. Detailed information about the content and use of the ADS is provided in the ADS User's Manual (order # DSPADSUM/AD). This manual provides specific information about the DSP56301 Application Development Module (DSP56301ADM). This section provides a summary description of the DSP56301ADM, additional requirements, and quick installation information. Detailed information about the DSP56301ADM design and operation is provided in the remaining sections of this manual.

1.2 EQUIPMENT

The following section gives a brief summary of the equipment required to use the DSP56301 Application Development Module (DSP56301ADM), some of which will be supplied with the module, and some of which must be supplied by the user.

1.2.1 What You Get with the DSP56301ADM

The following materials are provided with the DSP56301ADM:

- DSP56301 Application Development Module board
- DSP56301ADM Product Information
- DSP56301ADM User's Manual (this document)
- Motorola Digital Signal Processor Registration Form

1.2.2 What You Need to Supply

- Motorola Application Development System with appropriate host interface card
- Host Computer system:
  - PC-compatible computer (486 class or higher) with:
    - MS-DOS version 6.0 or later or Windows 3.1 or later or Windows 95
    - 8 Mbytes RAM
    - one open 16-bit ISA or a PCI expansion slot
    - free I/O addresses ($100–$102, $200–202, or $300–$303)
    - CD-ROM drive
    - hard drive with 4 Mbyte of free disk space
    - mouse
  - Sun Microsystems Sun 4 Workstation running Sun Operating System Release 4.1.1 or later (or Solaris Release 2.5 or later), one open SBus expansion slot, CD-ROM drive, and a mouse
  - Hewlett Packard HP7xx Workstation running HPUX Version 9.x (Version 10.x is not supported), one open EISA expansion slot, CD-ROM drive, and a mouse

1.3 INSTALLATION PROCEDURE

Installation requires the following steps:

1. Using information provided in the Motorola ADS User's Manual, install the Motorola Application Development System in the host computer.
2. Prepare the DSP56301ADM board
3. Connect the board to the external Command Converter card

1.3.1 Preparing the DSP56301ADM

CAUTION

Because all electronic components are sensitive to the effects of electrostatic discharge (ESD) damage, correct procedures should be used when handling all components in this kit and inside the supporting personal computer. Use the following procedures to minimize the likelihood of damage due to ESD:

- **Always handle all static-sensitive components only in a protected area, preferably a lab with conductive (anti-static) flooring and bench surfaces.**
- **Always use grounded wrist straps when handling sensitive components.**
- **Never remove components from anti-static packaging until required for installation.**
- **Always transport sensitive components in anti-static packaging.**

Locate the fourteen jumper blocks JP1–JP14 and switch block SW2 on the DSP56301ADM board, as shown in **Figure 1-1** on page 1-6. **Table 1-1** describes the default jumper and switch settings when shipped from the factory.

Read the technical summary in **Section 2** of this manual for additional information about the DSP56301ADM board and its components.

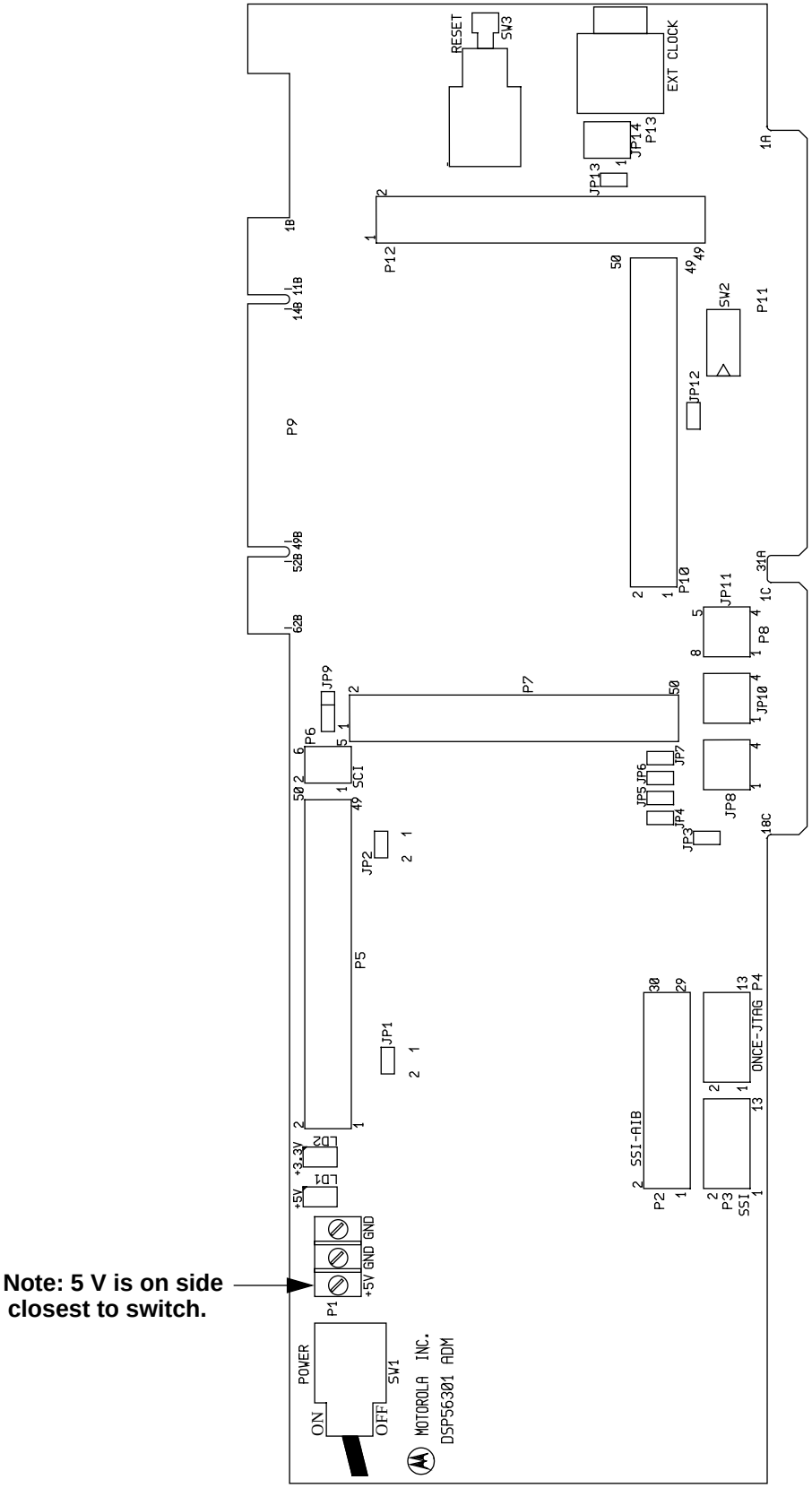


Figure 1-1 DSP56301ADM Key Component Layout

Table 1-1 DSP56301ADM Default Jumper Options

Jumper/Switch Block	Default Configuration as Shipped	Comment
JP1	Jumpered	Enable SRAM memory
JP2	Jumpered	Enable DRAM memory
JP3	Jumpered	Enable Flash memory
JP4,JP5, JP6, JP7	Jumpered	Enable ISA host interface
JP8,JP10	JP8—No jumpers JP10—Pins 3–6 and 4–5 jumpered	Set ISA DMA channel 5
JP9	Pins 1–2 jumpered	Set ISA clamp protection
JP11	Pins 4–5 jumpered	Set ISA Interrupt channel 10
JP12	Removed	Enable DSP PLL operation
JP13,JP14	JP13 Removed JP14 Pins 2–5 jumpered	Set clock source to clock generator.
SW2	SW2–1: Off SW2–2: On SW2–3: Off	Bootstrap from HOST ISA
Note: The factory default configuration selects ISA bus operation for the plug-in card feature. Refer to **Section 2.6 Host Port Selection** for other available port configurations.		

1.3.2 Connecting the DSP56301ADM to the PC and Power

Figure 1-2 shows the interconnection diagram for connecting the PC and the external power supply to the DSP56301ADM board. Using the instructions in the ADS User's Manual, connect the Command Converter to the ADM board. Power for the ADM is supplied from the Command Converter module.

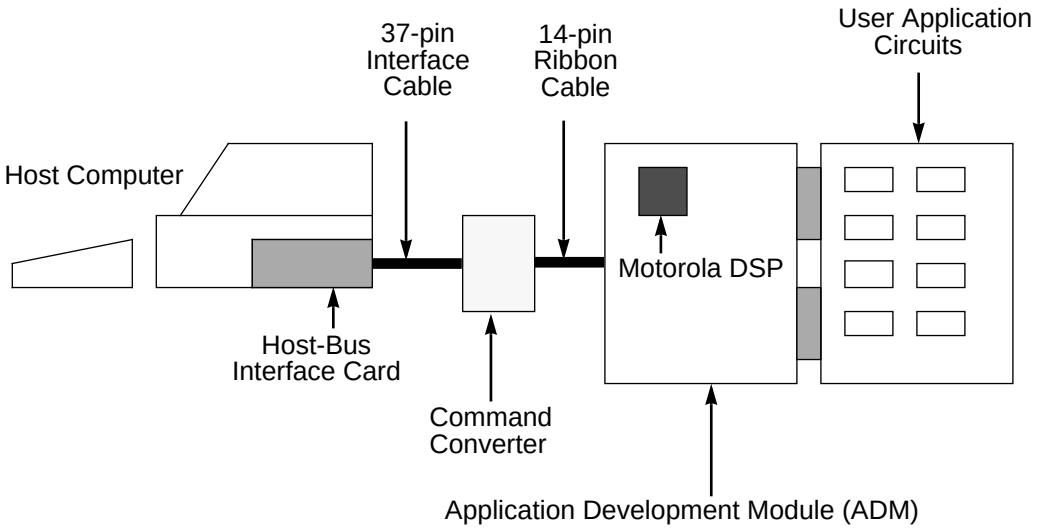


Figure 1-2 Application Development

1.4 USING THE DSP56301ADM

Once the ADM is installed, it becomes a part of the Application Development System. Use information in the Application Development System User's Manual to develop your application design, debug it, and test it.

SECTION 2

DSP56301ADM TECHNICAL SUMMARY

2.1 DSP56301ADM DESCRIPTION AND FEATURES

The DSP56301ADM is designed as a versatile card that can be used not only as a stand-alone board, but can also be plugged into other cards. Four 50-pin connectors allow access to all the DSP signals, including V_{DD} and V_{SS}. This plug-in feature permits special configurations, including, among others, connection to a customized wire-wrapped or other application board to permit enhanced functionality. An overview description of the DSP56301ADM is also provided in the DSP56301ADM Product Information document (order number DSP56301ADMP/D) included with this kit.

The main features of the DSP56301ADM include the following:

- DSP56301 24-bit Digital Signal Processor
- 32 K Word FSRAM with 12 ns access (5 V)
- 64 K Byte Flash PROM Memory, 200 ns access on-board (3 V) programmable
- 512 K Word DRAM, 70 ns access.
- ISA bus compatible edge-connector (slave only operation).
- PCI bus compatible edge-connector (master & slave operation).
- Table mounted (stand-alone) operation, or computer plug-in card operation.
- Integrated Expansion and Logic-Analyzer Connectors.
- Dedicated SSI and SCI port connectors.
- JTAG/OnCE port connector for easy hookup to Motorola command converter
- 5 V operation, with on board 3.3 V voltage regulation.
- Power terminals and 8-pin clock socket for stand-alone operation.

Note: Call your local Motorola sales office or distributor for additional information about the Motorola Application Development System (ADS) kit. The ADS kit includes two additional boards: a host interface card and an external universal command converter. The host interface card plugs in the host bus (on a PC-compatible, HP7xx workstation, or Sun/Sun-compatible system) inside the computer chassis. The external universal command converter card connects to the host card via a 37-pin ribbon cable. The command converter card connects to the JTAG connector on the DSP56301ADM via another short 14-pin ribbon cable. The ADS is only compatible with Motorola software tools.

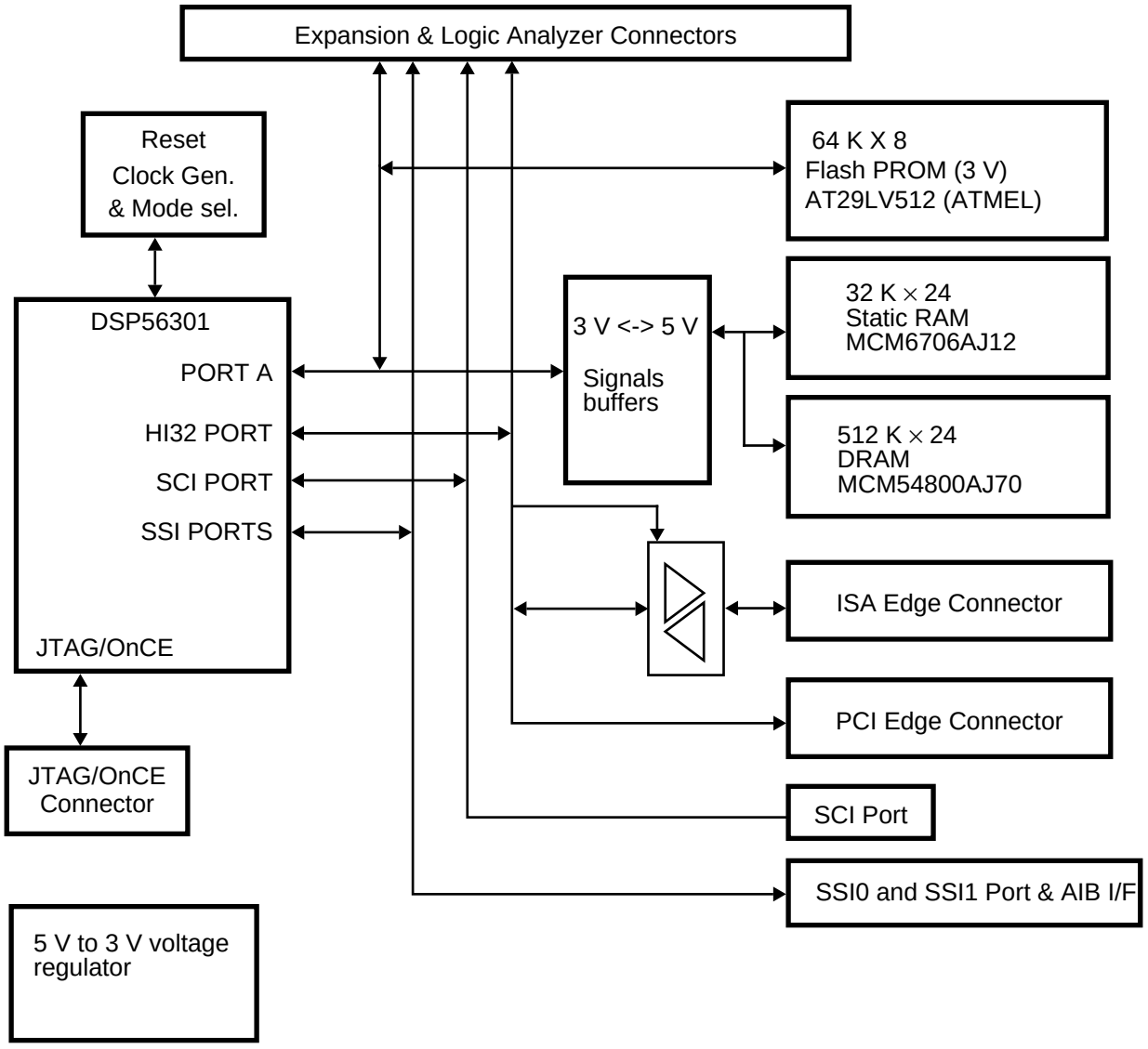


Figure 2-1 DSP56301ADM Functional Block Diagram

2.2 DSP56301 DESCRIPTION

A full description of the DSP56301, including functionality and user information is provided in the following documents included as a part of this kit (either as printed copies or on the documentation CD-ROM):

- **DSP56301 Technical Data—**Provides features list and specifications including signal descriptions, DC power requirements, AC timing requirements, and available packaging
- **DSP56301 User's Manual—**Provides an overview description of the DSP and detailed information about the on-chip components including the memory and I/O maps, peripheral functionality, and control and status register descriptions for each subsystem
- **DSP56300 Family Manual—**Provides a detailed description of the core processor including internal status and control registers and a detailed description of the family instruction set

Refer to these documents for detailed information about chip functionality and operation.

2.3 MEMORY

Table 2-1 lists the memory used in the DSP56301ADM.

Table 2-1 DSP56301ADM Memories

TYPE	SIZE	SPEED	AA line (used as chip select)
DRAM	512 K Word	70 ns	AA3
SRAM	32 K Word	12 ns	AA0
Flash PROM	64 K Byte	200 ns	AA1

2.3.1 DRAM Selection

The DSP56301ADM uses a single bank of three 512 K × 8, 70 ns, 5 V-only DRAMs (Motorola MCM54800AJ70). The DRAM is accessed by the DSP56301 using 3 wait-cycles during Page mode (not including the RAS precharge time at a beginning of a new page) and 11 wait-cycles in a non-page access, when the DSP operates at 66MHz. Address bus load capacitance from this configuration is 5 pF × 3, or 15 pF per address line. Data bus load capacitance is 7 pF. The AA3 (Address Attribute) signal is used as a Row Address Strobe ($\overline{RAS}$) and Chip Enable ($\overline{CE}$) line. The design uses the SOJ package to achieve greatest space reduction. DRAM refresh is provided by the DSP56301 DRAM controller. The DRAM connection is illustrated in **Figure 2-2**.

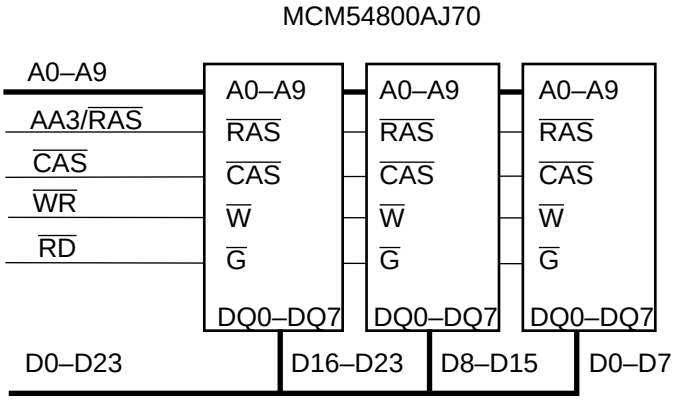


Figure 2-2 DSP56301ADM DRAM Interface

Note: The DRAM memory is enabled / disabled using jumper JP2. When JP2 is placed, the DRAM is enabled. When JP2 is removed, the DRAM is disabled, and the user may use AA3 for other purposes.

2.3.2 SRAM Selection

Three Motorola MCM6706AJ12 SRAMs are used to optimize performance. These SRAMs are 32 K × 8, Bi CMOS, 5 V-only devices with an access time of 12 ns. Address bus load capacitance in this configuration is 5 pF × 3, or 15 pF per address line. Data bus load capacitance is 6 pF. The SRAM is accessed by the DSP56301 with 1 wait-state when the DSP operates at 66MHz clock. The chip-select signal for the SRAM is generated using the DSP56301 AA0 line. The MCM6706AJ12 SRAM uses 5 V input power. Connection to the SRAM is shown in **Figure 2-3** on page 2-7.

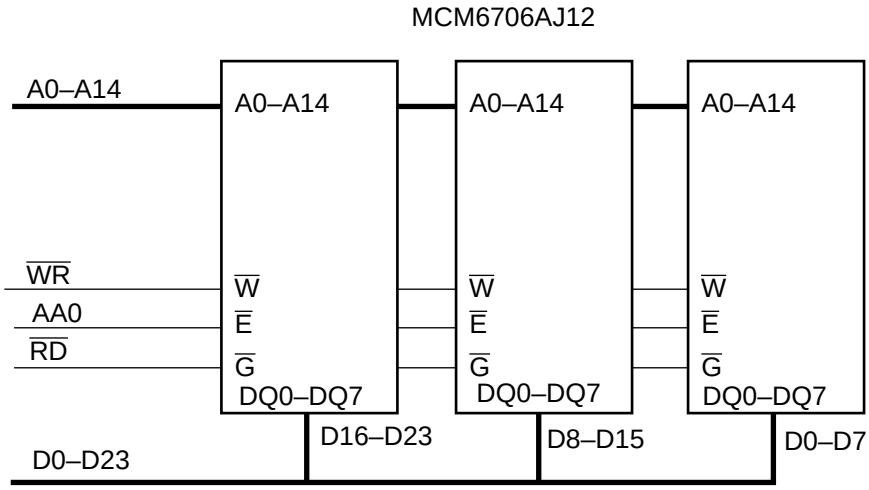


Figure 2-3 SRAM Connection

Note: The SRAM memory is enabled / disabled using jumper JP1.When JP1 is placed, the SRAM is enabled. When JP1 is removed, the SRAM is disabled, and the user may use AA0 for other purposes.

2.3.3 Flash PROM Selection

The DSP56301ADM includes a Flash PROM to facilitate stand-alone operation. The FPROM is on-board and programmable, making it ideal for programming updates. The DSP56031ADM uses a programmable, byte-wide, AT29LV512, 3 V-only (eliminating the need for additional supply or a DC-DC converter) FPROM with 200 ns access time. The load capacitance of this chip is 6 pF on the address lines and 12 pF max on the data lines. The Flash memory may tolerate up to 1000 program cycles per sector (each sector is 128 bytes—total of 512 sectors).

The AT29LV512 has a low-power write-protect feature to guard against inadvertent writes during power transitions. The FPROM also permits data polling during programming to shorten programming cycles. **Figure 2-4** on page 2-8 illustrates the DSP56301 hookup to a byte wide non-volatile memory. All actions to the device are controlled via a sequence of commands written to the device.

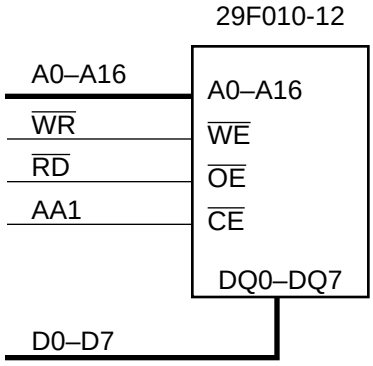


Figure 2-4 Flash PROM Connection

Note: The Flash memory is enabled / disabled using jumper JP3. When JP3 is placed, the Flash is enabled. When JP3 is removed, the Flash memory is disabled, and the user may use AA1 for other purposes.

2.4 DSP56301 OPERATING MODE SELECTION

Support is provided to enable the DSP56301 to enter one of six possible operating modes (two additional modes are reserved), via MODA / IRQA–MODC / IRQC and NMI / PINIT lines.These lines are sampled by the DSP56301 on the rising edge of RESET line and the sampled combination is moved to the OMR (Operating Mode Reg.). **Figure 2-5** illustrates the mode selection on the deassertion of the RESET signal. After reset, the mode selection lines are driven by pull-up resistors. JP12 is connected to the NMI / PINIT line.

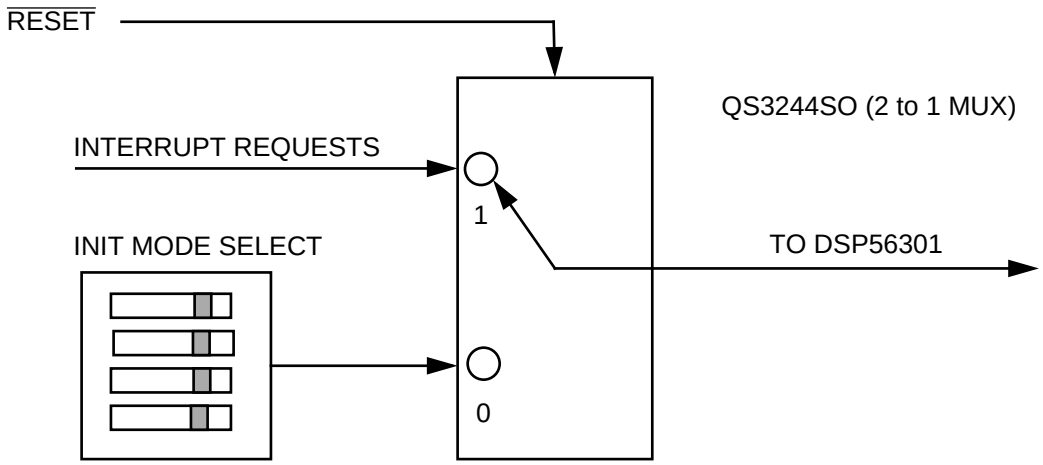


Figure 2-5 DSP Mode Selection

Table 2-2 DSP56301 Operating Mode Selection

MODE	SW2(1)	SW2(2)	SW2(3)
0—Expanded mode	On	On	On
1—Bootstrap from byte-wide FLASH	Off	On	On
2—Bootstrap through SCI	On	Off	On
3—Reserved	Off	Off	On
4—Host Bootstrap PCI mode (32-bit-wide)	On	On	Off
5—Host Bootstrap ISA Mode (16-bit-wide)	Off	On	Off
6—Host Bootstrap UB Mode (8-bit-wide)	On	Off	Off
7 —Reserved	Off	Off	Off

After the $\overline{\text{RESET}}$ line is released (high) the MOD / $\overline{\text{IRQ}}$ signals are connected to $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, and $\overline{\text{IRQC}}$ signals.

2.5 CLOCK SOURCE SELECTION

There are 3 clock sources to the DSP56301:

- On-board 33MHz clock generator, supplied from factory
- External BNC connector
- Crystal Oscillator

Note: When either of the first two options are used, set bits XTLD and COD in the PLL Control Register (PCTL) to disable unnecessary clock signals and avoid unnecessary on-board radio frequency emissions.

2.5.1 On-Board Clock Generator Selection

The clock generator is socketed to allow easy replacement with different frequency clock generators. The board is supplied with a 33 MHz clock generator. The PCB layout is designed so that either a 14-pin DIP packages or an 8-pin DIP packages may be accepted. The clock generator should be placed in the socket as shown in **Figure 2-6**. To select the on-board clock generator, JP13 should not be jumpered, and JP14 should be jumpered from pin 2 to pin 5. The DSP56301ADM comes with aDIP14 package 33 MHz clock generator.

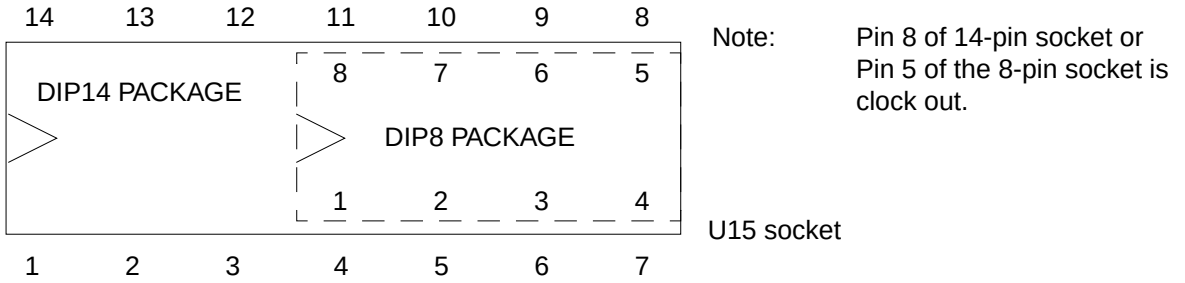


Figure 2-6 3.3 V Clock Generator Assembly

2.5.2 External Clock Selection

To support non-standard clock rates and frequency fine tuning, the DSP56301ADM provides a 50 Ω impedance, DC-coupled, BNC connector for a 3.3 V clock input. To select the external clock generator, JP13 should not be jumpered, and JP14 should be jumpered from pin 3 to pin 4.

Note: For proper operation, the external clock must have rise / fall times < 3 ns.

2.5.3 Crystal Oscillator Selection

By using a low-frequency crystal oscillator, the user can reduce external high frequency emissions, while still allowing the the DSP56301 to run at higher operating frequencies generated by the on-chip PLL. The crystal must have bypass capacitors at both ends. When the crystal oscillator is used, the user should install appropriately rated components C32,C33,R16,R17 and Y1 (See the *DSP56301 Technical Data* sheet for more information). To enable the on-board crystal oscillator, place a jumper on JP13 and another jumper across pins 1–6 on JP14.

Note: Power should be turned off prior to inserting / removing the crystal oscillator.

2.5.4 DSP56301 PLL Enable/Disable On Reset

The DSP56301 samples the PINIT / $\overline{\text{NMI}}$ line on exit from the reset state to determine whether the PLL should be enabled or disabled. To enable the PLL, JP12 should be jumpered. To disable the PLL, JP12 pins 1-2 should be jumpered.

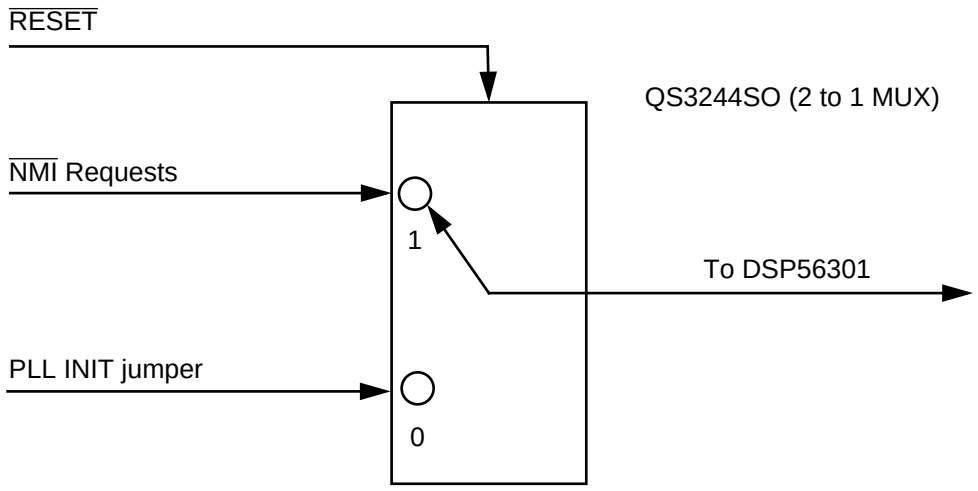


Figure 2-7 PLL Mode Selection

After the $\overline{\text{RESET}}$ line is deasserted the PINIT / $\overline{\text{NMI}}$ signal is connected to the $\overline{\text{NMI}}$ signal.

Note: The ADM is factory configured for PLL enabled (JP12 removed).

2.6 HOST PORT SELECTION

The DSP56301's HI32 port directly supports a PCI bus interface. Connection to an ISA bus interface requires the addition of external buffers. The DSP56301ADM supports application development for either bus by providing both a PCI edge connector and an ISA edge connector (with the appropriate buffers).

When the DSP56301ADM is used with ISA host, place a jumper across JP4, JP5, JP6, and JP7 with the components U16, U17, U18, U19, U20, RN1, and RN2 mounted in their sockets. When the ADM is used in PCI host or as a stand-alone device, there should be no jumpers on JP4, JP5, JP6, and JP7 and the components in U16, U17, U18, U19, U20, RN1, and RN2 should be removed.

Note: The ADM is factory configured for ISA Host Mode.

2.7 ISA DMA AND INTERRUPT CHANNELS

The ADM enables the user to configure one of four channels for DMA and one of four interrupt channels for an ISA bus interface. **Table 2-3** and **Table 2-4** describe these configurations options.

Table 2-3 ISA Bus DMA Channel Configuration

DMA Channel	JP8	JP10
0	None	1–8, 2–7
5	None	3–6, 4–5
6	3–6, 4–5	None
7	1–8, 2–7	None

Table 2-4 ISA Bus Interrupt Selection

Interrupt	JP11
5	3–6
6	2–7
7	1–8
10	4–5

2.8 CONNECTORS

The DSP56301ADM includes the following connectors:

- Expansion and Logic-Analyzer connector—four 2 × 25-pin SMD pin-rows
- Power—2-pin terminal block, two-part
- HI32 port—ISA and PCI edge connectors
- SSI I/F—Two connectors: 2 × 7 and 2 × 15 SMD pin-rows
- JTAGE/OnCE port connector—2 × 7 SMD pin-rows

2.8.1 Expansion And Logic Analyzer Connectors

The DSP56301ADM has a set of four dual-in-line 50-pin SMD pin rows connectors to support both hardware expansion and logic-analyzer connection. These connectors are connected to all the pins of the DSP56301 chip except for the PCAP, XTAL, EXTAL, MODA, MODB, MODC, and PINIT. All the other DSP56301 pins are routed to these connectors along with +3.3 V and GND pins. The power and ground pins facilitate hardware expansions powered by the DSP56301ADM. **Figure 2-8** on page 2-14, **Figure 2-9** on page 2-15, **Figure 2-10** on page 2-16, and **Figure 2-11** on page 2-17 show the pinouts for these connectors.

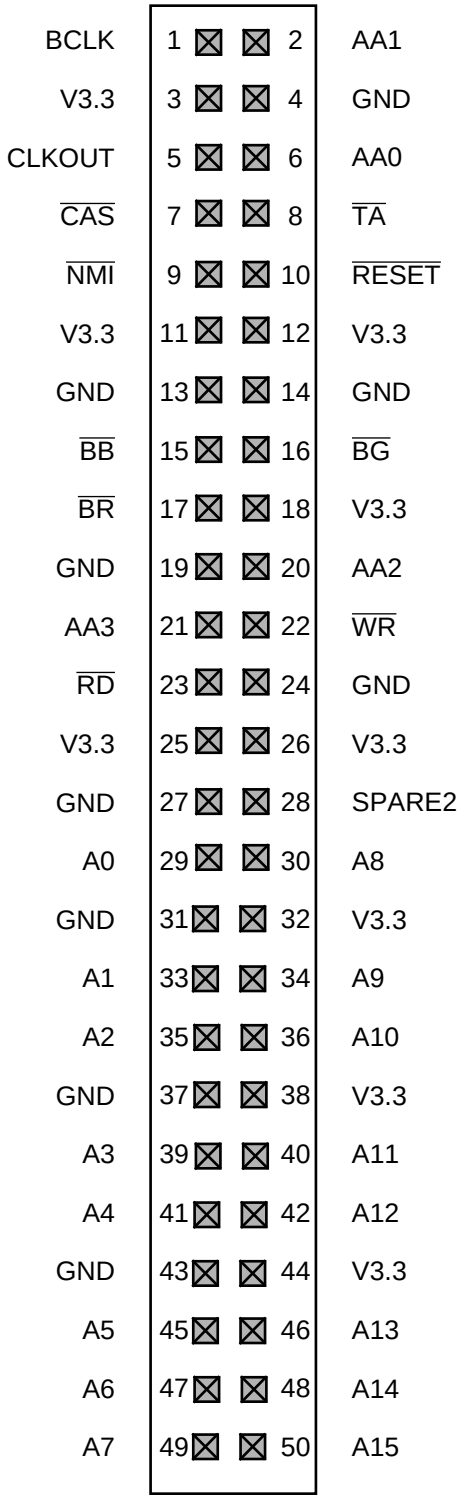


Figure 2-8 Expansion Connector (P10)

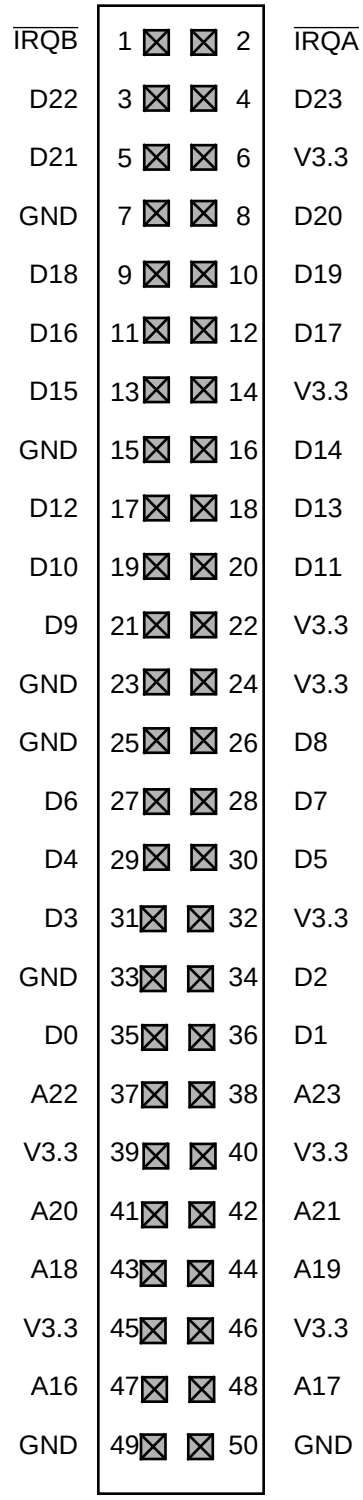


Figure 2-9 Expansion Connector (P12)

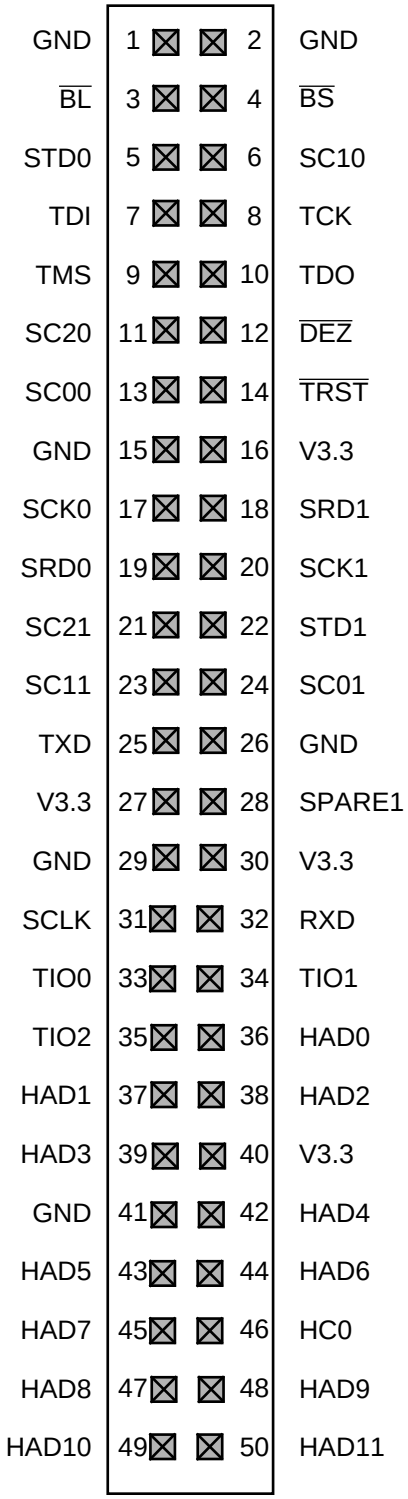


Figure 2-10 Expansion Connector (P5)

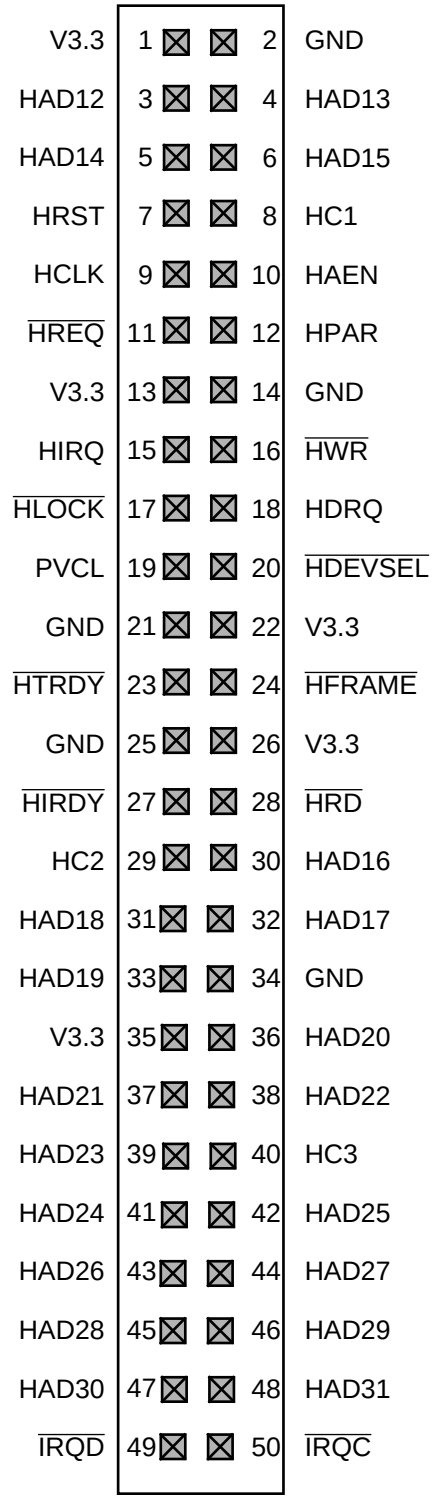


Figure 2-11 Expansion Connector (P7)

2.8.2 5 V Power Connector

The 5 V power connector to the DSP56301ADM is a 2-lead terminal block next to the power switch SW1. The power connector and power switch are only used for stand-alone operation; the power switch SW1 is used to turn the ADM on or off.

2.8.3 HI32 Connector

There are two HI32 connectors on the DSP56301ADM:

1. PCI edge connector, configured as 32-bit universal (5 V & 3.3 V) connector
2. ISA edge connector

These connectors are located on opposite sides of the DSP56301ADM, enabling it to operate using an ISA, EISA, or PCI bus interface. The PCI edge connector is keyed with both 5 V and 3.3 V keys to permit operation with either 5 V or 3.3 V PCI-backplanes.

2.8.4 SSI Port Connectors

The SSI port pins appear on three different connectors:

- The Expansion & Logic-Analyzer connectors
- Two dedicated SSI port connectors
- DSP56004 Audio Interface Bus (AIB) compatible connector

The SSI pins are multiplexed to these connectors to permit connection of the SSI pins to various applications. The dedicated general purpose connectors are for general purpose use to be connected via a ribbon cable to another board. To avoid crosstalk and supply concurrent impedance path for the ongoing signals, GND lines are inserted between the signal lines. To avoid incorrect insertion of the receptacle connector, keying is provided as pin 13 is cut while its corresponding hole in the receptacle connector is filled. The pinout of the independent SSI connector is shown in **Figure 2-12**

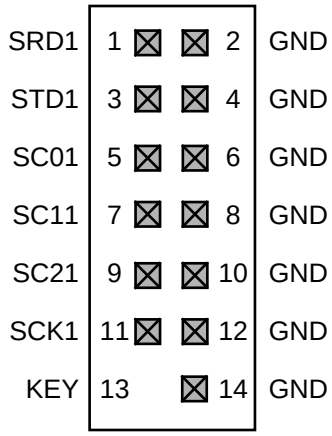


Figure 2-12 Dedicated SSI Connector (P3)

The AIB interface connector is meant to support the DSP56004 Audio Interface Board (AIB), a high-quality audio board with two stereo 18-bit ADCs and three stereo 18-bit DACs, originally designed to for the DSP56004. The pinout of the SSI-AIB connector is shown in **Figure 2-13** on page 2-20. In the figure, the leftmost column contains the AIB connector signal names, while the next column contains the DSP56301 signal names. The DSP56301ADM supports one stereo output channel and one stereo input channel when connected to the AIB.

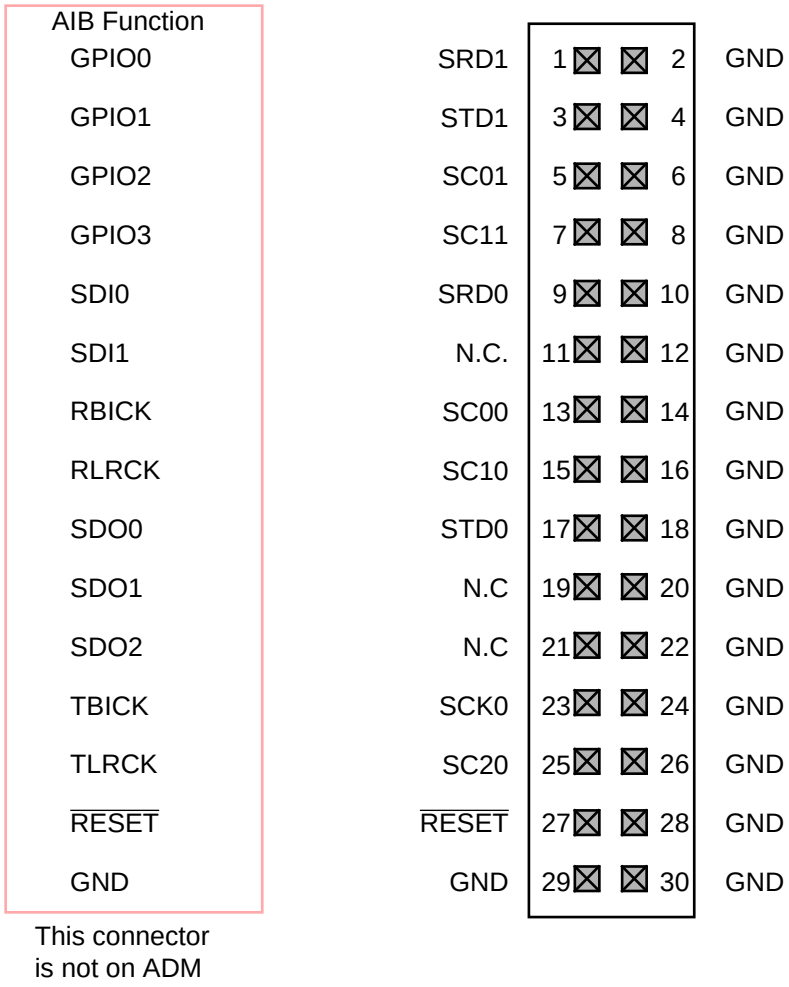


Figure 2-13 SSI - AIB Connector (P2)

2.8.5 SCI Port Connector

The SCI port pins are routed to two connectors:

- The Expansion & Logic-Analyzer connectors
- Dedicated SCI port connector

Routing to the expansion Logic-Analyzer connectors is done to support expansion boards and application debugging. The dedicated connector attaches to an application board via a ribbon cable. To avoid incorrect insertion of the plug into the receptacle, keying is provided via pin 6, which is cut, while its corresponding hole in the receptacle connector is filled.

The pinout of the SCI dedicated connector is shown in **Figure 2-14**.

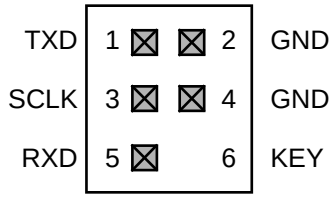


Figure 2-14 SCI Dedicated Connector (P6)

2.8.6 JTAG/OnCE Connector

The JTAG/OnCE connector is used both for JTAG testing during production, and for OnCE functions for code debugging and software development.The pinout of the JTAG/OnCE dedicated connector is shown in **Figure 2-15**.

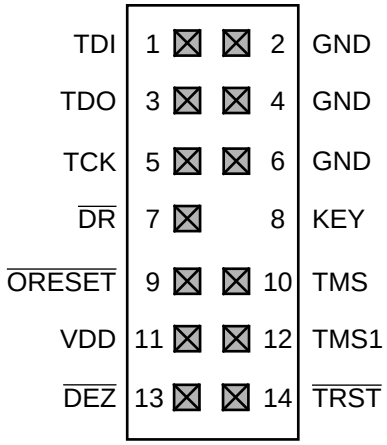
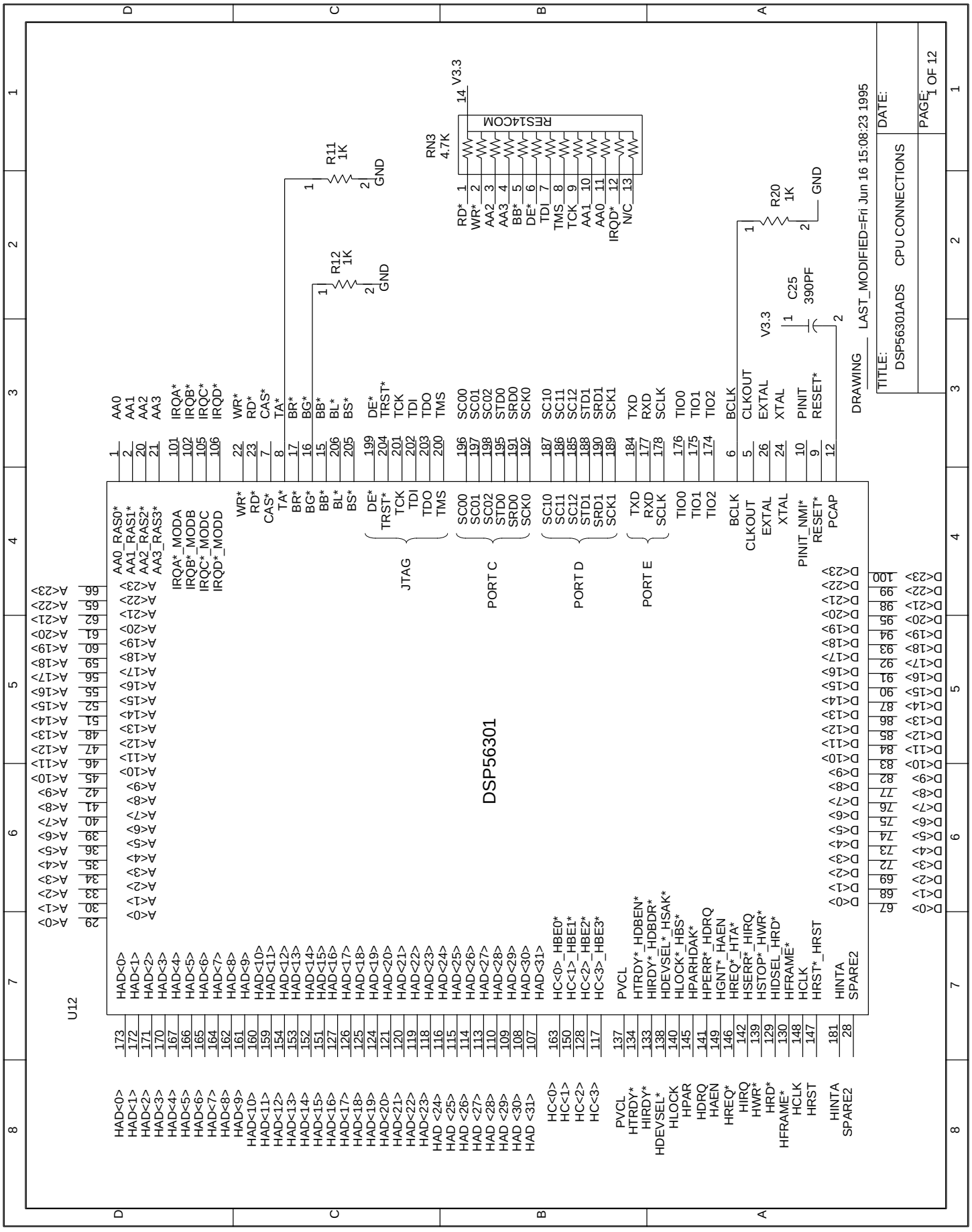
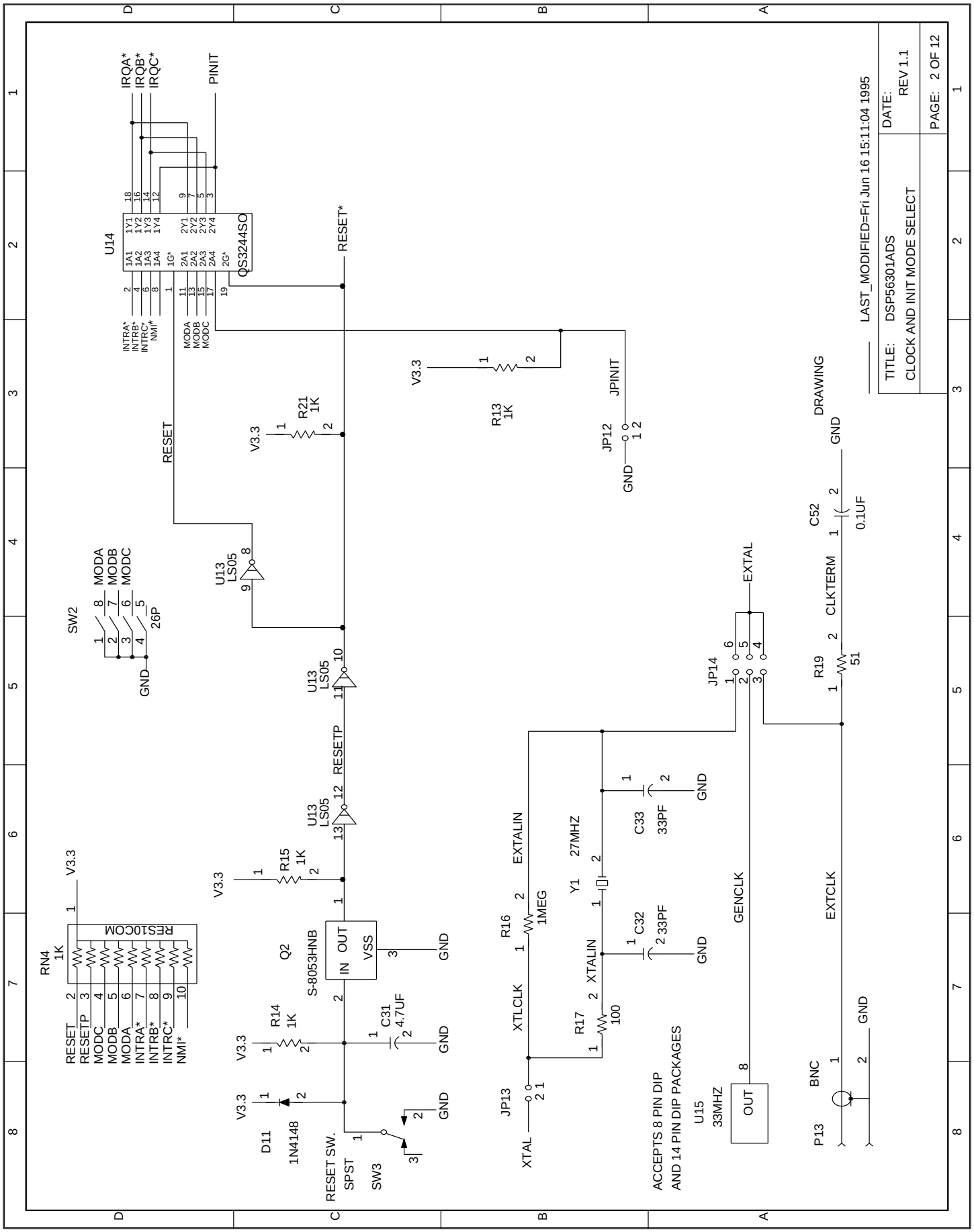


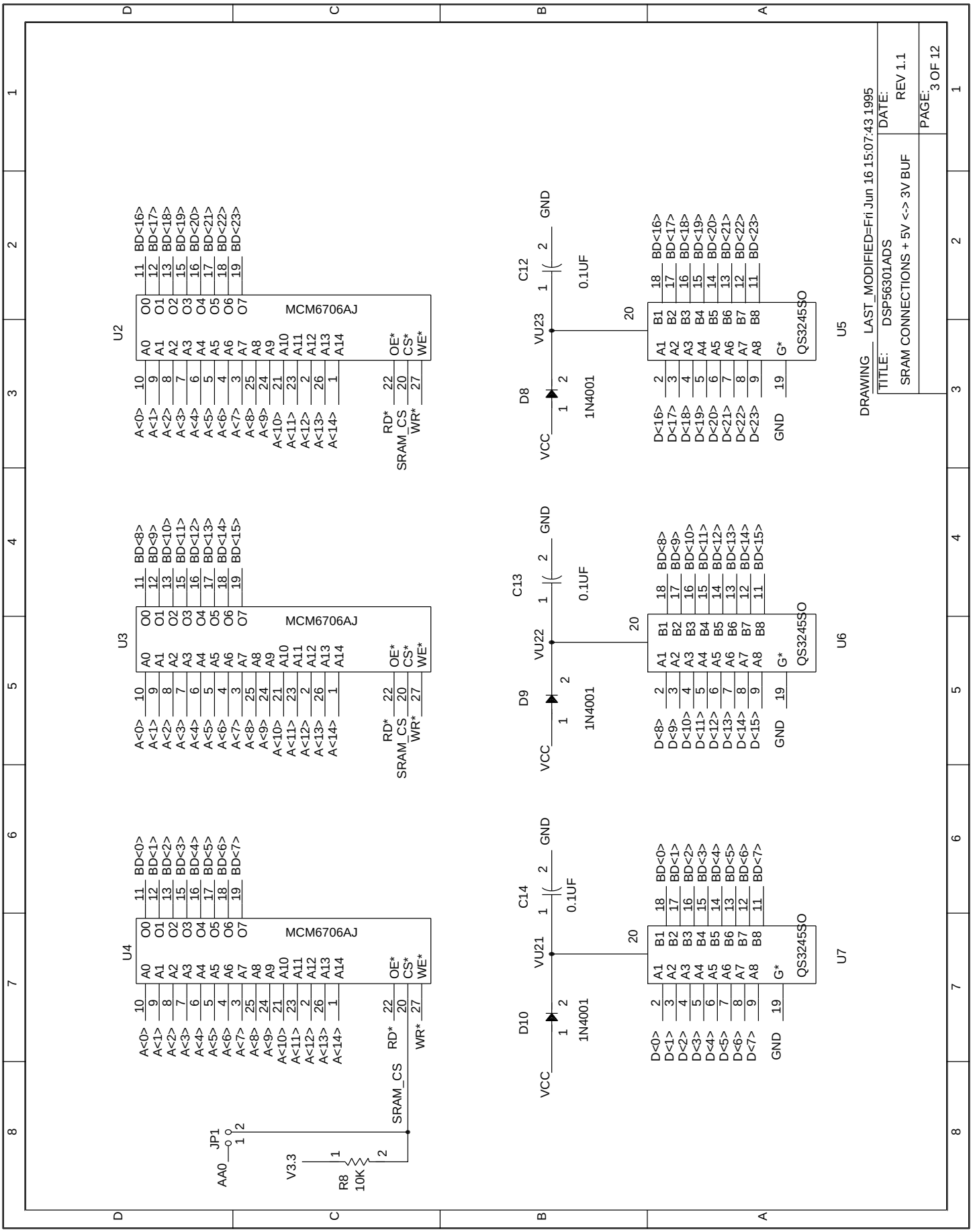
Figure 2-15 JTAG/OnCE Connector (P4)

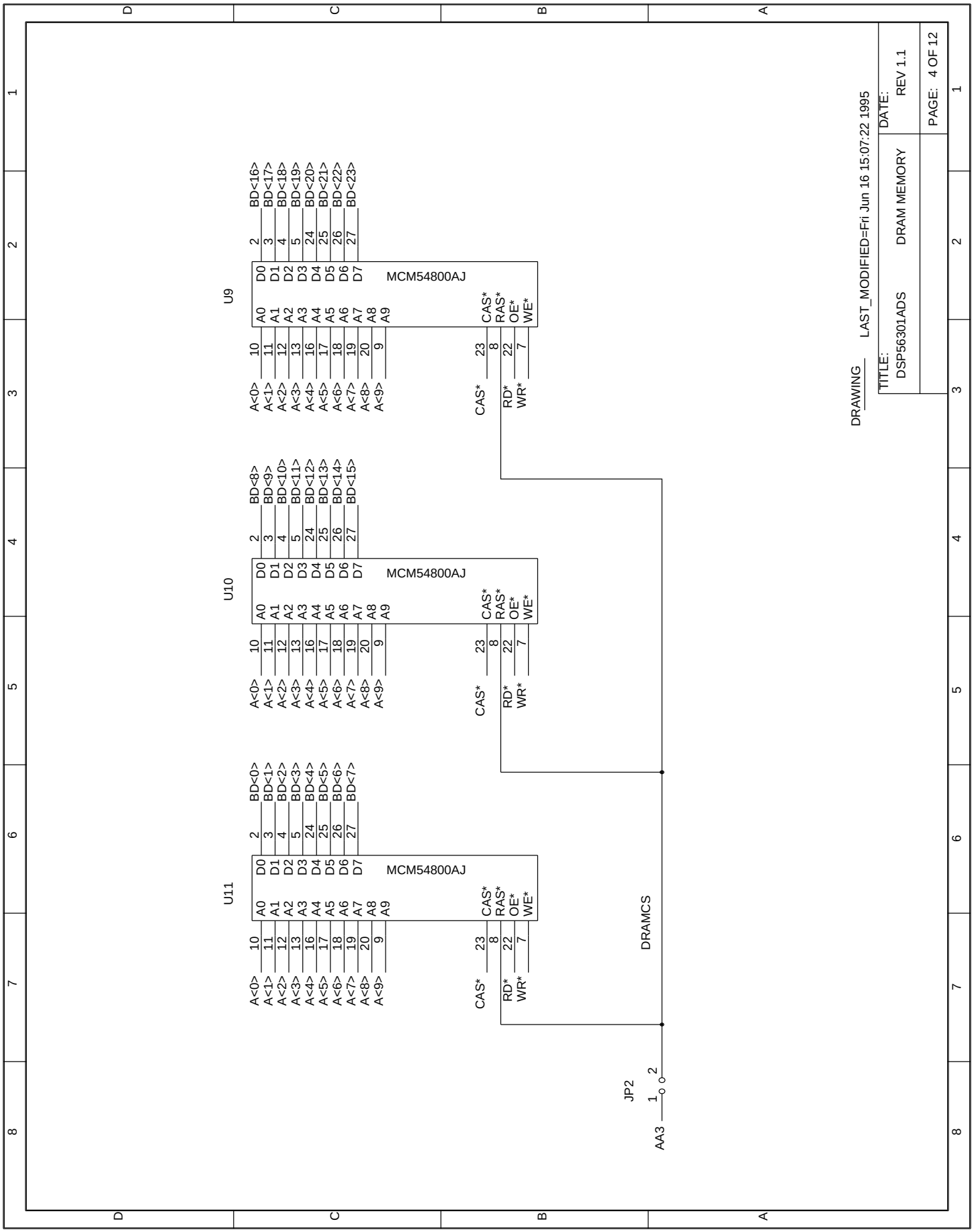
APPENDIX A

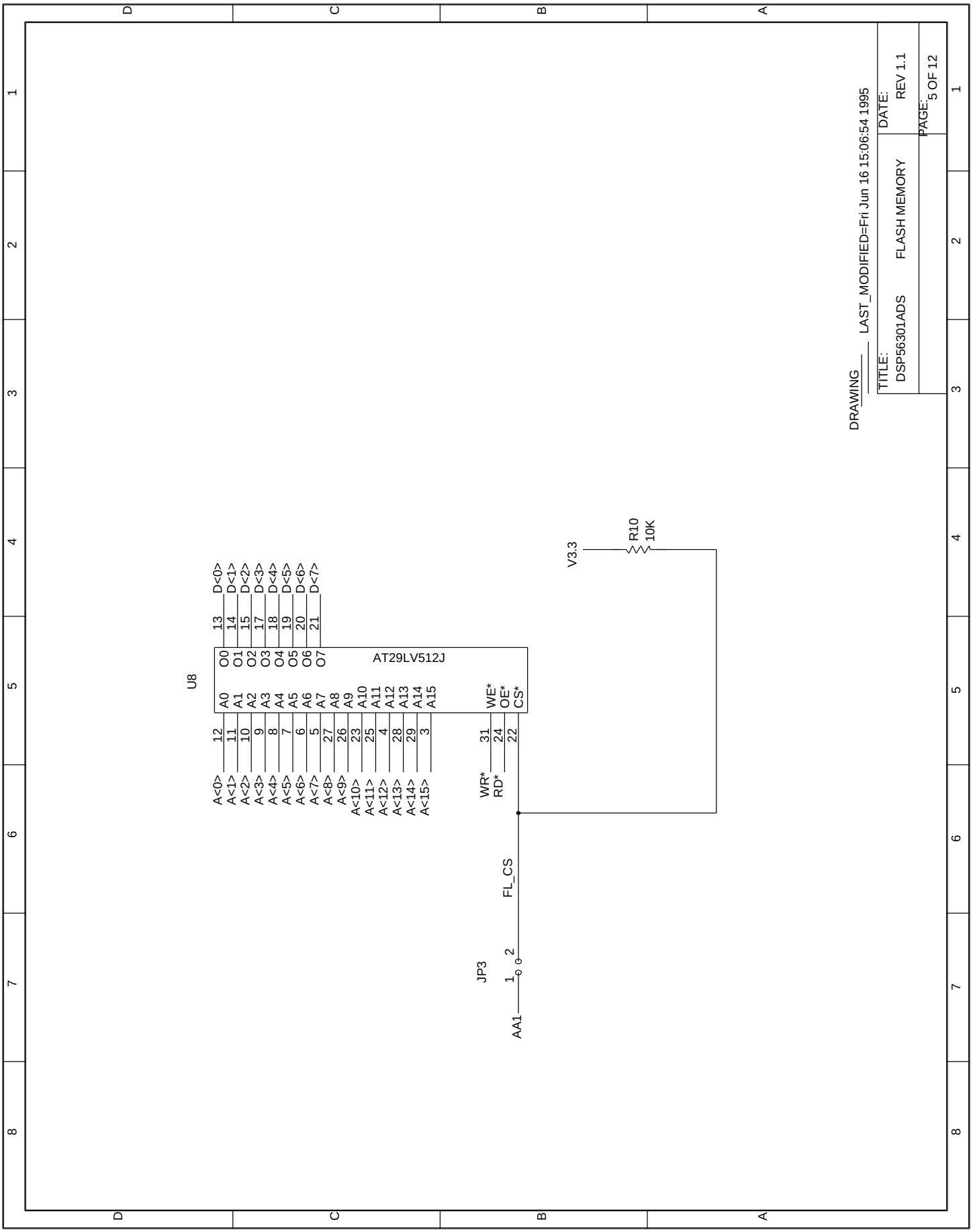
DSP56301ADM SCHEMATICS

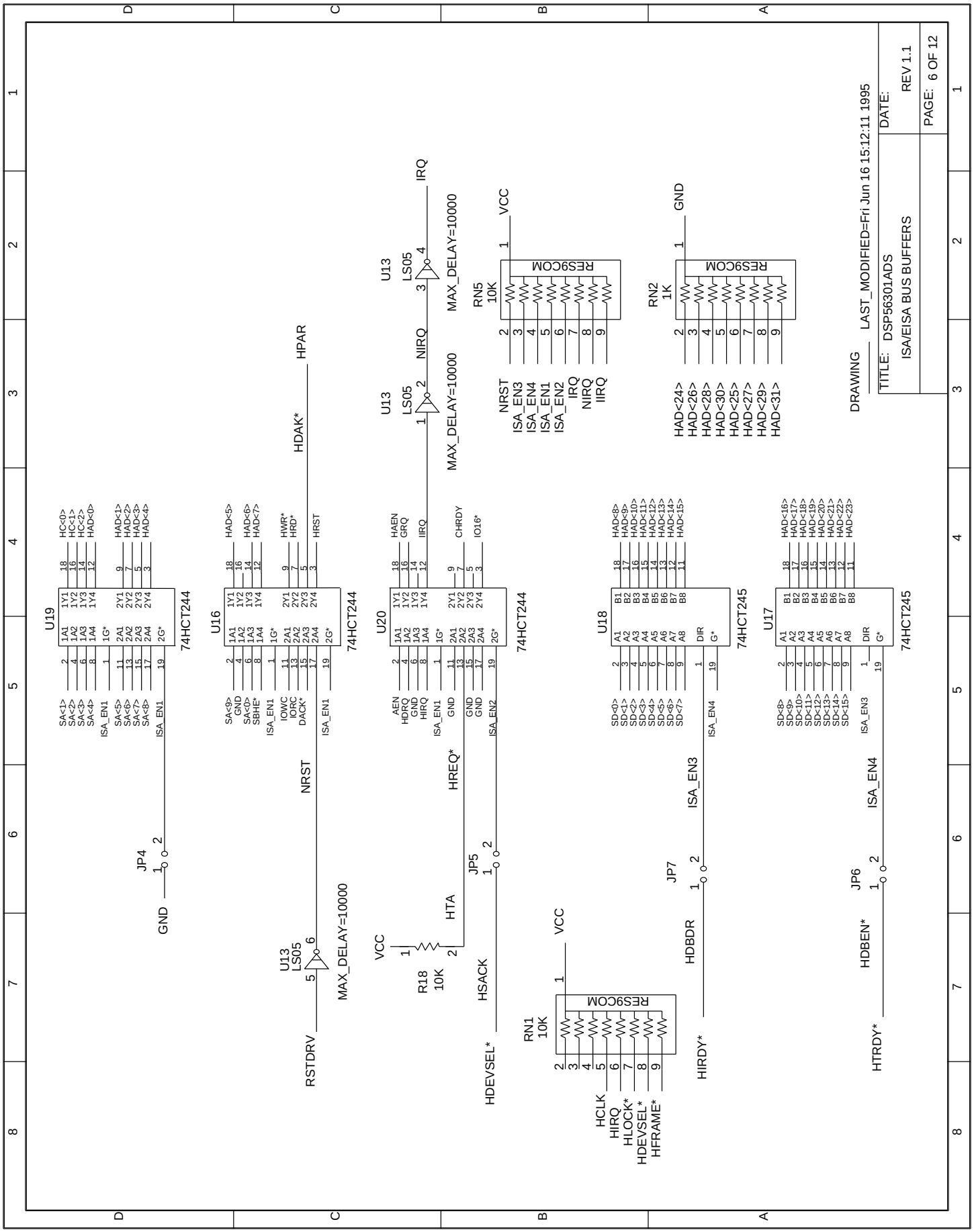


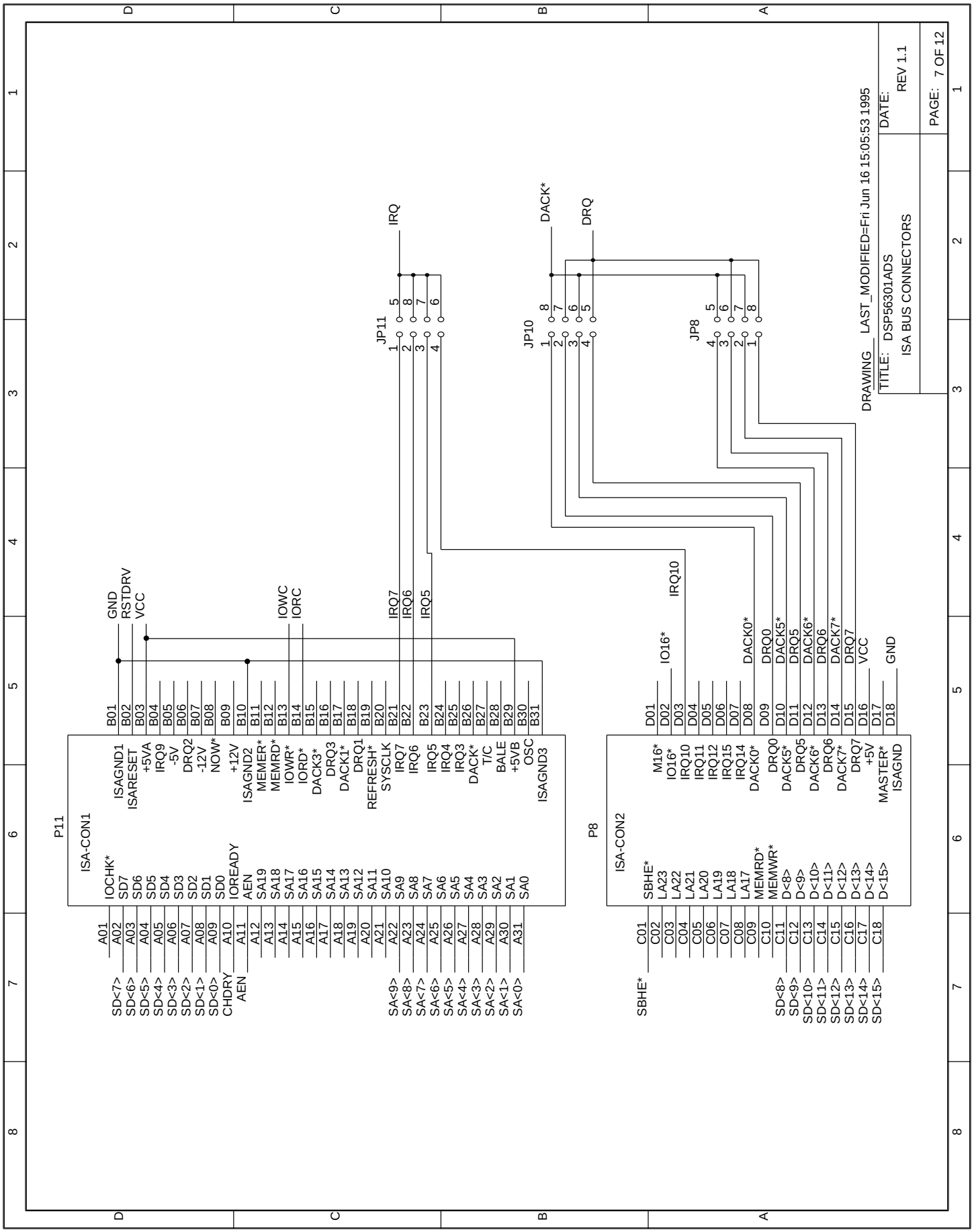


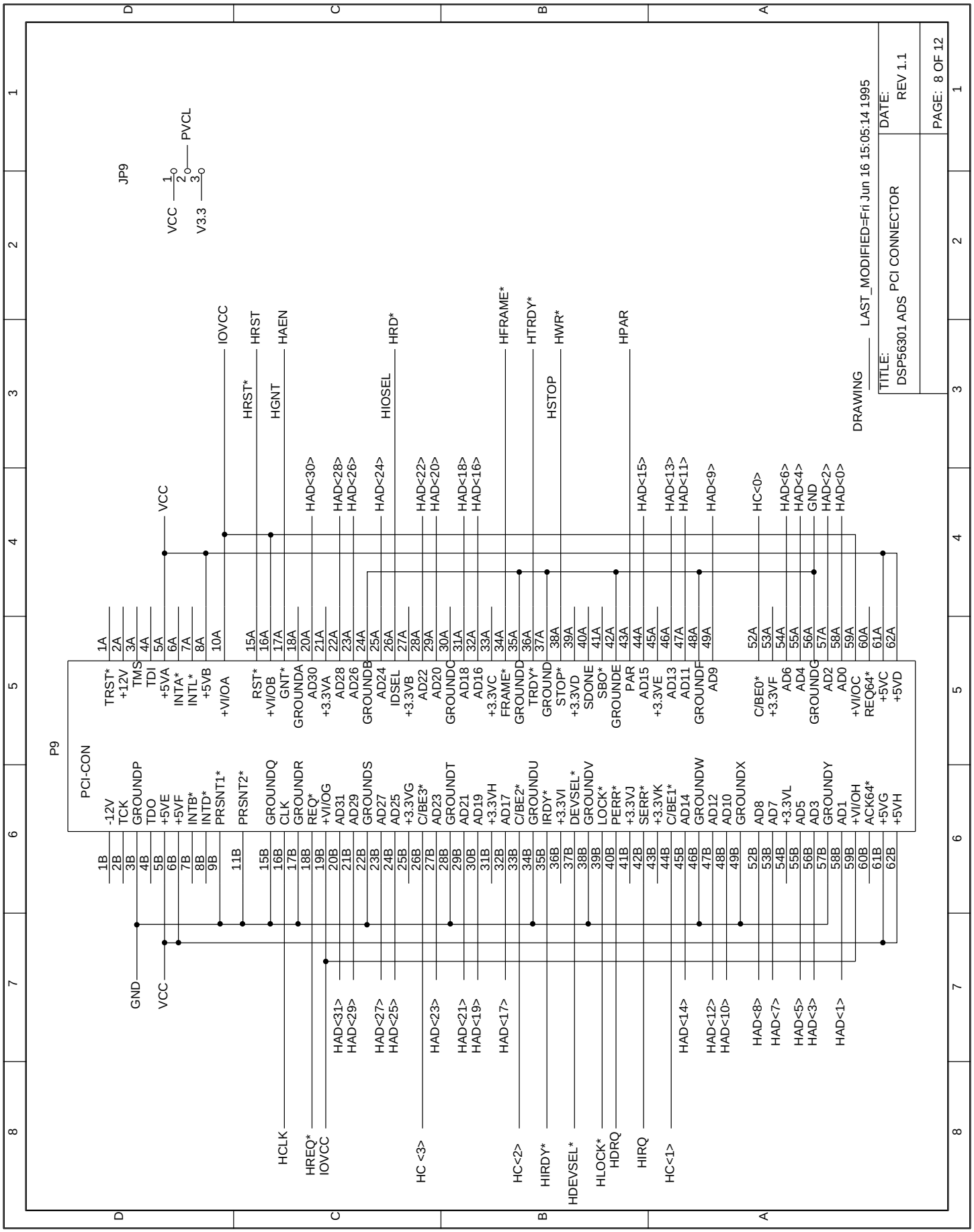


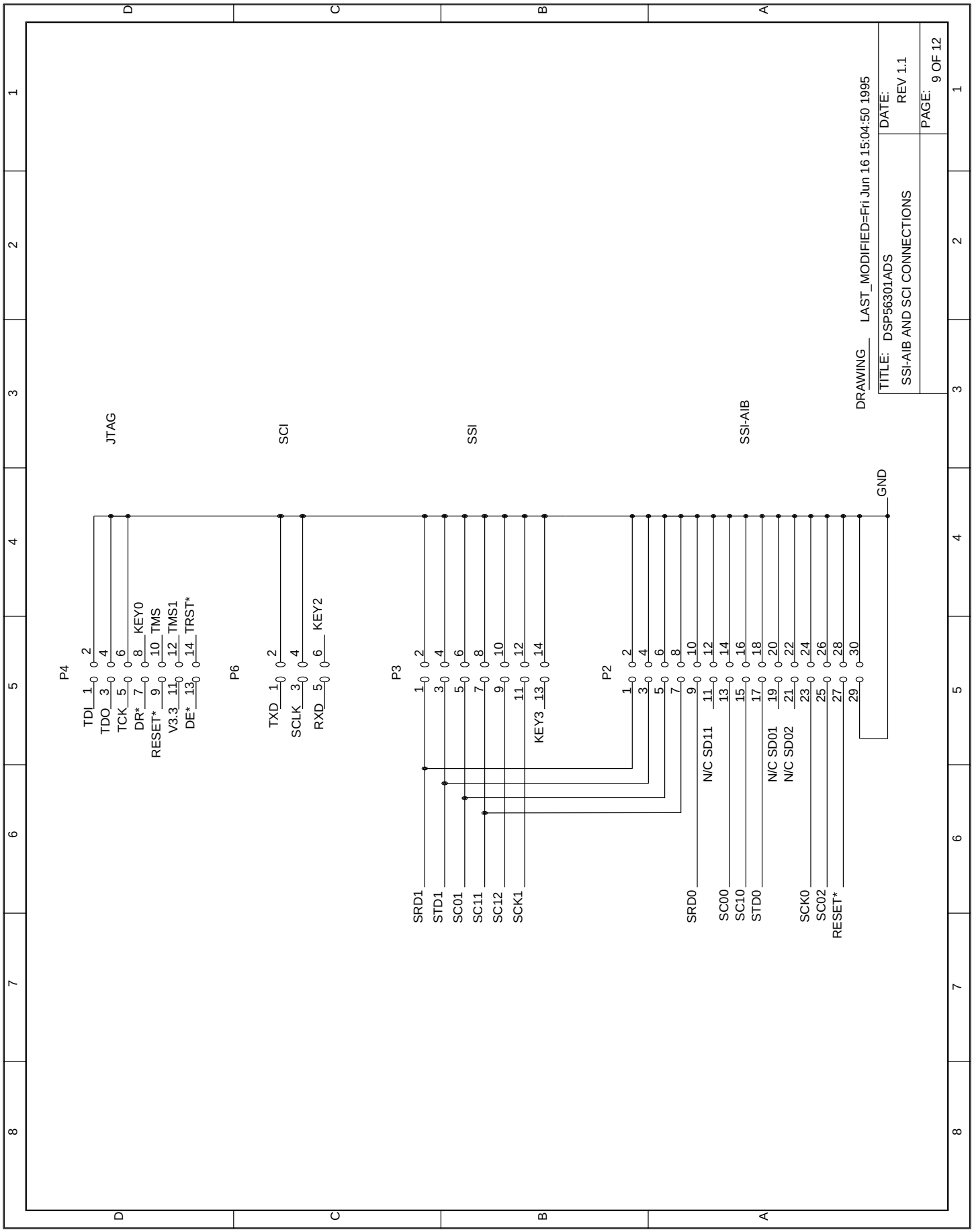


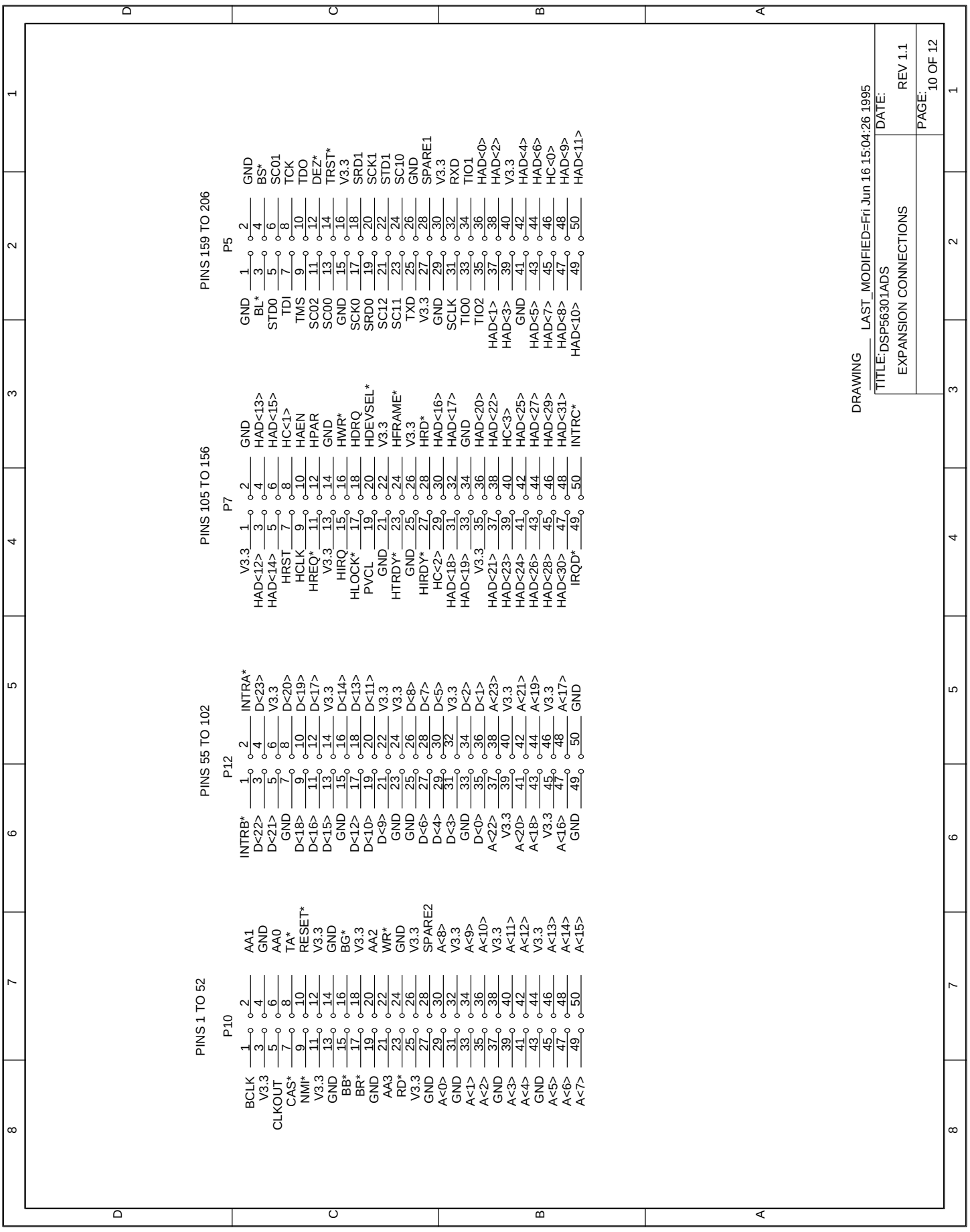


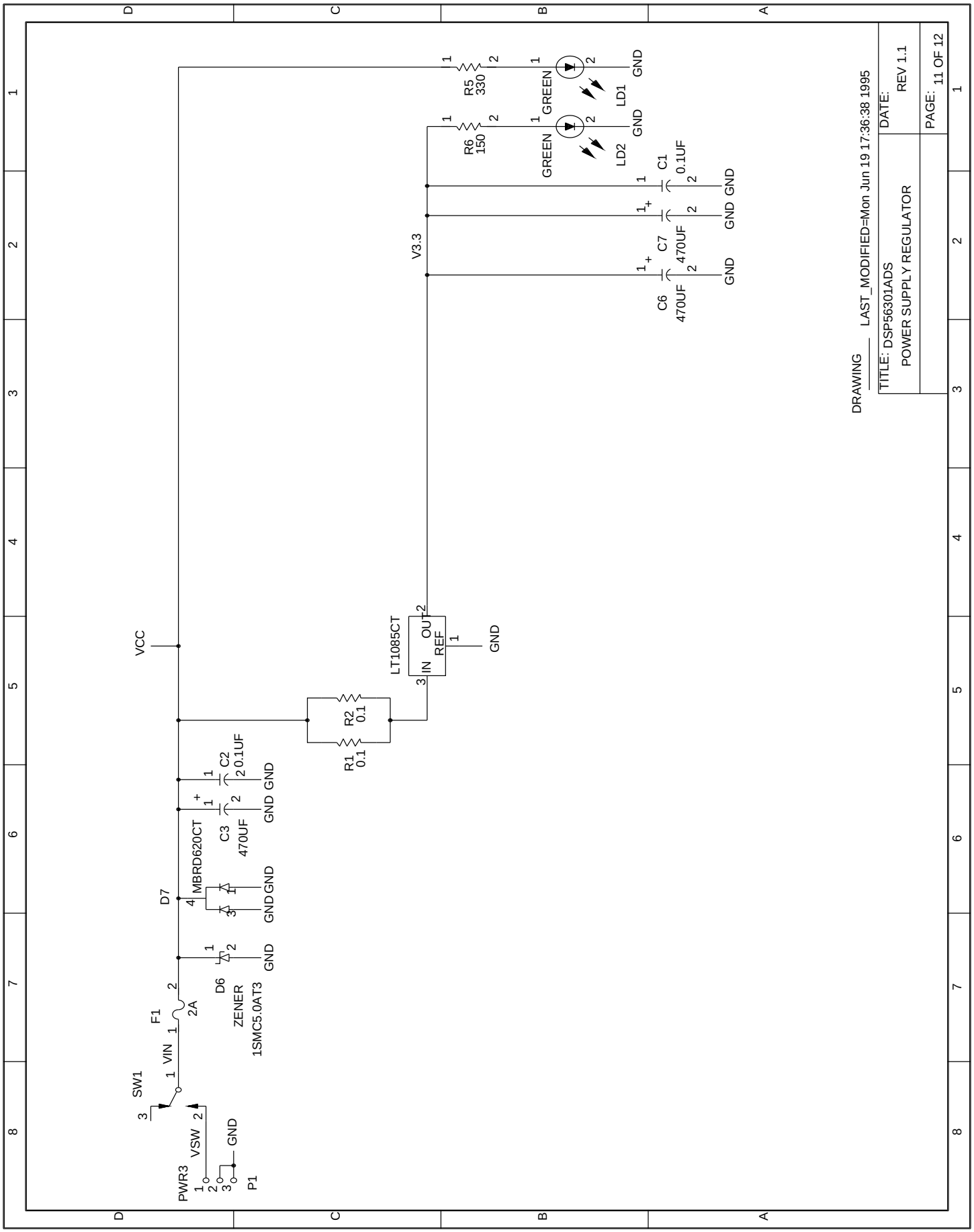


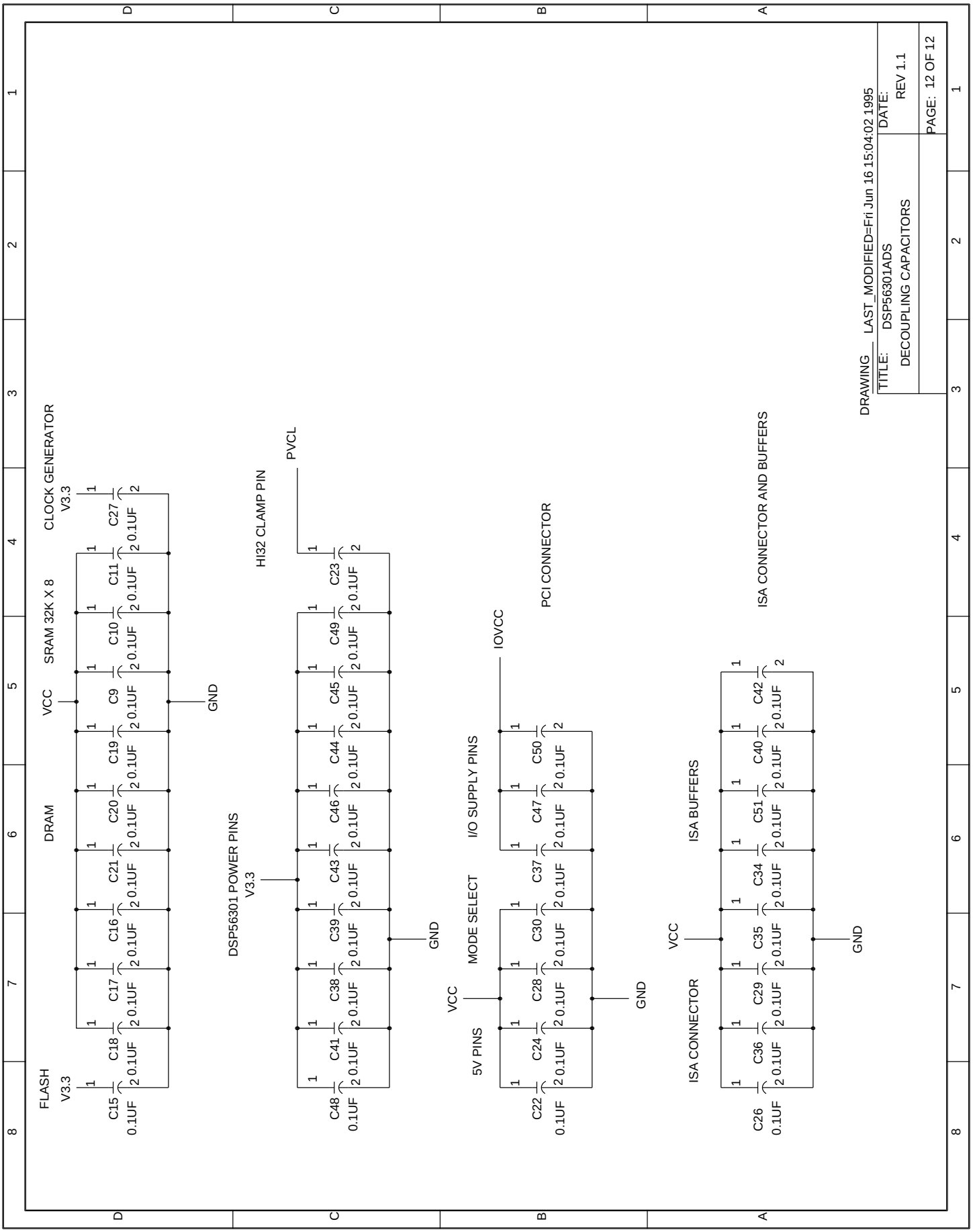












APPENDIX B

DSP56301ADM BILL OF MATERIALS

B.1 DSP56301ADM—ELECTRICAL PARTS LIST REV. 2.1—3/15/95

Qty	Description	Ref. Designators	Vendor Part #
		Integrated Circuits	
3	MCM6706AJ-12	U2, U3, U4	Motorola,IDT
3	QS3245SO	U5, U6, U7	Quality Semiconductor
1	AT29LV512-20J	U8	Atmel
3	MCM54800AJ-70	U9, U10, U11	Motorola, Toshiba
1	DSP56301	U12	Motorola
1	MC74LS05N	U13	
1	QS3244SO	U14	Quality Semiconductor
1	A53AA-33MHz	U15	Connor-Winfield
3	MC74HCT244AN	U16, U19, U20	Motorola
2	MC74HCT245AN	U17, U18	Motorola
		Crystal	
1	27 MHz	Y1	International Crystal #436161-27.00., FOX #HC94U-27.00MHz 30/50/20/10 Fundamental Frequency at Cut Crystal.
		Resistors	
2	0.1 Ω	R1, R2	1/4 W through hole
1	13 KΩ	R3	Bourns CR12061302JVCA
1	20 KΩ	R4	Bourns CR12062002JVCA
1	330 Ω	R5	Bourns CR12063300JVCA
1	150 Ω	R6	Bourns CR12061500JVCA
5	10 KΩ	R8, R9, R10, R18	Bourns CR12061002JVCA
7	1 KΩ	R11, R12, R13, R14, R15, R20, R21	Bourns CR12061001JVCA
1	1 MΩ	R16	Bourns CR12061004JVCA
1	100 Ω	R17	Bourns CR12061000JVCA
1	51 Ω	R19	Bourns CR120651R0JVCA

Qty	Description	Ref. Designators	Vendor Part #
		Resistor Networks	
3	10 KΩ	RN1, RN2, RN5	Bourns 4609X-101-103
1	4.7 KΩ	RN3	Bourns 4814P-002-472
1	1 KΩ	RN4	Bourns 4610X-101-102
		Transistors	
1	LT1085CT-3.3/3A	Q1	Linear
1	S-8053HNB	Q2	Seiko
		Fuse / Fuse Holder	
1	2 A	F1	Wickman 19197 2A Fast Blow Holder 19646
		LEDs	
2	Green LED	LD1,LD2	Hewlett Packard HSMG-C650
		Diodes	
2	Rectifier	D7	Motorola MBRD620CT
7	Rectifier	D8,9,10	Motorola 1N4001
1	Rectifier	D11	Micro-Semi 1N914
1	Rectifier	D6	Motorola 1SMC5.0AT3
		Capacitors	
43	0.1 µF	C1, C2, C9–C24, C26–C31, C35–C52	Murata Erie GRM42-6X7R104M25BB
3	470 µF	C3, C6, C7	Sprague 501D477M016MM
1	390 pF	C25	Murata Erie GRM42-6X7R391M50BB
2	33 pF	C32, C33	Murata Erie GRM42-6COG330M50BB

B.2 DSP56301 ADM—HARDWARE PARTS LIST REV. 2.1—3/15/95

Qty	Description	Ref. Designator	Vendor Part #
	Jumpers		
9	1 × 2 Bergstik	JP1–JP7, JP12, JP13	R.N. NSH-02SB-S2-TG30
3	8-pin Connector	JP8, JP10, JP11	Samtec TSM10401SDV
1	1 × 3 Bergstik	JP9	R.N. NSH-03SB-S2-TG30
1	6-pin Connector	JP14	Samtec TSM10301SDV
	Sockets		
1	32-pin PLCC	U8	Augat PCS-032SMU-1XT
1	14-pin DIP	U15	Augat 214-AG19SM
5	20-pin DIP	U16–U20	Augat 220-AG19SM
1	3-position Power	P1	Wieland 25.332.3353
3	1 × 9 Mach Strip	RN1, RN2, RN5	R.N. SBE-09-S-TG30
1	1 × 10 Mach Strip	RN4	R.N. SBE-10-S-TG30
	Connectors		
1	2-position Terminal Block	P1	Augat / RD1-MC6-P102-02
5	30-pin Connector	P2, P5, P7, P10, P12	Samtec TSM11501SDV
2	14-pin Connector	P3, P4	Samtec TSM10701SDV
4	20-pin Connector	P5, P7, P10, P12	Samtec TSM11001SDV
1	6-pin Connector	P6	Samtec TSM10301SDV
1	BNC	P13	Molex 73138-5003
	Switches		
1	Toggle	SW1	C&K E101MD1ABE
1	DIP	SW2	Grayhill 90HBW04S
1	Momentary	SW3	C&K E121SD1AGE
1	Pushbutton Cup		C&K 708902000
	Miscellaneous		
4	RUBBER FEET		Amatom #5186
1	4-40 SCREW	Located on Q1	
1	4-40 NUT	Located on Q1