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MODEL NAME : *Diaz UMA*

Project Code: *91.4AR01.001*

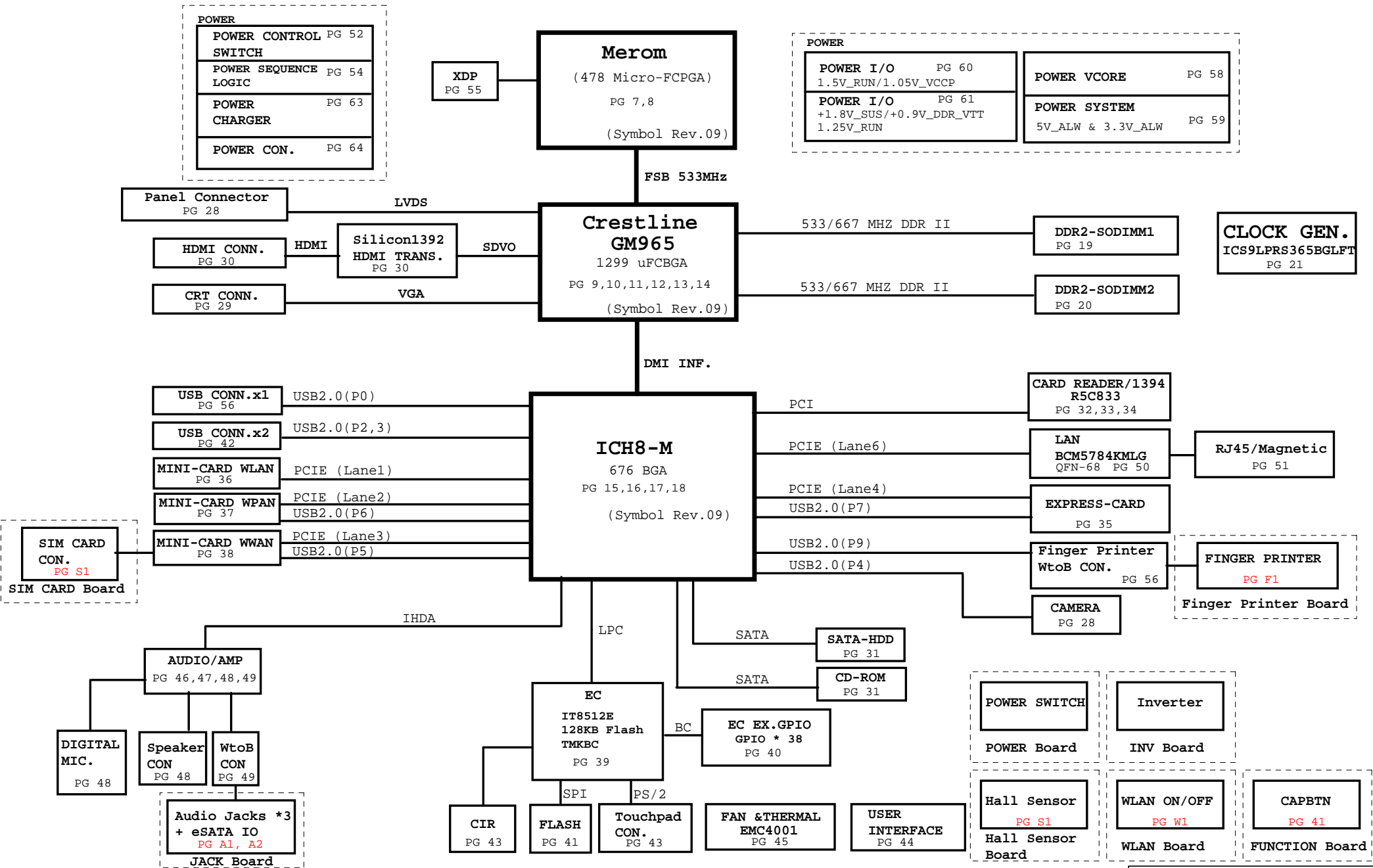
PCB NO : *08217-1*

Diaz Intergrate Intel GM Schematics Document uFCPGA Mobile Merom Intel Crestline-GM + ICH8M

REV : A00

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Cover Page			
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Diaz Block Diagram of Intel GM



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52	POWER CONTROL SWITCH	
53	Power Button Board	
54	Power Sequence Logic	
55	XDP	
56	USB PORT ,eSATA, FINGER	
57	SIM Board	
58-64	Power circuit	

Pg#	Description	DNI LIST
65	SCREW PAD	
A1	AUDIO_JACK	
A2	USB PORT & eSATA	
C1	CAPBTN	
F1	Fingerprint (AES2810)	
L1	LID Board	
S1	SIM Board	
W1	Wireless Switch Board	

Footprint Definition

Resistor	Footprint is 0402 if there is no description
Capacitor	Footprint is 0402 if there is no description
Ferrite Bead	Footprint is 0603 if there is no description

Layout Note

For all of ESD diode, they should be placed as close as possible to connectors and the signals from connectors should be routed to ESD diodes first. There is no branch or via before diodes

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
R5C833	PCI_AD17	PCI_REQ1# PCI_GNT1#	PCI_PIRQC# PCI_PIRQD#

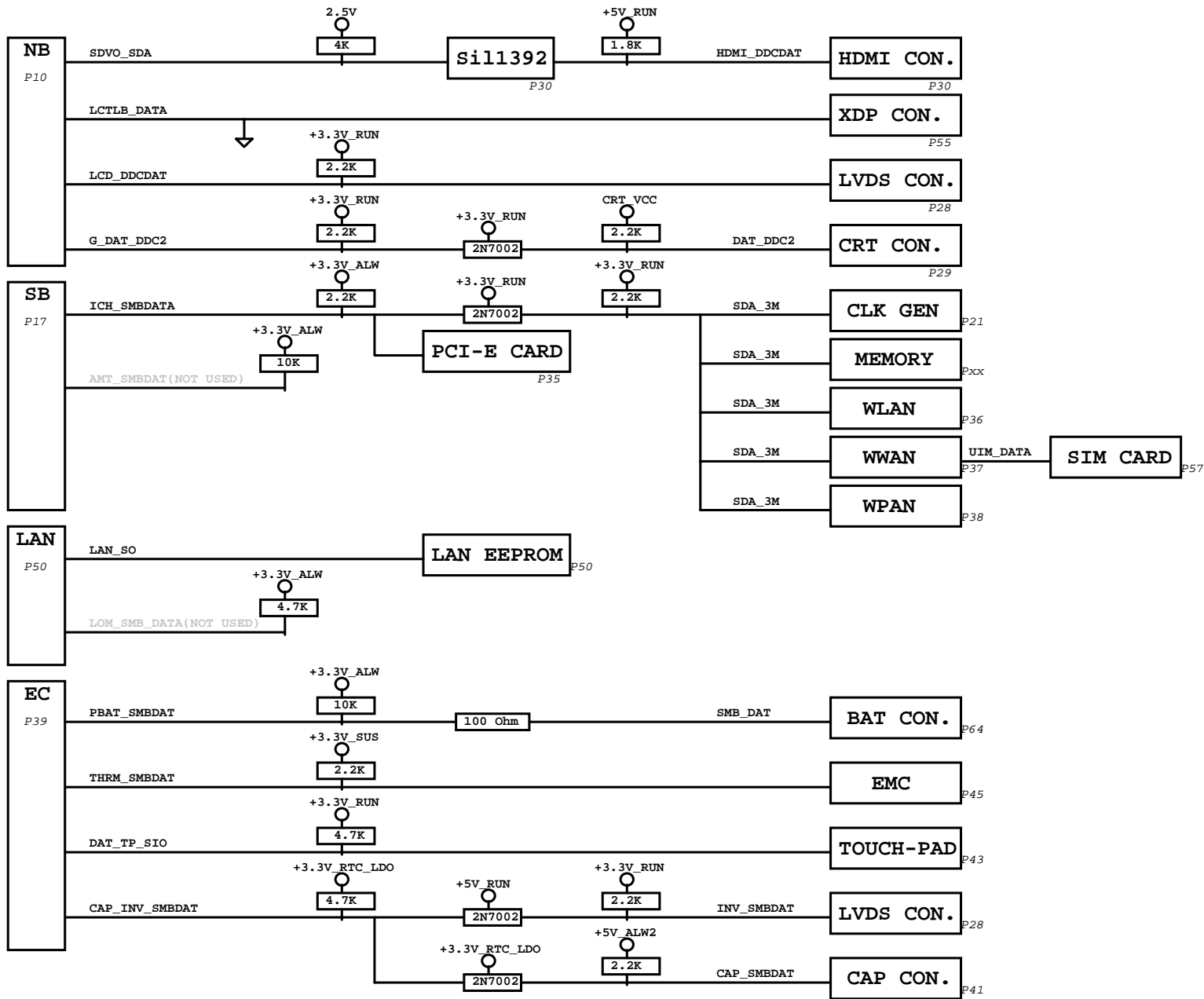
PCI Express TABLE

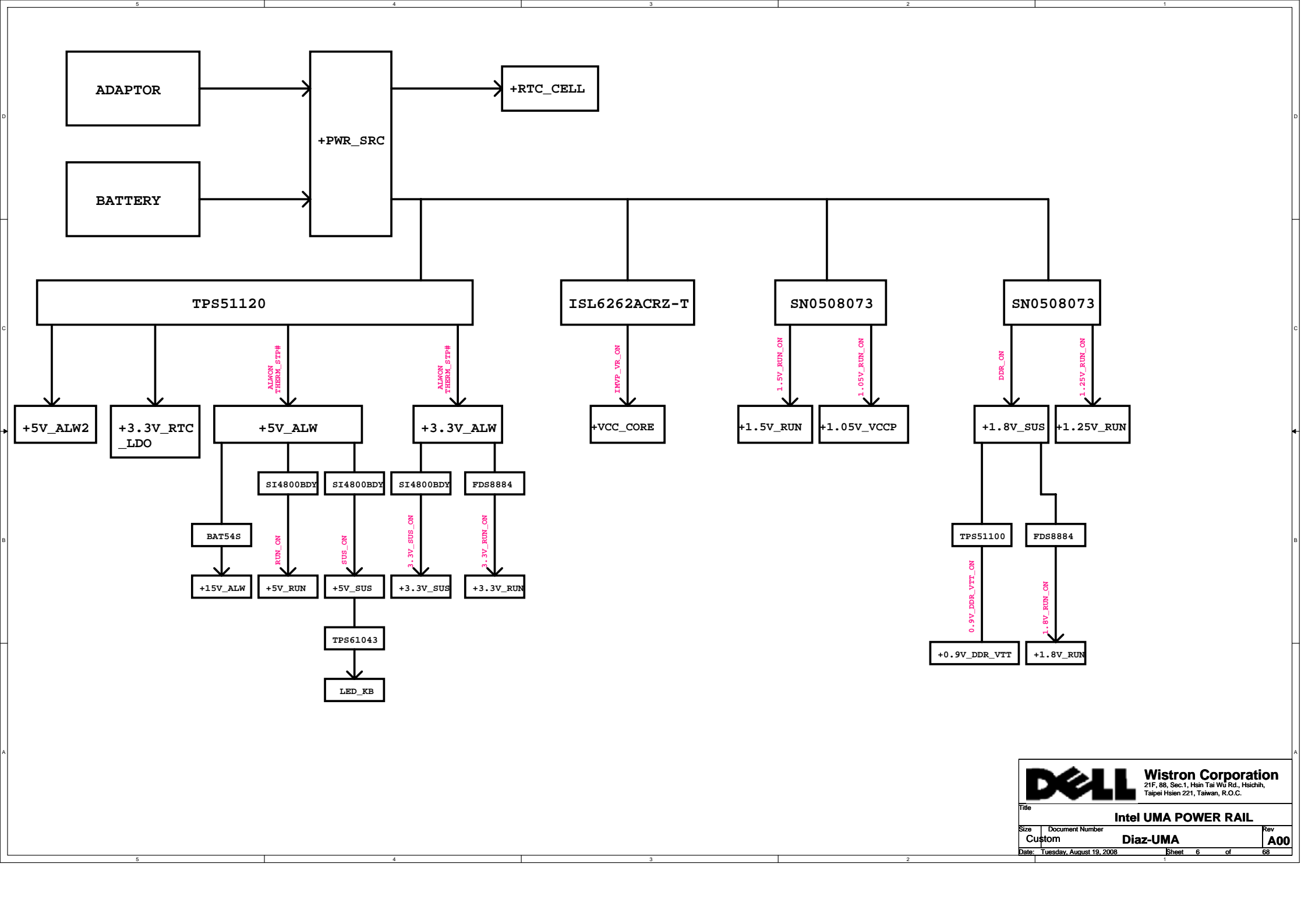
Lane 1	WLAN / Mini Card
Lane 2	WPAN / Mini Card
Lane 3	WWAN / Mini Card
Lane 4	ExpressCard
Lane 5	
Lane 6	LAN BCM5784KMLG

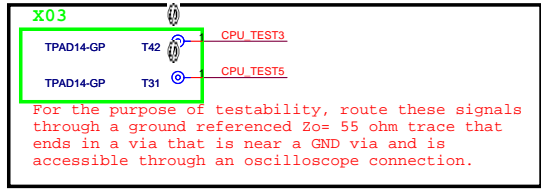
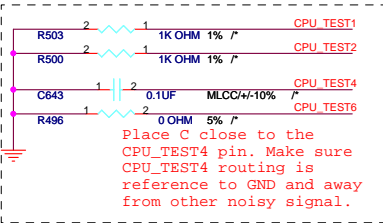
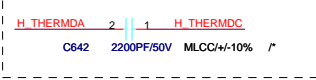
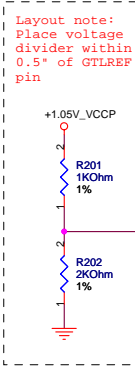
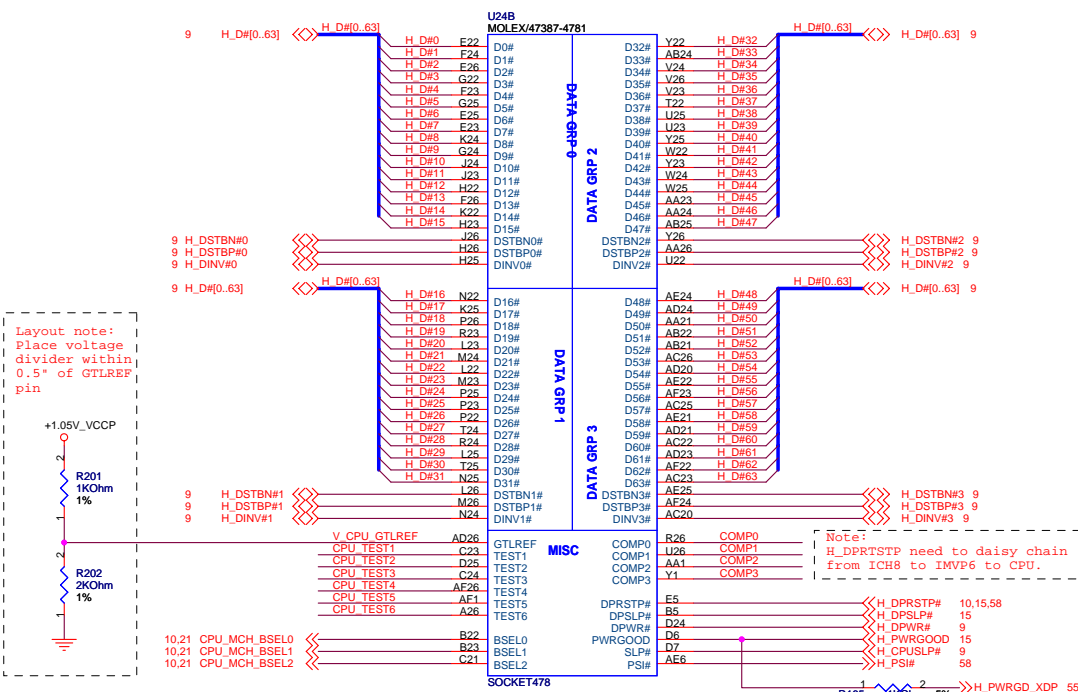
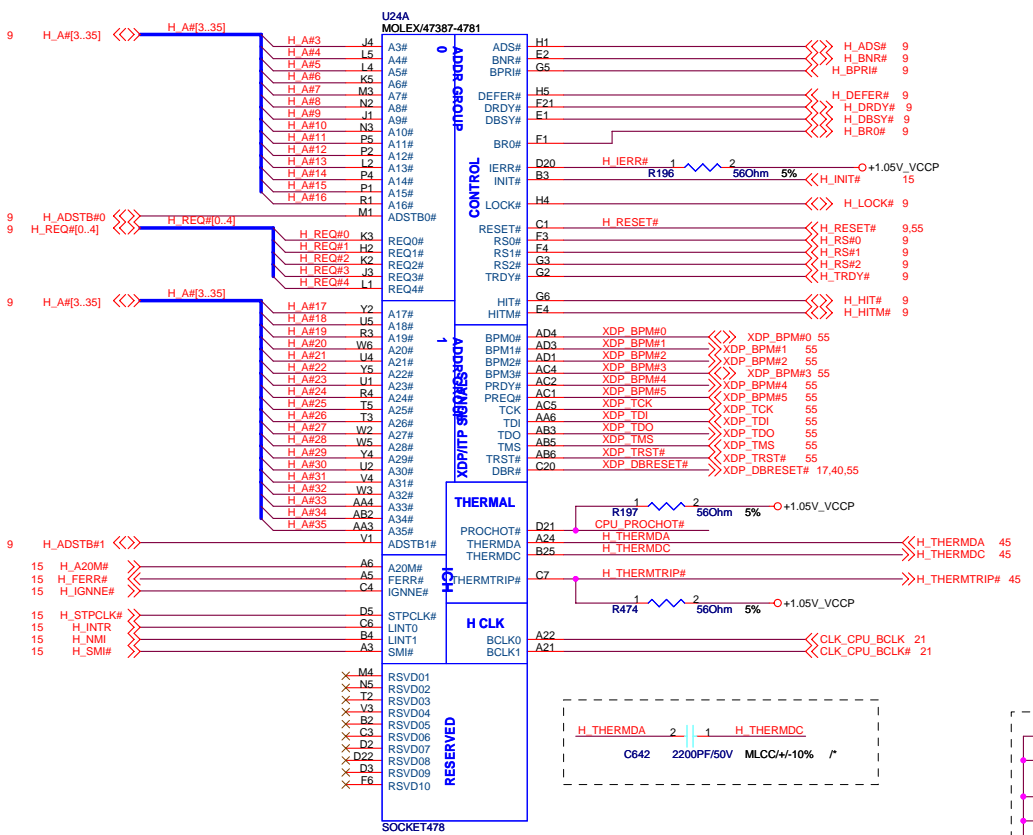
USB TABLE

ICH8-0 (EHCI#1)	User1 (Single port , in USB BD)
ICH8-1 (EHCI#1)	
ICH8-2 (EHCI#1)	User2 (Dual port-bottom , in I/O BD)
ICH8-3 (EHCI#1)	User3 (Dual port-top , in I/O BD)
ICH8-4 (EHCI#1)	Camera
ICH8-5 (EHCI#1)	WWAN / Mini Card
ICH8-6 (EHCI#2)	WPAN / Mini Card
ICH8-7 (EHCI#2)	ExpressCard
ICH8-8 (EHCI#2)	Note : No USB for WLAN
ICH8-9 (EHCI#2)	Finger Printer

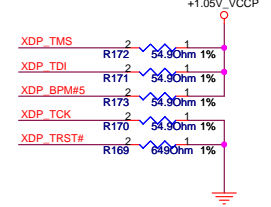
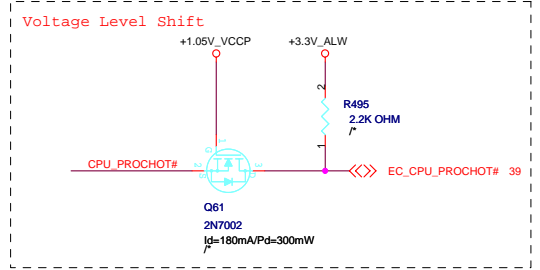
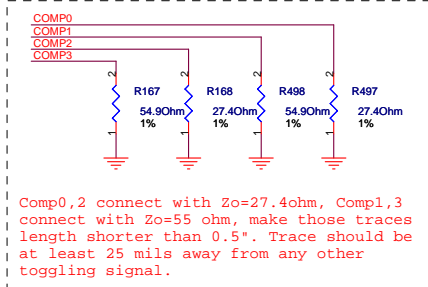








FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

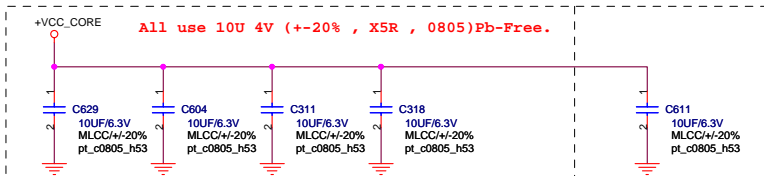


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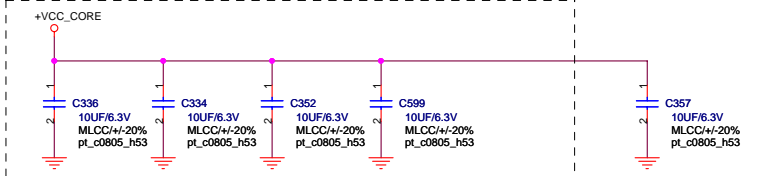
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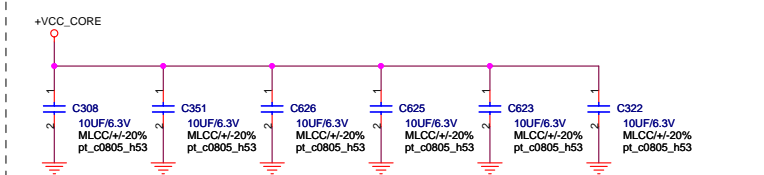
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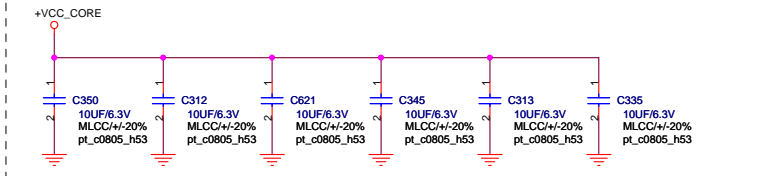
8 inside cavity, north side, secondary layer.



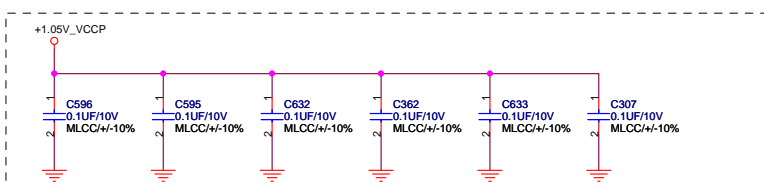
8 inside cavity, south side, secondary layer.



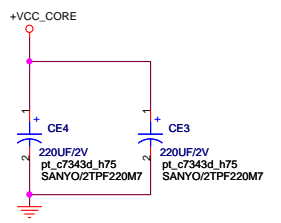
6 inside cavity, north side, primary layer.



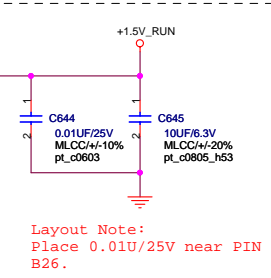
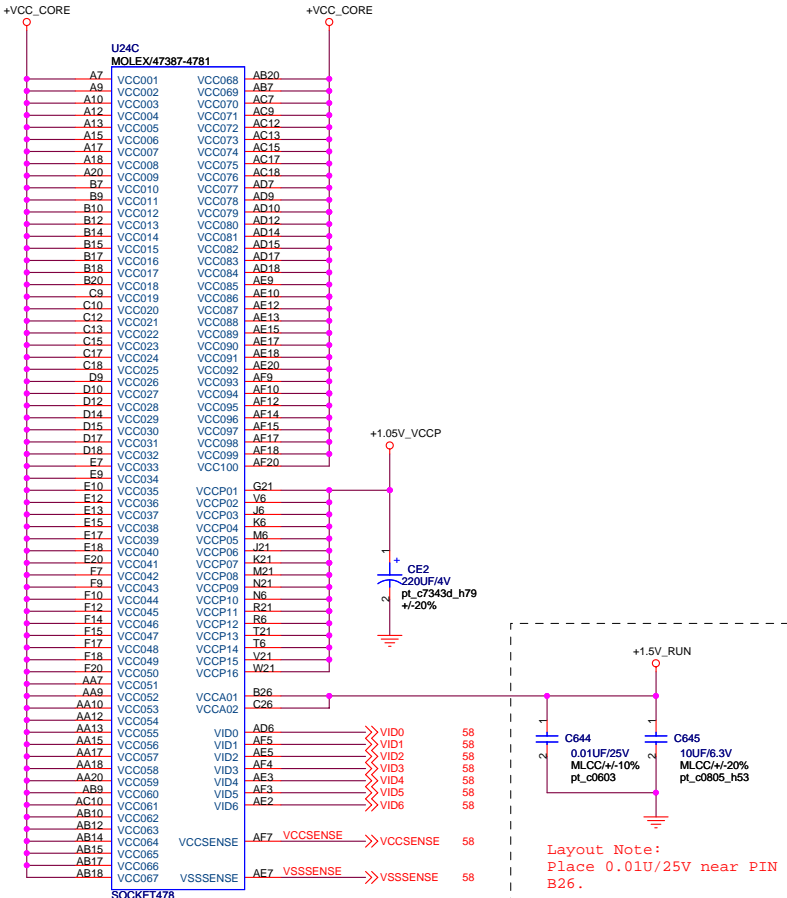
6 inside cavity, south side, primary layer.



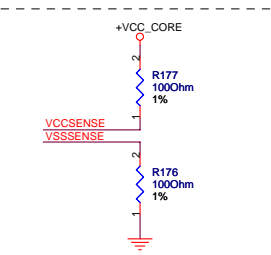
Layout out:
Place these inside socket cavity on North side secondary.



100U/25V *4 Remove to POWER CIRCUIT .

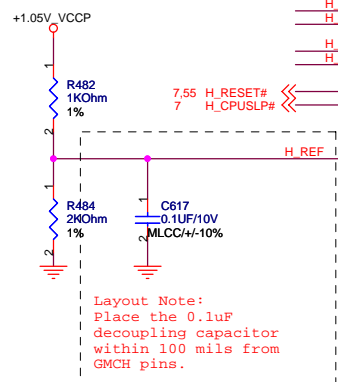
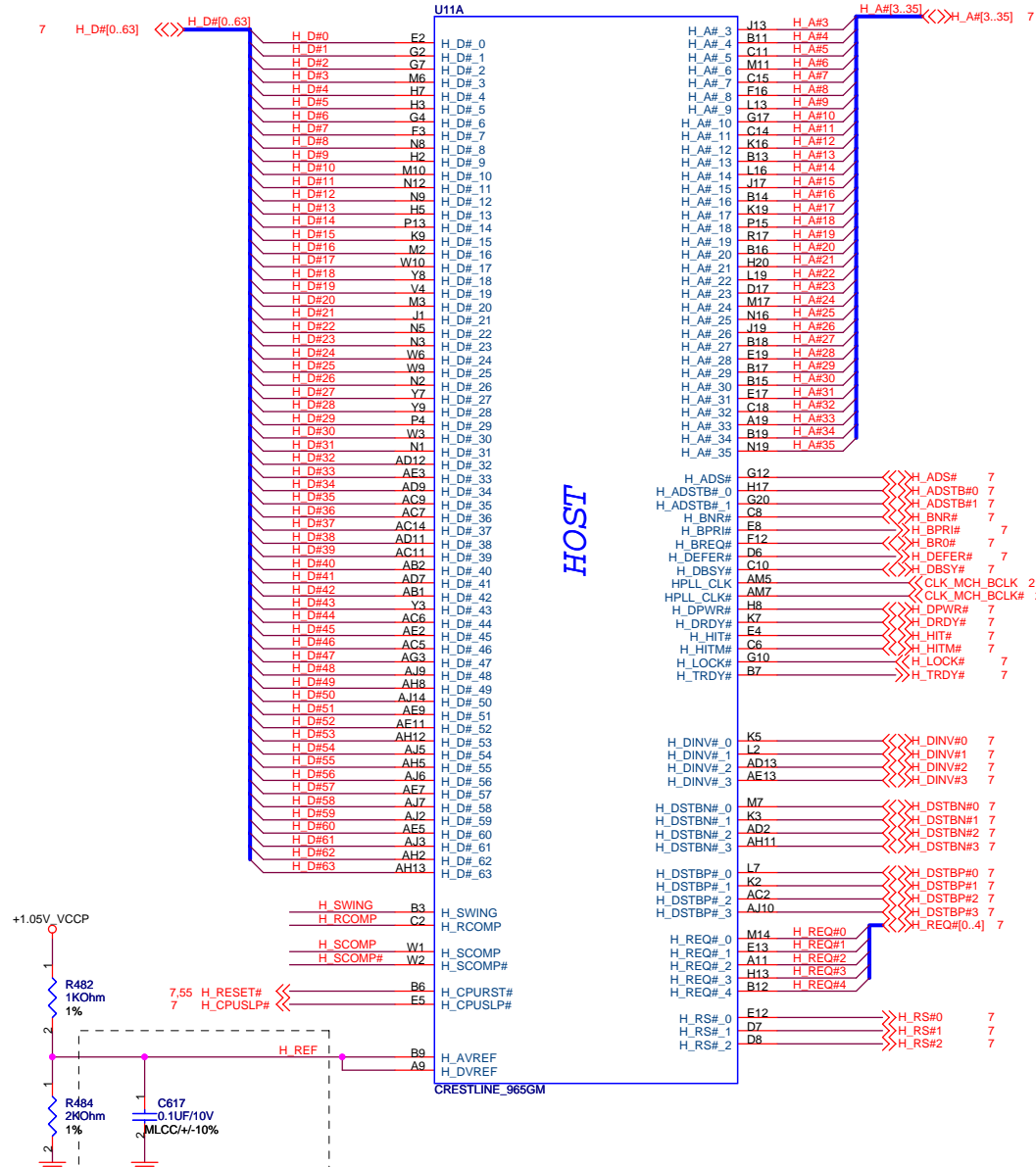
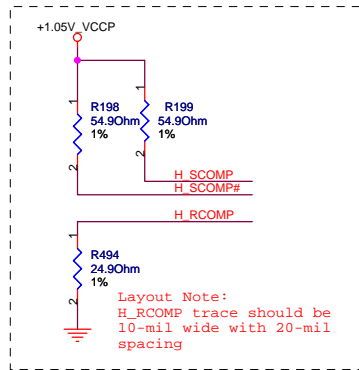
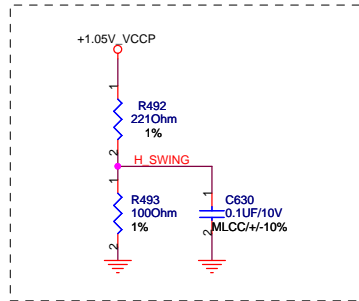


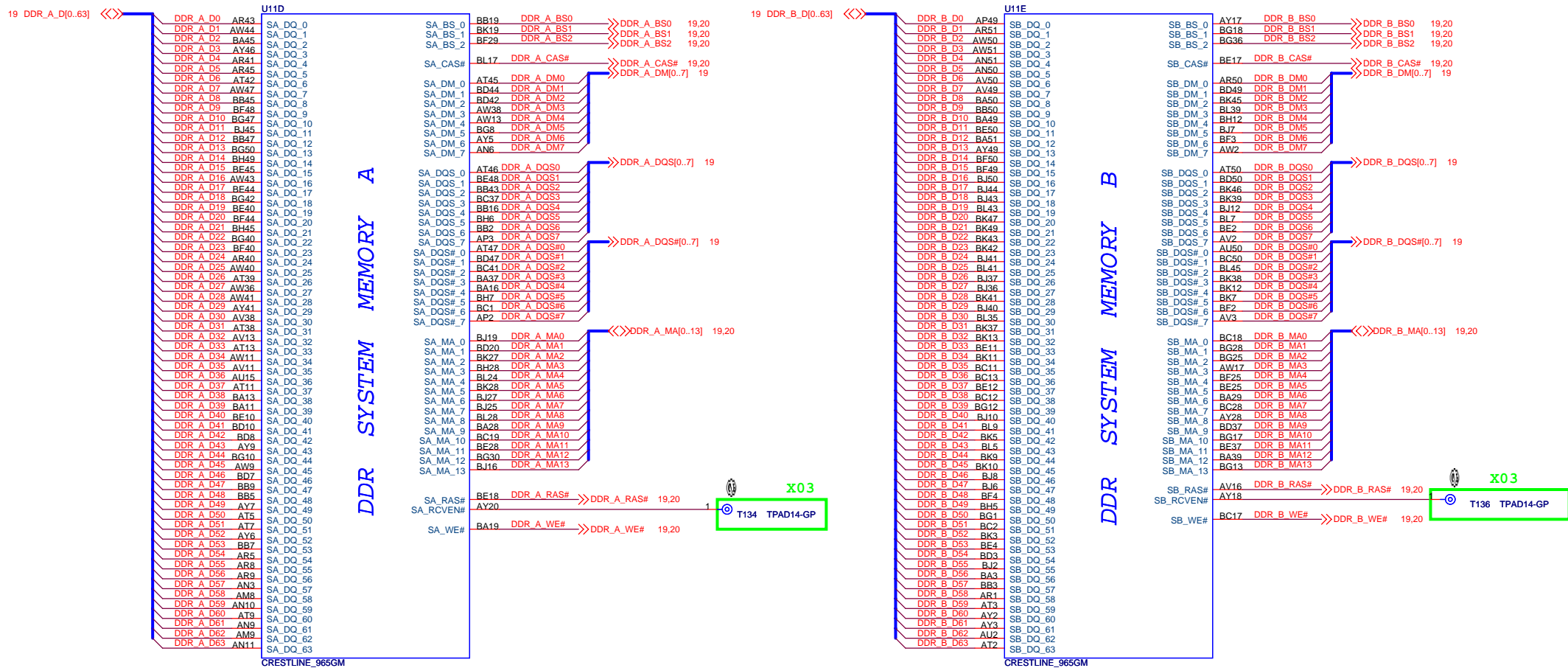
Layout Note:
Place 0.01uF/25V near PIN B26.



Route VCCSENSE and VSSSENSE traces at 27.4ohms with 50 mils spacing and length matched to within 25 mil. Place PU and PD within 1 inch of CPU.

U24D MOLEX/47387-4781	
A4	VSS001
A8	VSS002
A11	VSS003
A14	VSS004
A18	VSS005
A19	VSS006
A23	VSS007
AE2	VSS008
B6	VSS009
B8	VSS010
B11	VSS011
B13	VSS012
B16	VSS013
B19	VSS014
B21	VSS015
B24	VSS016
CA	VSS017
CA	VSS018
C11	VSS019
C14	VSS020
C16	VSS021
C19	VSS022
C2	VSS023
C22	VSS024
C25	VSS025
D4	VSS026
D4	VSS027
D8	VSS028
D11	VSS029
D16	VSS030
D19	VSS031
D23	VSS032
D26	VSS033
E3	VSS034
E6	VSS035
E8	VSS036
E11	VSS037
E14	VSS038
E19	VSS039
E21	VSS040
E24	VSS041
F5	VSS042
F8	VSS043
F11	VSS044
F16	VSS045
F19	VSS046
F2	VSS047
F22	VSS048
F25	VSS049
G4	VSS050
G1	VSS051
G23	VSS052
G26	VSS053
H3	VSS054
H6	VSS055
H21	VSS056
H24	VSS057
J2	VSS058
J5	VSS059
J2	VSS060
J2	VSS061
J2	VSS062
J2	VSS063
K1	VSS064
K4	VSS065
K23	VSS066
K26	VSS067
L3	VSS068
L6	VSS069
L21	VSS070
L24	VSS071
M2	VSS072
M5	VSS073
M2	VSS074
M25	VSS075
N1	VSS076
N4	VSS077
N23	VSS078
N26	VSS079
F3	VSS080
	VSS081
	VSS082
	VSS083
	VSS084
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	VSS163



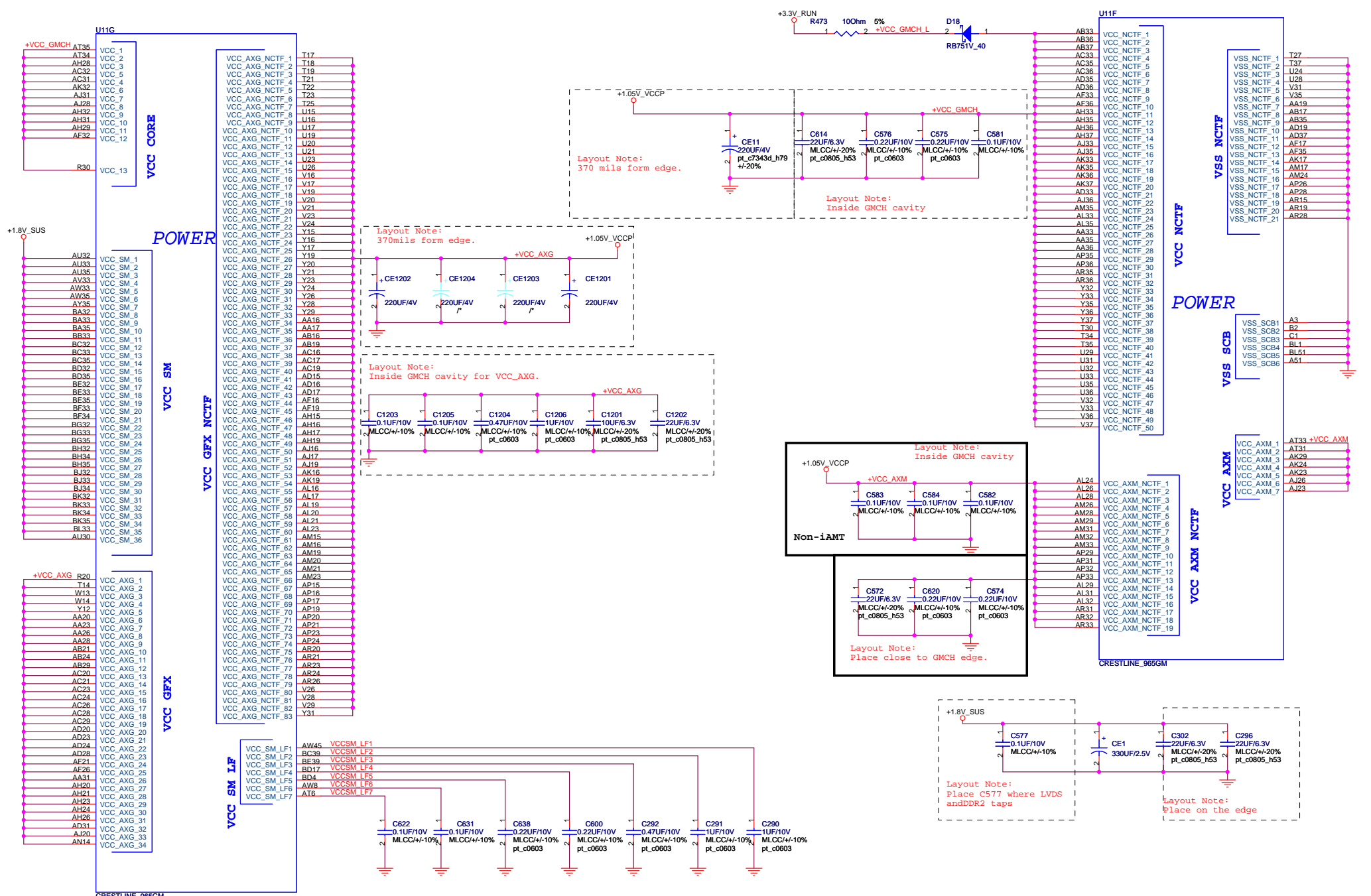


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Title: **Crestline(DDR2)**

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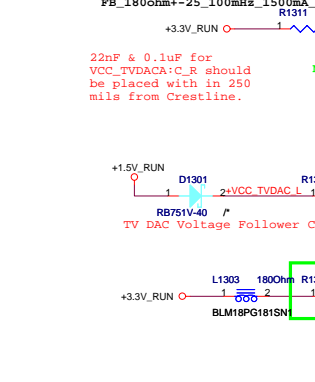
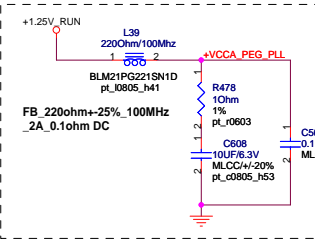
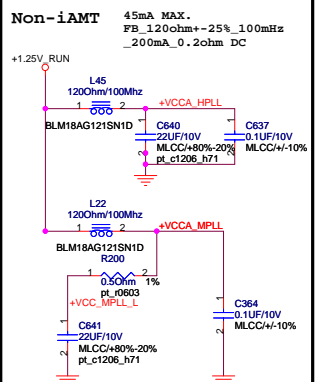
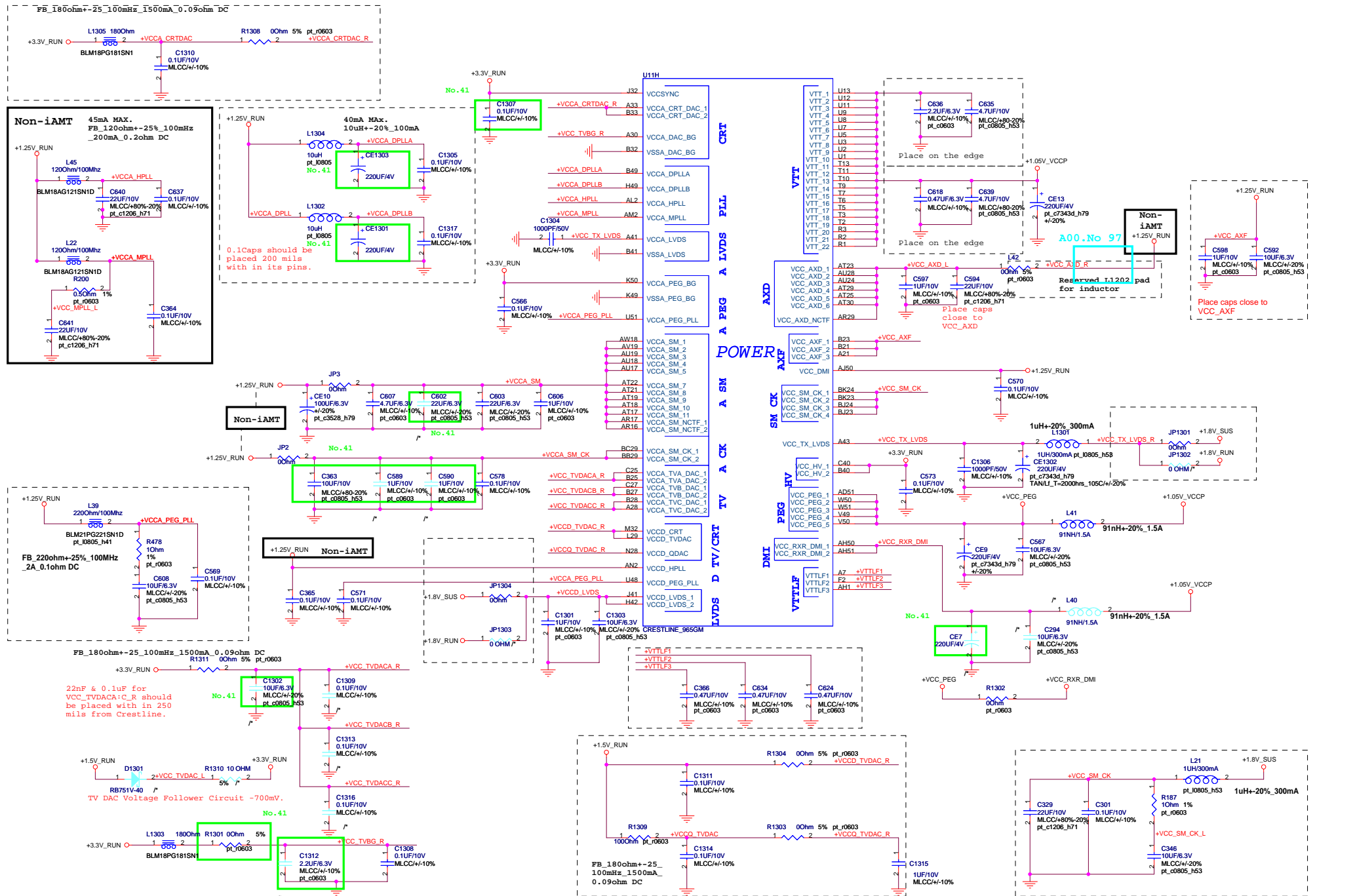


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File: **Crestline(VCC,NCTF)**

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0.1Caps should be placed 200 mils with in its pins.

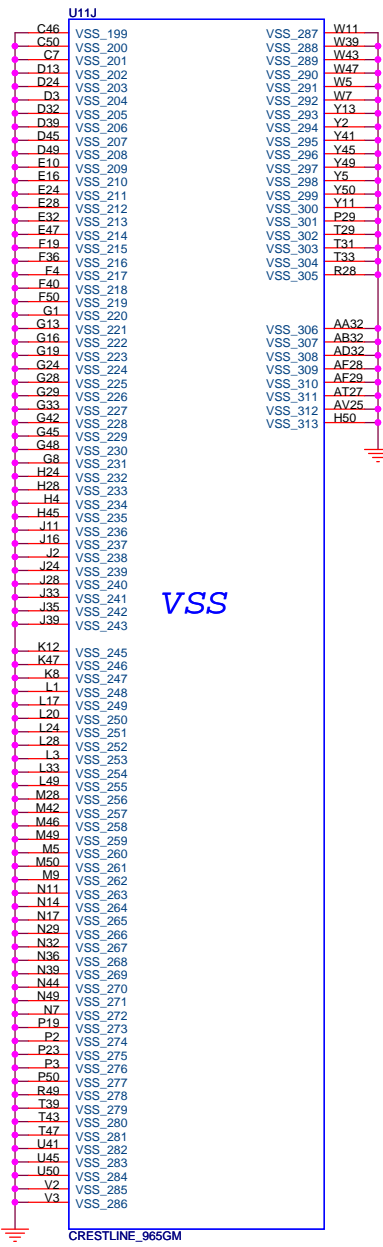
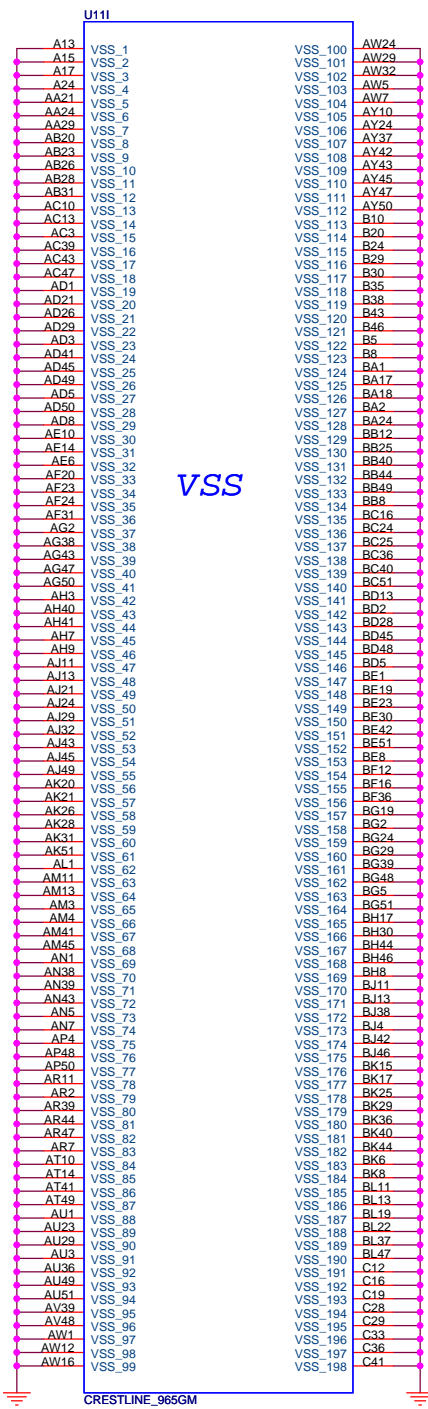
22nF & 0.1uF for VCC_TVDACA:C,R should be placed with in 250 mils from Crestline.

TV DAC Voltage Follower Circuit -700mV.

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Title: **Crestline(Power)**

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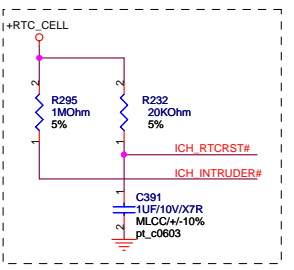
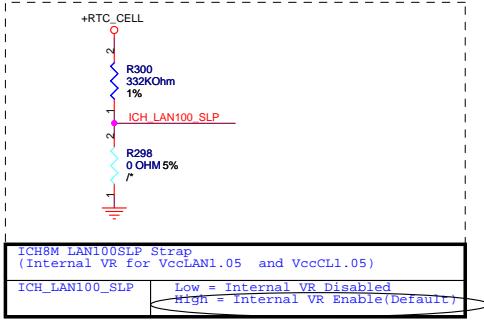
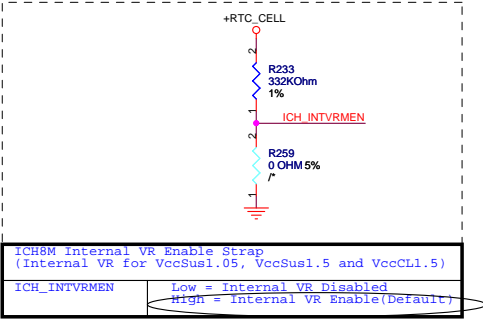
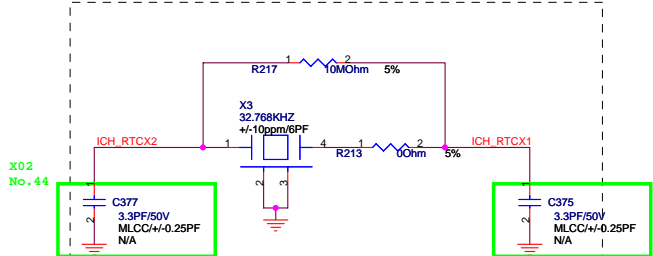


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Title: **Crestline(VSS)**

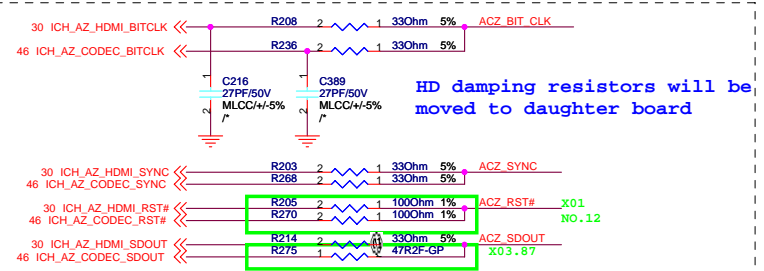
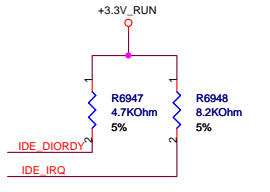
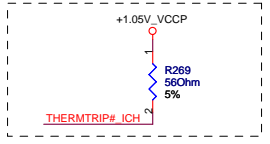
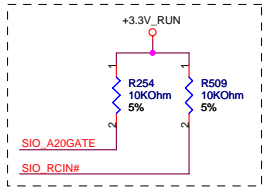
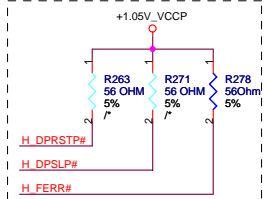
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ICH8M Internal VR Enable Strap
(Internal VR for VccSus1.05, VccSus1.5 and VccCl1.5)
ICH_INTVRMEN Low = Internal VR Disabled
High = Internal VR Enable(Default)

ICH8M LAN100SLP Strap
(Internal VR for VccLAN1.05 and VccCl1.05)
ICH_LAN100_SLP Low = Internal VR Disabled
High = Internal VR Enable(Default)



Place all series terms close to ICH8 except for SDIN input lines, which should be close to source. Placement of R235, R264, R265, R258 should equal distance to the T split trace point as R236, R268, R270, R275 respective. Basically, keep the same distance from T for all series termination resistors.

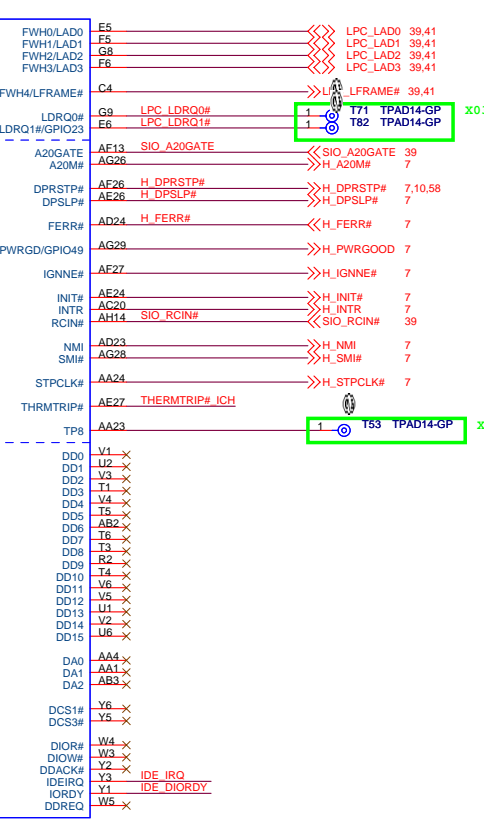
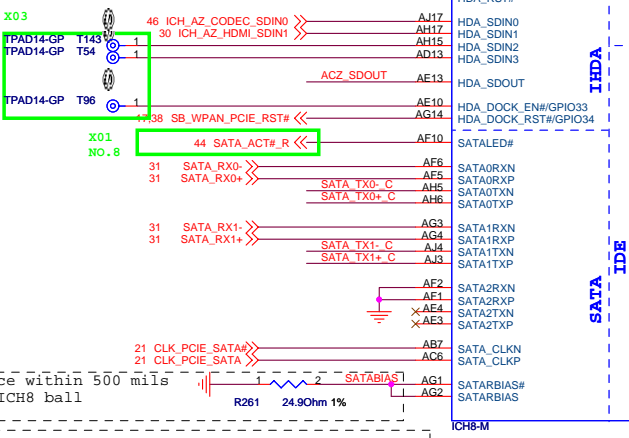
31	SATA_TX0<	C648	MLCC/+10%	2	1	3900PF/50V	SATA_TX0< C
31	SATA_TX0+	C650	MLCC/+10%	2	1	3900PF/50V	SATA_TX0+ C
31	SATA_TX1<	C652	MLCC/+10%	2	1	3900PF/50V	SATA_TX1< C
31	SATA_TX1+	C653	MLCC/+10%	2	1	3900PF/50V	SATA_TX1+ C

Distance between the ICH-8 M and cap on the "P" signal should be identical distance between the ICH-8 M and cap on the "N" signal for same pair.

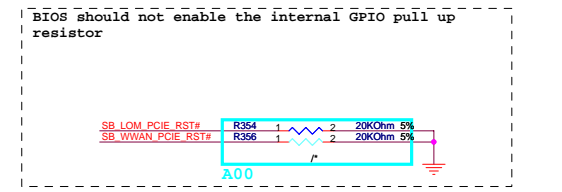
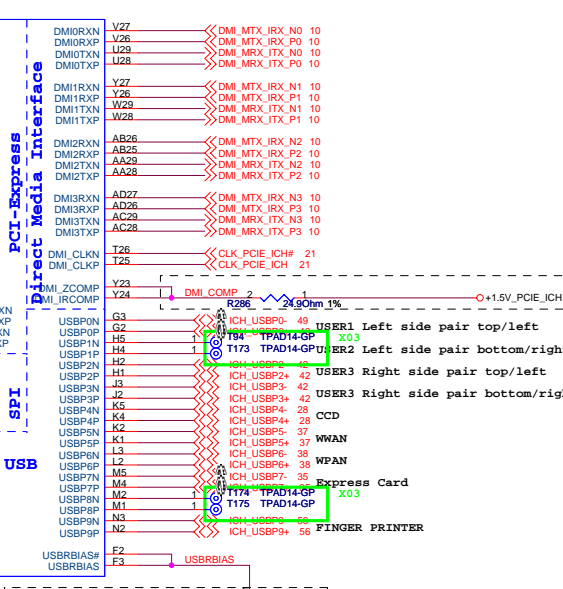
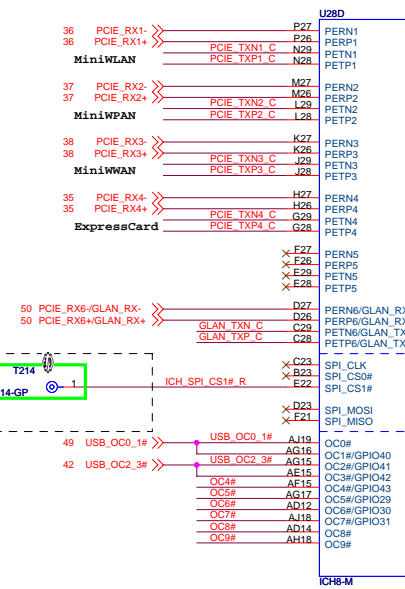
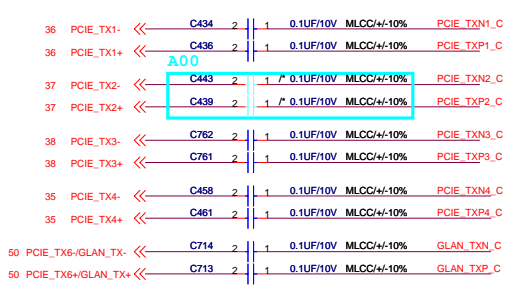


XOR Chain Entrance strap		
ICH_RSVD	ACZ_SDOUT	Description
0	0	RSVD
0	1	Enter XOR chain
1	0	Normal operation (Default)
1	1	Set PCIE port config bit 1

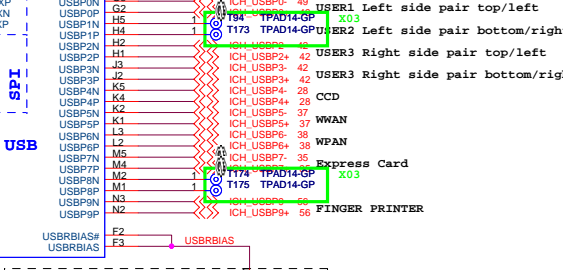
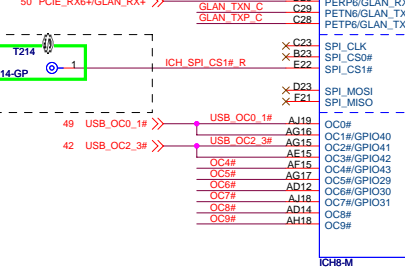
Place within 500 mils of ICH8 ball



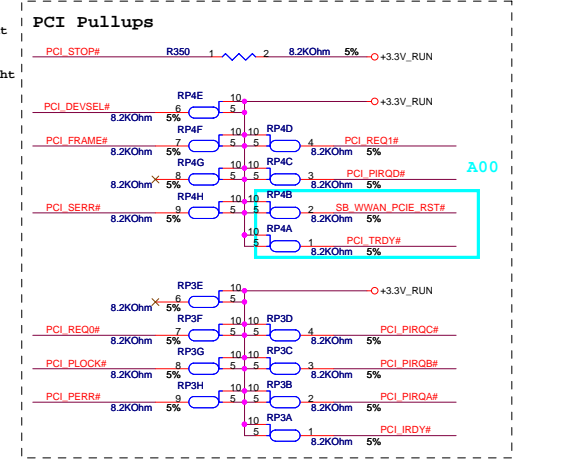
Place TX DC blocking caps close to ICH8.



Layout Note:
Place 15 ohm within 500 mils from ICH.

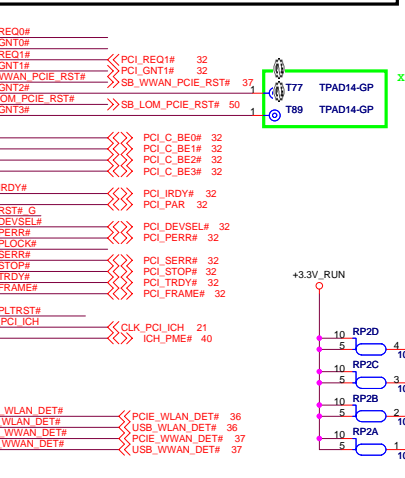
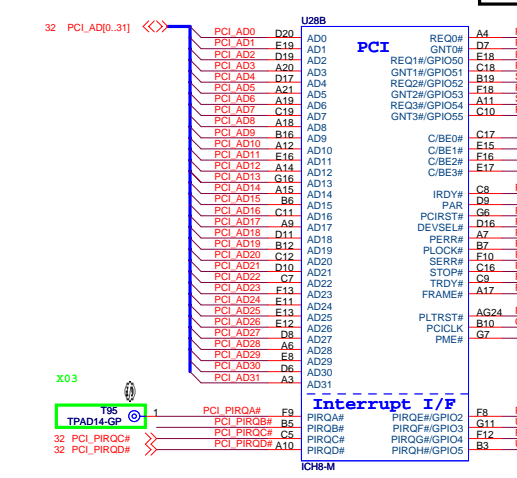
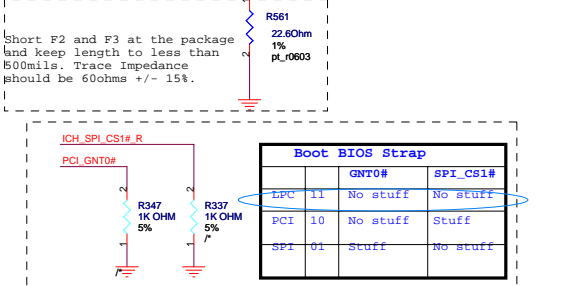
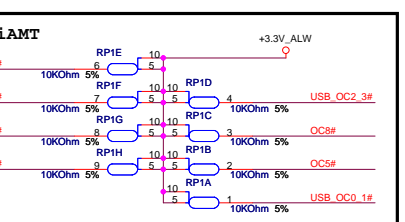


Place within 500 mils of ICH8

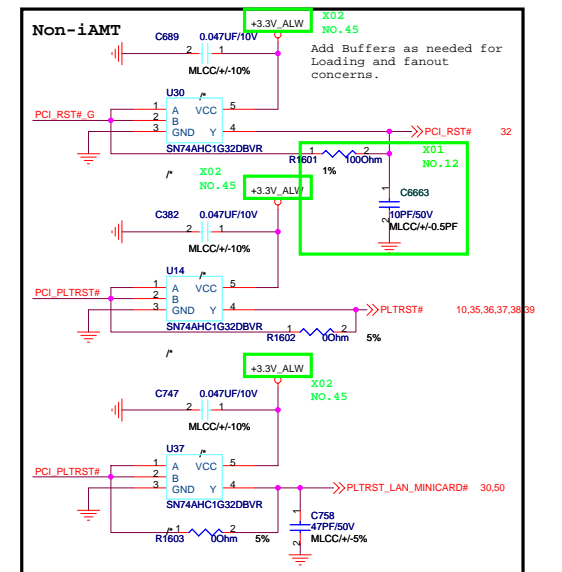
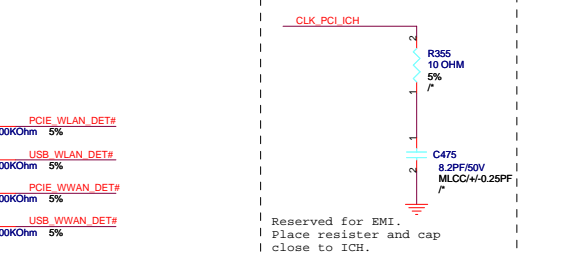


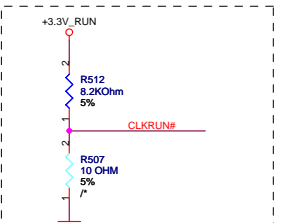
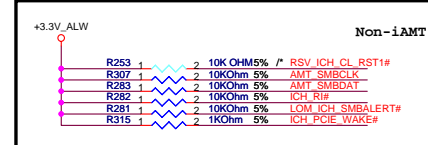
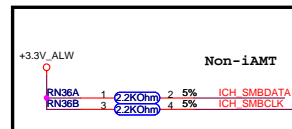
PCI Device

R5C833	IDSEL# AD17	REQ1# GNT1#	PIRQ# PIRQD#
--------	-------------	-------------	--------------

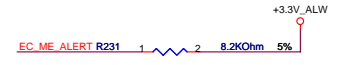
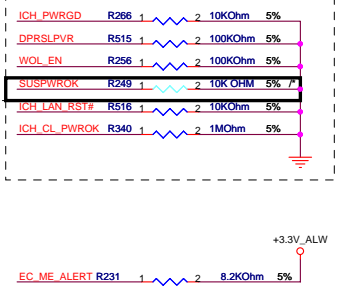
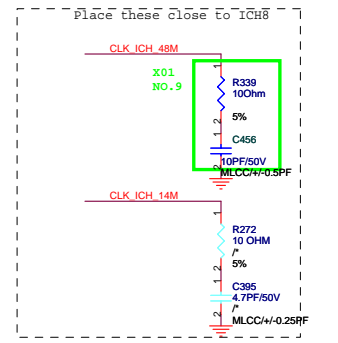
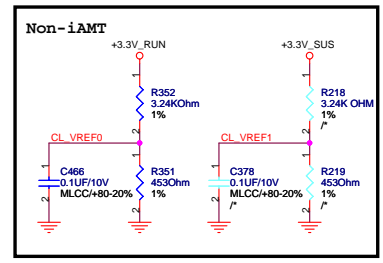
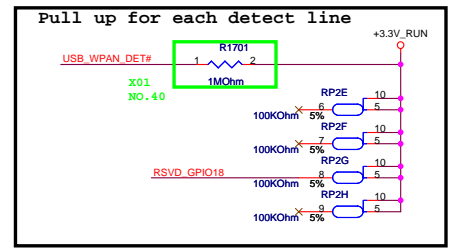
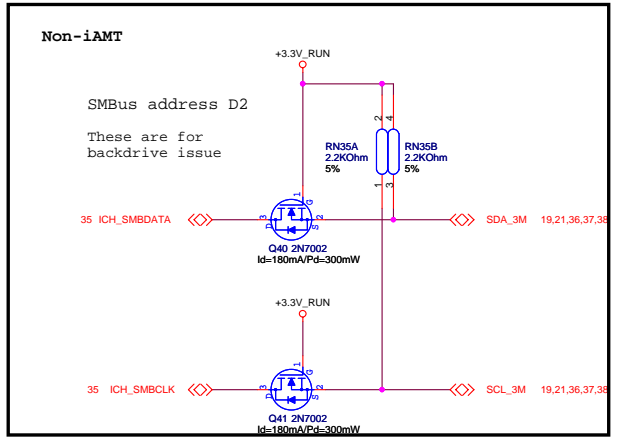
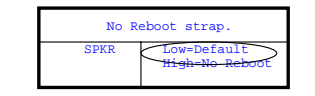
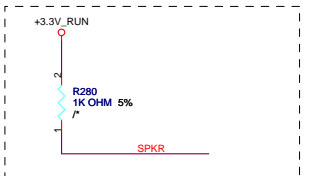
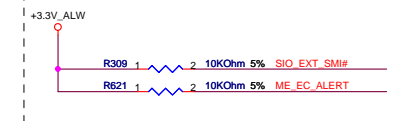
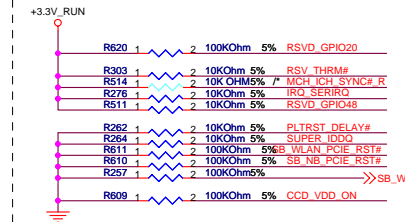
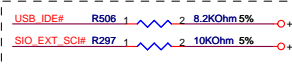


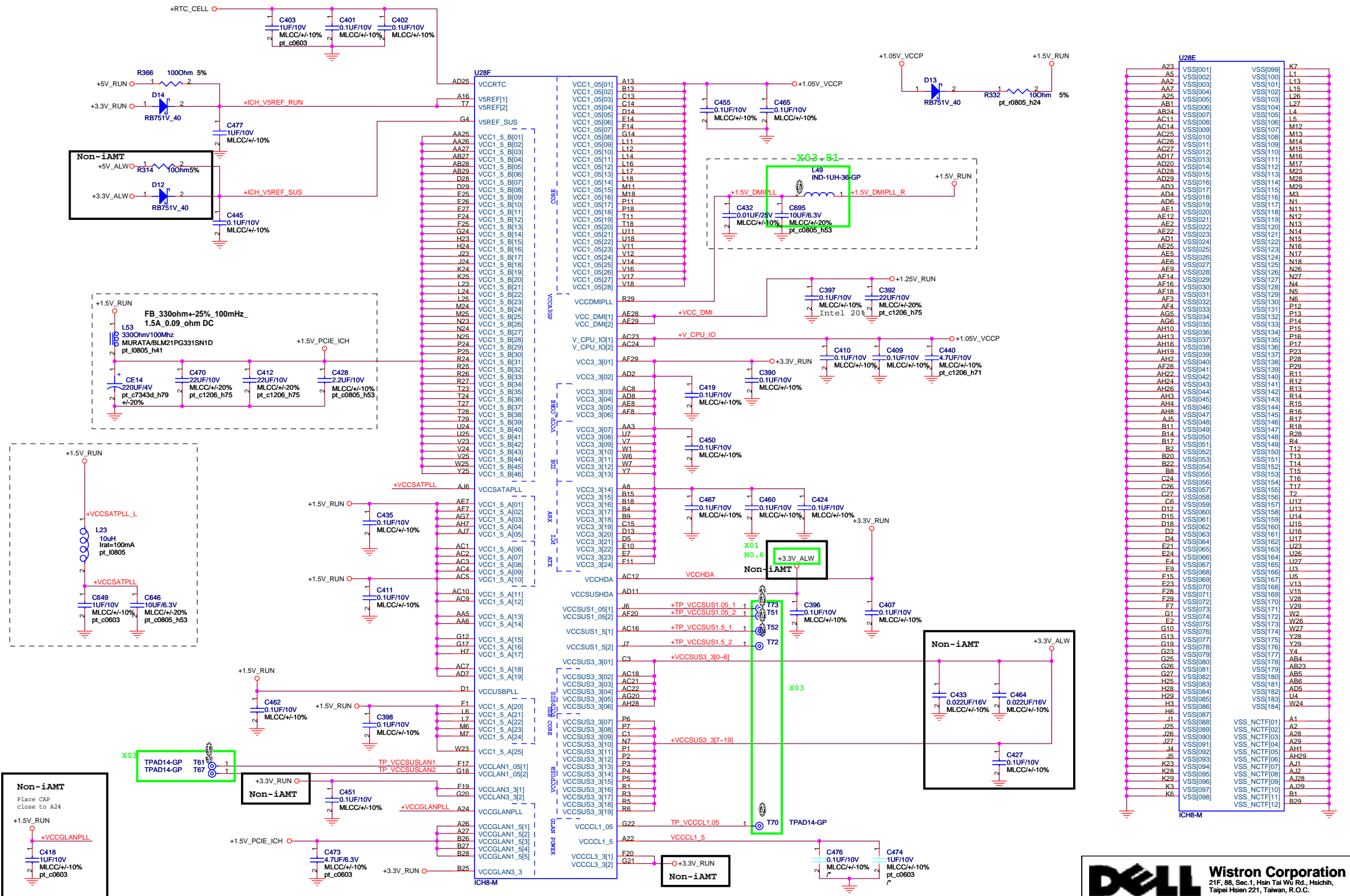
Al6 away override strap.
PCI_GNT3# Low = Al6_swap override enabled.
High = Default.



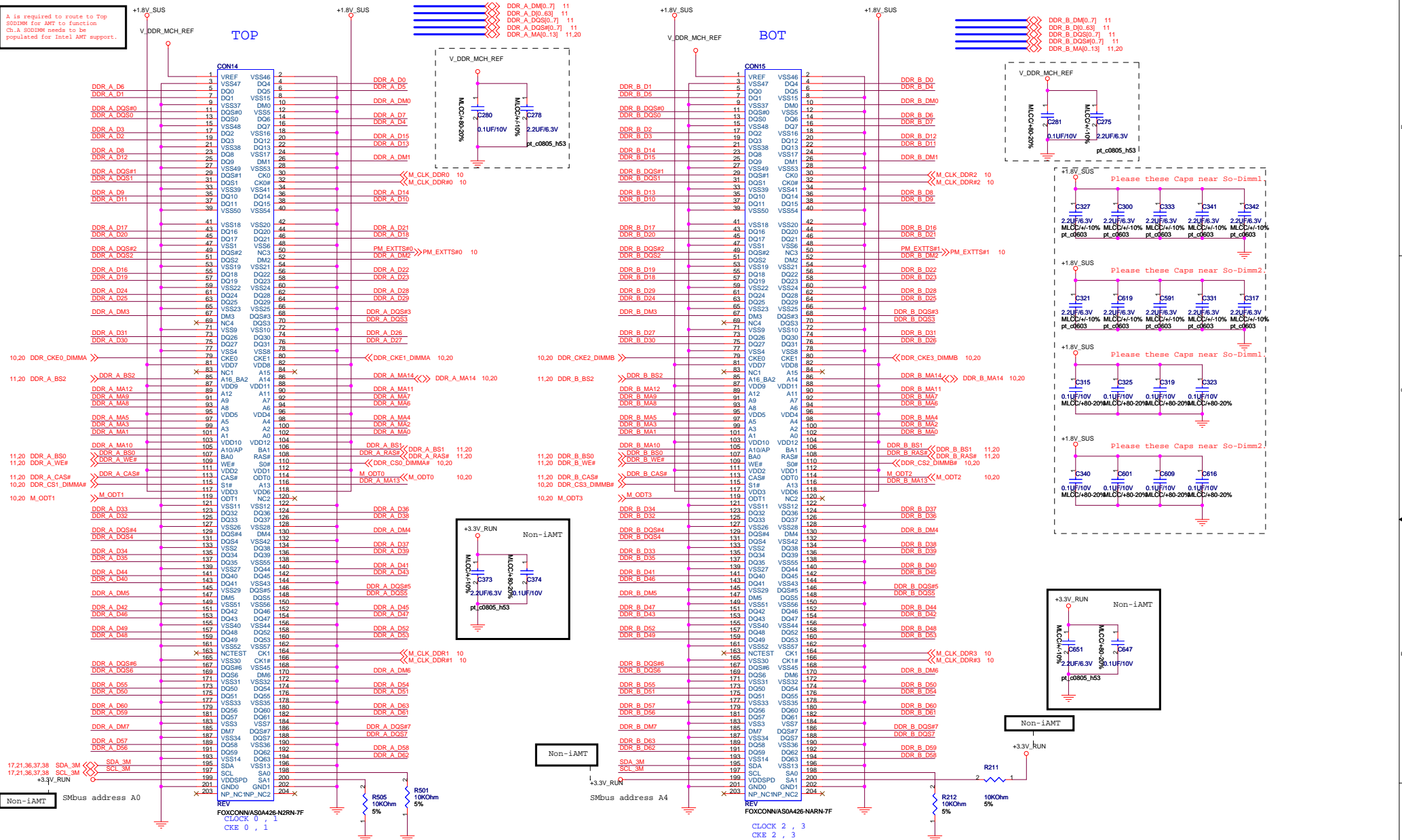


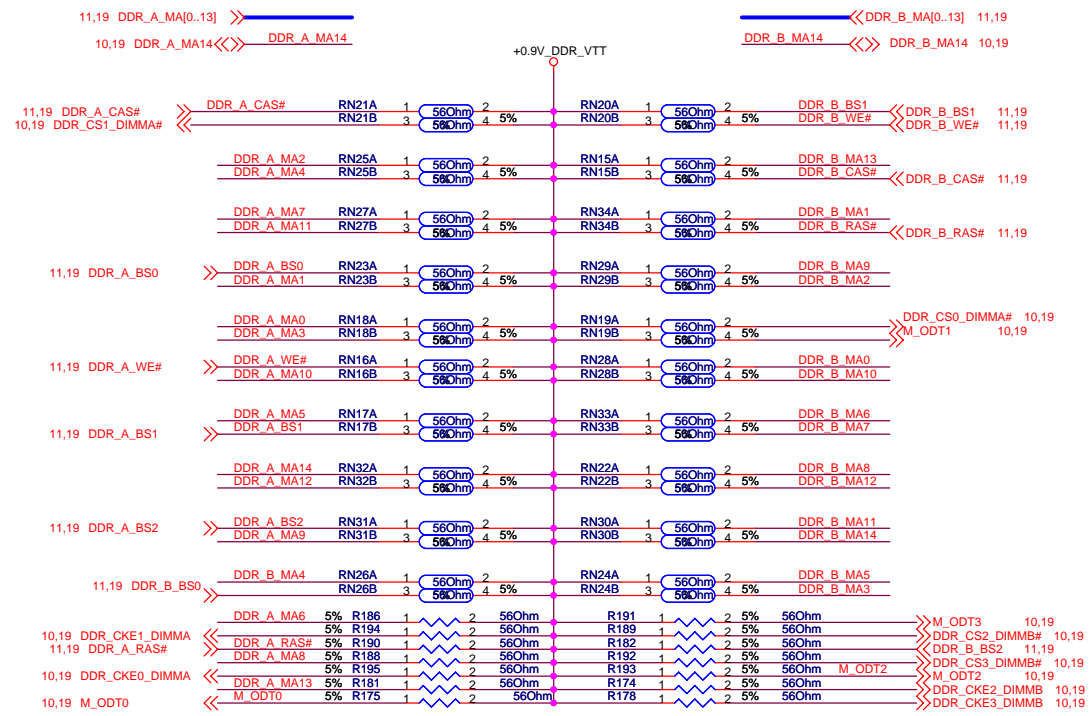
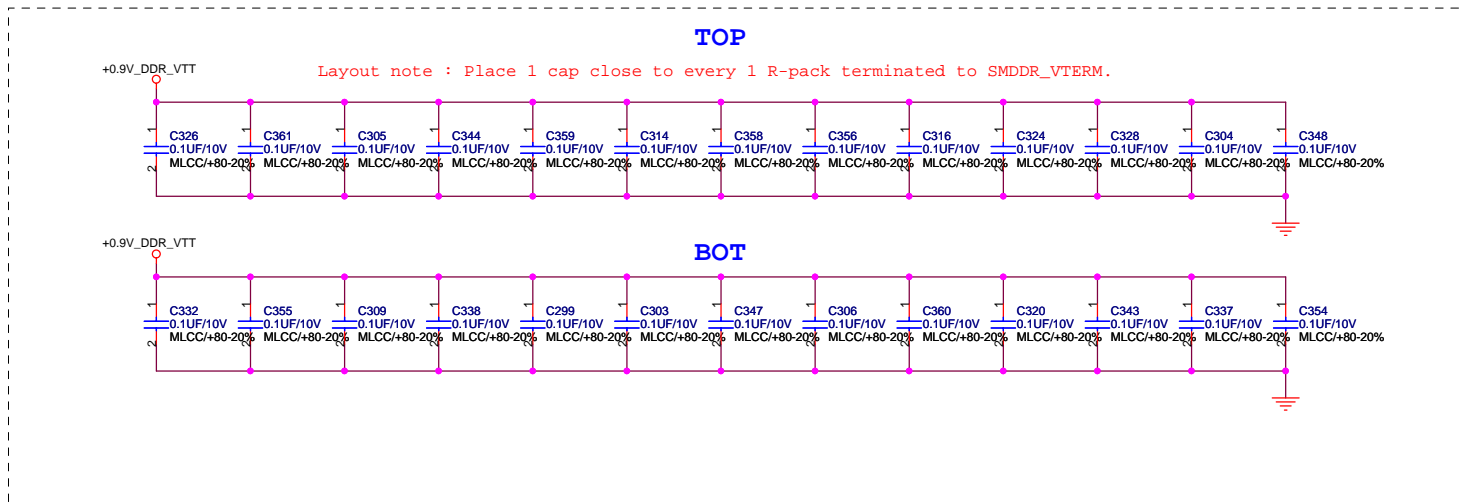
Option to "Disable" clkrun. Pulling it down will keep the clks running.





A is required to route to Top 80DIMM for AMT to Function. Ch.A 80DIMM needs to be populated for Intel AMT support.





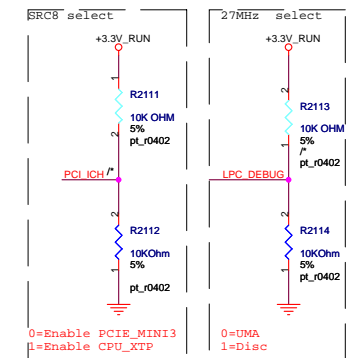
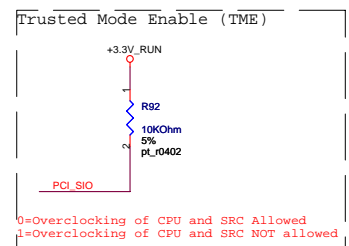
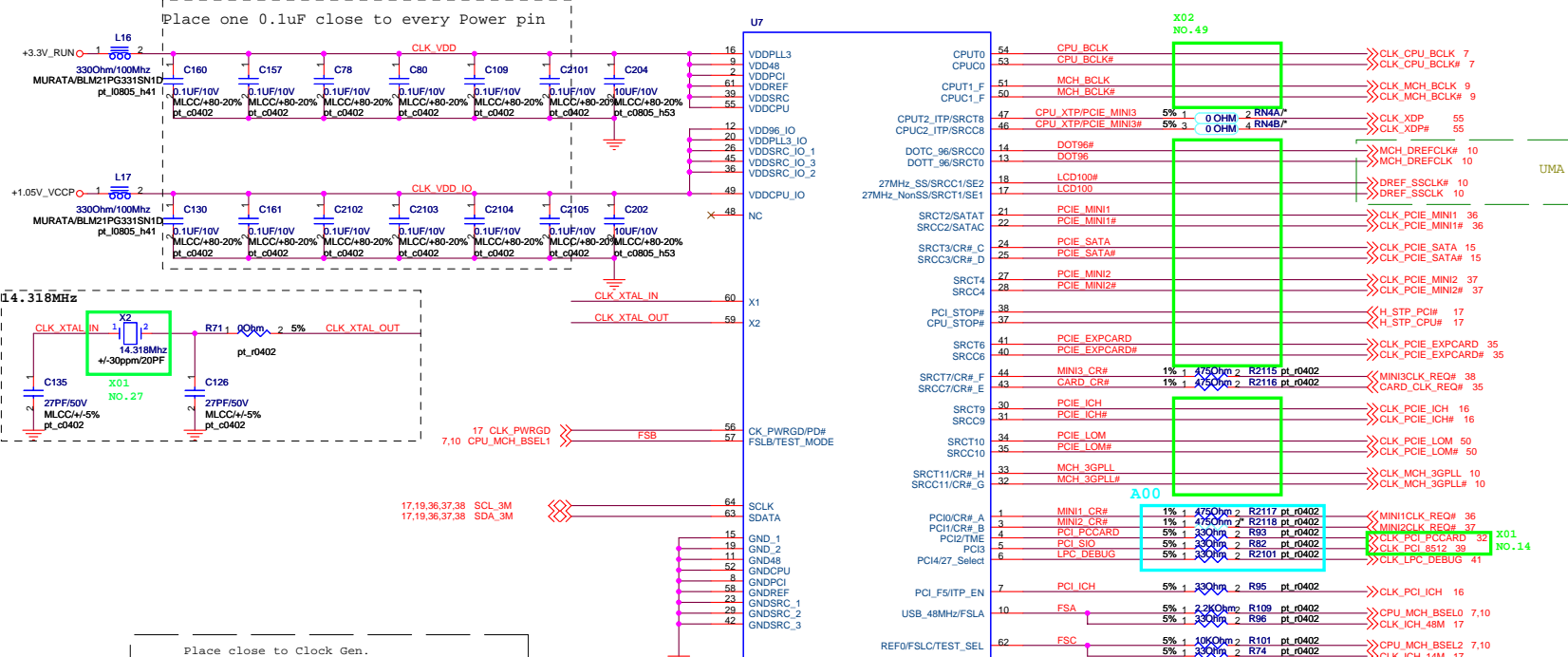
Please these resistor closely DIMMA, all trace length < 750 mil.

Please these resistor closely DIMMB, all trace length < 750 mil.

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DDR2 SO-DIMM (1)

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FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	RSVD	33

LPC_DEBUG=SEL_27M(Disc. VGA) or LCDCLK#

LPC_DEBUG(PIN 6)	Pin13	Pin14	Pin17	Pin18
0 = UMA	DOT96T	DOT96C	LCD100T	LCD100C
1 = Disc.	SRC0T	SRC0C	27M_NSS	27M_SS
GRFX down				


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Title: **CLK GEN. ICS9LPRS365BGLFT**


Size: Custom Document Number: **Diaz-UMA** Rev: **A00**

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Size	Document Number		Rev
A3	Diaz-UMA		A00
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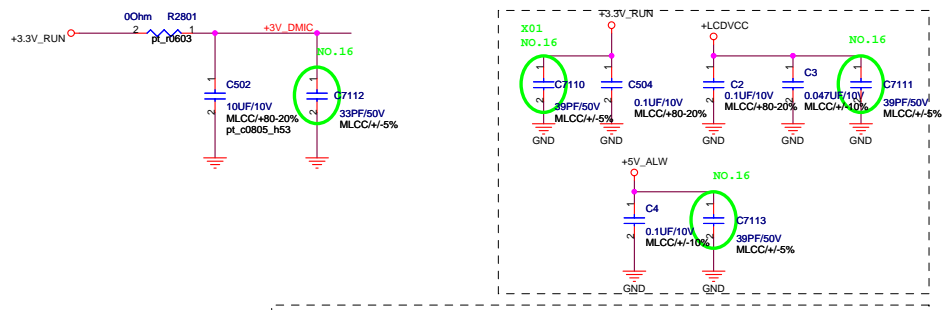
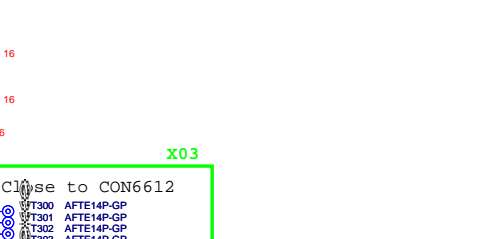
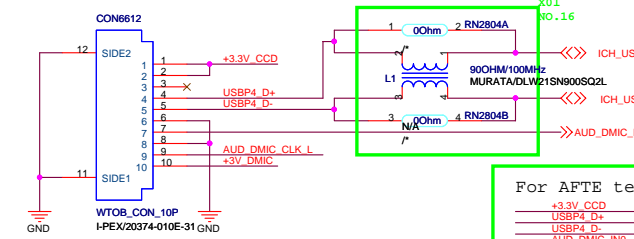
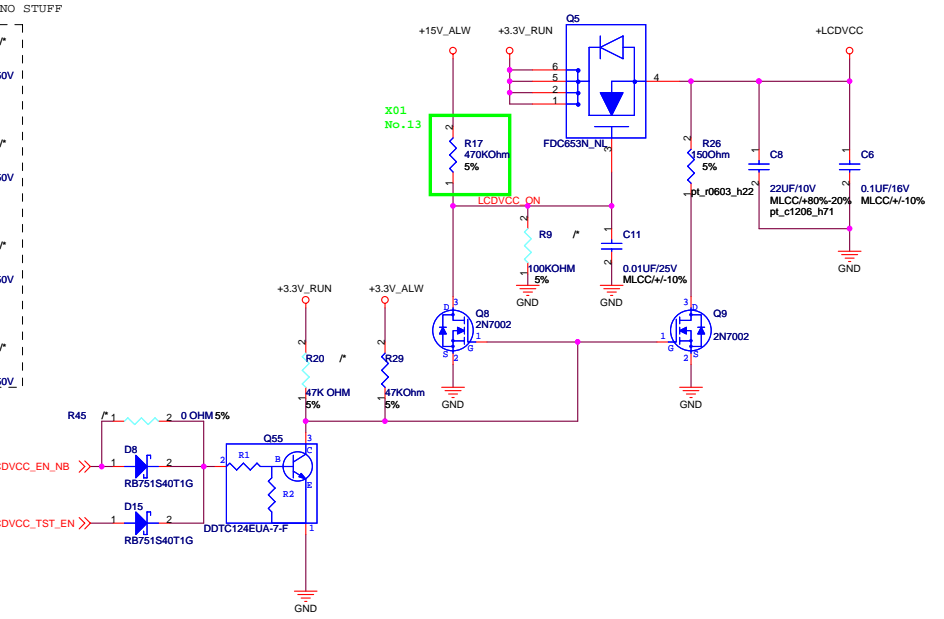
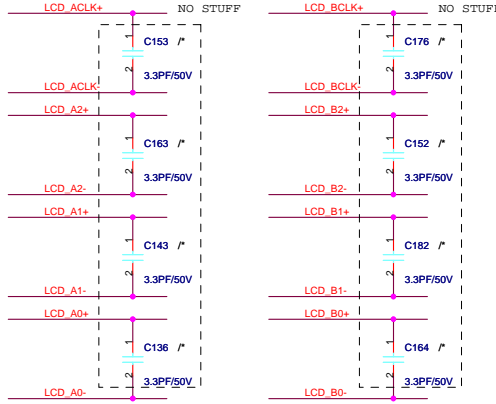
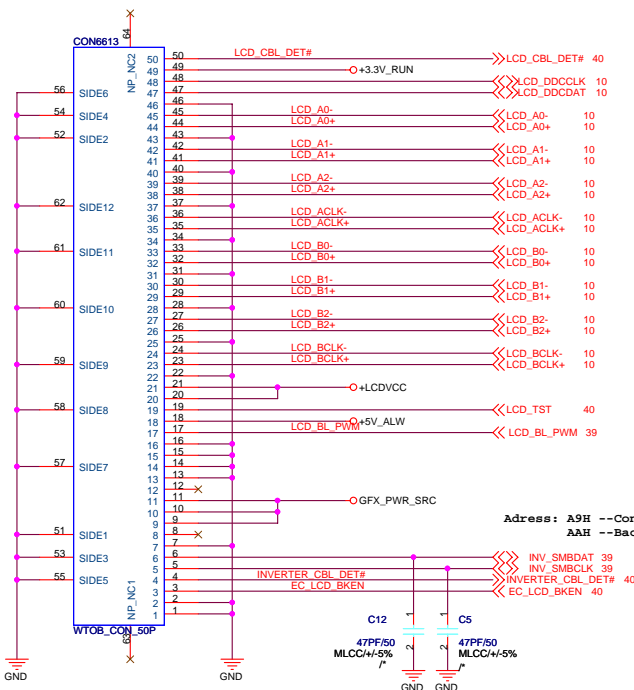
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Title		
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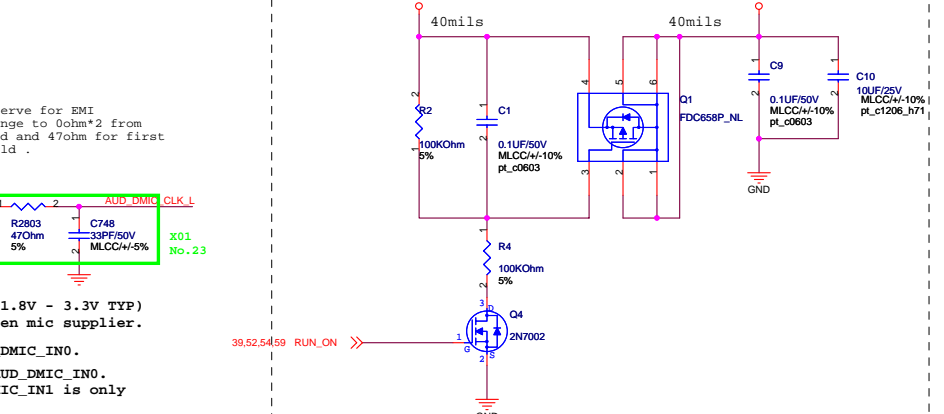
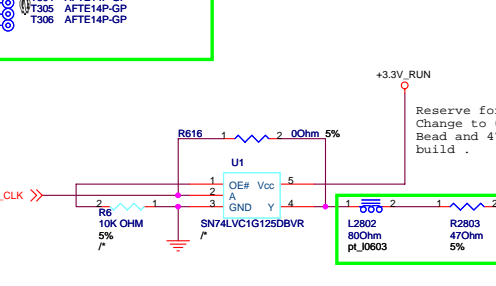
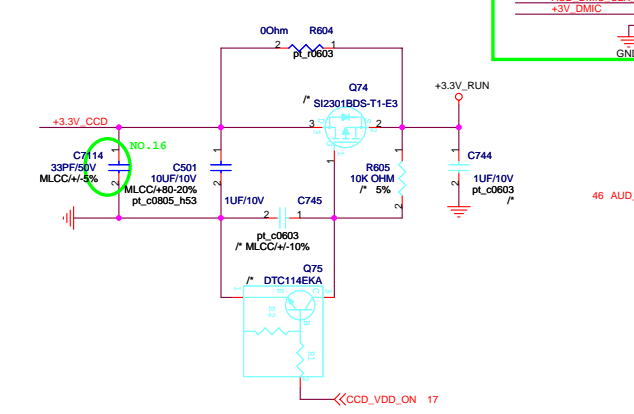


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For AFTE test Close to CON6612

+3.3V_CCD	1	T300	AFTE14P-GP
USBP4 D+	1	T301	AFTE14P-GP
USBP4 D-	1	T302	AFTE14P-GP
AUD_DMIC_IN0	1	T303	AFTE14P-GP
AUD_DMIC_CLK L	1	T304	AFTE14P-GP
+3V_DMIC	1	T305	AFTE14P-GP
	1	T306	AFTE14P-GP



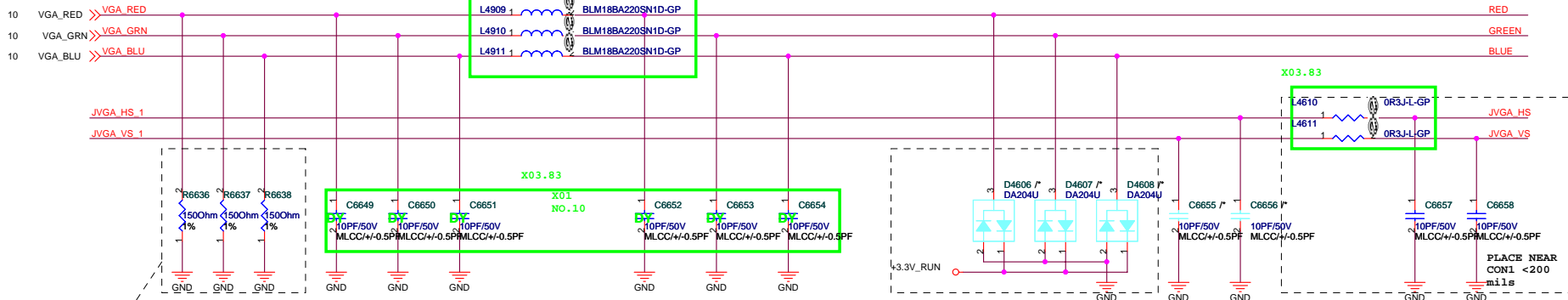
V_DMIC IS DEPENDENT ON MIC SELECTION (1.8V - 3.3V TYP)
 Verify to ensure operability with chosen mic supplier.
 Note1: If only 1 digital mic, use AUD_DMIC_IN0.
 Note2: If using 2 dig mics, also use AUD_DMIC_IN0.
 This input supports 2 digimics. AUD_DMIC_IN1 is only used to support 4 dig mics.

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File: **LVDS CON**
 Size: Custom Document Number
 Date: Tuesday, August 19, 2008 Sheet 28 of 68

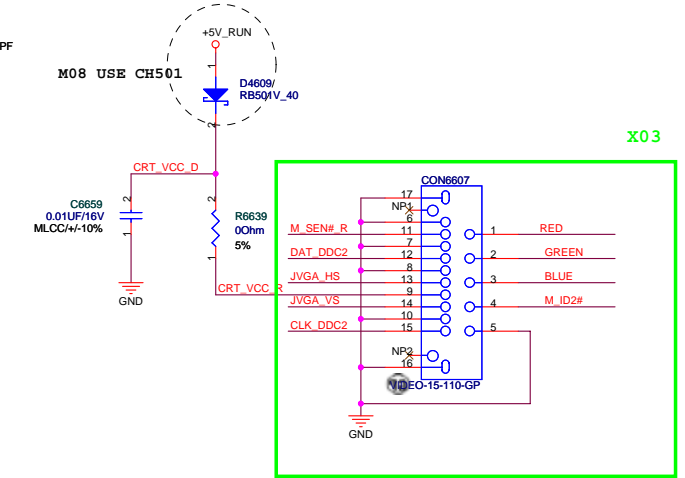
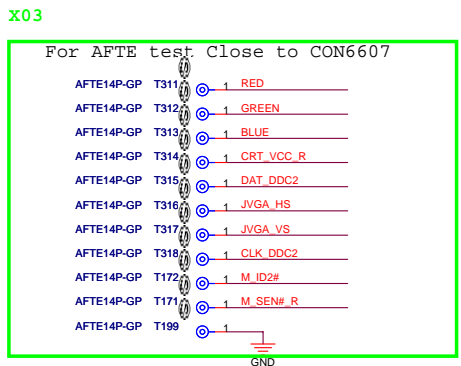
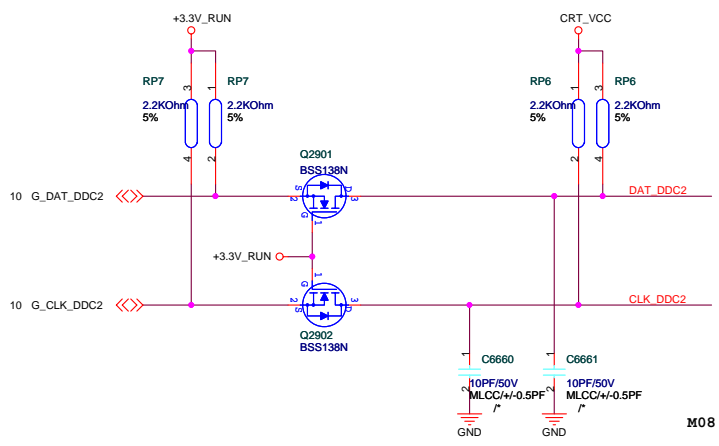
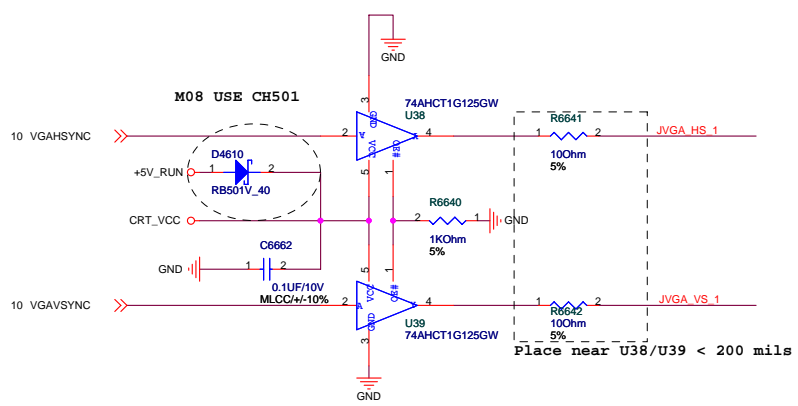
Rev: **A00**
 Custom **Diaz-UMA**

Setting R,G,B treac impedance to 50 ohm.



In addition to these 150 ohm terminations at the connector, 150 ohm terminations are also required at the Source. Route from source (GPU) at 50 ohm target impedance.

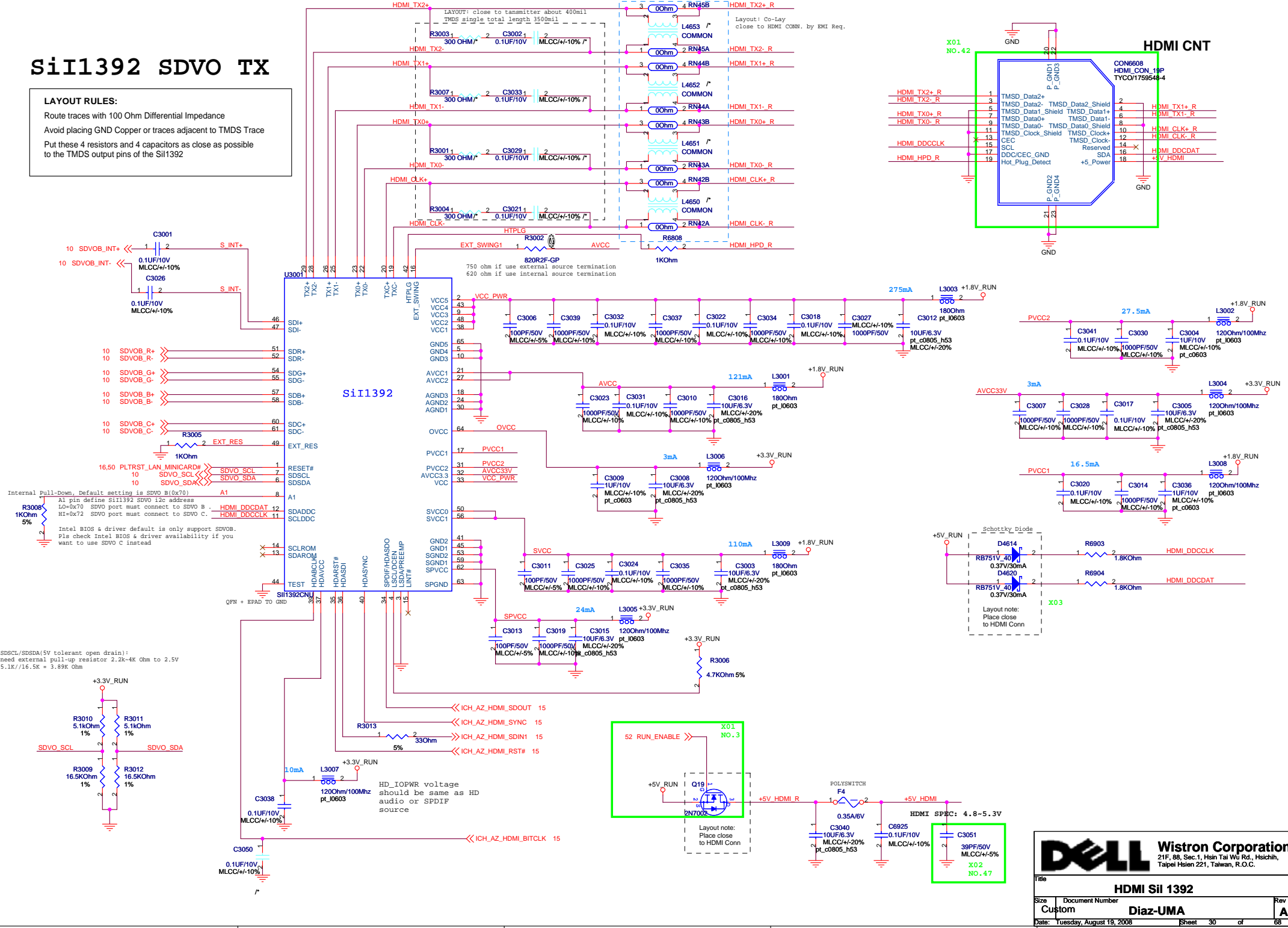
Put D2202, 2203, 2204 as close as possible to CON2201 (D-sub connector)



SiI1392 SDVO TX

LAYOUT RULES:

- Route traces with 100 Ohm Differential Impedance
- Avoid placing GND Copper or traces adjacent to TMDS Trace
- Put these 4 resistors and 4 capacitors as close as possible to the TMDS output pins of the SiI1392

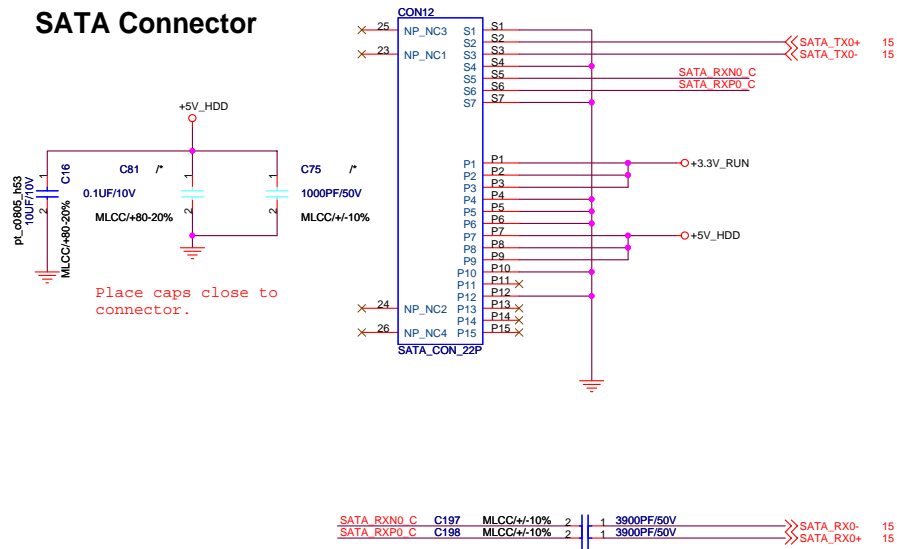


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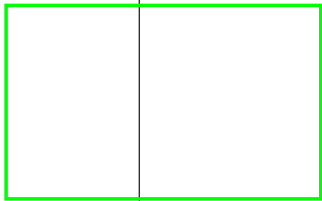
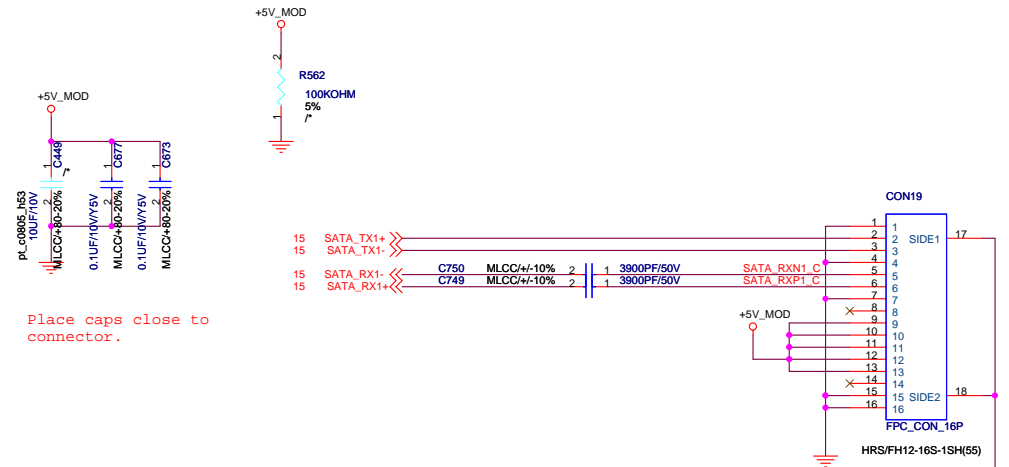
File: **HDMI SiI 1392**

Size	Document Number	Rev
Custom	Diaz-UMA	A00
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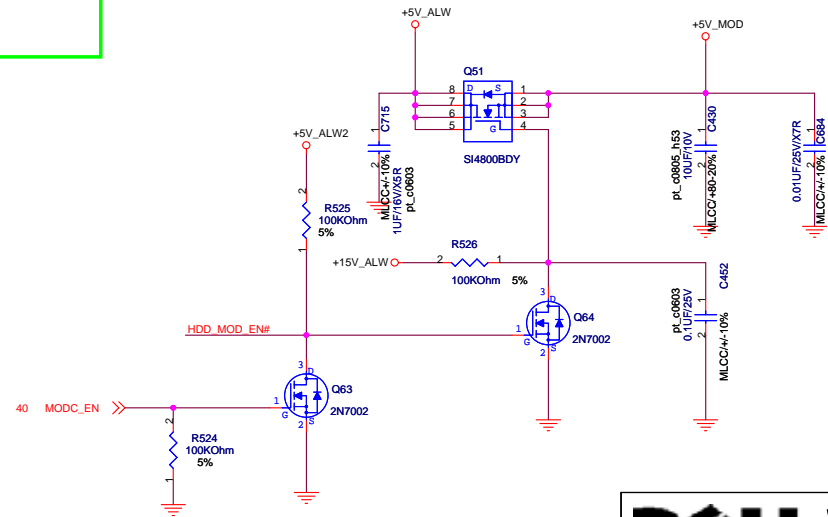
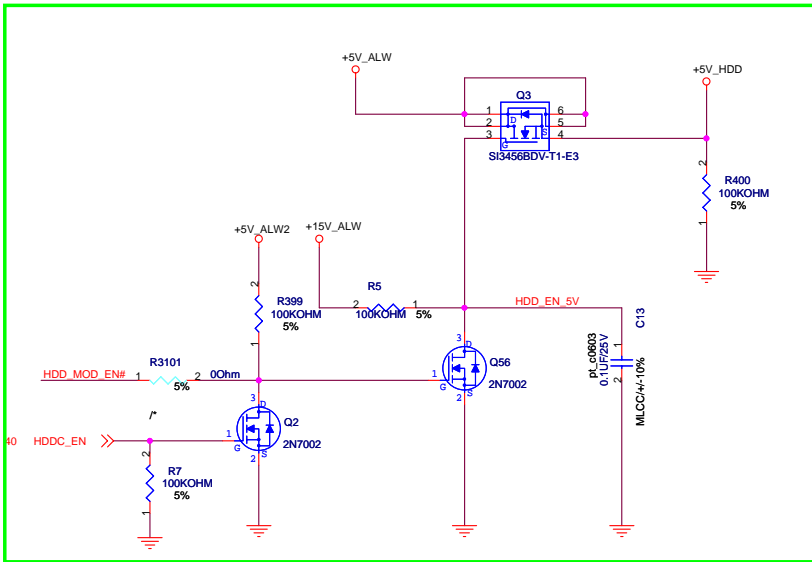
SATA Connector



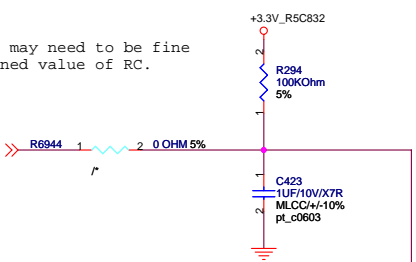
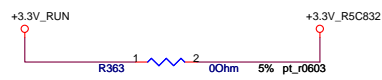
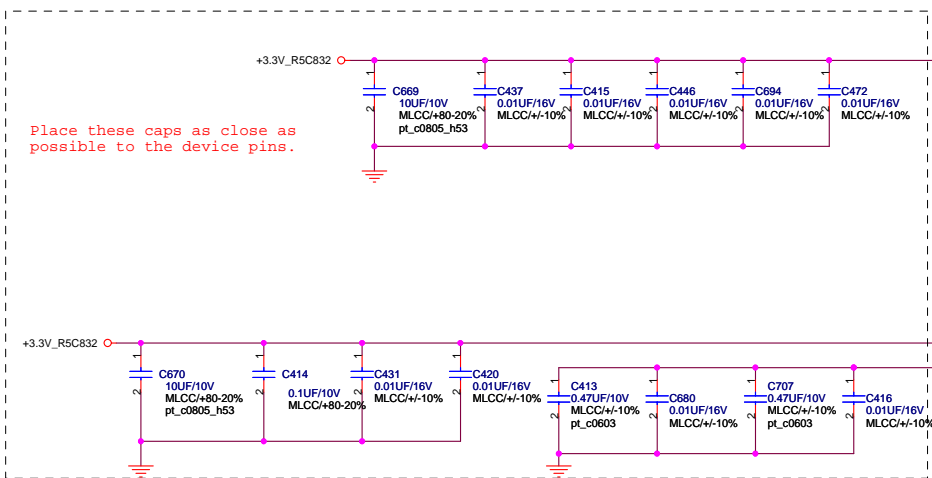
ODD Connector



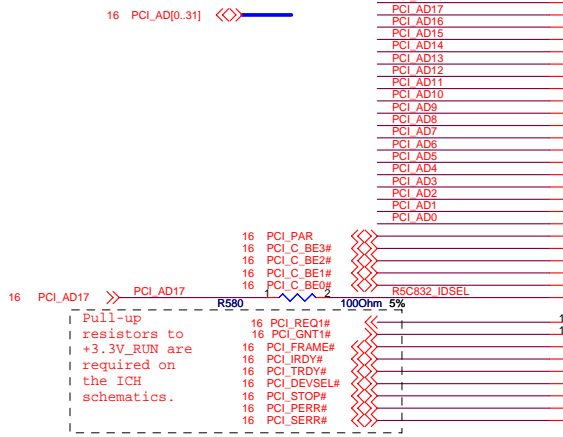
NO. 32



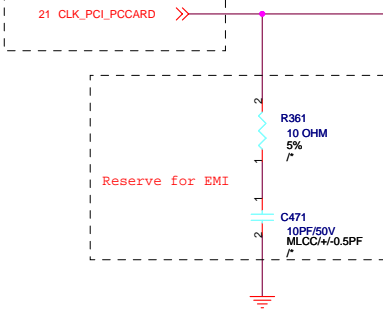
Title			SATA(HDD & CD_ROM)		
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17,39,54,58 IMVP_PWRGD >> R6944 1 2 0 OHM 5%



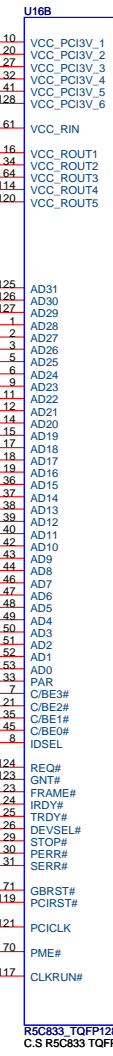
Route to CLK GEN .



40 SYS_PME# <<> Pull-up to +3.3V_ALW is required on SYS_PME# on EC schematics. (From EC). 0 ohm of PME# is no-stuff to prevent backdrive from this signal since the controller is powered of the RUN rail

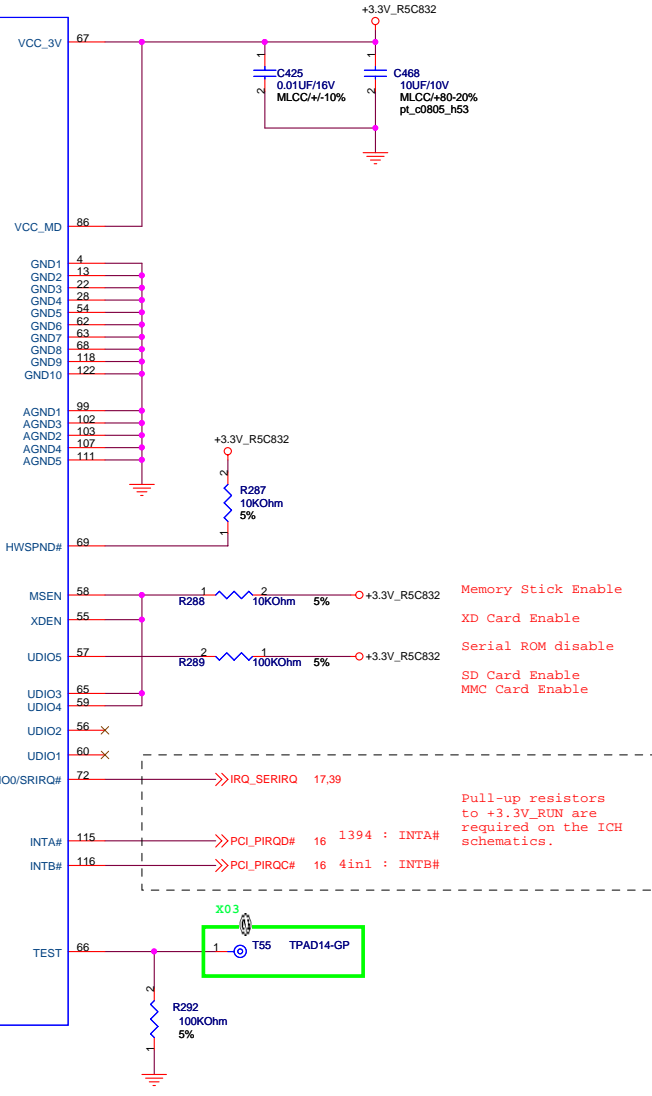
17,39 CLKRUN# <<> R566 1 2 0 OHM 5% The ICH schematics need to include a pull-up resistor to implement CLKRUN#, and the ICH schematics must have a pull-down, or constantly drive the signal low, in order to disable CLKRUN#.

PCI_AD31	125	AD31
PCI_AD30	126	AD30
PCI_AD29	127	AD29
PCI_AD28	1	AD28
PCI_AD27	2	AD27
PCI_AD26	3	AD26
PCI_AD25	5	AD25
PCI_AD24	9	AD24
PCI_AD22	11	AD23
PCI_AD21	12	AD22
PCI_AD20	14	AD20
PCI_AD19	17	AD19
PCI_AD18	17	AD18
PCI_AD17	18	AD17
PCI_AD16	19	AD16
PCI_AD15	37	AD15
PCI_AD14	37	AD14
PCI_AD13	38	AD13
PCI_AD12	38	AD12
PCI_AD11	40	AD11
PCI_AD10	42	AD10
PCI_AD9	43	AD9
PCI_AD8	44	AD8
PCI_AD7	46	AD7
PCI_AD6	47	AD6
PCI_AD5	48	AD5
PCI_AD4	49	AD4
PCI_AD3	50	AD3
PCI_AD2	51	AD2
PCI_AD1	52	AD1
PCI_AD0	53	AD0
PAR	33	PAR
PCI_C_BE3#	21	C/BE3#
PCI_C_BE2#	35	C/BE2#
PCI_C_BE1#	45	C/BE1#
PCI_C_BE0#	45	C/BE0#
IDSEL	8	IDSEL
REQ#	124	REQ#
GNT#	123	GNT#
FRAME#	23	FRAME#
IRDY#	24	IRDY#
TRDY#	25	TRDY#
DEVSEL#	26	DEVSEL#
STOP#	29	STOP#
PERR#	30	PERR#
SERR#	31	SERR#
GBRST#	71	GBRST#
PCIRST#	119	PCIRST#
PCICLK	121	PCICLK
PME#	70	PME#
CLKRUN#	117	CLKRUN#



PCI / OTHER

Ricoh R5C832 Package Type : TQFP-128-P1 (1414)



Memory Stick Enable
XD Card Enable
Serial ROM disable
SD Card Enable
MMC Card Enable

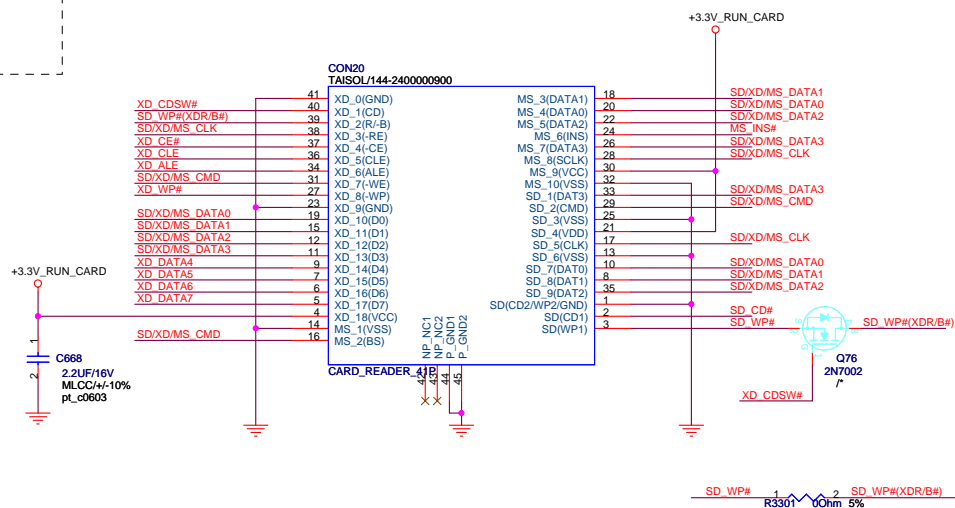
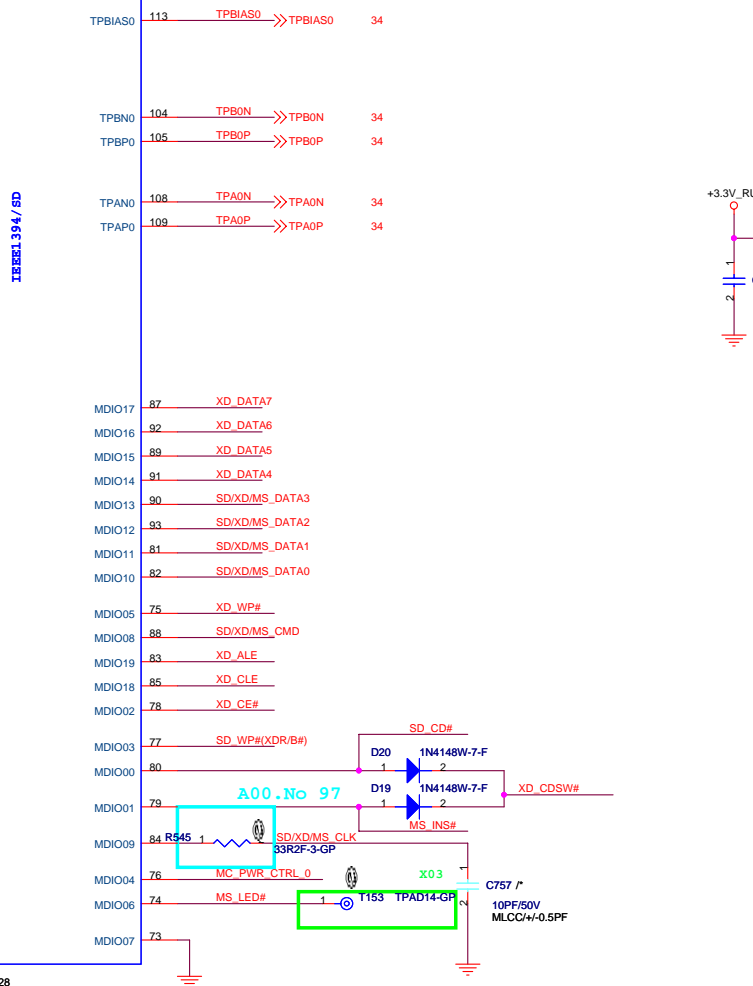
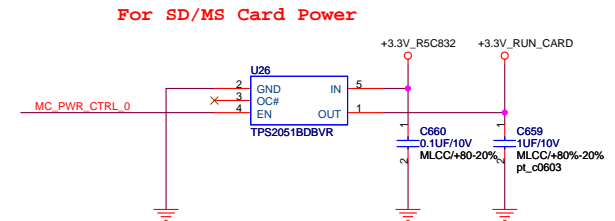
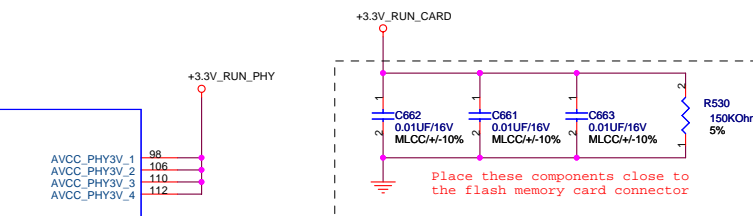
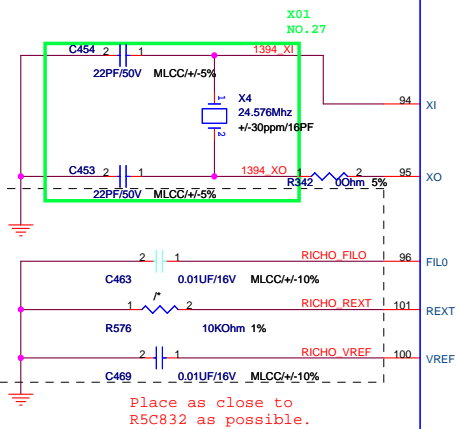
Pull-up resistors to +3.3V_RUN are required on the ICH schematics.



R5C833 - PCI INTERFACE			
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Date:	Tuesday, August 19, 2008	Sheet	32 of 68

Recommended Crystal Specs from Data Sheet:

Normal Frequency : 24.576 Mhz
 Frequency Tolerance : +/- 50ppm @ 25C
 Driver Level : .1 mW
 Load capacitance : 10pF
 Equ. Resistance : 50 Ohm Max
 Shunt Capacitance : 7.0pF Max

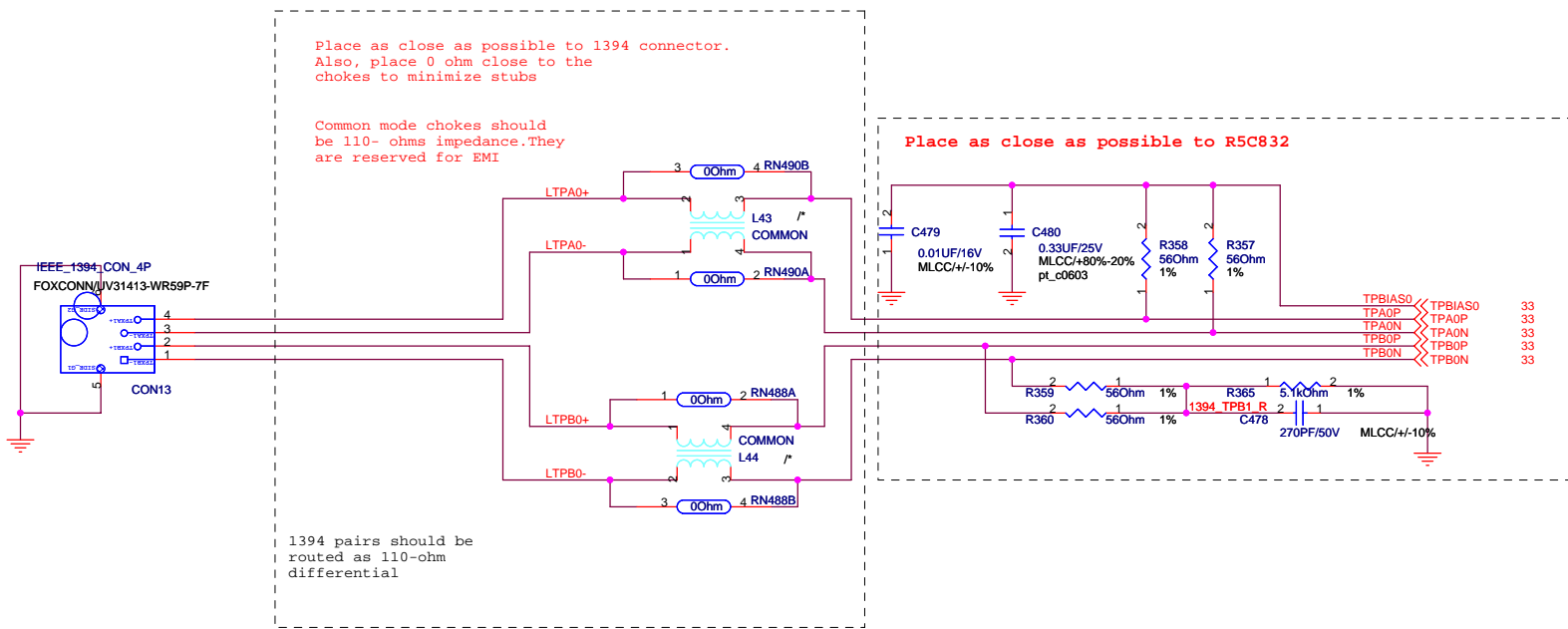
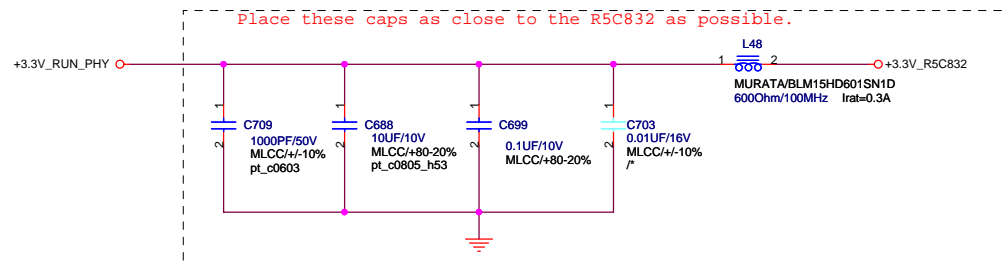


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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **R5C833 - FLASH MEMORY PART**

Size	Document Number	Rev
Custom	Diaz-UMA	A00

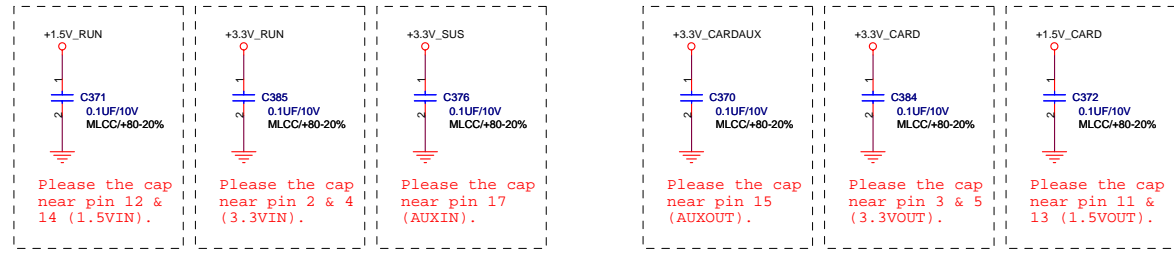
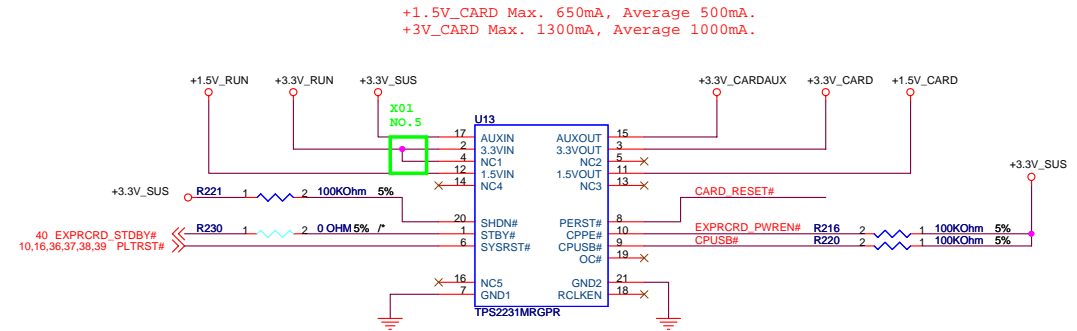
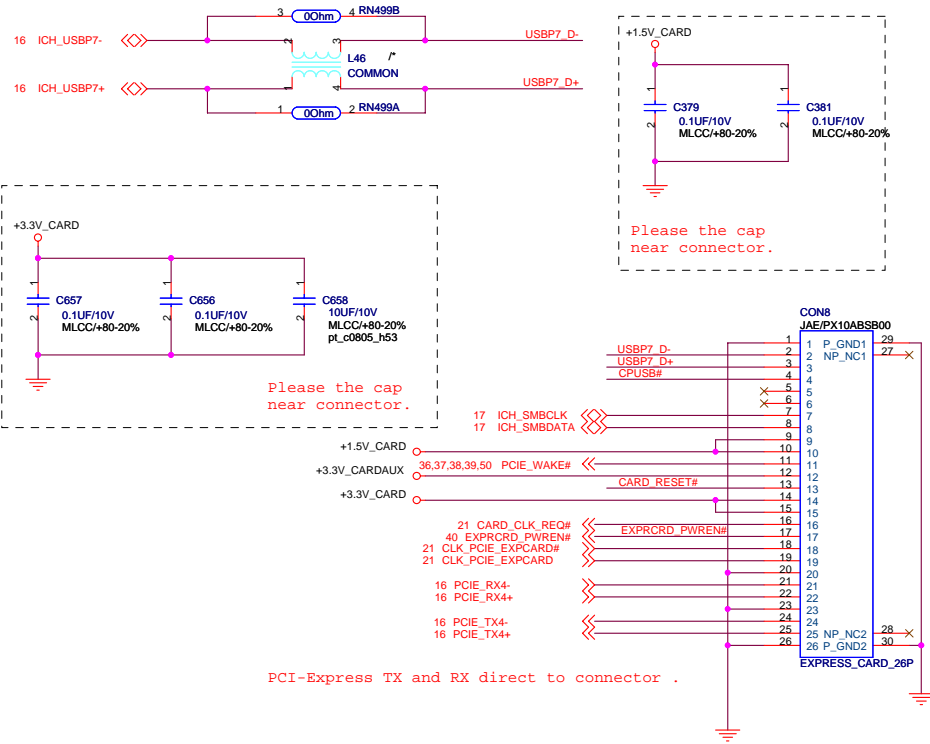
Date: Tuesday, August 19, 2008 Sheet 33 of 68



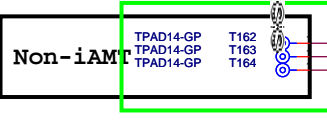
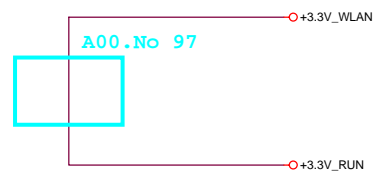
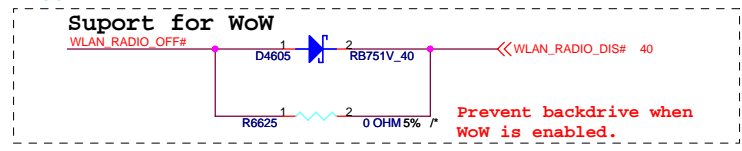
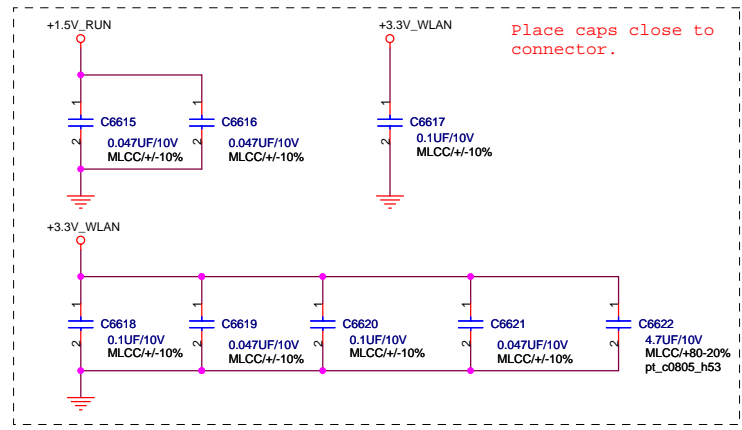
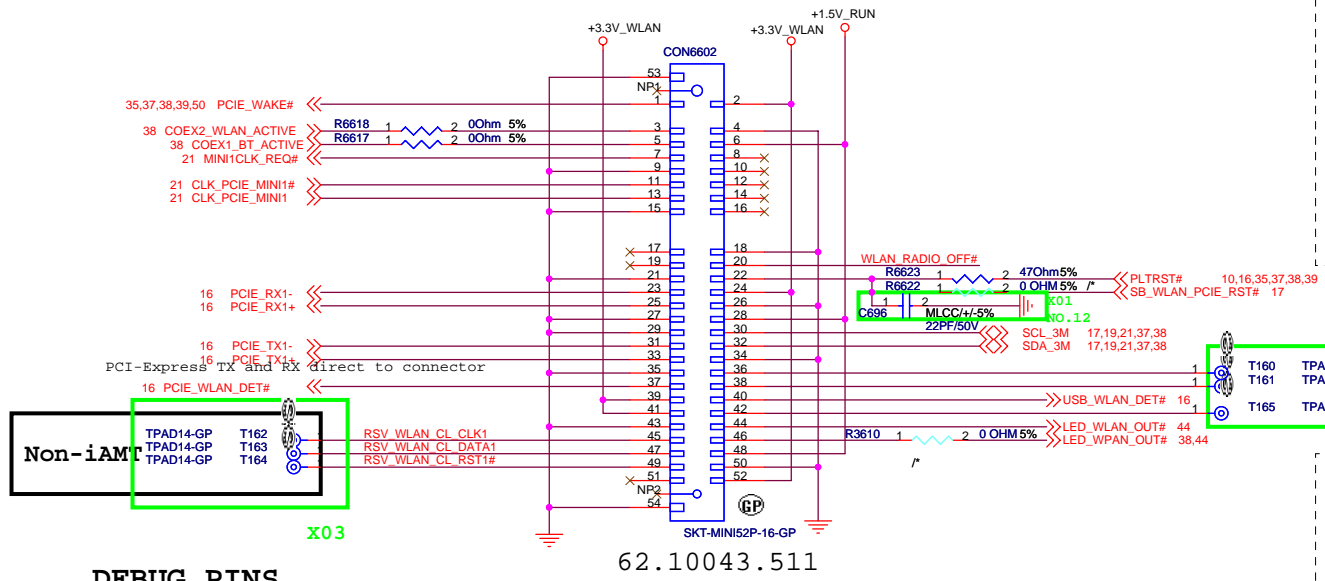
(20071005)for choke & 0ohm colayout

DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: R5C833 - IEEE1394 PART			
Size: A3	Document Number:	Diaz-UMA	Rev: A00
Date: Tuesday, August 19, 2008	Sheet: 34	of: 68	

Express Card



+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.



DEBUG PINS

JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81

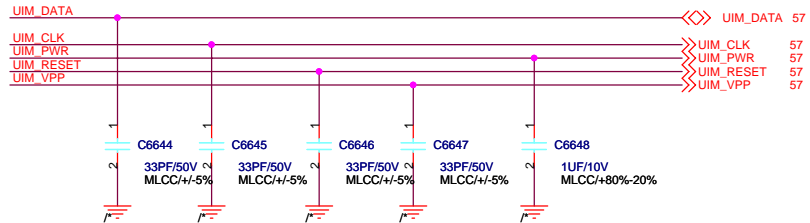
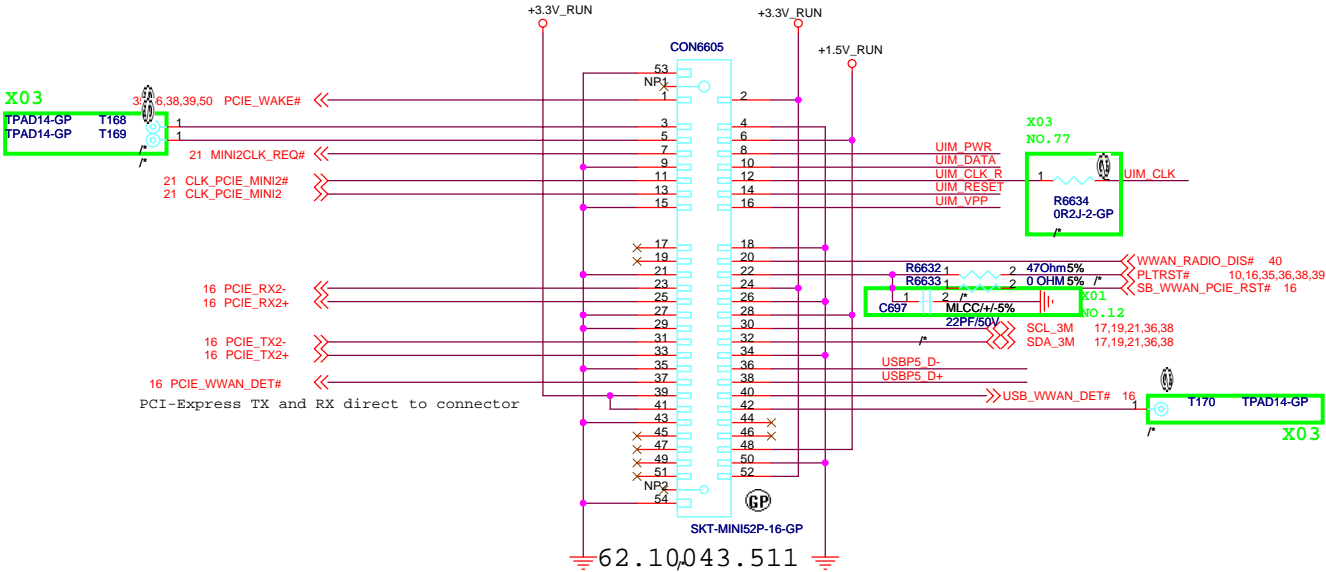
DELL Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **MINI CARD - Kedron**

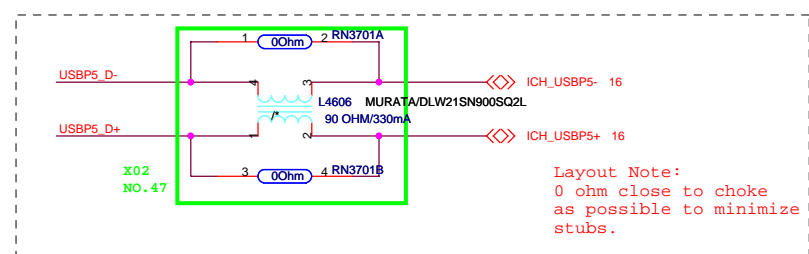
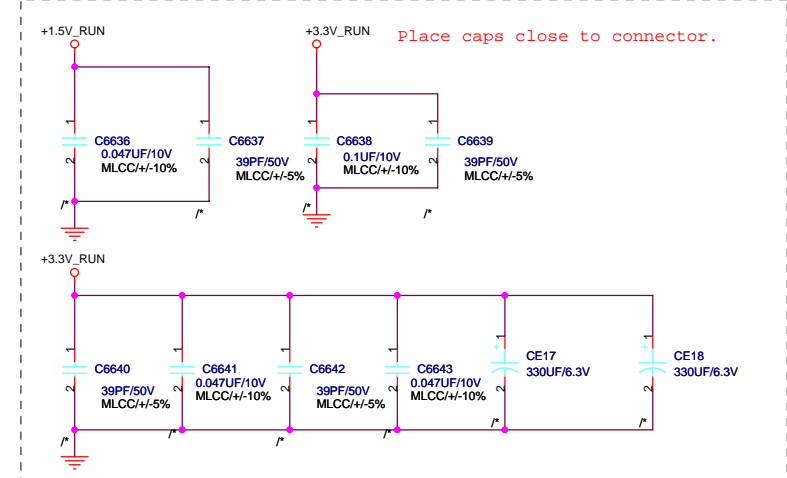
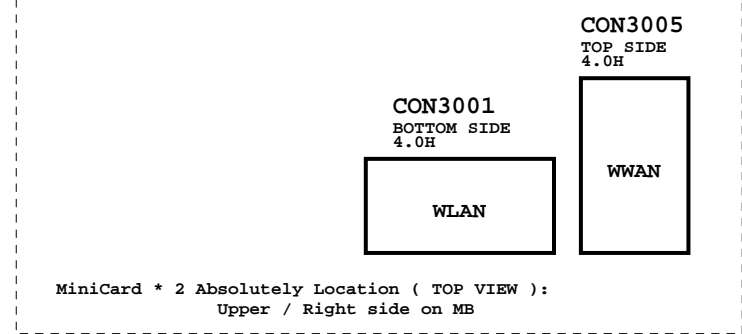
Size: A3 Document Number: **Diaz-UMA** Rev: **A00**

Date: Tuesday, August 19, 2008 Sheet 36 of 68

MiniCard WWAN connector

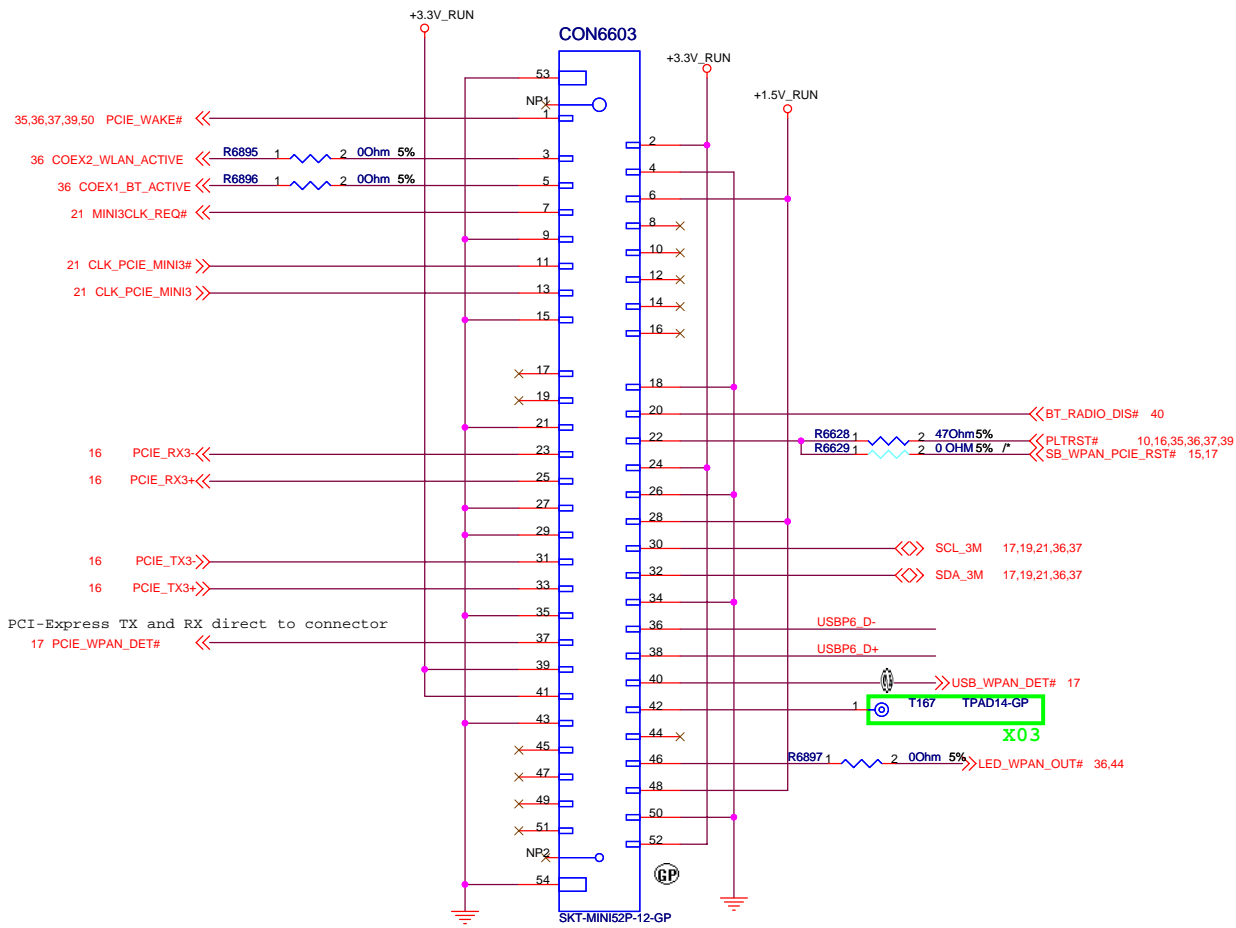


MiniCard Relative Location (TOP VIEW):



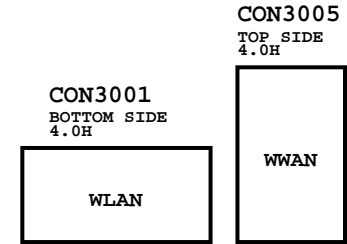
Title			MINI CARD - Robson		
Size	Document Number	Rev			
A3			A00		
Date:	Tuesday, August 19, 2008	Sheet	37	of	68

MiniCard WPAN connector

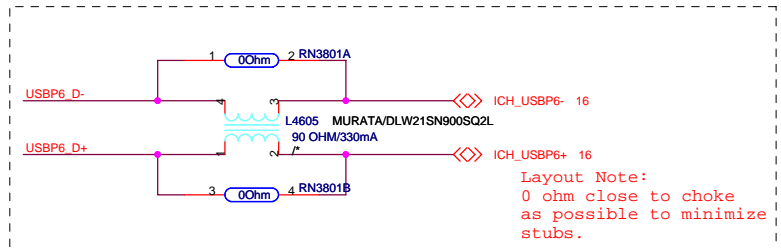
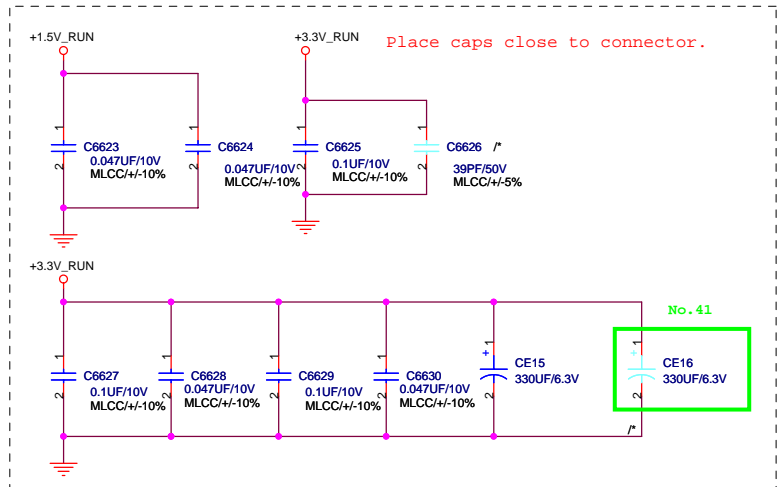


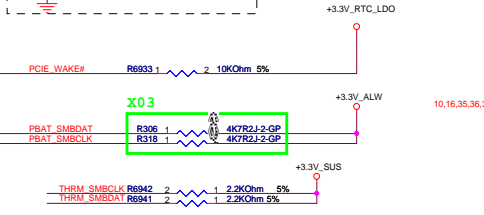
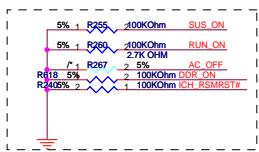
62.10043.441

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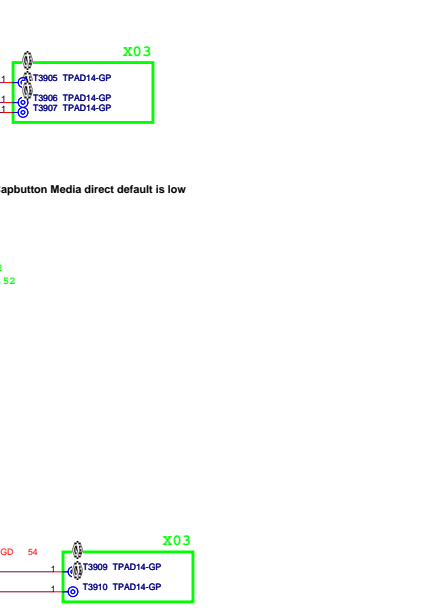
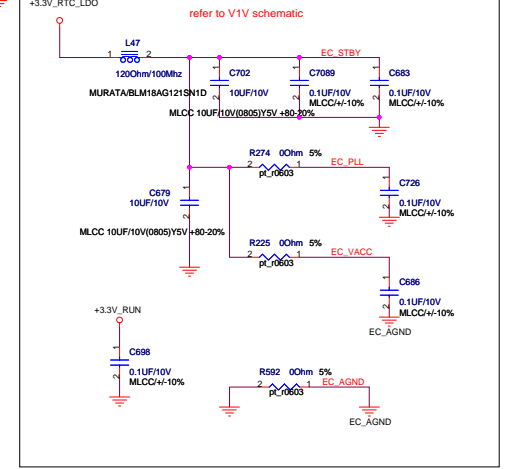
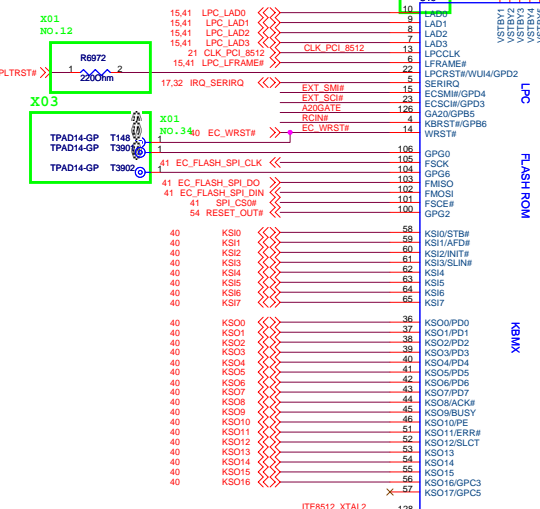
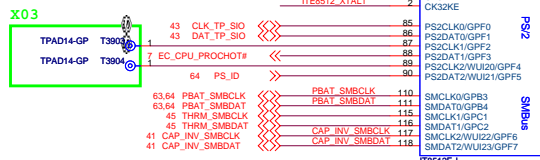
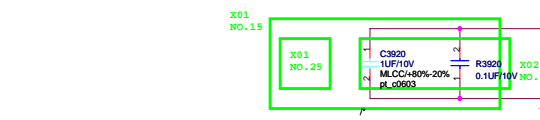
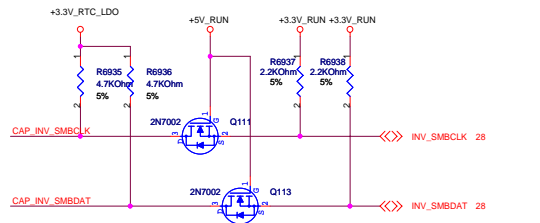
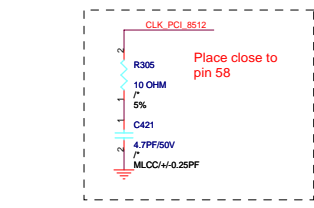
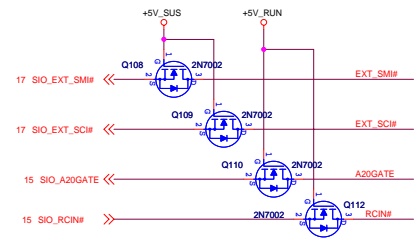
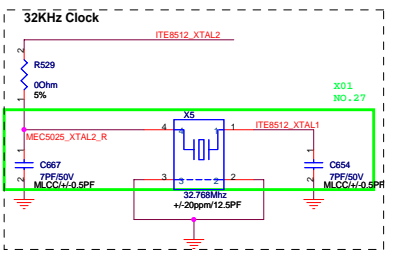
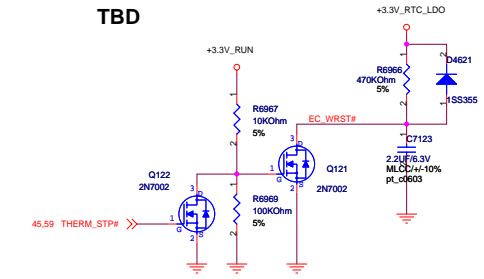


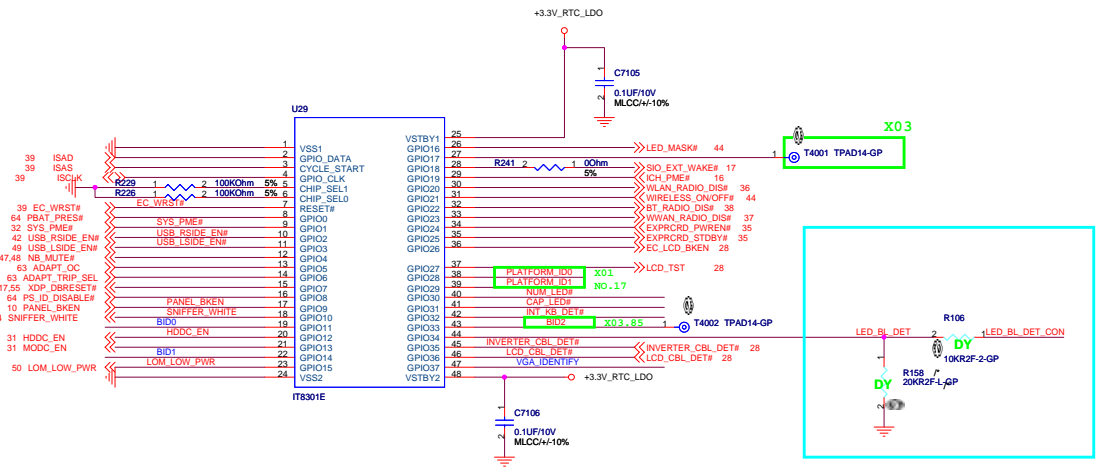
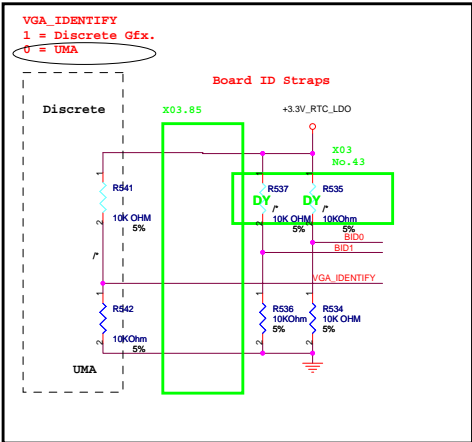
MiniCard * 2 Absolutely Location (TOP VIEW):
Upper / Right side on MB



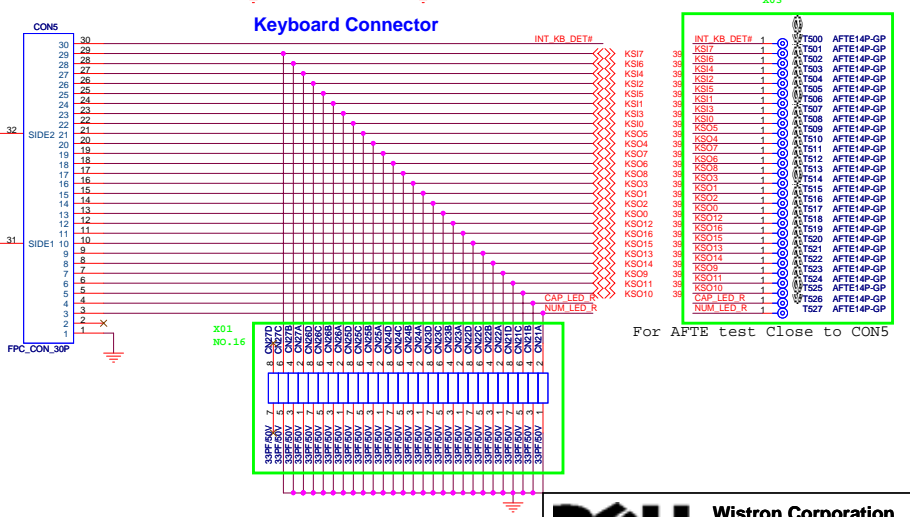
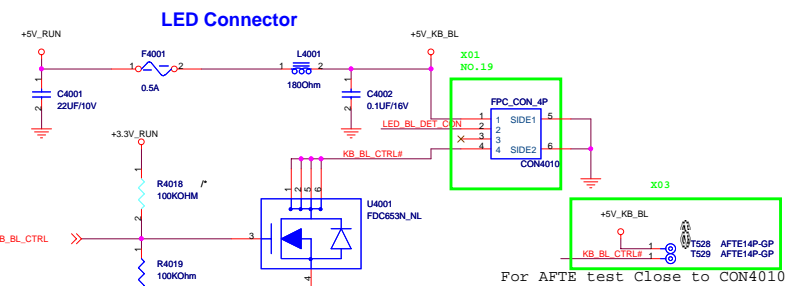
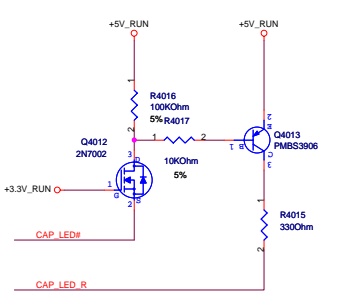
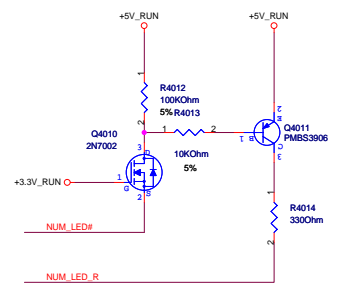
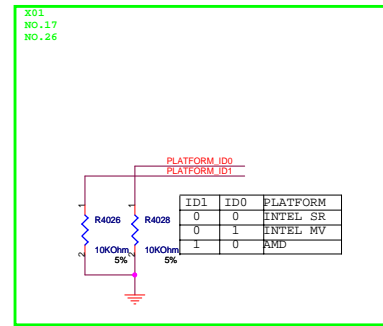
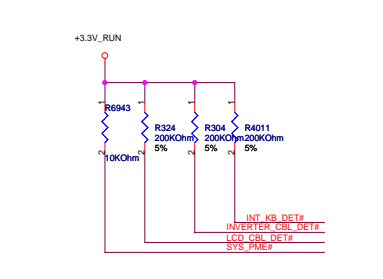
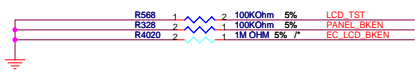


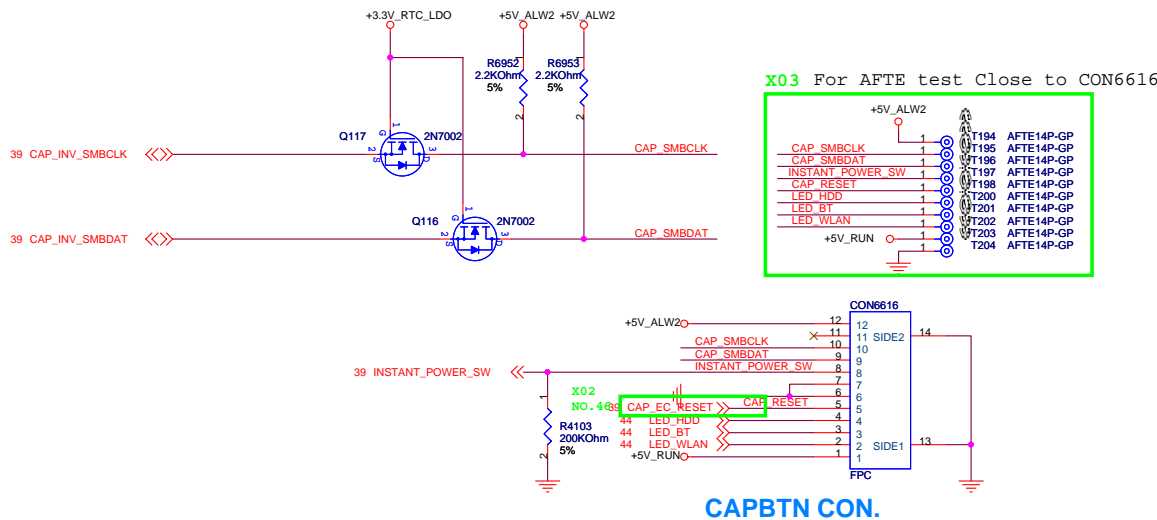
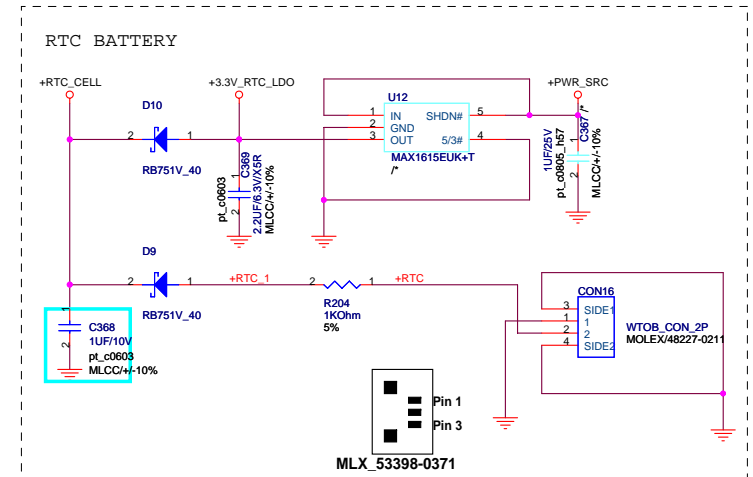
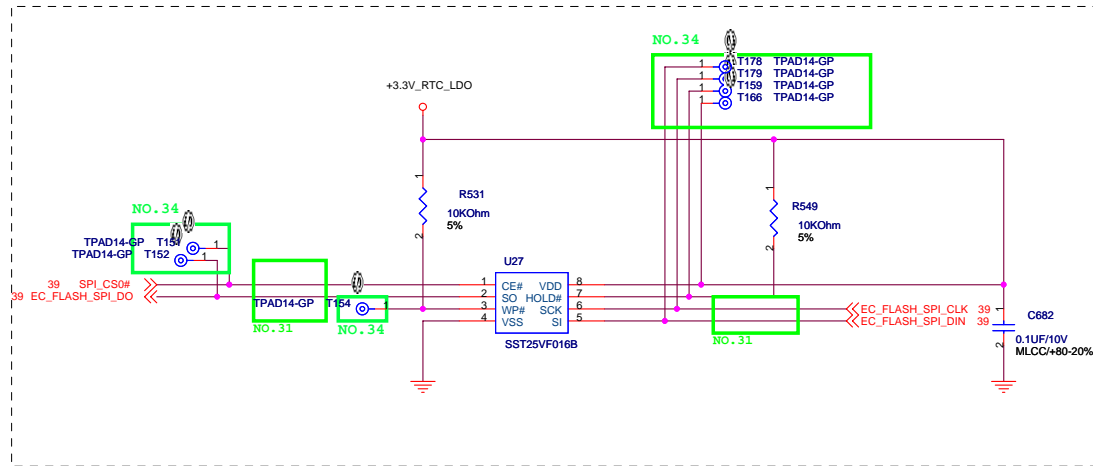
TBD



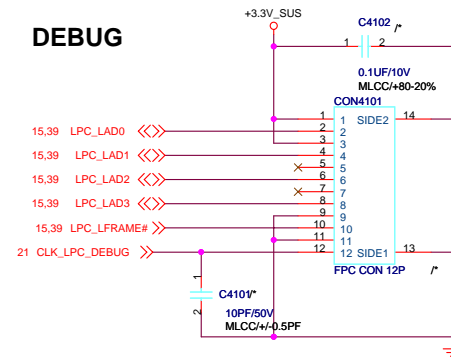


BID1	BID0	M/B VER
0	0	A00
0	1	A01
1	0	A02
1	1	A03

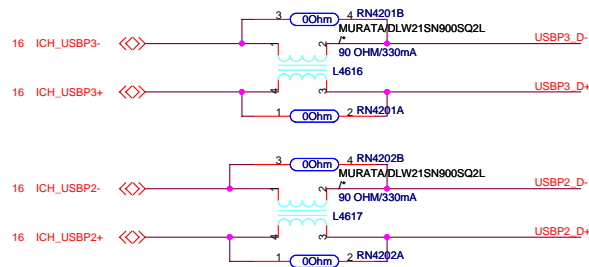




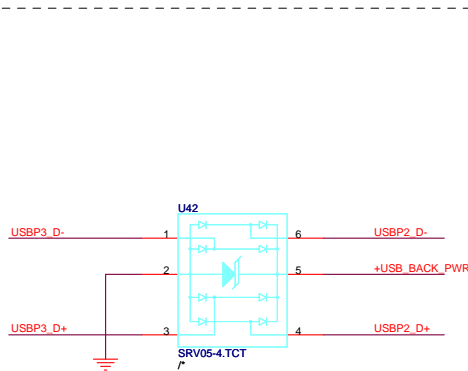
Note:
+5V_ALW2 => for Capbutton PSOC and Media direct LED only.
+5V_RUN => for Capbutton LED and Photo sensor.



External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently .

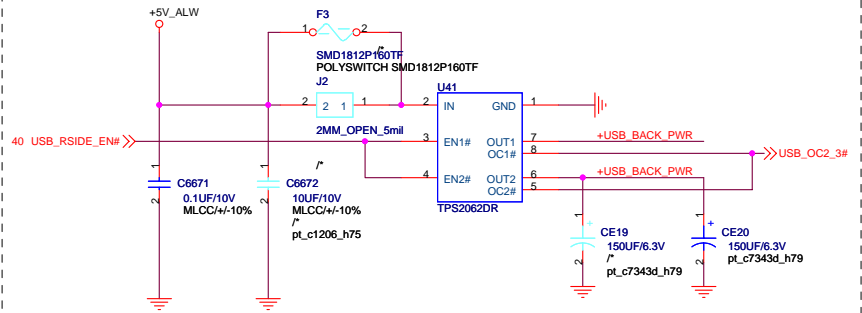


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.



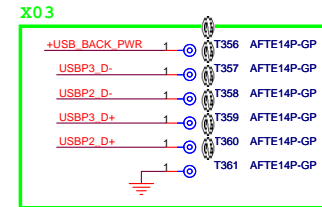
Place ESD diodes as close as USB connector. Semtech SRV05-4 can also be used but the Philips IP42220CZ6 have a lower input C (1pf vs 3pf) .

Place one 150uF cap by each USB connector



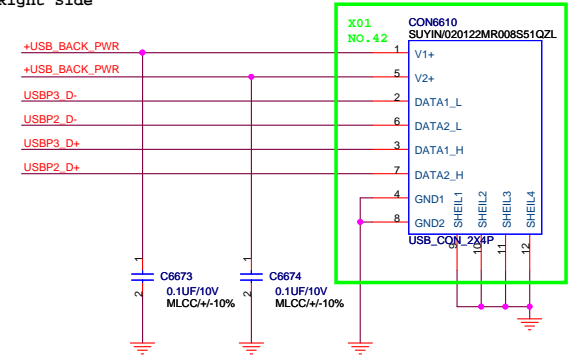
Each channel is 1A

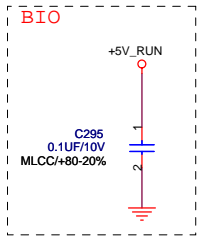
Consult you ESD Engineer if you think you may need to add ESD Supression Components to your USB lines. Add PADS ONLY until proven diodes are really needed.



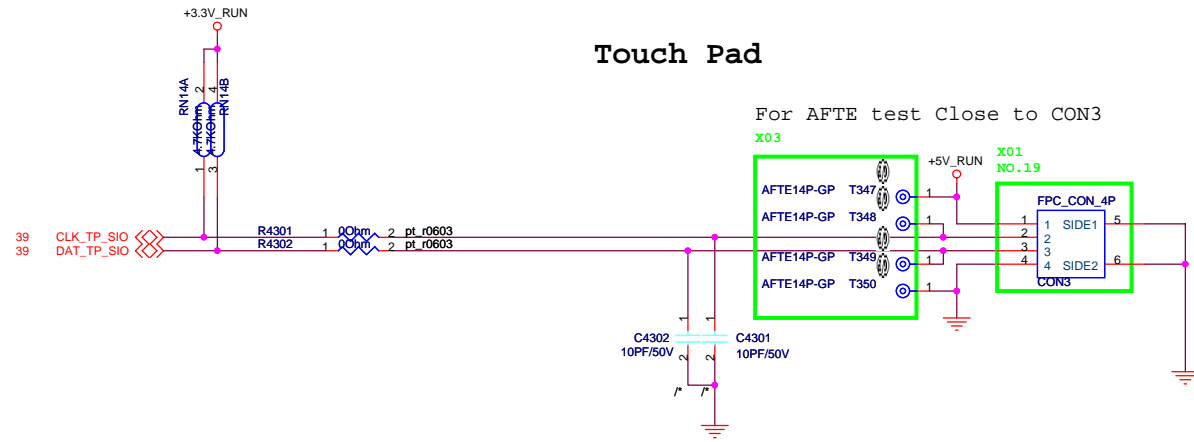
For AFTE test Close to CON6610

Right side

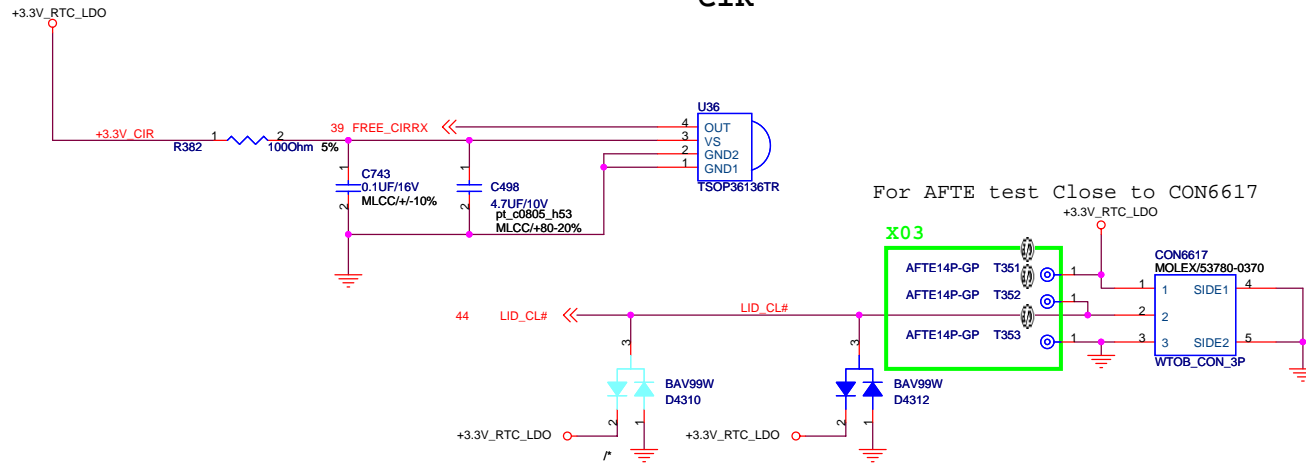




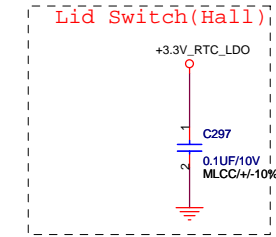
Touch Pad

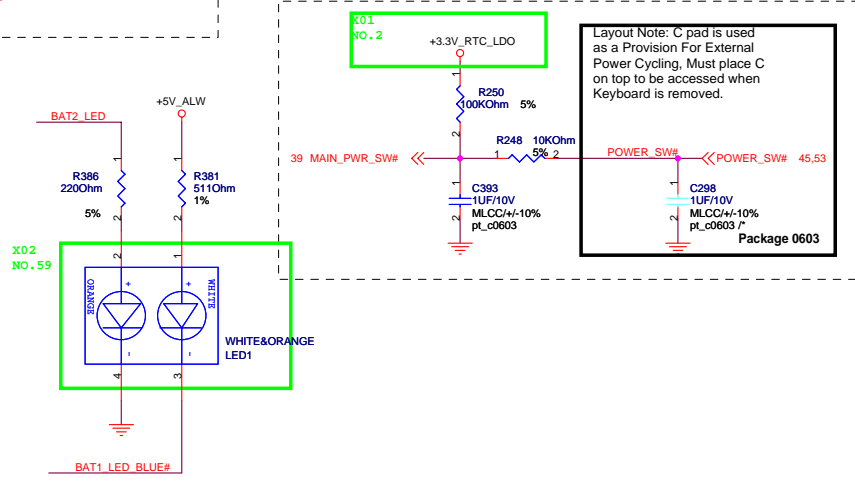
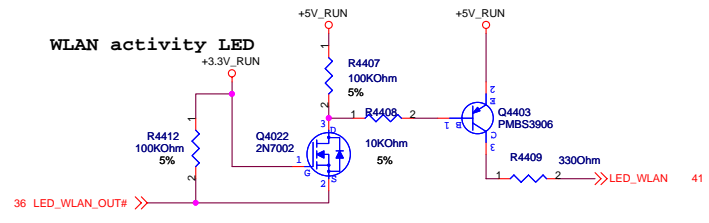
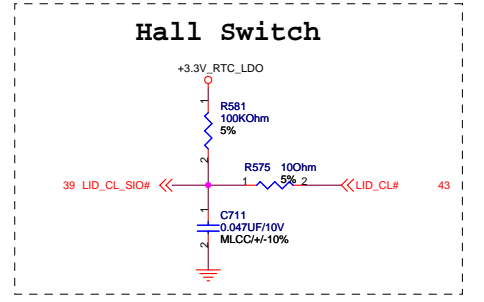
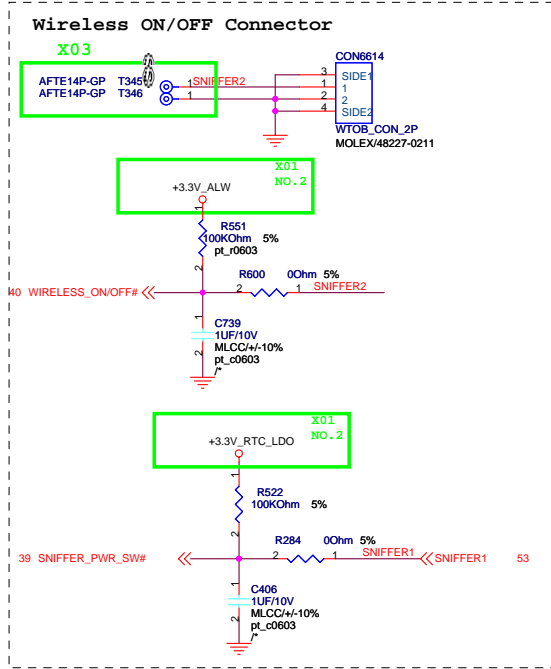
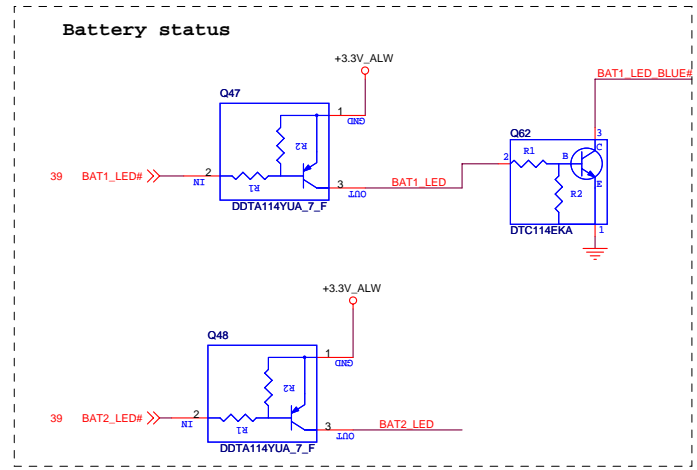
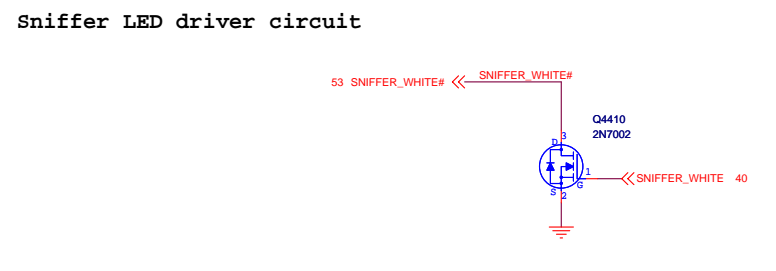
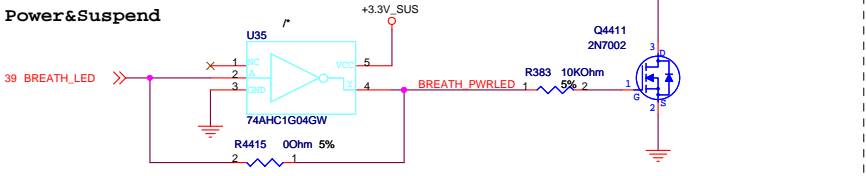
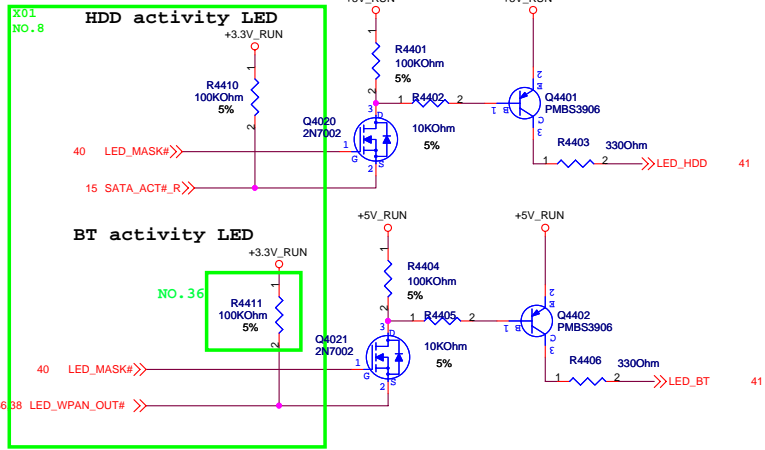


CIR



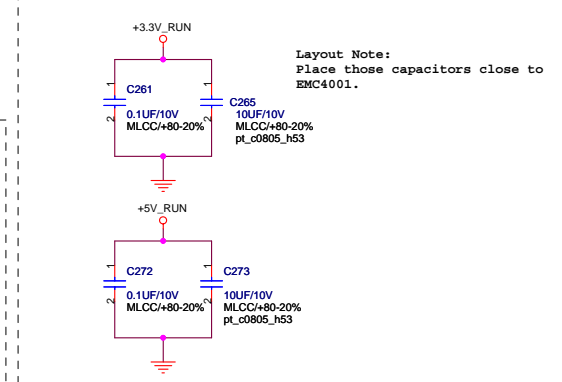
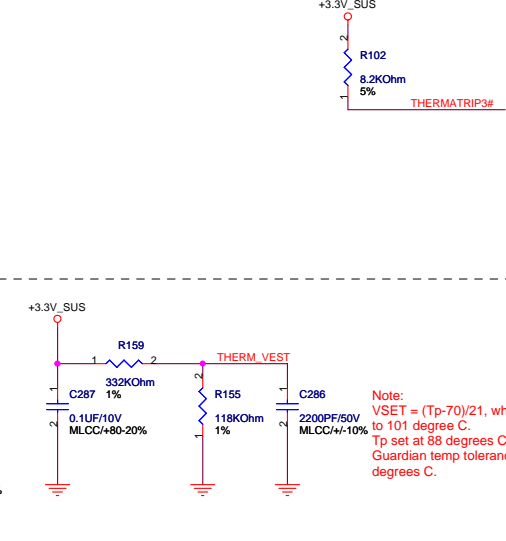
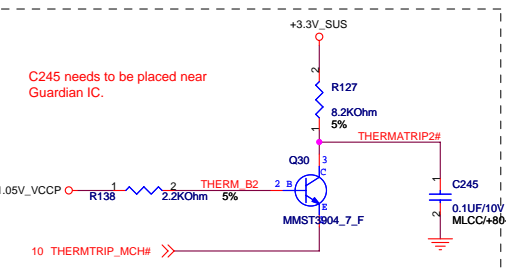
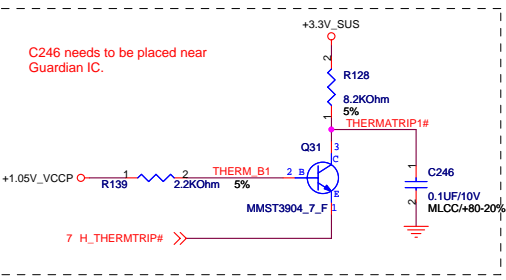
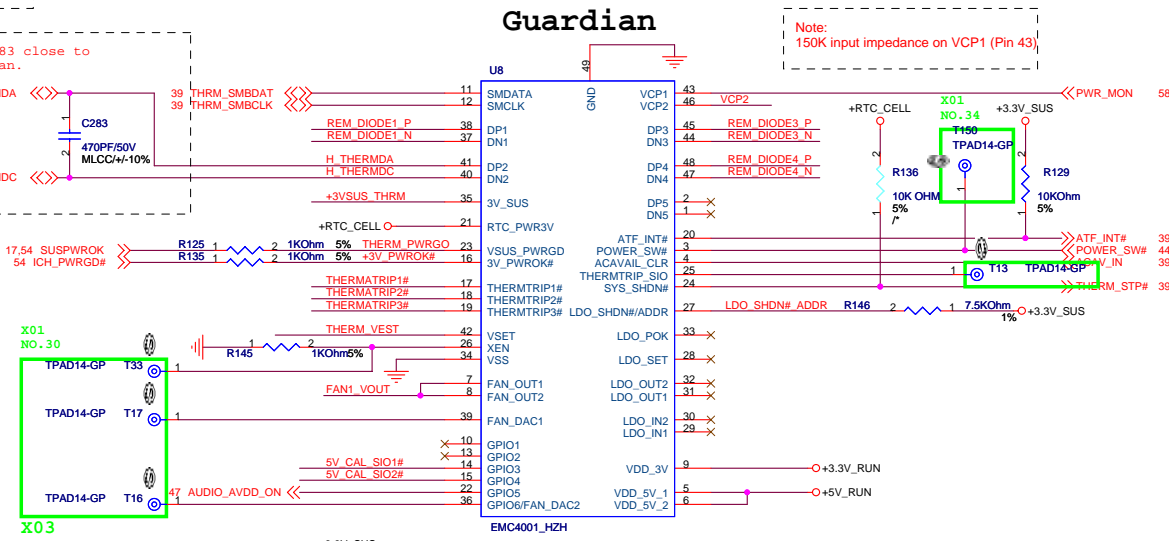
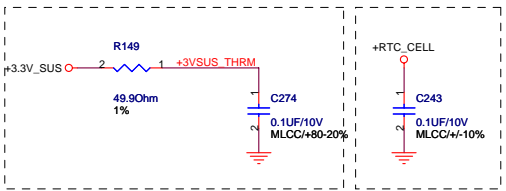
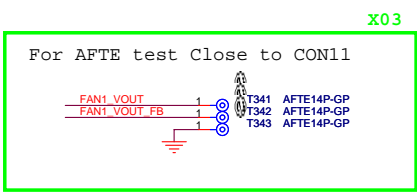
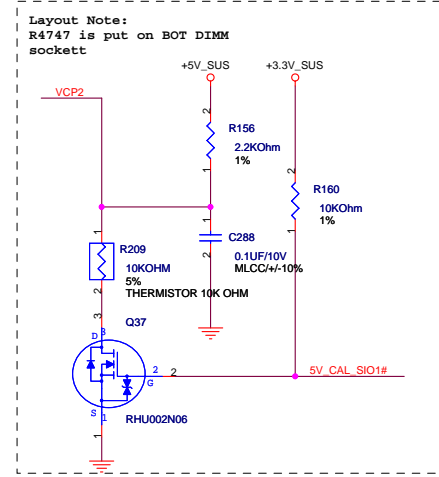
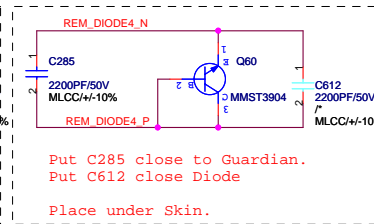
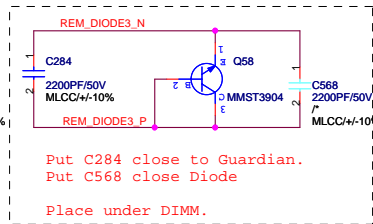
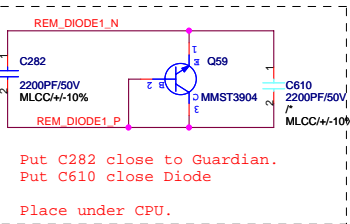
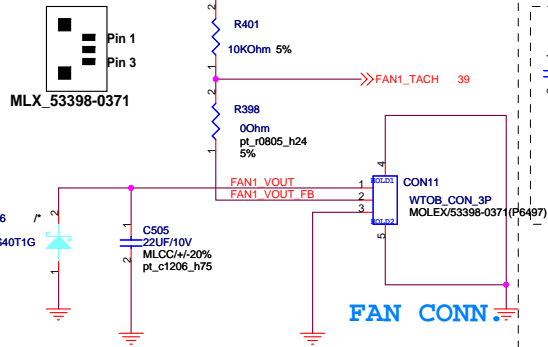
HALL SENSOR

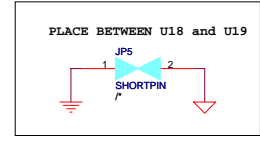
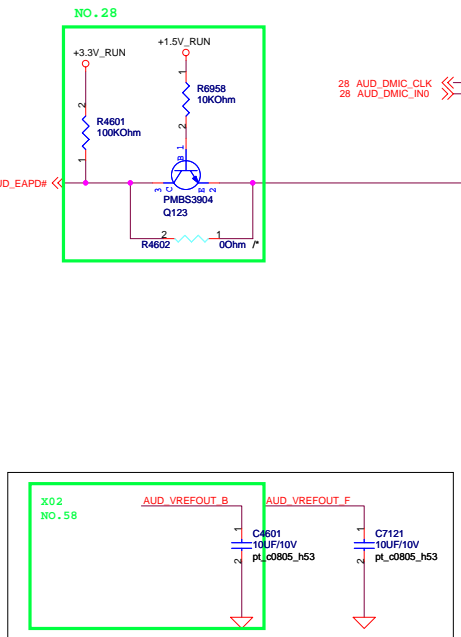
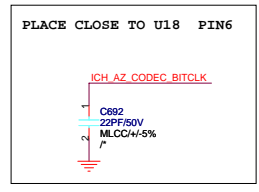
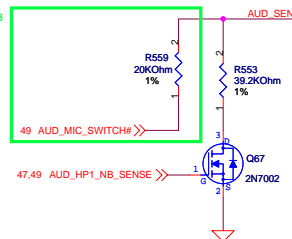
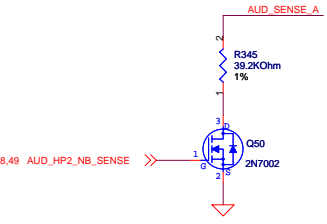
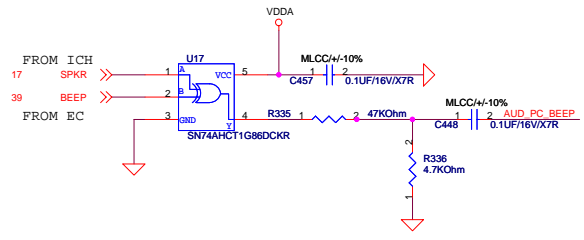




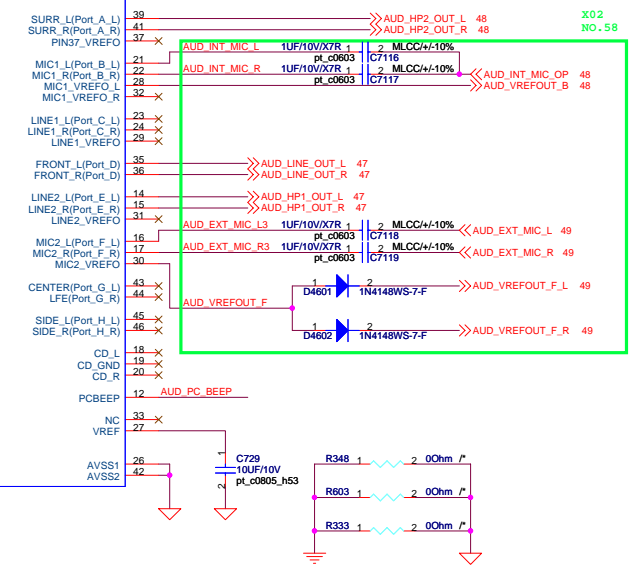
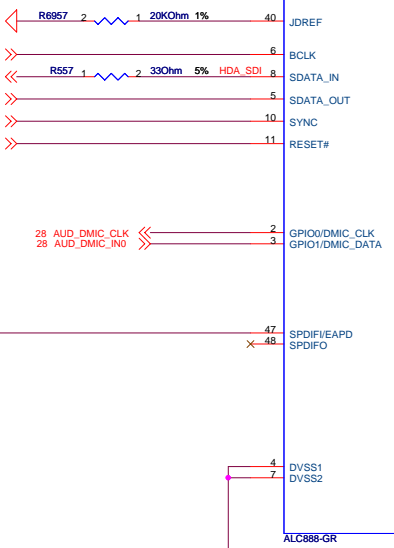
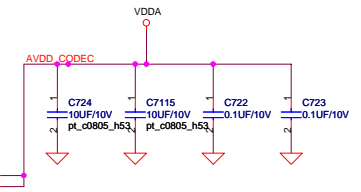
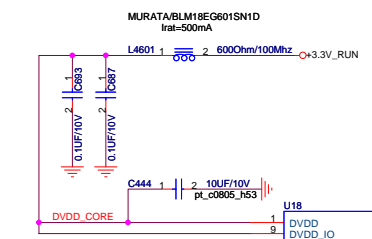
Layout Note: C pad is used as a Provision For External Power Cycling, Must place C on top to be accessed when Keyboard is removed.

Package 0603



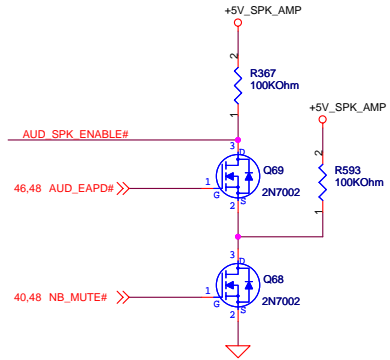


Port A----> HP2
 Port E----> HP1
 Port B----> INT MIC
 Port F----> ext Mic
 Port D----> Speaker

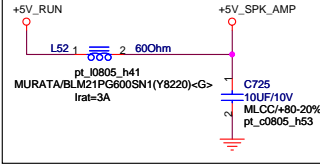


Title			ALC888		
Size	Document Number	Rev			
Custom	Diaz-UMA	A00			
Date:	Tuesday, August 19, 2008	Sheet	46	of	68

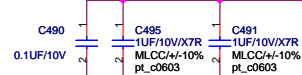
Signal Inverter for Speaker Shutdown
 Allow speakers to work while class driver is installed



PLACE JUST BEFORE +5V_MAX9789 CROSSES MOAT

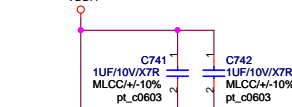


Place C490 close to Pin 30



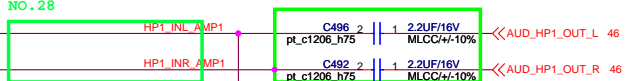
NOTE: For TPA6040A, pop C487 and C486 (0402 X5R) and no pop R601 and R376. C487 and C486 value should match C494 and C493

VDDA Range = 1.21V ~ 4.85V (SET = 1.23V).
 If SET=0 V, VDDA = 4.75V

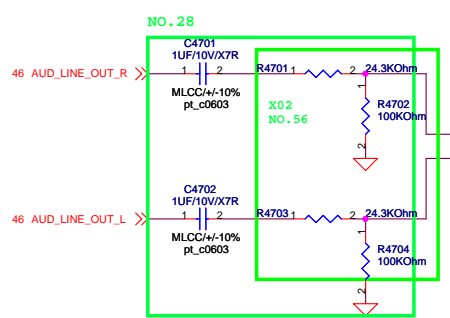


NO. 28

X02 NO. 48

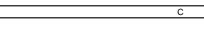
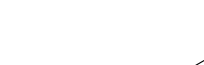
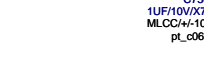
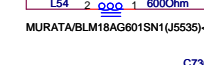
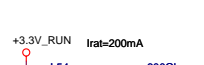
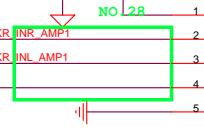
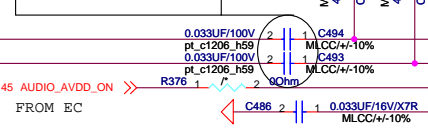


Note: For TPA6040A, pop R378 and no pop R375



TEMPORARY VALUES. FINAL VALUES CHOSEN IN PT PHASE.

NOTE: For TPA6040A, pop C486 and no pop R376

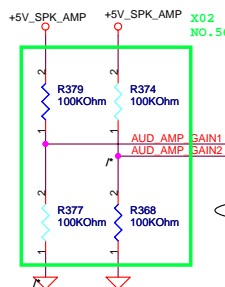


ROUTE VIA TRACE BACK TO TIE POINT.

ROUTE VIA TRACE BACK TO TIE POINT.

ROUTE VIA TRACE BACK TO TIE POINT.

GAIN SETTING RESISTORS



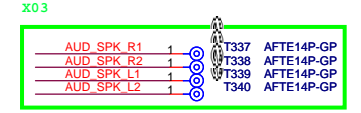
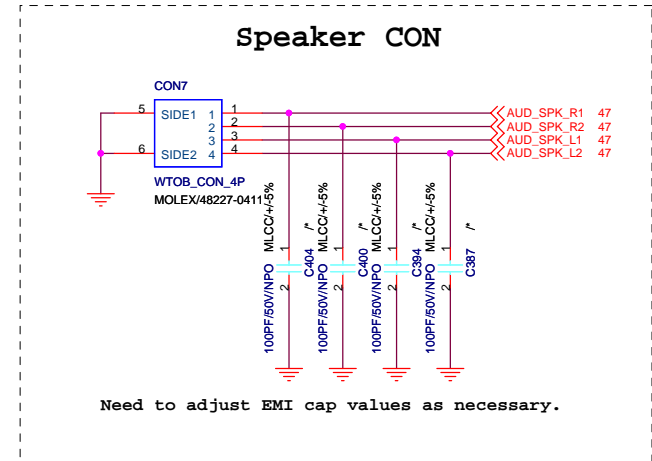
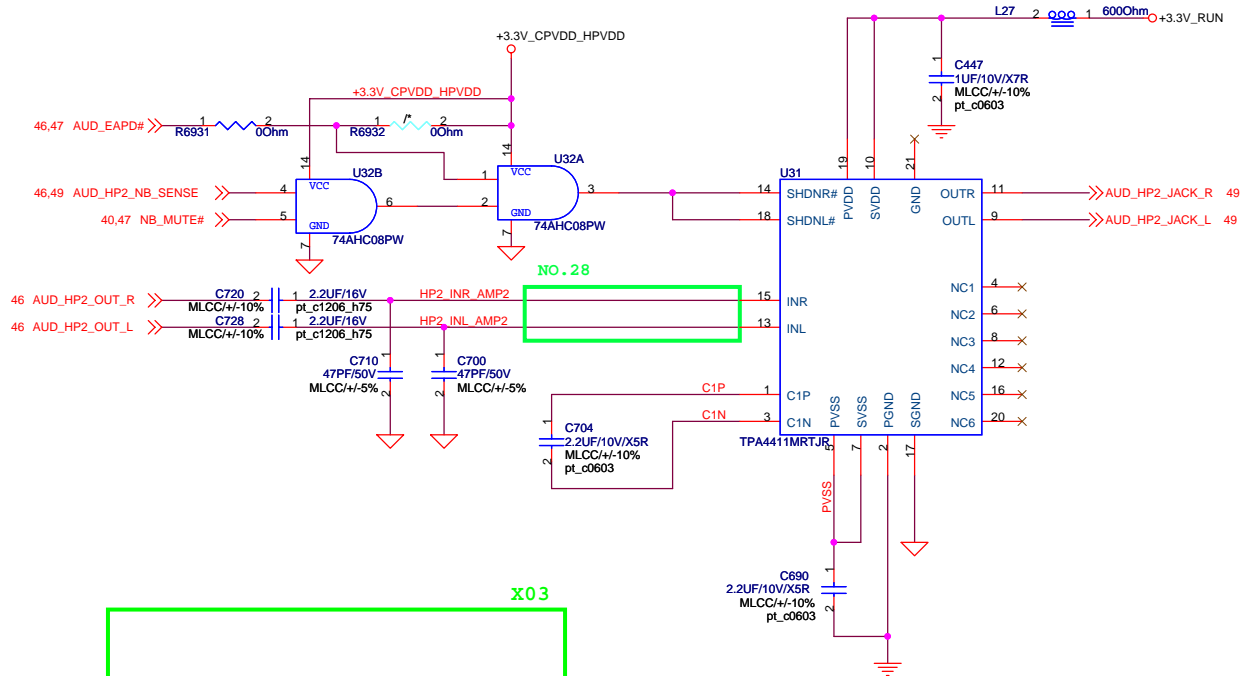
Gain1	Gain2	Gain
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

Maxim:1.8V ~ 3.6V
 TI:1.8V ~ 4.5V

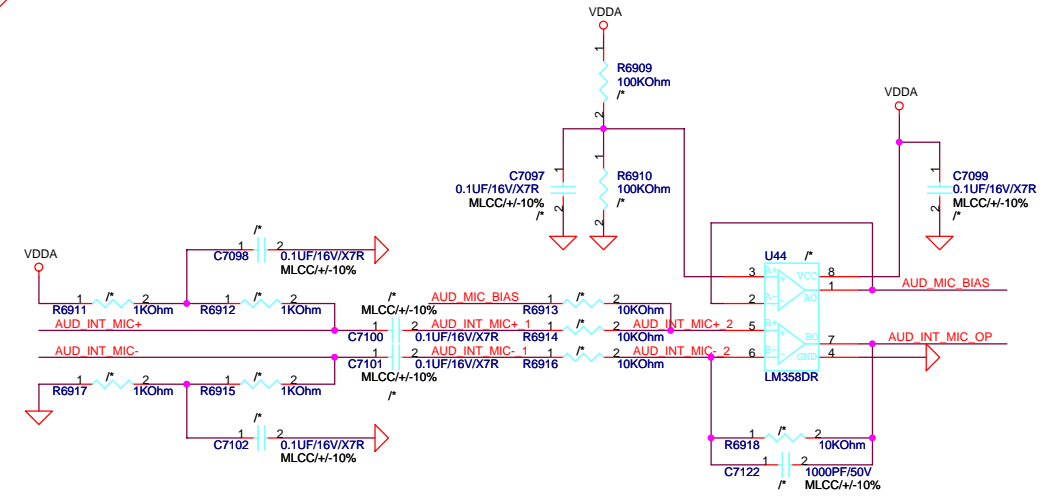
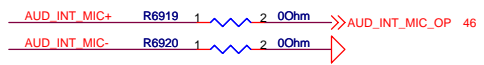
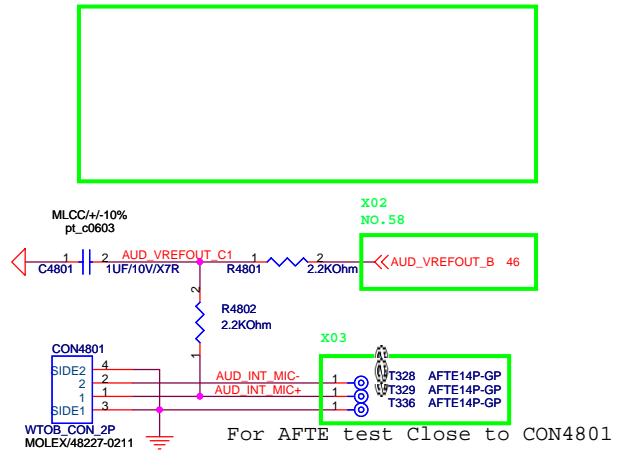
NOTE: MAKE SURE THERMAL PAD
 (Pin21) UNDER MAX4411 IS NOT
 CONNECTED TO GND

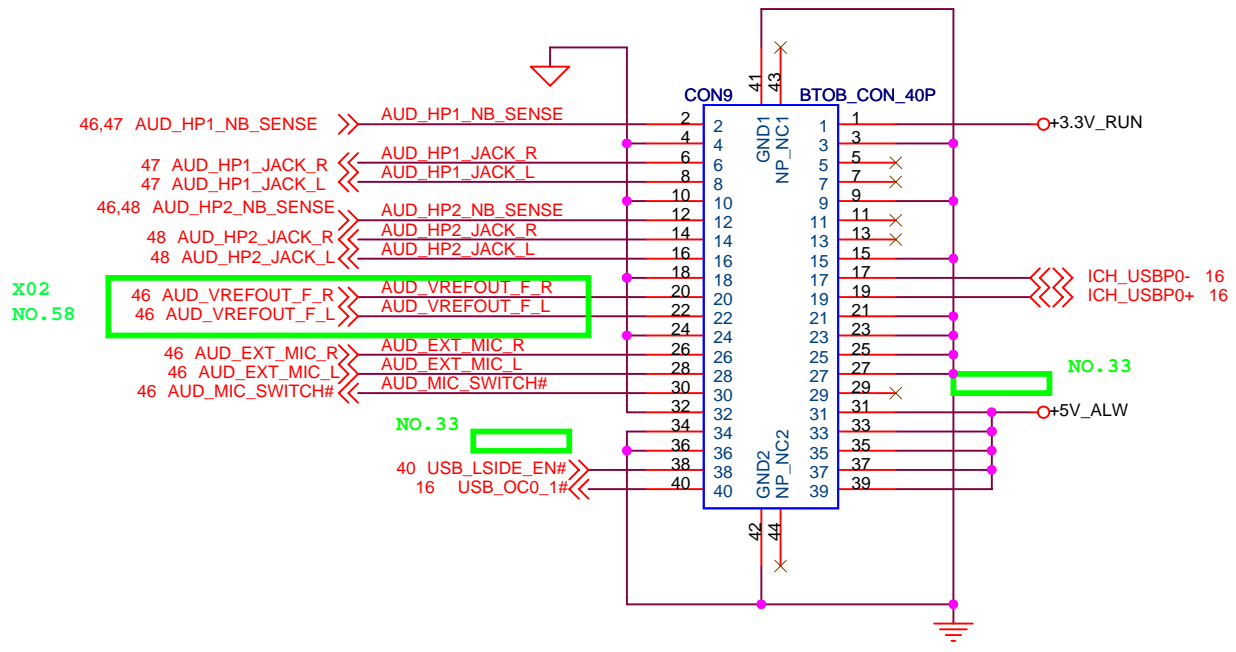
If AUD_EAPD# not be used,
 pop R6932 and depop R6931.


MURATA/BLM18AG601SN1 (J5535)<G>
 Irat=200mA



For AFTE test close to CON07





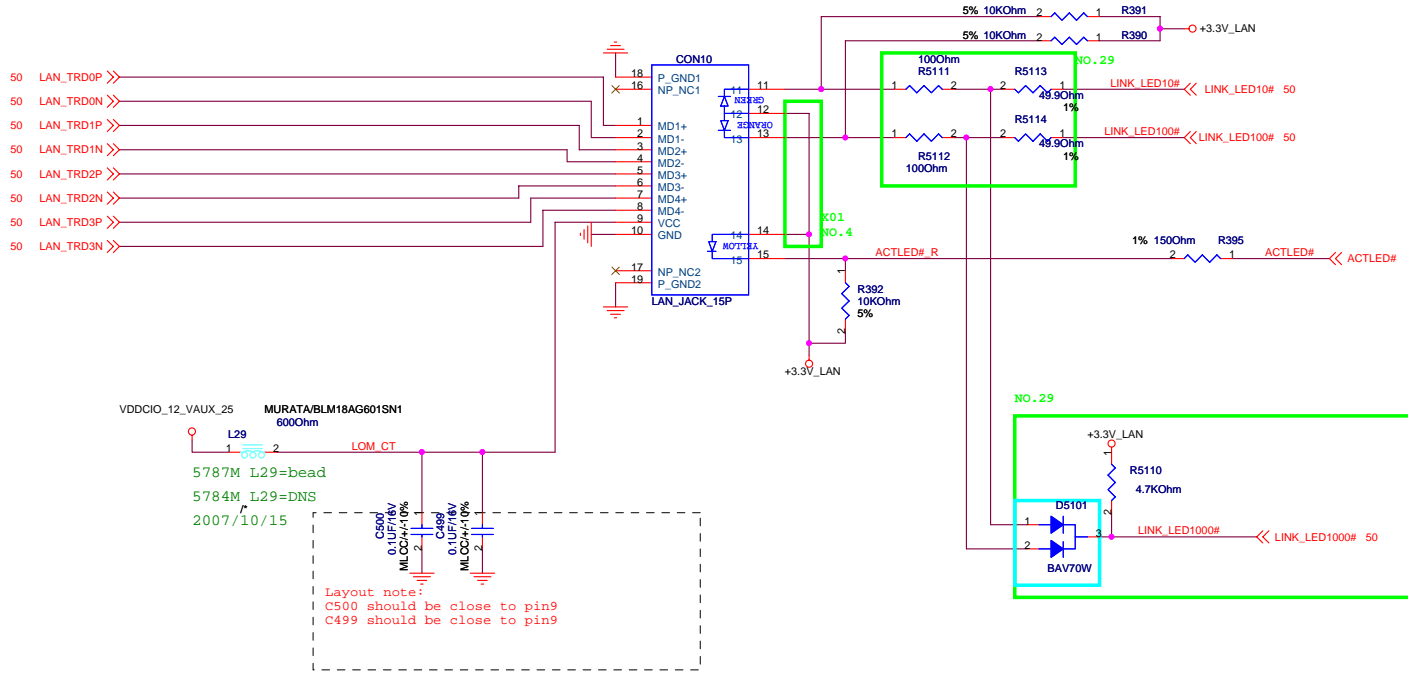
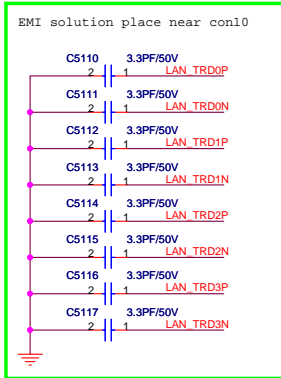
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title <h3 style="text-align: center;">AUDIO BtoB CON</h3>	
Size A4	Document Number Diaz-UMA	Rev A00	Date: Tuesday, August 19, 2008
Sheet 49 of 68		Date: Tuesday, August 19, 2008	

This BOM is 5784M

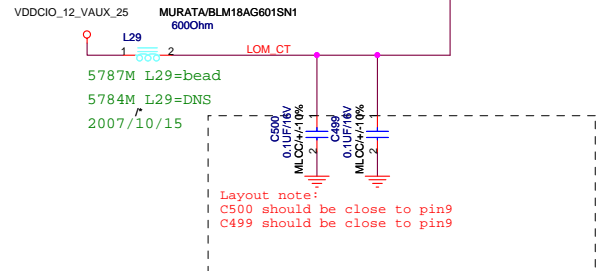
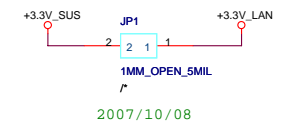
require S3 support wake on LAN 2007/10/05

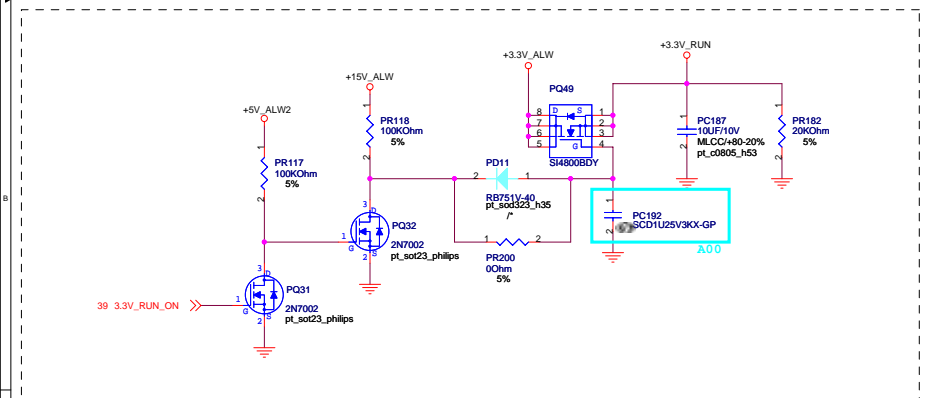
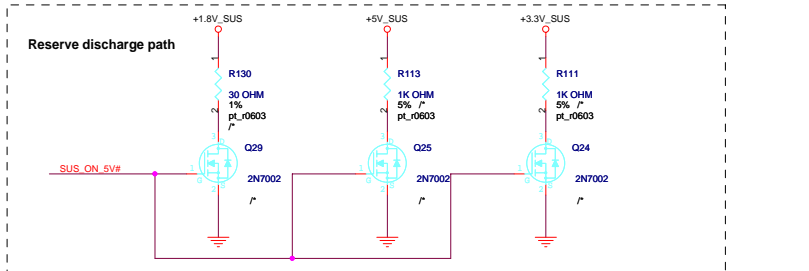
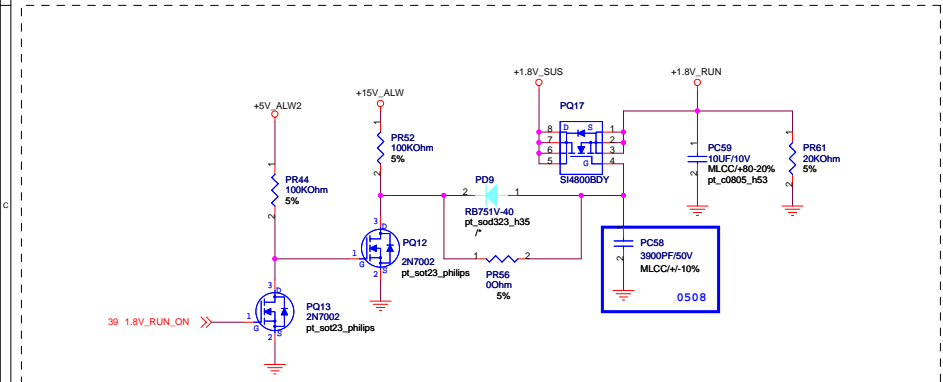
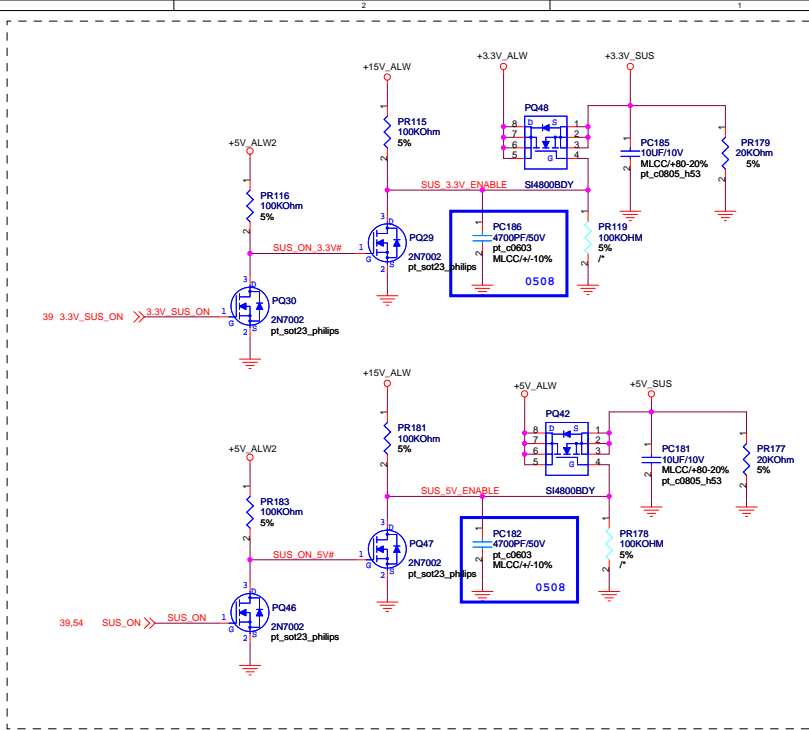
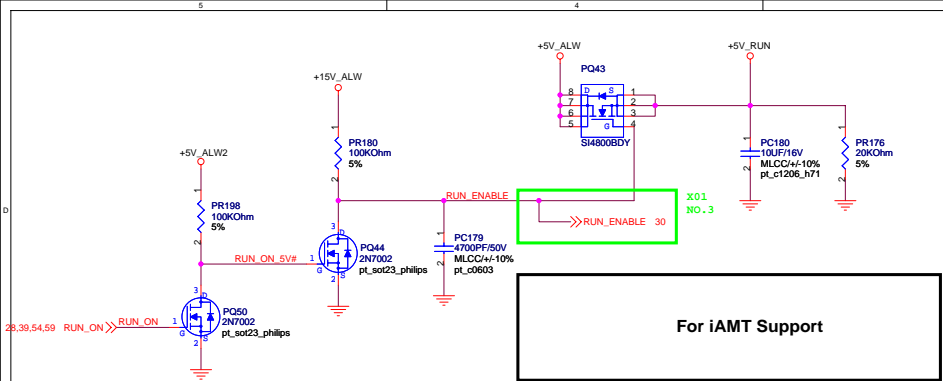
RJ45 should be 12G14801110KDE

NO.29

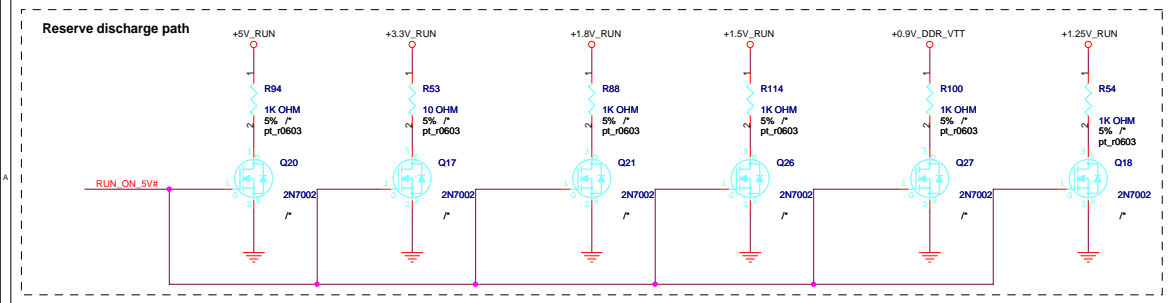


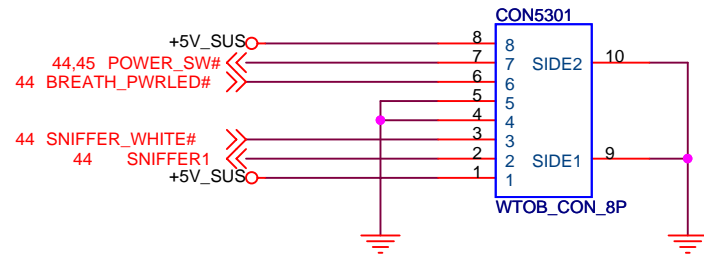
+3.3V_LAN Source Guideline:
 1. Use +3.3V_SUS if Wake-on-LAN is NOT required out of S4, S5
 2. Use +3.3V_SRC if Wake-on-LAN is required out of S4, S5





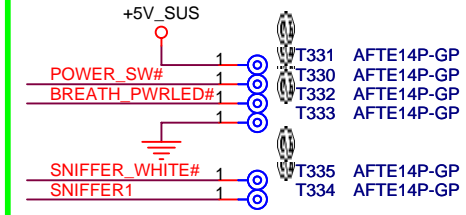
For iAMT Support



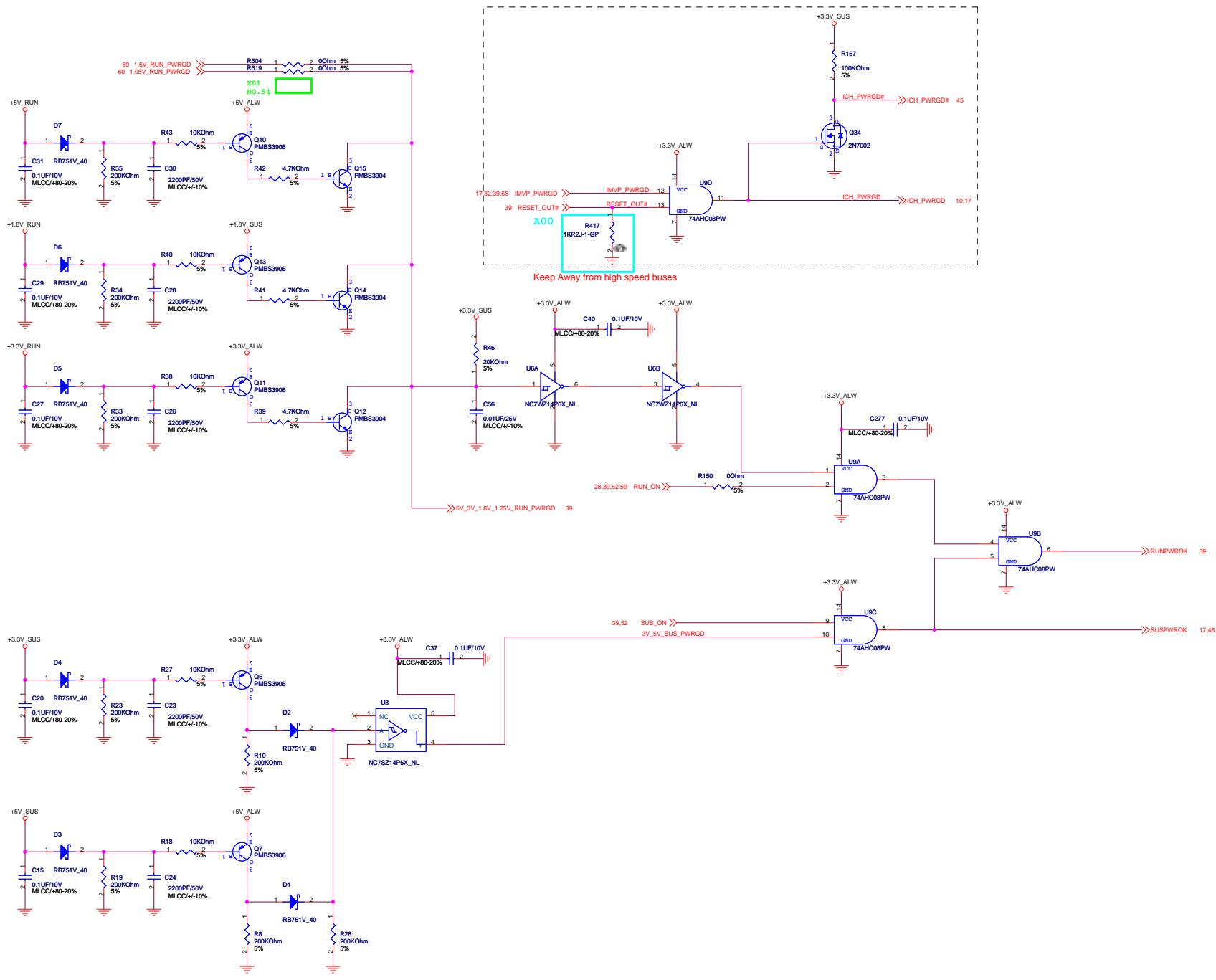


X03

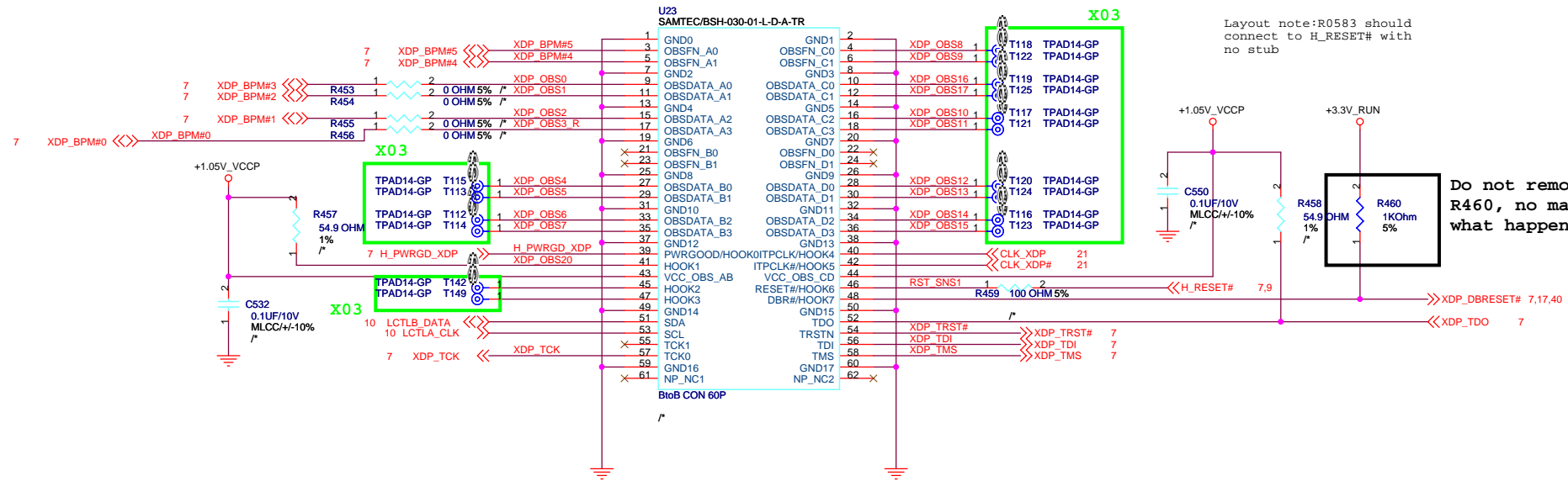
For AFTE test Close to CON5301



DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Power Button Board			
Size A4	Document Number Diaz-UMA	Rev A00	
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XDP



Layout note: R0583 should connect to H_RESET# with no stub

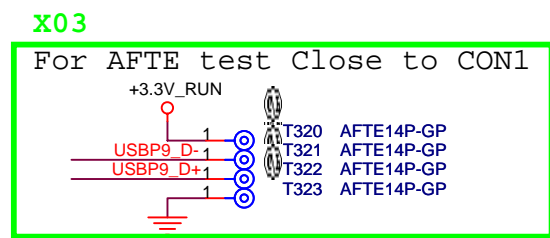
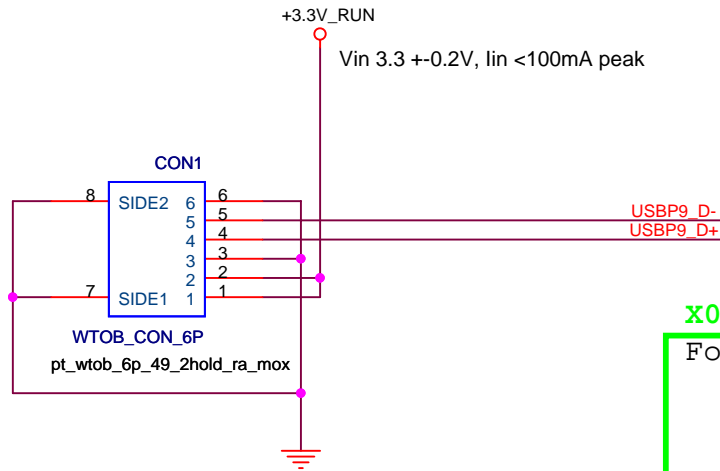
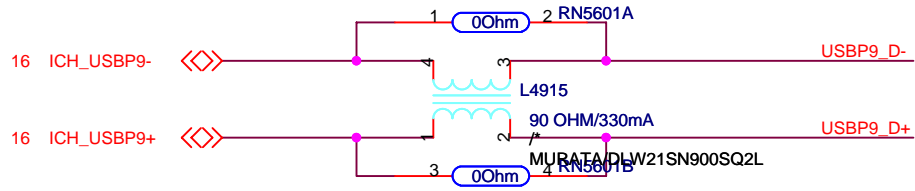
Do not remove R460, no matter what happen.

CAD NOTE:
Place the XDP connector on the primary side of the CRB and place all components near the connector.

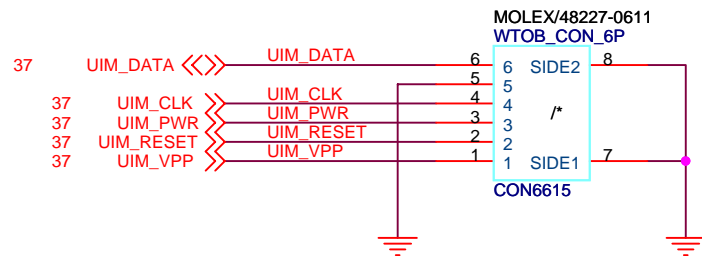


Title		
XDP		
Size	Document Number	Rev
A3	Diaz-UMA	A00
Date:	Tuesday, August 19, 2008	Sheet 55 of 68

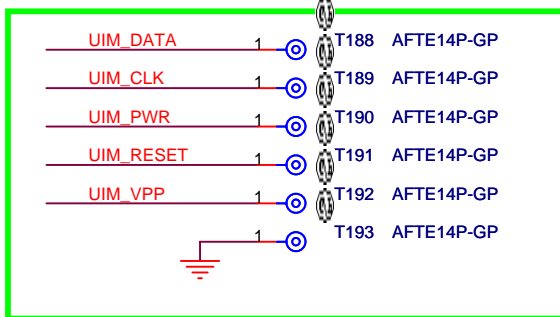
FINGER PRINTER



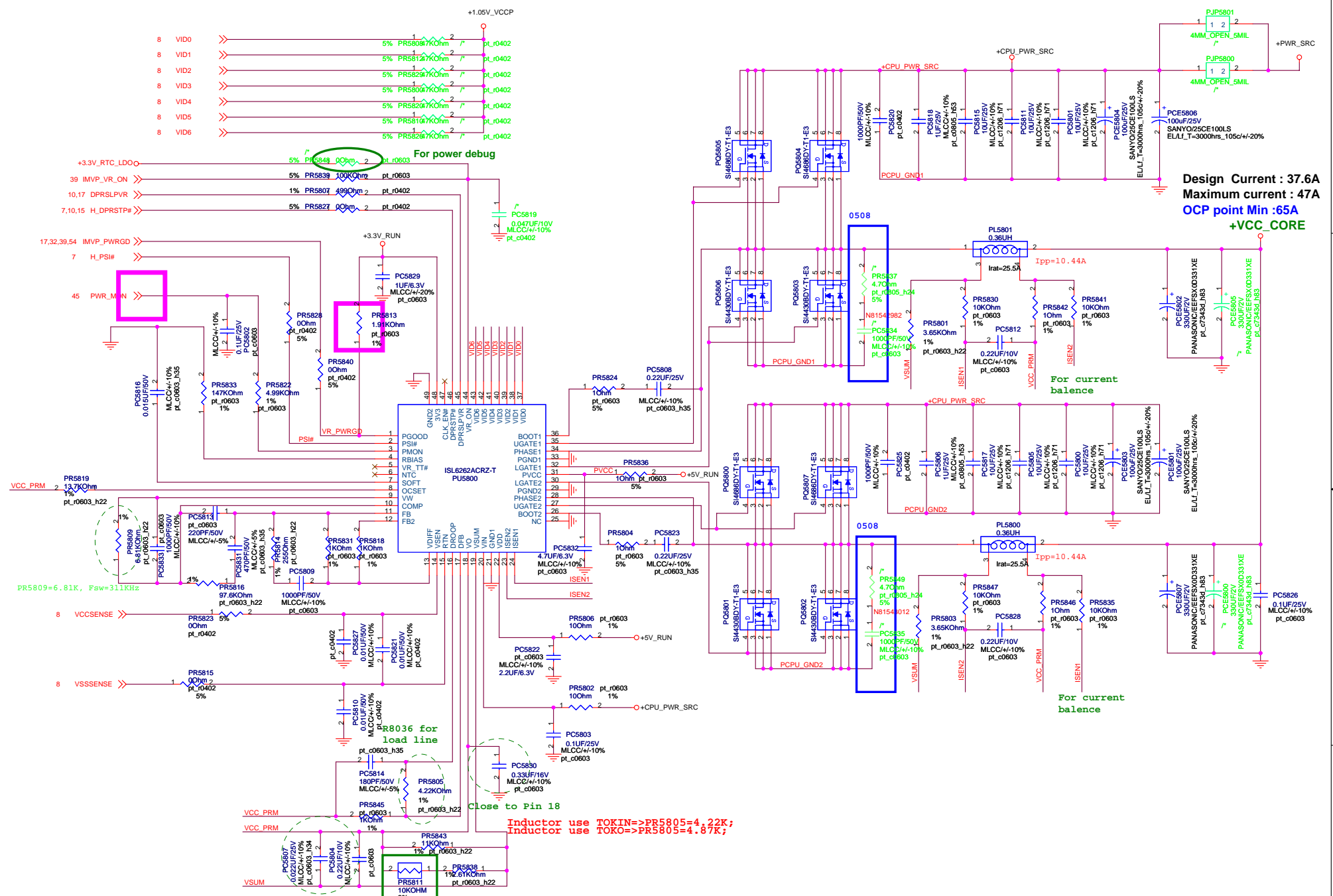
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
FINGER PRINTER Port			
Size	Document Number		Rev
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x03 For AFTE test Close to CON6615



DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
SIM CARD			
Size	Document Number		Rev
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Design Current : 37.6A
 Maximum current : 47A
 OCP point Min : 65A
 +VCC_CORE

Inductor use TOKIN=>PR5805=4.22K;
 Inductor use TOKO=>PR5805=4.87K;

C8021 & C8018 for transient response

Close to Phase 1 Inductor

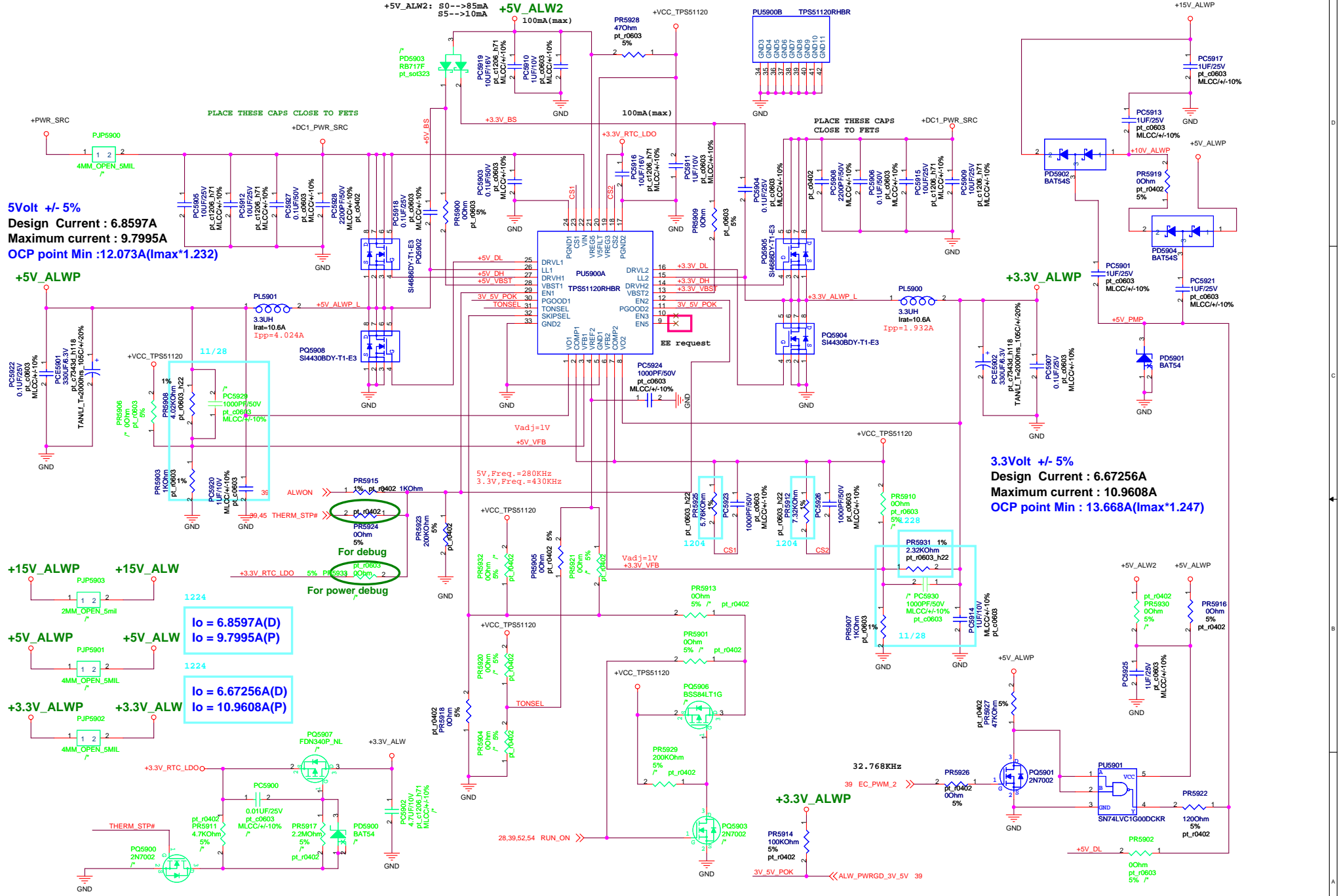
DELL Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
POWER_VCORE		
Title	Document Number	Rev
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5Volt +/- 5%
Design Current : 6.8597A
Maximum current : 9.7995A
OCP point Min :12.073A(I_{max}*1.232)

3.3Volt +/- 5%
Design Current : 6.67256A
Maximum current : 10.9608A
OCP point Min : 13.668A(I_{max}*1.247)

+15V_ALWP
+15V_ALW
+5V_ALWP
+5V_ALW
+3.3V_ALWP
+3.3V_ALW

Io = 6.8597A(D)
Io = 9.7995A(P)
Io = 6.67256A(D)
Io = 10.9608A(P)

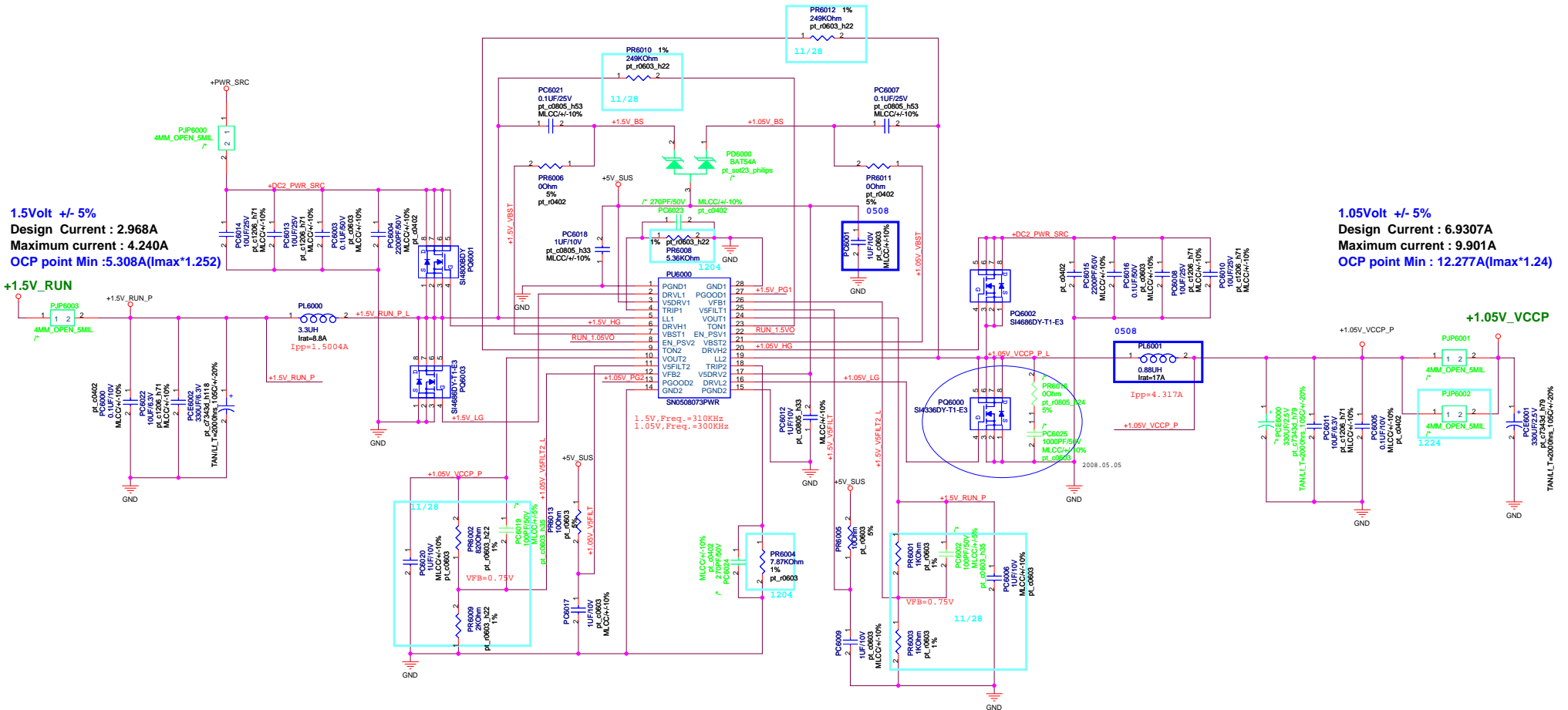


1.5Volt +/- 5%
Design Current : 2.968A
Maximum current : 4.240A
OCP point Min :5.308A(Imax*1.25)

+1.5V_RUN

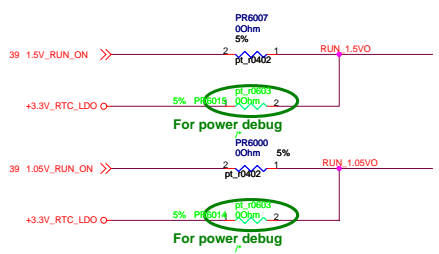
1.05Volt +/- 5%
Design Current : 6.9307A
Maximum current : 9.901A
OCP point Min : 12.277A(Imax*1.24)

+1.05V_VCCP



54 1.5V_RUN_PWRGD << +1.5V_PG1

54 1.05V_RUN_PWRGD << +1.05V_PG2



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 Taipei Hsien 221, Taiwan, R.O.C.

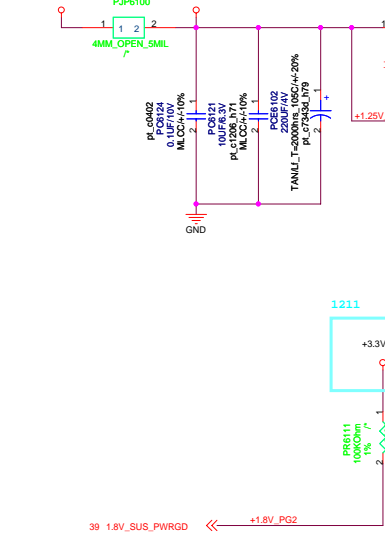
Title: **POWER_I/O_1.5VS & 1.05VS**

Size	Document Number	Rev
Custom	Diaz-UMA	A00

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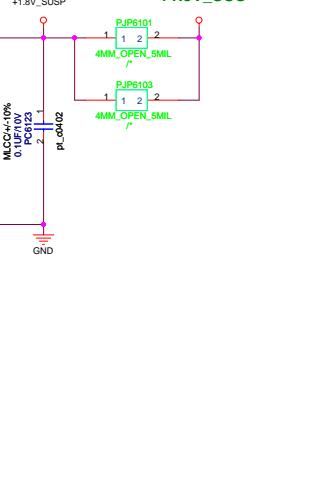
1.25Volt +/- 5%
Design Current : 1.729A
Maximum current : 2.470A
OCp point Min : 3.063A(I_{max}*1.24)

+1.25V_RUN

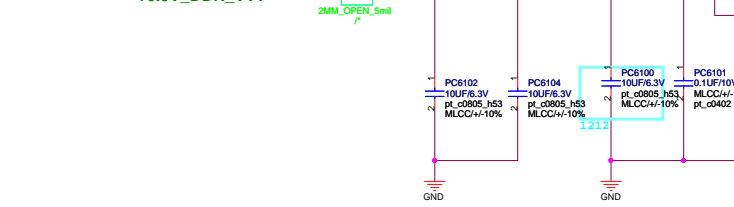


1.8Volt +/- 5%
Design Current : 9.170A
Maximum current : 13.100A
OCp point Min : 16.349A(I_{max}*1.248)

+1.8V_SUS



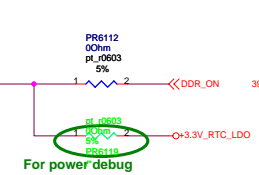
0.9Volt +/- 5%
Design Current : 1.05A
Maximum current : 1.5A
OCp point Min : 3.8A




For debug



For power debug



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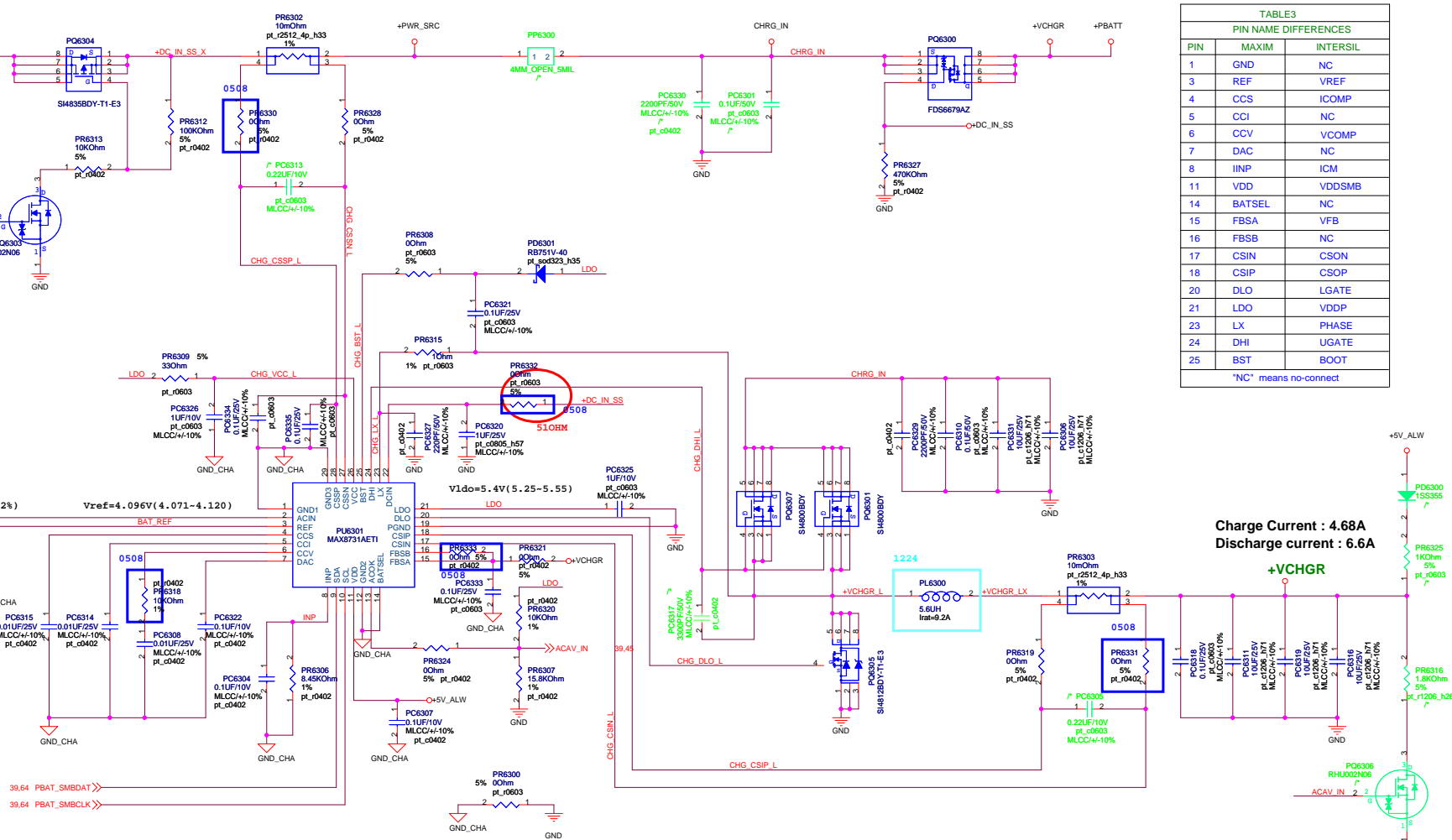
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Title			
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TOTAL POWER=65W
-->3.33A (Vin=19.5V)

TABLE3
PIN NAME DIFFERENCES

PIN	MAXIM	INTERSIL
1	GND	NC
3	REF	VREF
4	CCS	ICOMP
5	CCI	NC
6	CCV	VCOMP
7	DAC	NC
8	IINP	ICM
11	VDD	VDDSMB
14	BATSEL	NC
15	FBSA	VFB
16	FBSB	NC
17	CSIN	CSON
18	CSIP	CSOP
20	DLO	LGATE
21	LDO	VDDP
23	LX	PHASE
24	DHI	UGATE
25	BST	BOOT

"NC" means no-connect



Charge Current : 4.68A
Discharge current : 6.6A

TABLE2
MAXIM & INTERSIL BOM DIFFERENCES

REF DES	MAXIM	INTERSIL
PR6306	8.45K, 0402, 1%	16.0K, 0402, 1%
PC6323	0.01uF	No Stuff
PC6304	0.1uF, 0402, 10V	No Stuff
PC6300	1.0uF, 0603, 10V	No Stuff
PR6329	365K, 0402, 1%	215K, 0402, 1%
PR6319	0, 0402, 5%	10, 0402, 5%
PR6328	0, 0402, 5%	10, 0402, 5%
PC6305	No Stuff	0.22uF
PC6313	No Stuff	0.22uF
PC6314	0.01uF	No Stuff
PC6322	0.1uF, 0402, 10V	No Stuff
PC6327	220pF, 0402, 50V	No Stuff
PD6301	RB751V-40	No Stuff
PC6317	3.3nF	No Stuff
PR6315	1, 0603, 1%	0, 0603, 5%
PR6321	100, 0402, 5%	0, 0402, 5%
PR6318	10K, 0402, 5%	4.7K, 0402, 5%
PC6308	0.01uF	0.01uF
PC6315	0.01uF	0.01uF
PD6300	1SS355	No stuff
PR6325	1K, 0603, 5%	No stuff

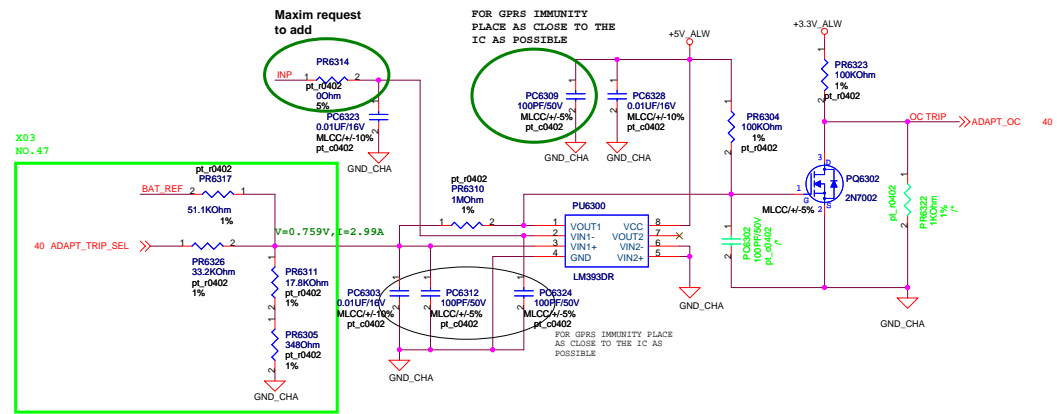
TABLE1

ADAPTOR (W)	TRIP CURRENT (A)	PR6311	PR6305	PR6326
65	3.17	57.6K	13.0K	105
90	4.43	51.1K	17.8K	348
130	6.43	32.4K	20.5K	100
150	7.43	30.9K	24.9K	432
200	9.75	19.1K	28K	301
230	11.28	32.4K	6.49K	115

Note 1: PR6326 is populated if ADAPT_TRIP_SET is used to program for the next lower adaptor. ADAPT_TRIP_SET is floating for the higher adaptor, grounded for the lower adaptor.

Note 2: 24.9K at PR6326 allows the 65W adaptor setting to switch down to 45W. (now is 33.2K for 90W)

Note 3: PR6302 must be 5m ohm instead of 10m ohm for the 230W adaptor



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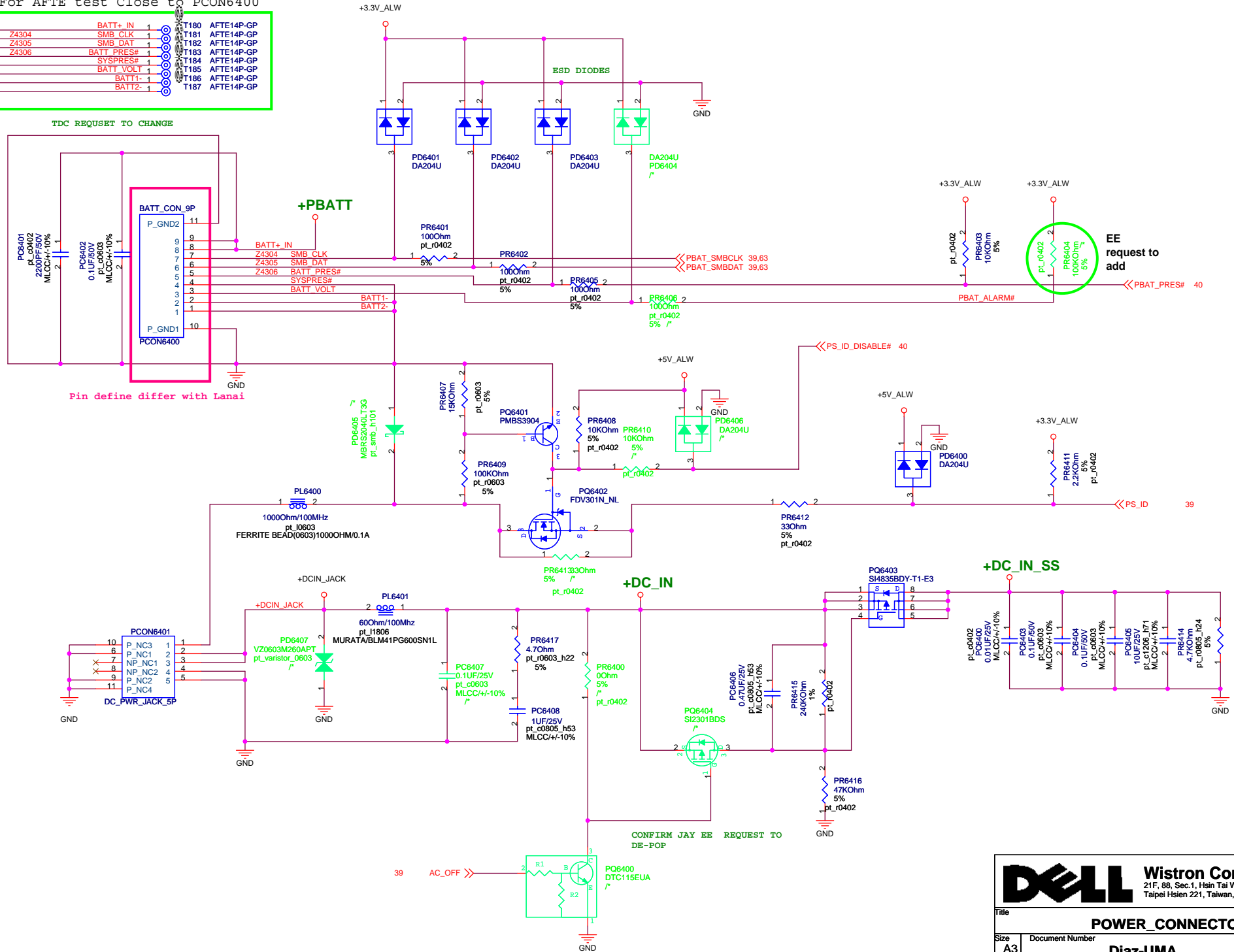
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Size: C Document Number: **Diaz-UMA** Rev: **A00**

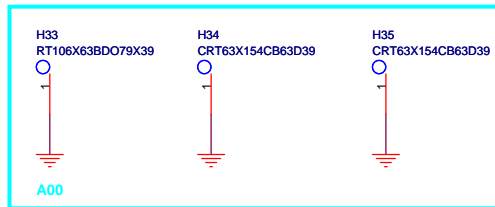
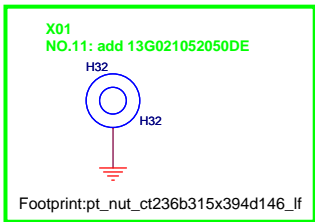
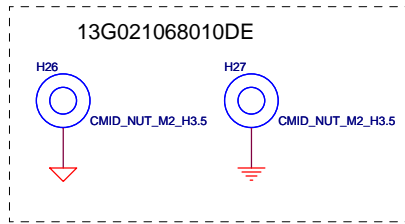
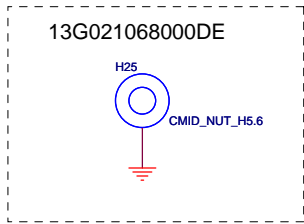
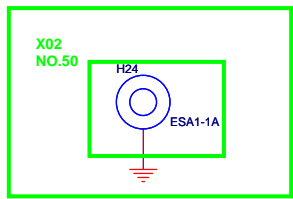
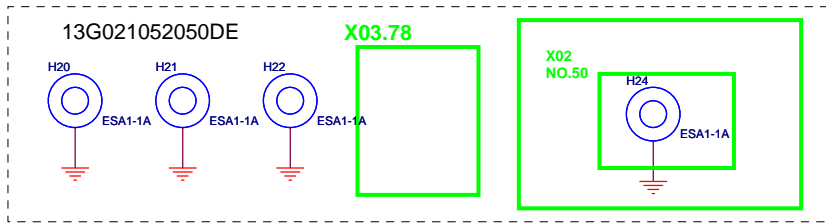
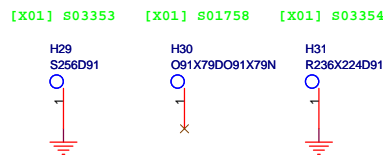
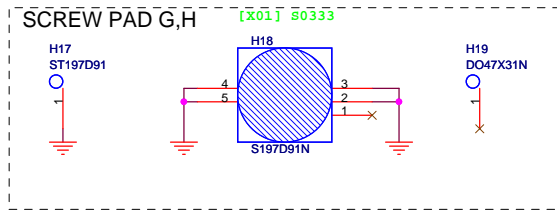
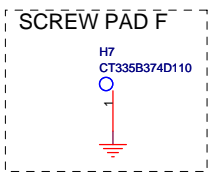
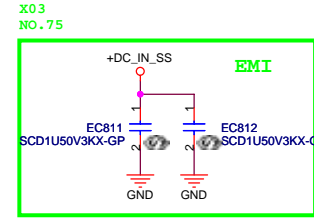
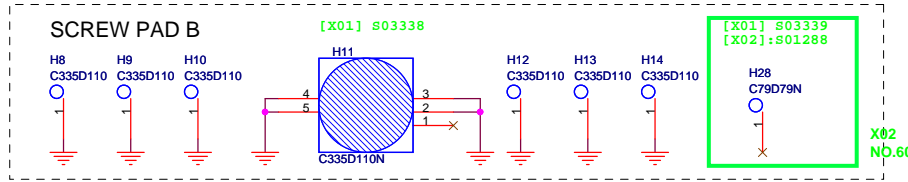
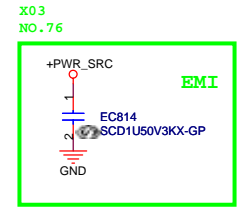
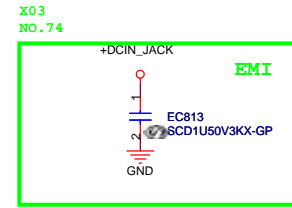
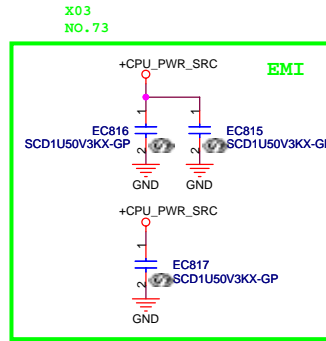
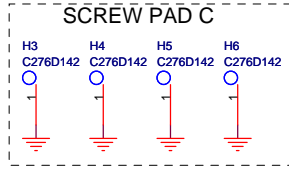
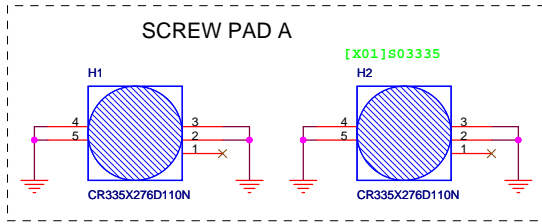
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x03 For AFTE test Close to PCON6400

Z4304	BATT+ IN	1	T180	AFTE14P-GP
Z4305	SMB_CLK	1	T181	AFTE14P-GP
Z4305	SMB_DAT	1	T182	AFTE14P-GP
Z4306	BATT_PRES#	1	T183	AFTE14P-GP
	SYSPRES#	1	T184	AFTE14P-GP
	BATT_VOLT	1	T185	AFTE14P-GP
	BATT1-	1	T186	AFTE14P-GP
	BATT2-	1	T187	AFTE14P-GP



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Item	Page	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	all	X00 release	10/24/2007		X00 release		X00
2	44	Switch power pull	11/30/2007	AA EE	Change main power switch and sniffer power switch power plane to +3.3V_RTC_LDO	Change +RTC_SELL to +3.3V_RTC_LDO	X01
3	30	HDMI power	11/30/2007	AA EE	Modify power diode to MOSFET for leakage current that can lower forward voltage and match HDMI 5V voltage range	Replace D4612 by Q19 and connect Q19 gate to RUN_ENABLE	X01
4	51	LAN LED	11/30/2007	AA EE	Changed LAN Jack (CON10) pin12 to +3.3V_LAN	Changed LAN Jack (CON10) pin12 to +3.3V_LAN	X01
5	35	Express card power switch	11/30/2007	AA EE	Express Card power switch (U13) pin4 should be connected to +3.3V_RUN for the purpose of using RICOH/R5538 as 2nd source	Connect U13 pin4 to +3.3V_RUN	X01
6	18	ICH8	11/30/2007	AA EE	ICH8 pin AD11 VCCSUSDA modify to +3.3V_ALW for +3.3V_RUN to solve S5 leakage issue	Connect ICH8 pin AD11 to +3.3V_ALW	X01
7	A1,A2	Audio Board	11/30/2007	AA EE	1.AH1change to NPTH;2.ACON5 change to 12G142001113DE; 3.AU3 pin1 rename to USBP0_D+;4.AU3 pin3 rename to USBP0_D-_U	1.AH1change to NPTH;2.ACON5 change to 12G142001113DE; 3.AU3 pin1 rename to USBP0_D+;4.AU3 pin3 rename to USBP0_D-_U	X01
8	15,44	LED mask circuit	12/05/2007	AA EE	1.Delete sniffer LED mask circuit 2.modify SATA and WPAN LED circuit.	1.Delete R246,R247,Q43 2.modify SATA and WPAN LED circuit	X01
9	17	CLK_ICH_48M	12/06/2007	AA EE	To improve 48MHz clock signal integrity , pop R339, change C456 to 10pF from 4.7pF and make it stuff.	Pop R339, change C456 to 10pF from 4.7pF and make it stuff. change C6649-C6654 to 10pF.	X01
10	29	CRT signals	12/06/2007	AA EE	Fine tune CRT signals	change C6649-C6654 to 10pF.	X01
11	65	Screw Hole	12/06/2007	AA EE	Added screw hole by NB thermal solution & ME request	Added H32, changed H24	X01
12	16,35,50	Reset signals	12/06/2007	AA EE	To improve RESET signals integrity	1. Audio ICH_AZ_CODEB_RST#, R270=100 ohm 2. HDMI:ICH_AZ_HDMI_RST#, R205=100ohm 3. RICOH:PCI_RST#, R1601=100 ohm, add C6663=10pF 4. WLAN:PLTRST#, add C696=22pF 5. WWAN:PLTRST#, add C697=22pF 6. EC:PLTRST#, add R6972=220ohm	X01
13	28	LCB_VCC	12/06/2007	AA EE	Fine tune LVDS power sequence TI time	Change R17 to 470K ohm from 330K ohm	X01
14	21	PCF clock	12/10/2007	AA EE	Fine tune PCF clock slew rate by EA	Swap net name: CLK_PCF_PCCARD & CLK_PCF_8512	X01
15	39	EC power	12/10/2007	AA EE	update EC pin12 net by vender request changed list for batter quality.	Added C3901=0.1uF, C3902=1uF, R3907=0 ohm	X01
16	21,28,40	EMI component	12/10/2007	AA EE	modify component by EMI Comm Team request.	P21: add C2107, C115, C159, C172, C194 P28: add C7110-7111, C7113, C7112 (33pF), C7114(33pF) P28: remove R2804A/B, add L1 P40: add CN21, CN22, CN23, CN24, CN25, CN26, CN28	X01
17	40	Platform ID	12/10/2007	AA EE	add platform indicator circuit	add R4025-28, net name: PLATFORM_ID[0:1]	X01
18	54	Power Sequence	12/10/2007	AA EE	Flow power circuit.	Remove R73 & net name: 1.25V_RUN_PWRGD	X01
19	40,43	Connector	12/10/2007	AA EE	Changed Connector by ME request.	page 40 -> change CON4010 page 43 -> change CON3	X01
20	C1	CAPBTN I2C	12/12/2007	AA EE	Fine tune CAPBTN I2C timing.	1.Change I2C damping R (CBT_R795) from 330ohm to 100ohm 2.Add through holes CBT_H15(s01291) & CBT_H28(s03350)	X01
21	F1	FingerPrinter LDO	12/12/2007	AA EE	Fine tune LDO performance.	1.F_U3, Pin3(Cb pin) connects with Pin1(Vin) 2.F_U3, Pin4(ECO pin) connects with Pin1(Vin)	X01
22	S1	SIM Screw Hole	12/12/2007	AA EE	ME update DXF	change screw hole SH2 & SH3 & SCON1	
23	28	Digital MIC	12/13/2007	AA EE	DMIC clock EMI solution modify	1.R2802 change to 80ohm bead(follow Lanai P/N) 2.R2803 change to 47ohm 3.Mount C748 (33P)	
24	A2	Audio Board	12/14/2007	AA EE	Update eSATA connector for USB function only.	changed ACON5 = 12G142001115DE	
25	39	IT8512E	12/15/2007	AA EE	Del C3921 (IT8512E I version pop 0ohm, J version pop 0.1uF)	Del C3921	
26	40	Platform ID	12/15/2007	AA EE	Del R4025,R4027 to force PCB platform type (Intel SR)	Del R4025,R4027	
27	21,33,39,50	XTAL	12/15/2007	AA EE	Change XTAL for better capability	(1) X4 24.576MHz change to 07G010222452DE,C453 change to 22pF,C454 change to 22pF (2) X1 25MHz change to 07G010222509DE, C47,C55 change to 33pF (3) X2 14.318MHz change to 07G01021143CDE , (4) X5 32.768KHz change to 07G01020327ADE, change C667,C654 to 15pF	
28	46-48	Audio	12/18/2007	AA EE	Modify Audio BOM	1.Unmount R4602 2.Mount R4601,Q123,R6958 3.Delete R6964,R6965,R6960,R6961,R6970,R6962,R6963,R6971 4.Add R4701,R4702,R4703,R4704,C4701,C4702	
29	50-51	LAN	12/18/2007	AA EE	Modify schematic for triple LED control & EMI solution	1.Add R5110-R5114,D5101; del T5004, add LINK_LED1000# 2.Add C5110-C5117	
30	45,47	Test Point	12/18/2007	AA EE	Add test point for factory ICT team request	Add T33 in U19.23 & T34 in U8.26	
31	41	SPI Flash	12/18/2007	AA EE	Remove SPI Flash dymp RES.	Remove R310, R316, R317, R4102	

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32	31	HDD/ODD Power	2007/12/18	AA EE	Modify HDD/ODD power circuit by customer request	1.unmount JP4, R3101 2.POP BOM: R5, R7, R399, R400, C13, Q2, Q3, Q56	X01
33	49, A1 A2	USB charged	2007/12/19	AA EE	Remove USB charged circuit by customer request	1.Delete AU2 2.rename USBP0_D_U & USBP0_D+U to USBP0_D- & USBP0_D+ 3.connect CON9, ACON1 pin36 to DGND, pin29 NC.	X01
34	39, 41 45, 50	Test Point	2007/12/19	AA EE	Add test point by ICT factory request	1.Add T151, T152, T159, T166, T178, T179 for U27 signal pin 2.Add T222, T219, T220, T221 for U2 signal pin 3.Add T148 at U15 pin14, T150 at U8 pin3	X01
35	A2	Audio Board	2007/12/20	AA EE	Modify USB differential signals.	1.Delete AL7 2.rename USBP0_D+ & USBP0_D- to AICH_USBPF0+3 & AICH_USBPF0-	X01
36	44	WPAN LED	2007/12/21	AA EE	Pop BOM for WPAN LED support	POP BOM: R4411(100K Ohm)	X01
37	65	Screw Hole	2007/12/25	AA EE	add screw hole for IR Blockade	Add: H32, H33	X01
38	C1	CAPBTN	2007/12/25	AA EE	update CAPBTN Circuit by customer ID modified	Swap net SNS_REWIND & SNS_PLAY, LED_REWIND# & LED_PLAY#	X01
39	F1	FingerPrint Screw	2007/12/25	AA EE	Screw hole (NPTH) modified the internal diameter to 1.7mm and the external diameter to 3mm	Modify F_H1, F_H2	X01
40	17	WPAN CTRL	2007/12/26	AA EE	Modify WPAN detect signals by different WLAN module support.	changed net USB_WPAN_DET# to R1701 & pull up to +3.3V_RUN	X01
41	13, 38	Cost Down Plan	2007/12/27	AA EE	Cost Down Plan	CE1303, CE1301 => Change to POSCAP 220U/4V De-pop => C602, C589, C590, C1302, C1312, CE7 C363 => Change 10uF/10V Y5V C1309 => Pop 0.1uF R1301 => Change to 0 ohm De-pop => CE16	X01
42	30, 42	Connector	2007/12/28	AA EE	By ME connector changed list	Changed CON6610 = 12G13141108ADE Changed CON6608 = 12G24110193RDE	X01
43	40	Board ID	2008/02/14	AA EE	Changed pcb id to X02	Changed pcb id to X02	X02
44	15	XTAL	2008/02/14	AA EE	Modify C375, C377 per XTAL report	Change C375, C377 to 3.3pF	X02
45	16	ICHB reset signal	2008/02/14	AA EE	U14, U30, U37: power modify to +3.3V_ALW from +3.3V_RUN	U14, U30, U37: power modify to +3.3V_ALW from +3.3V_RUN	X02
46	41, C1	CapBTN	2008/02/14	AA EE	Add CapBTN IC reset signal	1. Add CBT_RESET pin, add two jumpers on the CapBtN board. 2. Sense pad modify to elliptic through hole 3. Add a reserved 10uF capacitor parallel to +5V_ALW2 on the CapBtN board	X02
47	30, 37	Comm. team solution	2008/02/14	AA Comm. Team	Add comm. team solutions	1.Pop L4606, depop RN3701 by comm. Team request 2.CMIU: Add C3051 39PF close to C6925	X02
48	47, A1	Audio	2008/02/14	AA EE	Modify ACON2, ACON3, ACON4 footprint. Change value of C492, C496 to improve AP performance	1.ACON4 PCB footprint change to pt_phone_j_6p_4hd_col_lf 2.ACON3, ACON2 footprint change to pt_phone_j_6p_4h_col_lf 3.C492 and C496 Bom change to 2.2U(11G236122511310DE) from 1uF	X02
49	21	Clock	2008/02/18	AA EE	Delete reserved resistors	Delete RN1, RN2, RN3, RN5, RN6, RN7, RN8, RN9, RN10, RN11	X02
50	65	Nut	2008/02/18	AA ME	Swap FN of H23, H24 base on updated DXF	Swap FN of H23, H24	X02
51	C1	CAPBTN	2008/02/19	AA EE	LED Mute/VD/VU of power rail update	LED Mute/VD/VU are connect to +5V_ALW2 power rail	X02
52	39	EC	2008/02/19	AA EE	Support CAPBTN reset signals.	modify net_name U15.I09: CAP_EC_RESET, Delete: R3907	X02
53	F1	Finger Print	2008/02/19	AA EE	update F_X1 footprint	update F_X1 footprint: modify pin1 indication	X02
54	C1	CAPBTN	2008/02/19	AA EE	Modify level shift circuit & Hole	1.Add elliptic through holes for BT, WiFi, and HDD LEDs 2.Change CBT_C1 to PT footprint	X02
55	39	EC	2008/02/19	AA EE	Modify Chip version.	update Chip version: 06G042005012DE, option R3920, mount C3920	X02
56	47	Speaker gain	2008/02/21	AA EE	Fine tune gain	1.Unmount R374, R377 and Mount R379, R368 2.R4701, R4703 change 24.3Kohm and R4702, R4704 mount 100Kohm Add F_T14 Test Point	X02
57	F1	Finger Print	2008/02/22	AA EE	Add Test Point by Factory Request	Add F_T14 Test Point	X02
58	46	Audio	2008/02/22	AA EE	Modify Audio solve pop issue	Modify Audio Circuit	X02
59	44	Switch LED	2008/02/25	AA EE	Modify LED Color by customer request	LED1 changed to 07G01520097SDE, WHITE&ORANGE	X02
60	60, 61	POWER	2008/05/7	W EE	PL6001 12.4A change to 17A ; PL6101 14.3A change to 17A; Add PC6001(1u/10V)	Modify power Circuit	X02
61	58	POWER	2008/05/7	W EE	PR5817 change location to PR5837(4.7K 0805); PC5824 change location to PC5834(1000PF/50V); PR5821 change location to PR5849(4.7R 0805); PC5834 change location to PR5835(1000PF/50V);	Modify power Circuit	X02
62	61	POWER	2008/05/7	W EE	PU6101 Pin6, PIN7 swap	Modify power Circuit	X02
63	60	POWER	2008/05/7	W EE	PQ6004(SI4430BDY) change location to PQ6000 (SI4336BY) add PR6016(DY)0R 0805; PC6025(DY) 1000PF/50V;	Modify power Circuit	X02
64	60	POWER	2008/05/7	W EE	POP FC182, POP FC186; PC58 change to 3900pF	Modify power SW Circuit	X02
65	61	POWER	2008/05/7	W EE	POP PR6330(0R), POP PR6332(0R), POP PR6318(10K), POP PR6333(0R), PR6331(0R)	Modify power Circuit	X02
66		POWER	2008/05/7	W EE	D21 GM M/B Close GAP (J2, J3, PJP5800, PJP5801, PJP5900, PJP5901, PJP5902, PJP5903, PJP5903, PJP6000, PJP6001, PJP6002, PJP6003, PJP6100, PJP6101, PJP6102, PJP6103, PJP6104, PJP6105, PJP6200, PJP6201, PJP6202, PJP6203, PP6300) D21 GM CAPBTN Board Close GAP(CBT_JP1, CBT_JP2) D21 GM Audio Board Close GAP(AJ1)	Close power GAP	X02
67	29	CRT	2008/05/16	W EE	Q2901, Q2902 "BSS138N" change to "2N7002"	change part X02	X02



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68	60,61	POWER	2008/06/30	W EE	PR6004 change to 7.87Kohm;PR6100 change to 249Kohm;PR6116 change to 5.1Kohm	change part	X03
69	40	Board ID	2008/06/30	W EE	Board ID change to X03=> R534"Dummy"/POP "R535"	change PCB ID	X03
70	L1	Lid Board	2008/06/30	W EE	Lid Board: add HALL1 connect "20.P0866.003"	change part	X03
71	A2	Audio Board	2008/06/30	W EE	Audio Board:ACON5 change to "PN:12G142001115DE" waiting wistron P/N	change part	X03
72	66-74	I/O Board	2008/07/04	W EE	I/O board schematic remove	Independence I/O board shecmatic for layout ME issue	X03
73	65	For EMI	2008/07/04	W EMI	For EMI :+CFU_PWR_SRC add EC816,EC815,EC817 0.1u/50V EMI CAP	EMI solution	X03
74	65	For EMI	2008/07/04	W EMI	For EMI :+DCIN_JACK add EC813 0.1u/50V EMI CAP	EMI solution	X03
75	65	For EMI	2008/07/04	W EMI	For EMI :+DC_IN_SS add EC811,EC812 0.1u/50V EMI CAP	EMI solution	X03
76	65	For EMI	2008/07/04	W EMI	For EMI :+PWR_SRC add EC814 0.1u/50V EMI CAP	EMI solution	X03
77	37	SIM CARD	2008/07/04	W EE	For SI : UIM_CLK add R6634 OR	For SI	X03
78	65	HOLD	2008/07/07	W ME	Cost down remove H23	remove part	X03
79		For ATE	2008/07/07	W ME	all test point change to "ZZ.PAD14.001" page 7 test point T31,42 change to "ZZ.PAD14.001" page 10 test point T127,T27,T29,T28,T126,T18,T19,T21,T25,T23,T35,T37,T40,T38,T39,T36,T20,T24,T22,T26,T41,T137,T32,T135,T128,T130,T131,T30,T1002,T1001 page 11 test point T134,T136 page 15 test point T92,T91,T93,T84,T85,T80,T90,T143,T54,T96,T71,T82,T53 page 16 test point T74,T175,T77,T89,T214,T95 page 17 test point T45,T74,T56,T139,T158,T157,T177,T176,T210,T144,T156,T49,T147,T146,T48,T47,T140,T41,T46 page 18 test point T61,T67,T70,T72,T52,T51,T73 page 32 test point T55 page 33 test point T153 page 36 test point T160,T161,T162,T163,T164,T165 page 37 test point T168,T169,T170 page 38 test point T167 page 39 test point T148,T390,T3902,T3905,T3906,T3907,T3909,T3910,T3903,T3904 page 40 test point T4001,T4005 page 41 test point T178,T179,T159,T166,T151,T152,T154 page 45 test point T33,T17,T16,T150,T13 page 50 test point T222,T219,T220,T221,T5002,T5003 page 55 test point T118,T122,T119,T125,T117,T121,T120,T124,T116,T123,T115,T113,T112,T114,T142,T149	New ATE test point change to 14 mils	X03
80		For AFTE	2008/07/07	W ME	Add AFTE test point "ZZ.AFT14.101" Page29 add AFTE test point T311,T312,T313,T314,T315,T316,T317,T318,T171,T172 Page 40 add AFTE test point T500-T529 "ZZ.AFT14.101" for Con5&CON4010 Page 42 add AFTE test point T356-T361 "ZZ.AFT14.101" for Con6610 Page 43 add AFTE test point T347,T348,T349,T350 "ZZ.AFT14.101" for Con663 Page 43 add AFTE test point T351,T352,T353 "ZZ.AFT14.101" for Con6617 Page 44 add AFTE test point T345-T346 "ZZ.AFT14.101" for Con6614 Page 45 add AFTE test point T341,T342,T343 "ZZ.AFT14.101" for Con11 Page 48 add AFTE test point T328,T329,T336 "ZZ.AFT14.101" for Con4801 Page 48 add AFTE test point T337,T338,T339,T340 change to "ZZ.AFT14.101" for Con7 Page 48 add AFTE test point T331,T330,T332,T333,T335,T334 "ZZ.AFT14.101" for Con5301 Page 56 add AFTE test point T320,T321,T322,T323 "ZZ.AFT14.101" for Con1 Page 57 add AFTE test point T188,T189,T190,T191,T192,T193 "ZZ.AFT14.101" for Con6615 Page 64 add AFTE test point T180-T187 "ZZ.AFT14.101" for PCon6400	New AFTE test point change to 14 mils	X03
81	18	Board ID	2008/07/07	W ME	Page 18 L49 change to "68.1R090.10A" ;	change bead dimension	X03
82	29	For ME	2008/07/07	W ME	page 29 con8607 change to wisntron P/N "20.20768.015"	ME modify PCB foot pin	X03
83	29	For SI	2008/07/07	W ME	Page29 L4909,L4910,L4911 CHANGE TO "68.00143.111" BLM18BA220SN1D-GP L4610,L4611 change to "63.R0033.L03" OR DUMMY C6649,C6650;C6651;C6652;C6653;C6654	For SI issue	X03
84	31	For EE	2008/07/07	W ME	Page 31 remove J4 power GAP	Sparate HBD and ODD powe plane	X03
85	40	Board id	2008/07/07	W ME	page 40 add R538 (DY),R539 (DY) connect to U29 Pin43 "BID2" for next stage board ID	for board id	X03
86	65	For ME	2008/07/07	W ME	PAGE 65 REMOVE H33,H34	IR trace issue	X03
87	15	For SI	2008/07/07	W ME	page 15 change R275 to "47R"64.47R05.6DL" for ICH_A2_CODEC_SDOUT	For SI issue	X03
88	39	For SI	2008/07/08	W ME	R308,R308 change to 4.7K R	For SI issue	X03
89	65	For ME	2008/08/01	W ME	Page 65 H33,H34,H35 for IR Hold	IR HOLD change	A00
90	33	For SI	2008/08/01	W EE	Page 33 R545 change to 33R	For R5C833 SI Singel	A00
91	30	For SI	2008/08/01	W EE	Page 30 R3002 change to 820R	for HDMI singel	A00
92	52	For Boot	2008/08/01	W EE	Page 52 PCI92 change to 0.1u	Drop	A00
93	40	For KB detect	2008/08/01	W EE	Page 40 add R406 10K and R458 20K for LED_BL_DET	add KB B/L Detect	A00
94	40	For Board ID	2008/08/01	W EE	Page 40 remove BID2 change Board VER to 00	Board change	A00
95	54	For Boot	2008/08/01	W EE	Page 54 add R417 1KR RESET_OUT# to GND	for Boot	A00
96	16,21 37,57	Remove WWAN	2008/08/01	W EE	WWAN remove Page 16 DY R356 ,RF4 connect SB_WWAN_PCIE_RST# to +3.3V_RUN Page 16 DY C443,C439 for WWAN remove Page 21 DY R2118,R66 Page 37 DY CON6605,C6644,C6645,C6646,C6647,C6648,C6636,C6637,C6638,C6639,C6640,C6641,C6642,C6643,CE17,CE18 Page 57 DY CON6615	Remove WWAN	A00
97	13,36	For Layout	2008/08/01	W EE	Page 36 Remove J3,Page 13 remove J4	Remove J3 modify for Layout	

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