

BLF6G13L-250P; BLF6G13LS-250P(G)

Power LDMOS transistor

Rev. 5. — 1 September 2015

AMPLEON

Product data sheet

1. Product profile

1.1 General description

250 W LDMOS power transistor intended for CW applications at a frequency of 1.3 GHz.

Table 1. Test information

Typical RF performance at $T_{case} = 25\text{ °C}$; $I_{Dq} = 100\text{ mA}$; in a class-AB production test circuit.

Test signal	f	V _{DS}	P _{L(1dB)}	G _p	η _D
	(GHz)	(V)	(W)	(dB)	(%)
CW	1.3	50	250	17	56

1.2 Features and benefits

- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- Industrial, scientific and medical applications

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF6G13L-250P (SOT1121A)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		
BLF6G13LS-250P (SOT1121B)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		
BLF6G13LS-250PG (SOT1121E)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF6G13L-250P	-	flanged LDMOST ceramic package; 2 mounting holes; 4 leads	SOT1121A
BLF6G13LS-250P	-	earless flanged LDMOST ceramic package; 4 leads	SOT1121B
BLF6G13LS-250PG	-	earless flanged LDMOST ceramic package; 4 leads	SOT1121E

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Min	Max	Unit
V_{DS}	drain-source voltage	-	100	V
V_{GS}	gate-source voltage	-0.5	+13	V
T_{stg}	storage temperature	-65	+150	°C
T_j	junction temperature [1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the on-line MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_{case} = 85\text{ °C}; P_L = 250\text{ W}$	0.26	K/W

6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ °C}$; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 1.4\text{ mA}$	100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 235\text{ mA}$	1.4	1.8	2.4	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V}$	-	-	1.4	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	21	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	240	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 120\text{ mA}$	-	1	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 4.75\text{ A}$	-	200	-	mΩ

Table 7. RF characteristics

Test signal: CW; $f = 1.3\text{ GHz}$; RF performance at $V_{DS} = 50\text{ V}; I_{Dq} = 100\text{ mA}; T_{case} = 25\text{ °C}$; unless otherwise specified, in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$P_L = 250\text{ W}$	-	-	50	V
G_p	power gain	$P_L = 250\text{ W}$	15	17	-	dB
RL_{in}	input return loss	$P_L = 250\text{ W}$	-	-30	-20	dB
η_D	drain efficiency	$P_L = 250\text{ W}$	52	56	-	%

7. Application information

7.1 Ruggedness in class-AB operation

The BLF6G13L-250P, BLF6G13LS-250P and BLF6G13LS-250PG are capable of withstanding a load mismatch corresponding to VSWR = 5 : 1 through all phases under the following conditions: $V_{DS} = 50\text{ V}$; $I_{Dq} = 100\text{ mA}$; $P_L = 250\text{ W}$; $f = 1.3\text{ GHz}$.

7.2 Impedance information

Table 8. Typical impedance

Typical values valid per section unless otherwise specified.

f (MHz)	Z_S (Ω)	Z_L optimized for G_p (Ω)	Z_L optimized for η_D (Ω)
1200	3.03 – j8.15	2.03 – j0.25	1.46 – j0.47
1300	4.06 – j9.52	1.67 – j0.92	1.19 – j0.95
1400	7.00 – j9.61	1.50 – j1.48	1.22 – j1.49

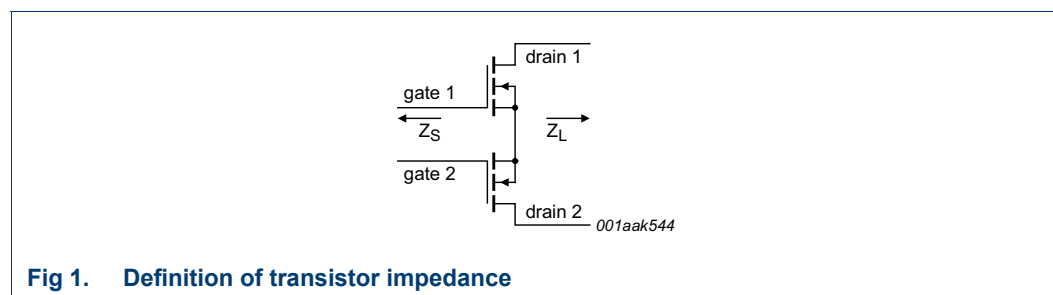


Fig 1. Definition of transistor impedance

7.3 Circuit information

Table 9. List of components

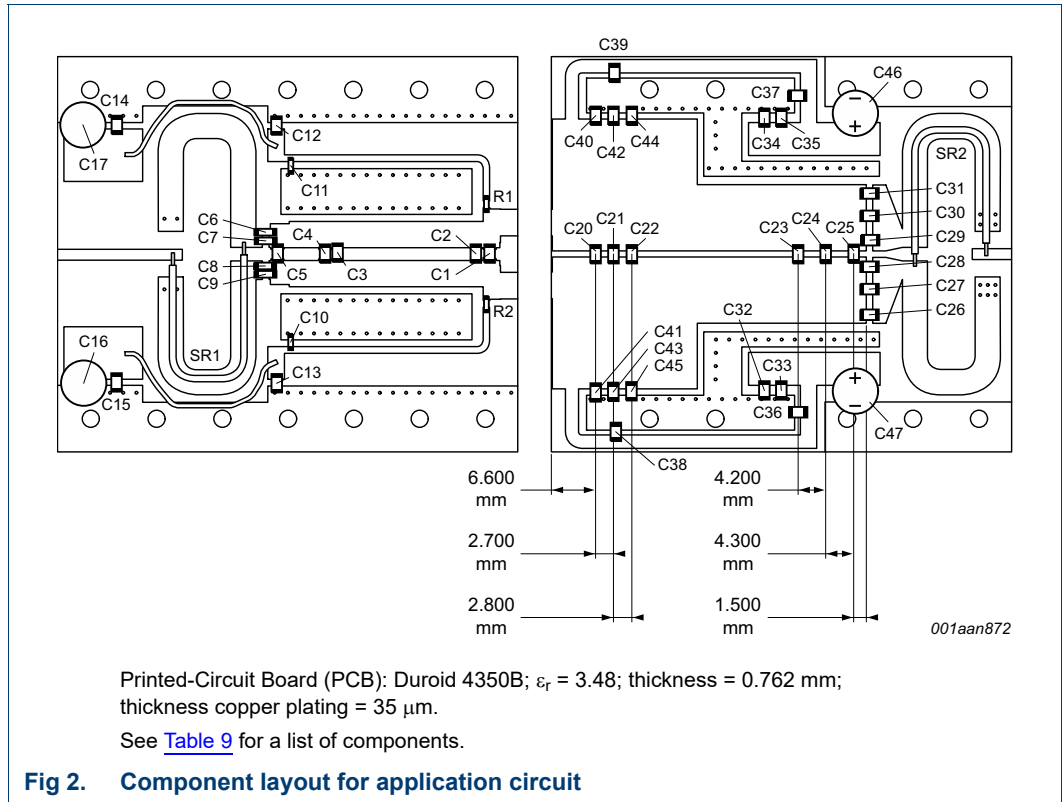
For application circuit see [Figure 2](#).

Component	Description	Value	Remarks
C1, C2	multilayer ceramic chip capacitor	1.9 pF	[1]
C3, C4	multilayer ceramic chip capacitor	4.7 pF	[1]
C5	multilayer ceramic chip capacitor	10 pF	[1]
C6, C7, C8, C9, C10, C11, C38, C39	multilayer ceramic chip capacitor	56 pF	[1]
C12, C13	multilayer ceramic chip capacitor	100 pF	[2]
C14, C15, C32, C34	multilayer ceramic chip capacitor	1 nF	[2]
C16, C17	electrolytic capacitor	10 μ F, 50 V	220 X5R
C20, C21, C22, C23	multilayer ceramic chip capacitor	3.0 pF	[1]
C40, C41	multilayer ceramic chip capacitor	2.4 pF	[1]
C42, C43, C44, C45	multilayer ceramic chip capacitor	2.7 pF	[1]
C24	multilayer ceramic chip capacitor	0.8 pF	[1]
C25	multilayer ceramic chip capacitor	0.6 pF	[1]

Table 9. List of components ...continued
 For application circuit see [Figure 2](#).

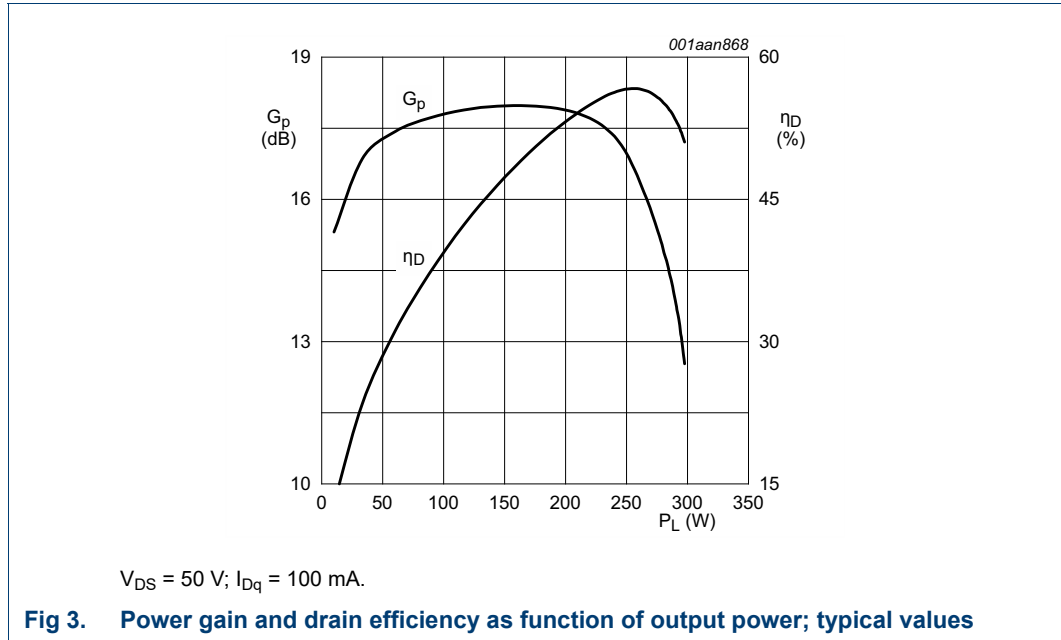
Component	Description	Value	Remarks
C26, C27, C28, C29, C30, C31, C33, C35	multilayer ceramic chip capacitor	100 pF	[1]
C36, C37	multilayer ceramic chip capacitor	20 nF	[3]
C46, C47	electrolytic capacitor	100 μ F, 63 V	
R1, R2	SMD resistor 0603	5.1 Ω	
SR1	COAX	25 Ω	UT-141C-25-TP
SR2	COAX	35 Ω	UT-141C-35-TP

- [1] American Technical Ceramics type 800B or capacitor of same quality.
- [2] American Technical Ceramics type 100B or capacitor of same quality.
- [3] American Technical Ceramics type 200B or capacitor of same quality.

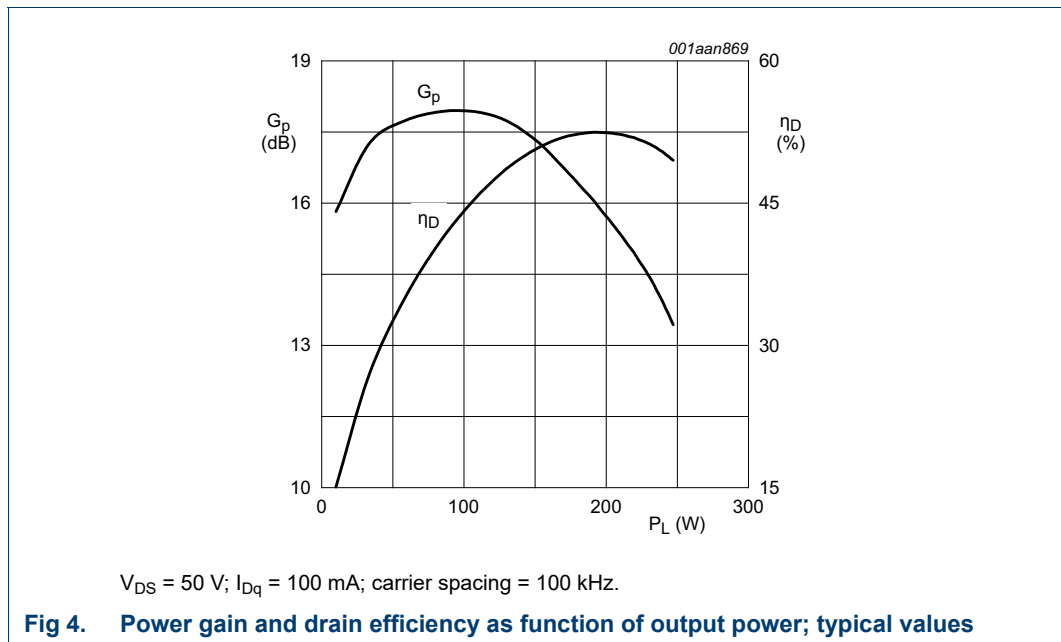


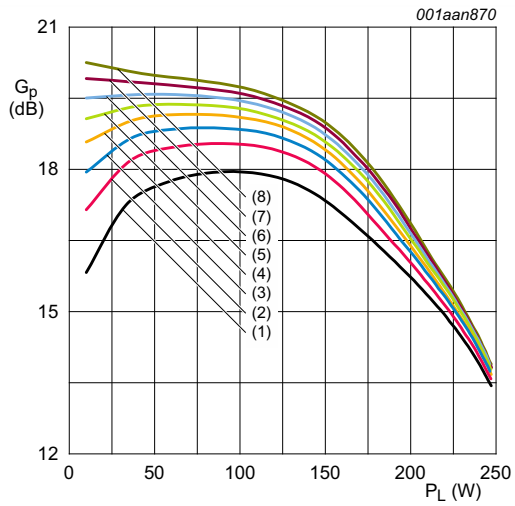
7.4 Graphical data

7.4.1 CW



7.4.2 2-Carrier CW

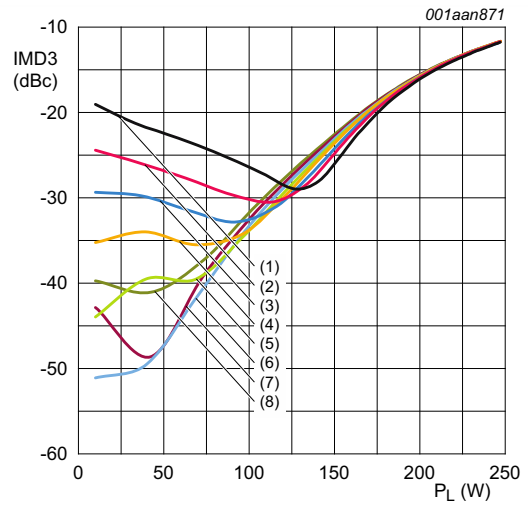




$V_{DS} = 50 \text{ V}$; $f = 1300 \text{ MHz}$; carrier spacing = 100 kHz.

- (1) $I_{Dq} = 100 \text{ mA}$
- (2) $I_{Dq} = 300 \text{ mA}$
- (3) $I_{Dq} = 500 \text{ mA}$
- (4) $I_{Dq} = 700 \text{ mA}$
- (5) $I_{Dq} = 900 \text{ mA}$
- (6) $I_{Dq} = 1100 \text{ mA}$
- (7) $I_{Dq} = 1300 \text{ mA}$
- (8) $I_{Dq} = 1500 \text{ mA}$

Fig 5. Power gain as a function of output power; typical values



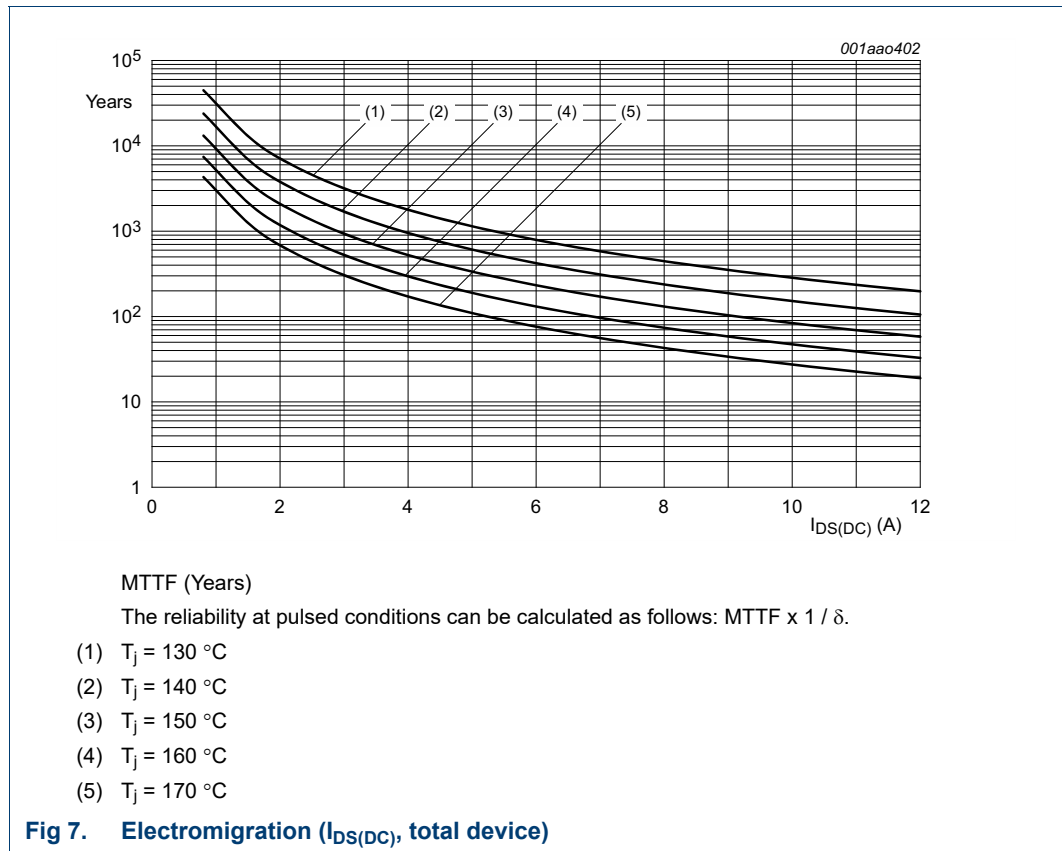
$V_{DS} = 50 \text{ V}$; $f = 1300 \text{ MHz}$; carrier spacing = 100 kHz.

- (1) $I_{Dq} = 100 \text{ mA}$
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- (5) $I_{Dq} = 900 \text{ mA}$
- (6) $I_{Dq} = 1100 \text{ mA}$
- (7) $I_{Dq} = 1300 \text{ mA}$
- (8) $I_{Dq} = 1500 \text{ mA}$

Fig 6. Third order intermodulation distortion as a function of output power; typical values

8. Test information

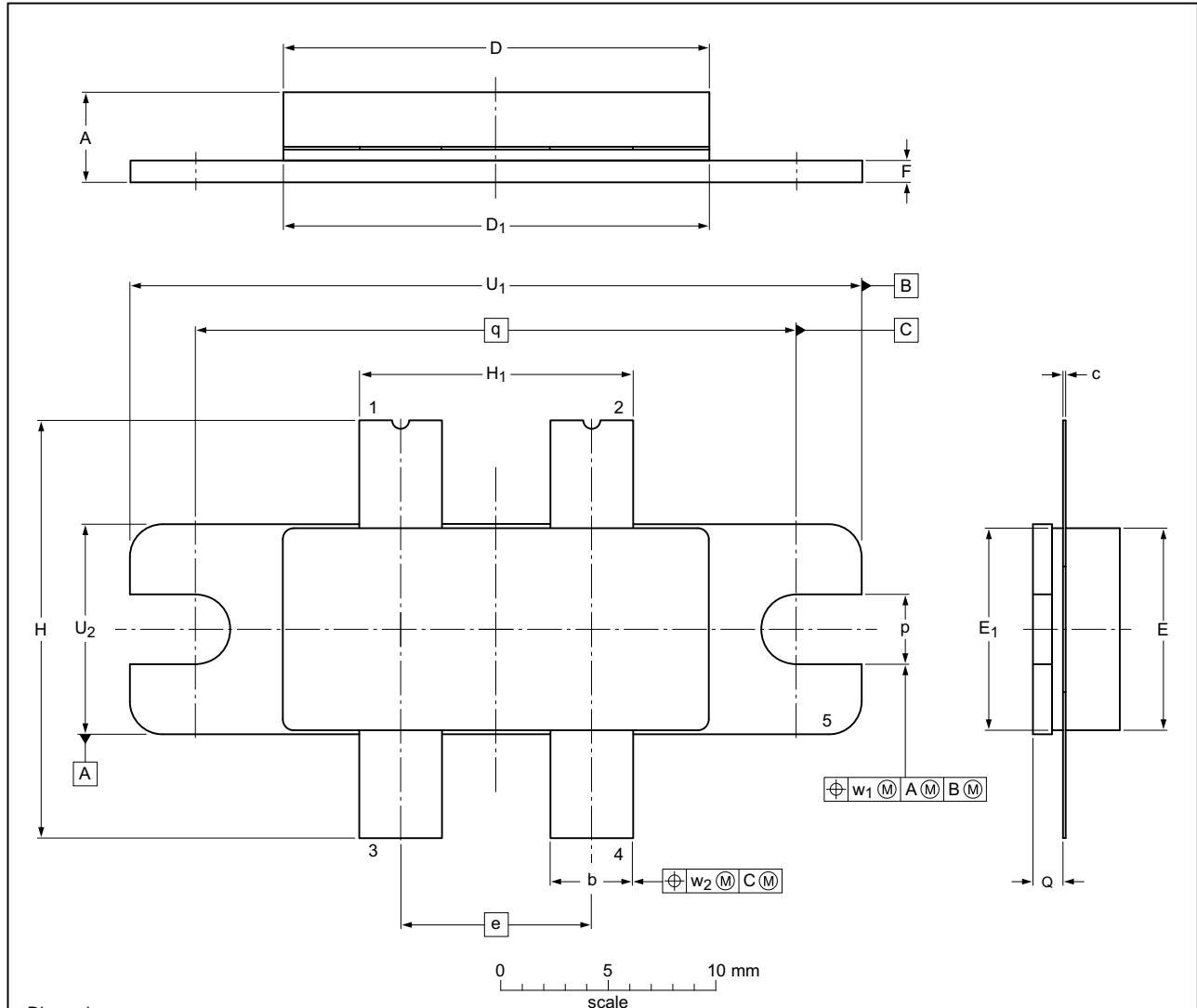
8.1 Reliability



9. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 4 leads

SOT1121A



Dimensions

Unit ⁽¹⁾	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	p	Q ⁽²⁾	q	U ₁	U ₂	w ₁	w ₂
mm	max	4.75	3.94	0.18	20.02	19.96	9.53	9.53	1.14	19.94	12.83	3.38	1.70	34.16	9.91		0.25	0.51
	nom					8.89								27.94				
	min	3.45	3.68	0.10	19.61	19.66	9.27	9.27	0.89	18.92	12.57	3.12	1.45	33.91	9.65			
inches	max	0.187	0.155	0.007	0.788	0.786	0.375	0.375	0.045	0.785	0.505	0.133	0.067	1.345	0.39		0.01	0.02
	nom					0.35								1.1				
	min	0.136	0.145	0.004	0.772	0.774	0.365	0.365	0.035	0.745	0.495	0.123	0.057	1.335	0.38			

Note

- 1. millimeter dimensions are derived from the original inch dimensions.
- 2. dimension is measured 0.030 inch (0.76 mm) from the body.

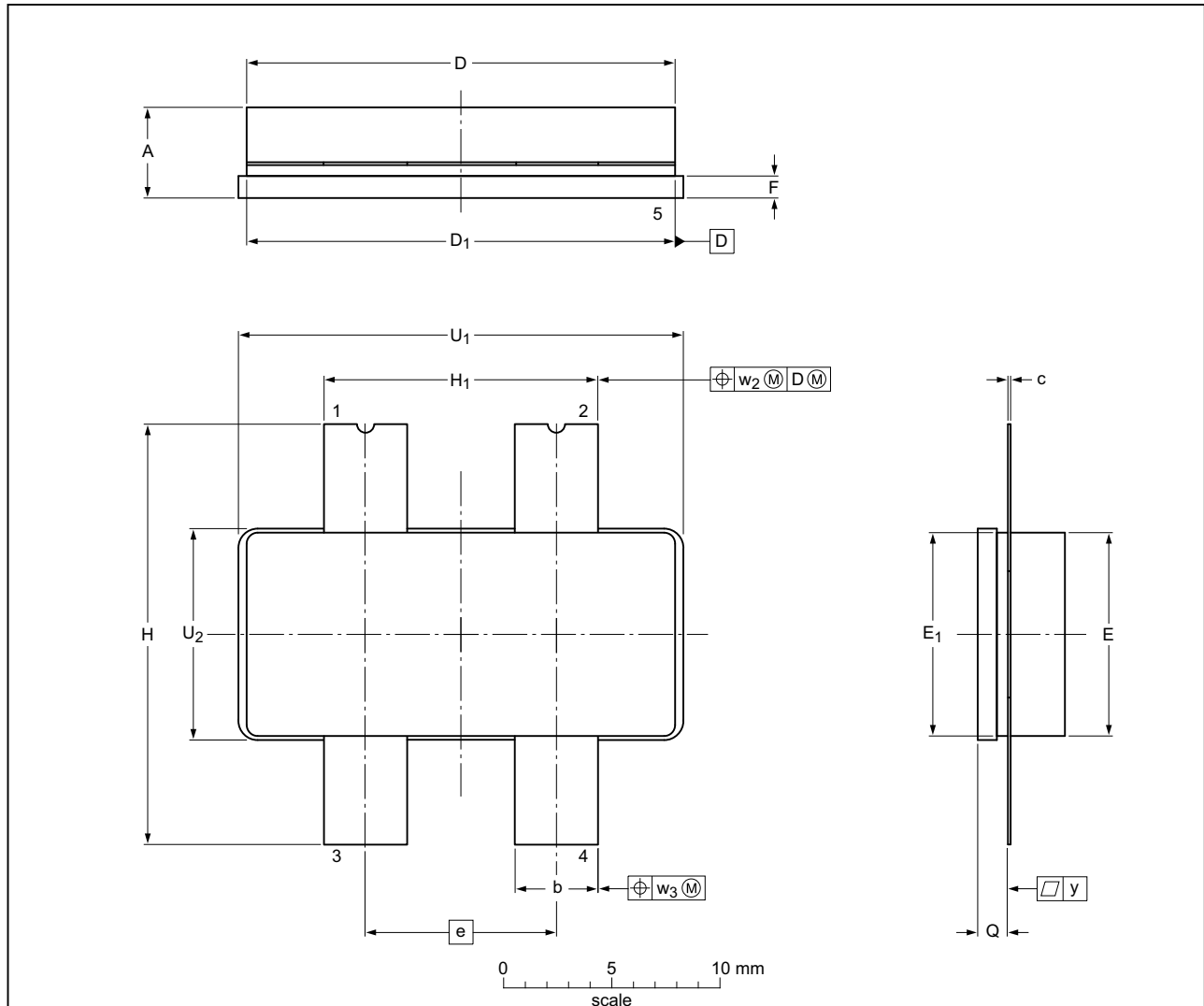
sot1121a_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1121A					09-10-12 10-02-02

Fig 8. Package outline SOT1121A

Earless flanged ceramic package; 4 leads

SOT1121B



Dimensions

Unit ⁽¹⁾	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	Q	U ₁	U ₂	w ₂	w ₃	y
mm	max	4.75	3.94	0.18	20.02	19.96	9.53	9.53	1.14	19.94	12.83	1.70	20.70	9.91	0.51	0.25	0.10
	nom					8.89											
	min	3.45	3.68	0.08	19.61	19.66	9.27	9.27	0.89	18.92	12.57	1.45	20.45	9.65			
inches	max	0.187	0.155	0.007	0.788	0.786	0.375	0.375	0.045	0.785	0.505	0.067	0.815	0.39	0.02	0.01	0.004
	nom					0.35											
	min	0.136	0.145	0.003	0.772	0.774	0.365	0.365	0.035	0.745	0.495	0.057	0.805	0.38			

Note

1. millimeter dimensions are derived from the original inch dimensions.
2. dimension is measured 0.030 inch (0.76 mm) from the body.

sot1121b_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1121B					12-06-07 15-07-21

Fig 9. Package outline SOT1121B

Earless flanged LDMOST ceramic package; 4 leads

SOT1121E

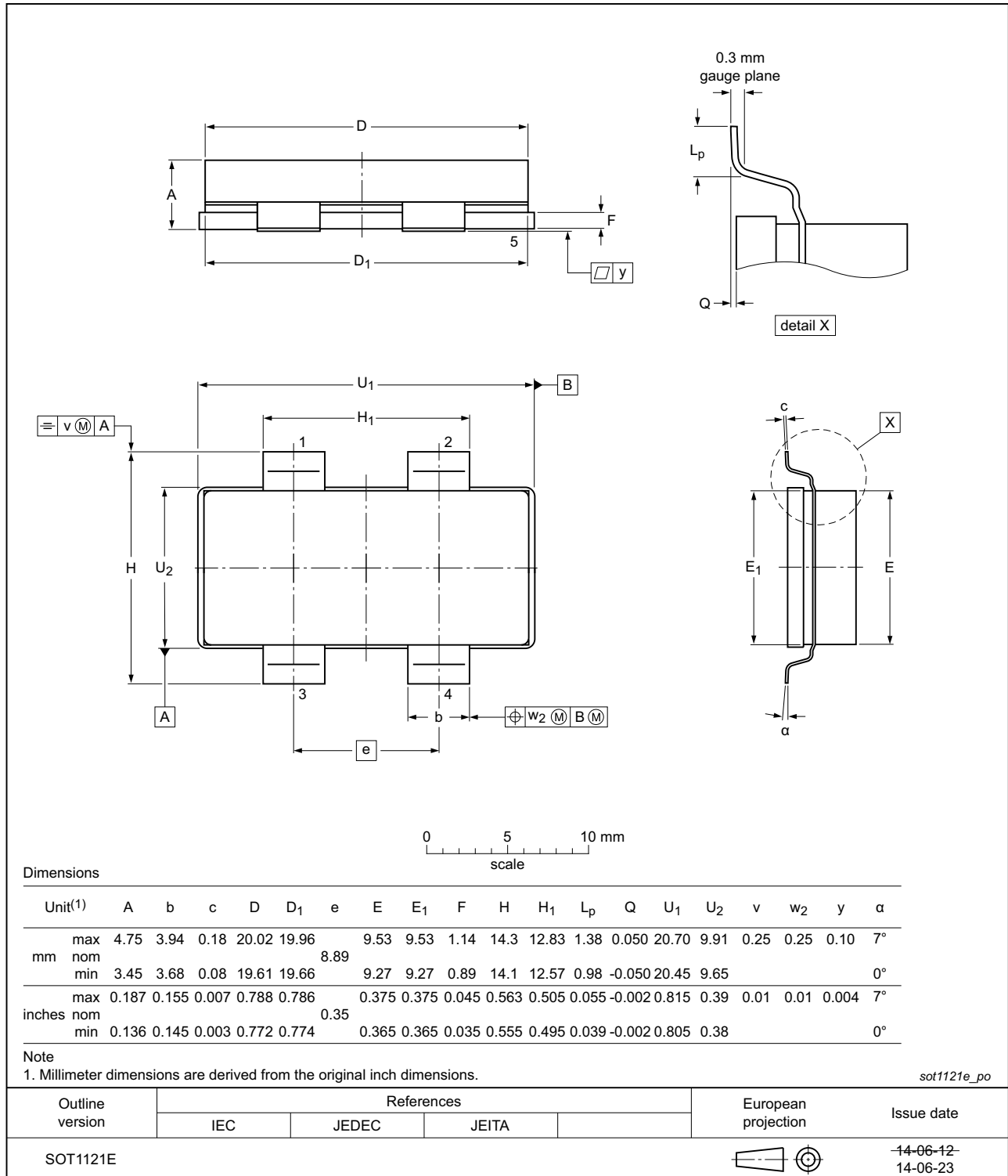


Fig 10. Package outline SOT1121E

10. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

11. Abbreviations

Table 10. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
MTF	Median Time to Failure
MTTF	Mean Time to Failure
SMD	Surface-Mounted Device
VSWR	Voltage Standing-Wave Ratio

12. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF6G13L-250P_LS-250P_LS-250PG#5	20150901	Product data sheet	-	BLF6G13L-250P_6G13LS-250P v.4
Modifications:	<ul style="list-style-type: none"> The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. Legal texts have been adapted to the new company name where appropriate. 			
BLF6G13L-250P_LS-250P_LS-250PG v.4	<tbd>	Product data sheet	-	BLF6G13L-250P_6G13LS-250P v.3
BLF6G13L-250P_6G13LS-250P v.3	20111014	Product data sheet	-	BLF6G13L-250P_6G13LS-250P v.2
BLF6G13L-250P_6G13LS-250P v.2	20110321	Objective data sheet	-	BLF6G13L-250P_6G13LS-250P v.1
BLF6G13L-250P_6G13LS-250P v.1	20101102	Objective data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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