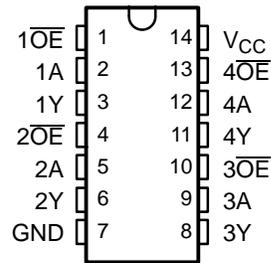


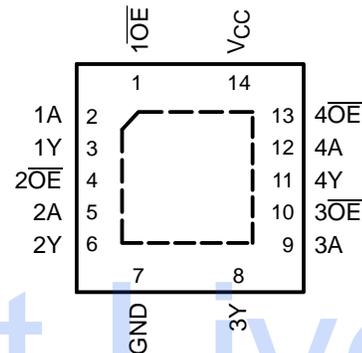
FEATURES

- Operates From 1.65 V to 3.6 V
- Specified From -40°C to 85°C and -40°C to 125°C
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.8 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) $<0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^{\circ}\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) $>2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^{\circ}\text{C}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

D, DB, NS, OR PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

This quadruple bus buffer gate is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC125A features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (\overline{OE}) input is high.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QFN – RGY	Reel of 1000	SN74LVC125ARGYR	LC125A
-40°C to 125°C	SOIC – D	Tube of 50	SN74LVC125AD	LVC125A
		Reel of 2500	SN74LVC125ADR	
		Reel of 250	SN74LVC125ADT	
	SOP – NS	Reel of 2000	SN74LVC125ANSR	LVC125A
	SSOP – DB	Reel of 2000	SN74LVC125ADBR	LC125A
	TSSOP – PW	Tube of 90	SN74LVC125APW	LC125A
		Reel of 2000	SN74LVC125APWR	
Reel of 250		SN74LVC125APWT		

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

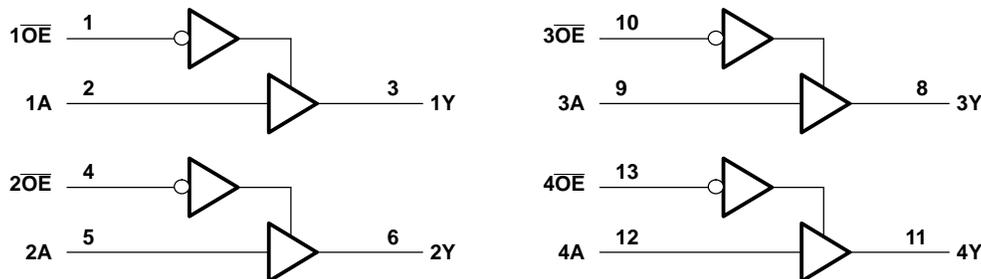
SN74LVC125A QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

SCAS2900–JANUARY 1993–REVISED AUGUST 2005

**FUNCTION TABLE
(EACH BUFFER)**

INPUTS		OUTPUT Y
\overline{OE}	A	
L	H	H
L	L	L
H	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	6.5	V
V_I	Input voltage range ⁽²⁾	-0.5	6.5	V
V_O	Output voltage range ⁽²⁾⁽³⁾	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current		-50	$V_I < 0$ mA
I_{OK}	Output clamp current		-50	$V_O < 0$ mA
I_O	Continuous output current		±50	mA
	Continuous current through V_{CC} or GND		±100	mA
θ_{JA}	Package thermal impedance		86	°C/W
		D package ⁽⁴⁾		
		DB package ⁽⁴⁾	96	
		NS package ⁽⁴⁾	76	
		PW package ⁽⁴⁾	113	
	RGY package ⁽⁵⁾	47		
T_{stg}	Storage temperature range	-65	150	°C
P_{tot}	Power dissipation		500	$T_A = -40^\circ\text{C to } 125^\circ\text{C}^{(6)(7)}$ mW

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) The package thermal impedance is calculated in accordance with JESD 51-5.
- (6) For the D package: above 70°C, the value of P_{tot} derates linearly with 8 mW/K.
- (7) For the DB, NS, and PW packages: above 60°C, the value of P_{tot} derates linearly with 5.5 mW/K.

Recommended Operating Conditions⁽¹⁾

			T _A = 25°C		–40°C to 85°C		–40°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	Operating	1.65	3.6	1.65	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		0.65 × V _{CC}		0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		1.7		1.7		
		V _{CC} = 2.7 V to 3.6 V	2		2		2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}		0.35 × V _{CC}		0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	0.7		0.7		0.7		
		V _{CC} = 2.7 V to 3.6 V	0.8		0.8		0.8		
V _I	Input voltage	0	5.5	0	5.5	0	5.5	V	
V _O	Output voltage	0	V _{CC}	0	V _{CC}	0	V _{CC}	V	
I _{OH}	High-level output current	V _{CC} = 1.65 V	–4		–4		–4		mA
		V _{CC} = 2.3 V	–8		–8		–8		
		V _{CC} = 2.7 V	–12		–12		–12		
		V _{CC} = 3 V	–24		–24		–24		
I _{OL}	Low-level output current	V _{CC} = 1.65 V	4		4		4		mA
		V _{CC} = 2.3 V	8		8		8		
		V _{CC} = 2.7 V	12		12		12		
		V _{CC} = 3 V	24		24		24		
Δt/Δv	Input transition rise or fall rate	8		8		8		ns/V	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = –100 μA	1.65 V to 3.6 V	V _{CC} – 0.2			V _{CC} – 0.2		V _{CC} – 0.3		V
	I _{OH} = –4 mA	1.65 V	1.29			1.2		1.05		
	I _{OH} = –8 mA	2.3 V	1.9			1.7		1.55		
	I _{OH} = –12 mA	2.7 V	2.2			2.2		2.05		
	I _{OH} = –24 mA	3 V	2.4			2.4		2.25		
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V	0.1			0.2		0.3		V
	I _{OL} = 4 mA	1.65 V	0.24			0.45		0.6		
	I _{OL} = 8 mA	2.3 V	0.3			0.7		0.75		
	I _{OL} = 12 mA	2.7 V	0.4			0.4		0.6		
	I _{OL} = 24 mA	3 V	0.55			0.55		0.8		
I _I	V _I = 5.5 V or GND	3.6 V	±1			±5		±20		μA
I _{OZ}	V _O = V _{CC} or GND	3.6 V	±1			±10		±20		μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	1			10		40		μA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500			500		5000		μA
C _i	V _I = V _{CC} or GND	3.3 V	5							pF

SN74LVC125A

QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

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Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

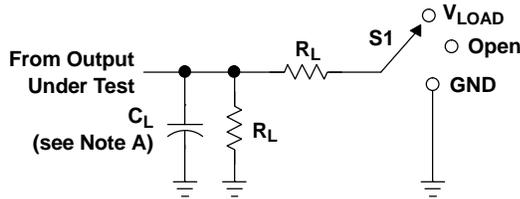
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	1.8 V ± 0.15 V	1	4.5	11.8	1	12.3	1	13.8	ns
			2.5 V ± 0.2 V	1	2.7	5.8	1	6.3	1	8.4	
			2.7 V	1	3	5.3	1	5.5	1	7	
			3.3 V ± 0.3 V	1	2.5	4.6	1	4.8	1	6	
t _{en}	\overline{OE}	Y	1.8 V ± 0.15 V	1	4.3	13.8	1	14.3	1	15.8	ns
			2.5 V ± 0.2 V	1	2.7	6.9	1	7.4	1	9.5	
			2.7 V	1	3.3	6.4	1	6.6	1	8.5	
			3.3 V ± 0.3 V	1	2.4	5.2	1	5.4	1	7	
t _{dis}	\overline{OE}	Y	1.8 V ± 0.15 V	1	4.3	10.6	1	11.1	1	12.6	ns
			2.5 V ± 0.2 V	1	2.2	5.1	1	5.6	1	7.7	
			2.7 V	1	2.5	4.8	1	5	1	6.5	
			3.3 V ± 0.3 V	1	2.4	4.4	1	4.6	1	6	
t _{sk(o)}			3.3 V ± 0.3 V					1		1.5	ns

Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC}	TYP	UNIT
C _{pd}	Power dissipation capacitance per gate	f = 10 MHz	1.8 V	7.4	pF
			2.5 V	11.3	
			3.3 V	15	

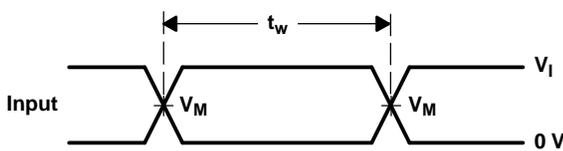
PARAMETER MEASUREMENT INFORMATION



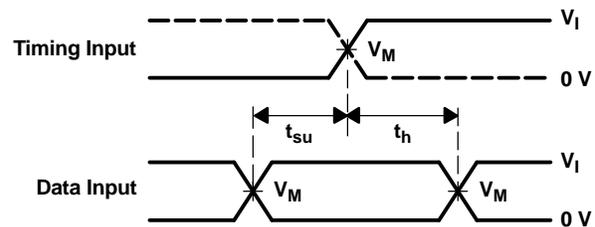
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

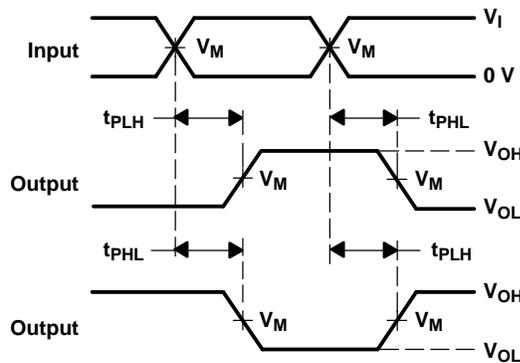
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V



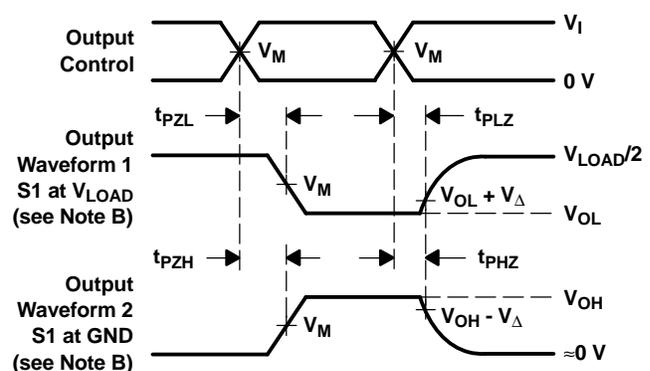
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PZL} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LVC125AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125ADBLE	OBSOLETE	SSOP	DB	14		TBD	Call TI	Call TI
SN74LVC125ADBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125ADBRG4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74LVC125ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125ADT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125ADTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125ANSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125APW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125APWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125APWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125APWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI
SN74LVC125APWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125APWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125APWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125APWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125APWTE4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125APWTG4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125ARGYR	ACTIVE	QFN	RGY	14	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74LVC125ARGYRG4	ACTIVE	QFN	RGY	14	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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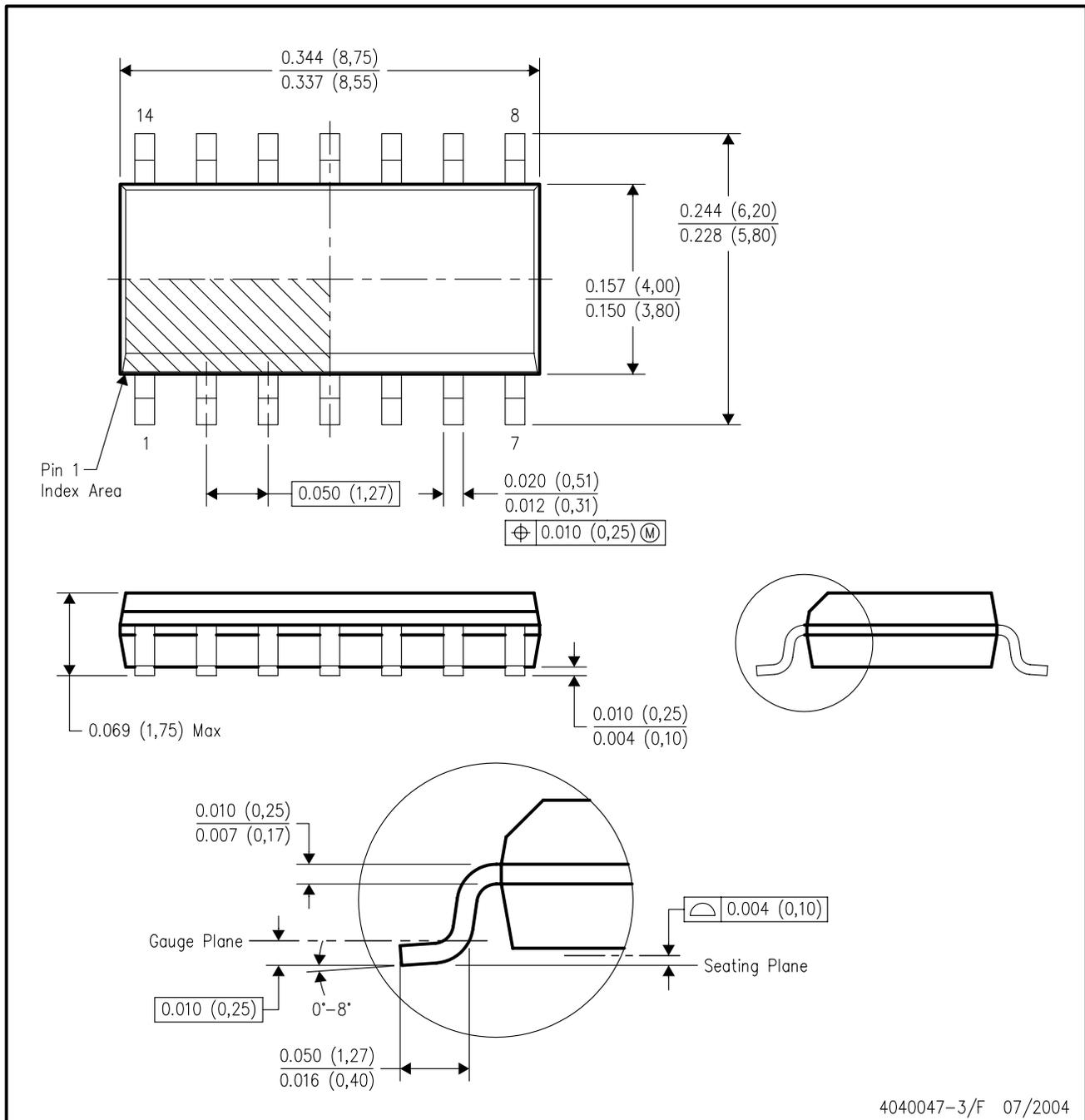
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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D (R-PDSO-G14)

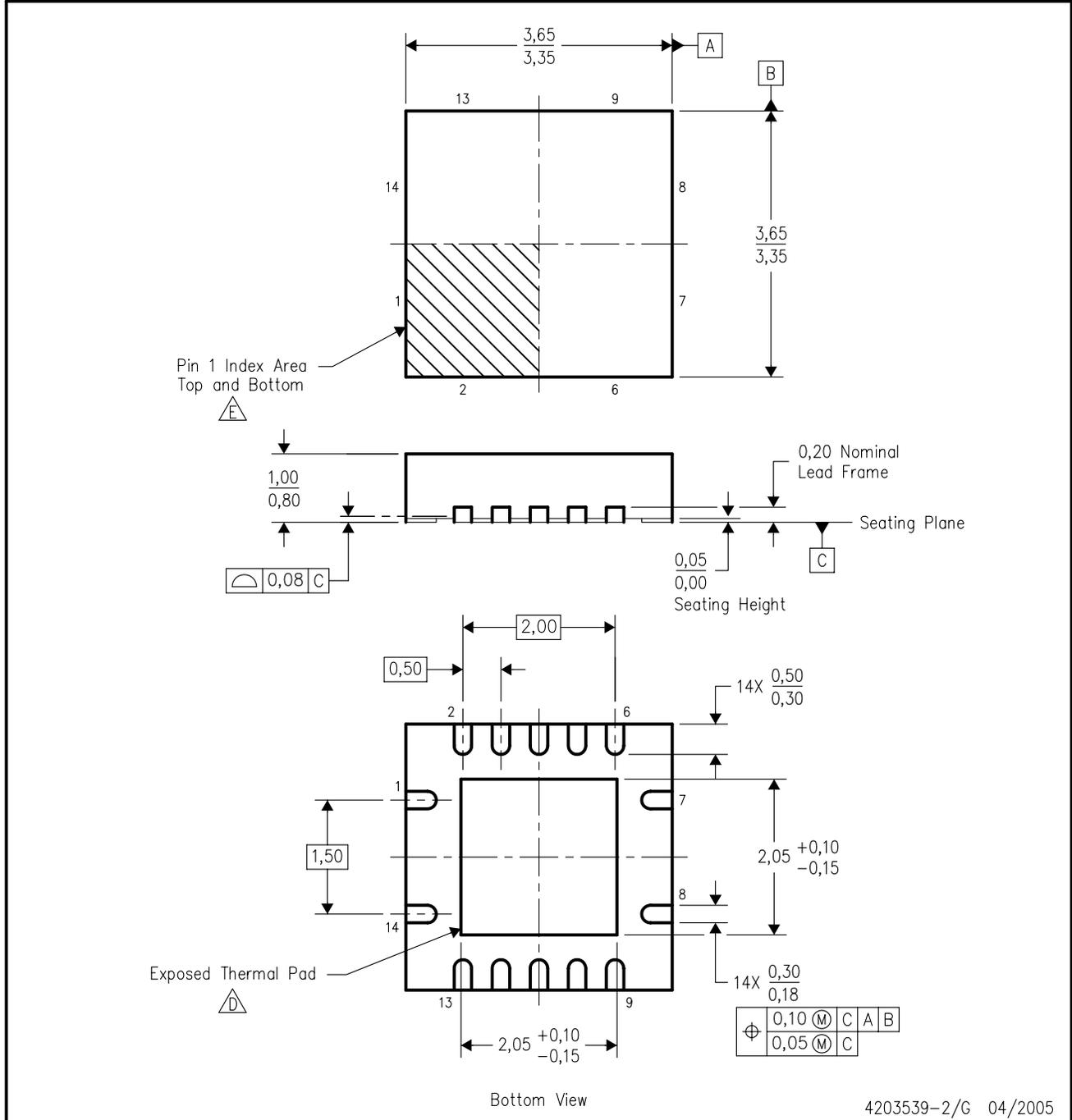
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AB.

RGY (S-PQFP-N14)

PLASTIC QUAD FLATPACK



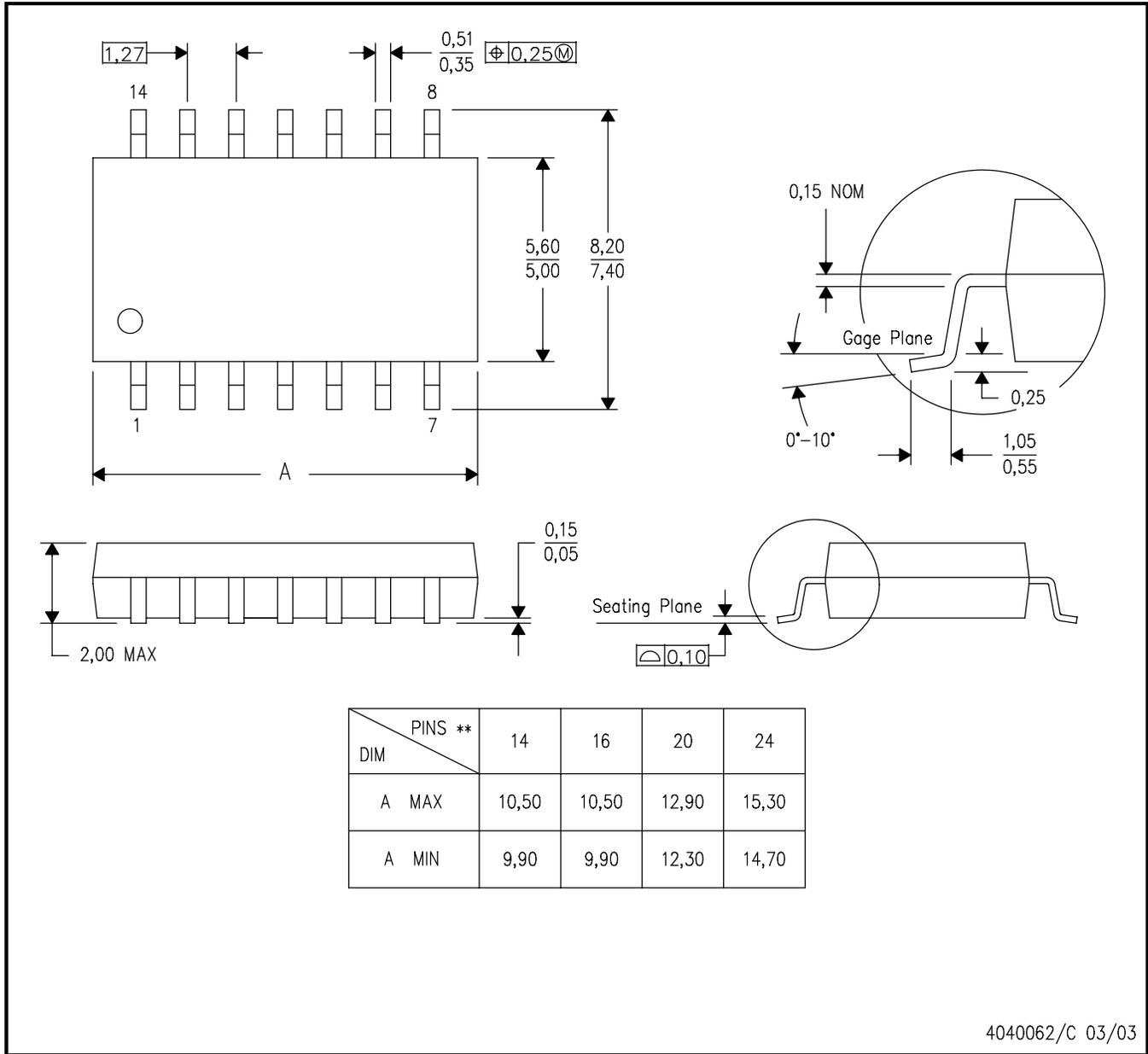
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - F. Package complies to JEDEC MO-241 variation BA.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

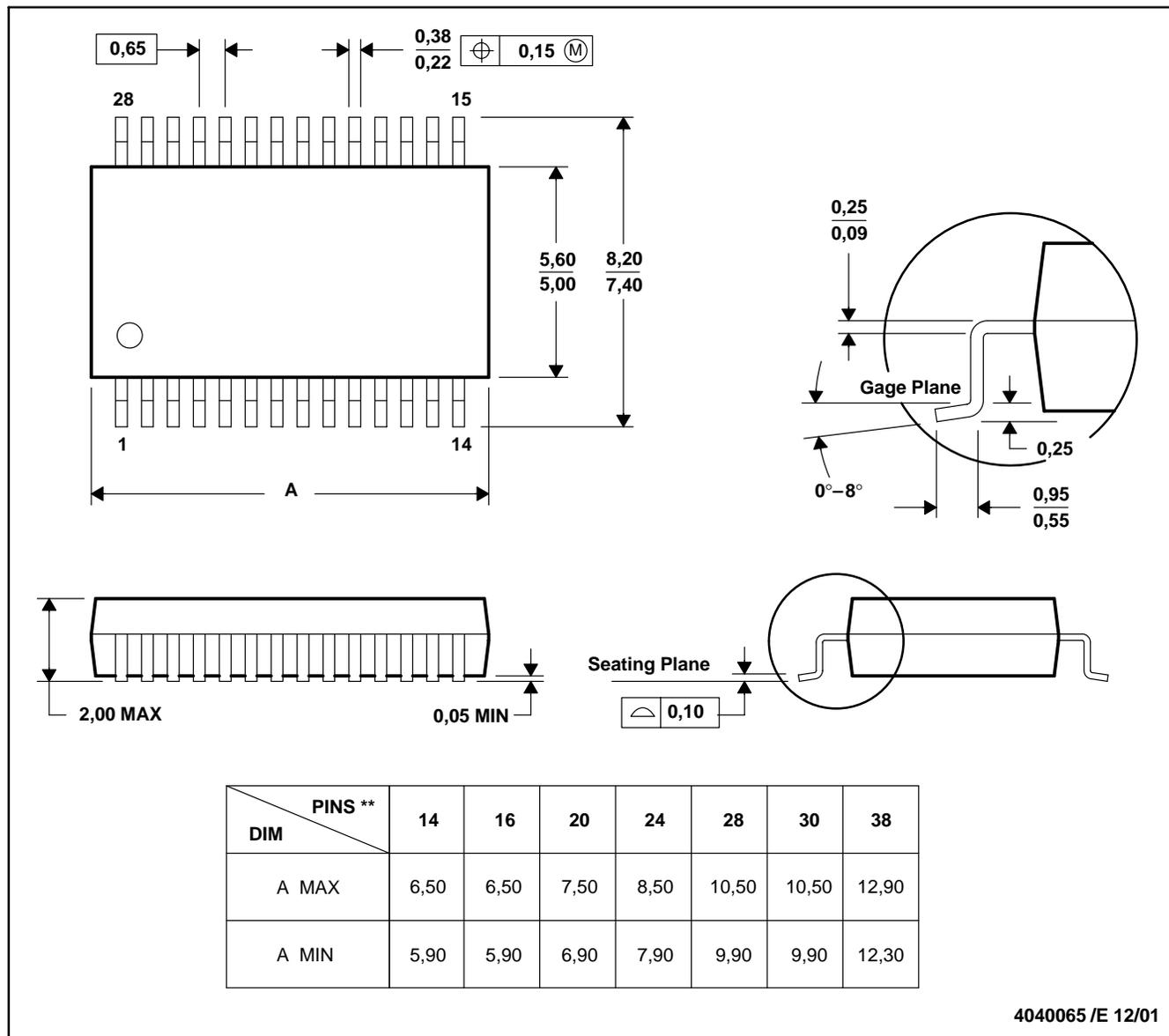


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN

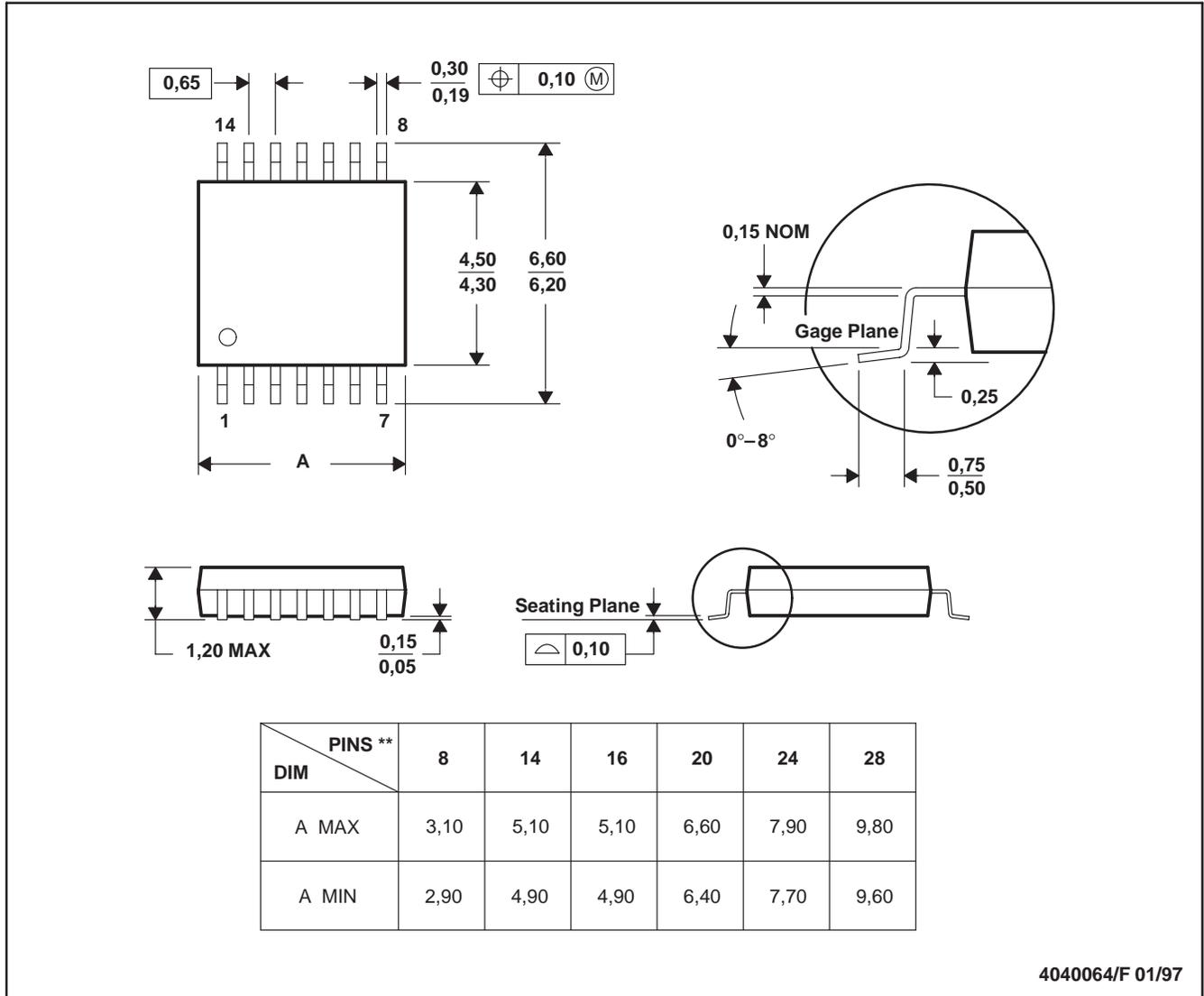


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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SN74LVC125A, Status: ACTIVE

Quadruple Bus Buffer Gate With 3-State Outputs



clear gif

<input type="checkbox"/> Features	<input type="checkbox"/> Samples	<input type="checkbox"/> Technical Documents
<input type="checkbox"/> Quality & Pb-Free Data	<input type="checkbox"/> Pricing/Packaging	<input type="checkbox"/> Applications Notes
<input type="checkbox"/> Related Products	<input type="checkbox"/> Inventory	<input type="checkbox"/> Simulation Models
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Datasheet



Download Datasheet **SN74LVC125A (Rev. O)** (sn74lvc125a.pdf, 346 KB)
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	SN74LVC125A
Voltage Nodes(V)	3.3, 2.7, 2.5, 1.8
Vcc range(V)	1.65 to 3.6
Logic	True
Input Level	TTL/CMOS
Output Level	LVTTTL
Output Drive(mA)	-24/24
No. of Outputs	4
tpd max(ns)	4.8
Static Current	0.01
	Samples
	Inventory

Product Information

Features Save this to your personal library

Operates From 1.65 V to 3.6 V
Specified From -40°C to 85°C and -40°C to 125°C
Inputs Accept Voltages to 5.5 V
Max t_{pd} of 4.8 ns at 3.3 V
Typical V_{OLP} (Output Ground Bounce)
< 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
Typical V_{OHV} (Output V_{OH} Undershoot)
> 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
Latch-Up Performance Exceeds 250 mA Per JESD 17
ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DESCRIPTION/ORDERING INFORMATION

This quadruple bus buffer gate is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC125A features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is high.

To ensure the high-impedance state during power up or power down, OE should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

Pricing/Packaging/CAD Design Tools/Samples

			Price	Packaging			CAD Design Tools	Samples
Device	Status	Temp (°C)	Budget Price (\$US) QTY	Industry Standard (TI Pkg) Pins	Top Side Marking	Standard Pack Quantity	Footprints	Samples
SN74LVC125AD	ACTIVE	-40 to 125	0.20 1KU	SOIC (D) 14	View	50	<input type="checkbox"/>	Purchase Samples
SN74LVC125ADBLE	OBSOLETE	-40 to 125		SSOP (DB) 14	View		<input type="checkbox"/>	Not Available
SN74LVC125ADBR	ACTIVE	-40 to 125	0.17 1KU	SSOP (DB) 14	View	2000	<input type="checkbox"/>	Contact TI Distributor or Sales Office
SN74LVC125ADBRG4	ACTIVE	-40 to 125	0.19 1KU	SSOP (DB) 14	View	2000	<input type="checkbox"/>	Purchase Samples
SN74LVC125ADE4	ACTIVE	-40 to 125	0.20 1KU	SOIC (D) 14	View	50	<input type="checkbox"/>	Purchase Samples
SN74LVC125ADR	ACTIVE	-40 to 125	0.20 1KU	SOIC (D) 14	View	2500	<input type="checkbox"/>	Contact TI Distributor or Sales Office
SN74LVC125ADRE4	ACTIVE	-40 to 125	0.22 1KU	SOIC (D) 14	View	2500	<input type="checkbox"/>	Purchase Samples
SN74LVC125ADRG4	ACTIVE	-40 to 125	0.22 1KU	SOIC (D) 14	View	2500	<input type="checkbox"/>	Purchase Samples
SN74LVC125ADT	ACTIVE	-40 to 125	0.31 1KU	SOIC (D) 14	View	250	<input type="checkbox"/>	Purchase Samples
SN74LVC125ADTE4	ACTIVE	-40 to 125	0.31 1KU	SOIC (D) 14	View	250	<input type="checkbox"/>	Purchase Samples
SN74LVC125ANSR	ACTIVE	-40 to 125	0.17 1KU	SO (NS) 14	View	2000	<input type="checkbox"/>	Contact TI Distributor or Sales Office
SN74LVC125ANSRE4	ACTIVE	-40 to 125	0.17 1KU	SO (NS) 14	View	2000	<input type="checkbox"/>	Request Free Samples
SN74LVC125APW	ACTIVE	-40 to 125	0.17 1KU	TSSOP (PW) 14	View	90	<input type="checkbox"/>	Purchase Samples
SN74LVC125APWE4	ACTIVE	-40 to 125	0.19 1KU	TSSOP (PW) 14	View	90	<input type="checkbox"/>	Purchase Samples
SN74LVC125APWG4	ACTIVE	-40 to 125	0.22 1KU	TSSOP (PW) 14	View	90	<input type="checkbox"/>	Purchase Samples
SN74LVC125APWLE	OBSOLETE	-40 to 125		TSSOP (PW) 14	View		<input type="checkbox"/>	Not Available
SN74LVC125APWR	ACTIVE	-40 to 125	0.20 1KU	TSSOP (PW) 14	View	2000	<input type="checkbox"/>	Contact TI Distributor or Sales Office
SN74LVC125APWRE4	ACTIVE	-40 to 125	0.22 1KU	TSSOP (PW) 14	View	2000	<input type="checkbox"/>	Purchase Samples
SN74LVC125APWRG4	ACTIVE	-40 to 125	0.22 1KU	TSSOP (PW) 14	View	2000	<input type="checkbox"/>	Purchase Samples
SN74LVC125APWT	ACTIVE	-40 to 125	0.31 1KU	TSSOP (PW) 14	View	250	<input type="checkbox"/>	Purchase Samples
SN74LVC125APWTE4	ACTIVE	-40 to 125	0.55 1KU	TSSOP (PW) 14	View	250	<input type="checkbox"/>	Purchase Samples
SN74LVC125APWTG4	ACTIVE	-40 to 125	0.53 1KU	TSSOP (PW) 14	View	250	<input type="checkbox"/>	Purchase Samples
SN74LVC125ARGYR	ACTIVE	-40 to 125	0.36 1KU	QFN (RGY) 14	View	1000		Request Free Samples
SN74LVC125ARGYRG4	ACTIVE	-40 to 125	0.24 1KU	QFN (RGY) 14	View	1000		Request Free Samples

Inventory

		TI Inventory Status			Reported Distributor Inventory			
SN74LVC125AD		As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase	

View all Distributors

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	10k*	2082 30 Nov	10 Weeks	None Reported View Distributors			
		>10k 3 Mar					
SN74LVC125ADT	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 6 Mar	14 Weeks	None Reported View Distributors			
SN74LVC125ADTE4	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 6 Mar	14 Weeks	None Reported View Distributors			
SN74LVC125ANSR	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	396 6 Jan	10 Weeks	Americas	DigiKey	>1k	<input type="text"/>
		267 13 Jan					
		633 20 Jan					
		980 27 Jan					
		1980 17 Feb					
SN74LVC125ANSRE4	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	396 6 Jan	10 Weeks	None Reported View Distributors			
		267 13 Jan					
		633 20 Jan					
		980 27 Jan					
		1980 17 Feb					
SN74LVC125APW	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	1080 3 Feb	12 Weeks	Americas	Avnet	86	<input type="text"/>
		1080 27 Feb					
SN74LVC125APWE4	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 3 Apr	16 Weeks	None Reported View Distributors			
SN74LVC125APWG4	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 3 Apr	16 Weeks	None Reported View Distributors			
SN74LVC125APWR	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase

	0*		16 Weeks	Europe	Farnell InOne	467	<input type="text"/>
SN74LVC125APWRE4	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	2000 13 Mar	15 Weeks	None Reported View Distributors			
		>10k 3 Apr					
SN74LVC125APWRG4	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	4000*	>10k 12 Dec	12 Weeks	None Reported View Distributors			
SN74LVC125APWT	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	2500*	29 2 Dec	12 Weeks	None Reported View Distributors			
SN74LVC125APWTE4	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 3 Apr	16 Weeks	None Reported View Distributors			
SN74LVC125APWTG4	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 3 Apr	16 Weeks	None Reported View Distributors			
SN74LVC125ARGYR	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 12 Dec	4 Weeks	Americas	Avnet	>1k	<input type="text"/>
					DigiKey	871	<input type="text"/>
				Europe	Avnet-SILICA	1k	<input type="text"/>
SN74LVC125ARGYRG4	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 12 Dec	4 Weeks	None Reported View Distributors			

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Quality & Lead (Pb)-Free Data

Device	Product Content			MTBF/FIT Rate	
	Eco Plan*	Lead/Ball Finish	MSL Rating/Peak Reflow	Details	Details
SN74LVC125AD <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC125ADBR <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC125ADBRG4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR	View	View
SN74LVC125ADE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC125ADR <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC125ADRE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC125ADRG4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC125ADT <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC125ADTE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC125ANSR <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC125ANSRE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC125APW <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC125APWE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC125APWG4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC125APWR <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC125APWRE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC125APWRG4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC125APWT <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC125APWTE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC125APWTG4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC125ARGYR <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR	View	View
SN74LVC125ARGYRG4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR	View	View

* The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please click on the Product Content Details "View" link in the table above for the latest availability information and additional product content details.

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Technical Documents

Datasheets	Keep track of what's new
SN74LVC125A (Rev. O) (sn74lvc125a.pdf, 346 KB) 27 Jul 2005 Download	
Application Notes	
Semiconductor Packing Material Electrostatic Discharge (ESD) Protection (szza047.htm, 9 KB) 08 Jul 2004 Abstract	
Selecting the Right Level Translation Solution (Rev. A) (scea035a.htm, 9 KB) 22 Jun 2004 Abstract	
Shelf-Life Evaluation of Lead-Free Component Finishes (szza046.htm, 9 KB) 24 May 2004 Abstract	
Use of the CMOS Unbuffered Inverter in Oscillator Circuits (szza043.htm, 9 KB) 06 Nov 2003 Abstract	
Understanding and Interpreting Standard-Logic Data Sheets (Rev. B) (szza036b.htm, 8 KB) 28 May 2003 Abstract	
Texas Instruments Little Logic Application Report (scea029.htm, 9 KB) 01 Nov 2002 Abstract	
TI IBIS File Creation, Validation, and Distribution Processes (szza034.htm, 9 KB) 29 Aug 2002 Abstract	
16-Bit Widebus Logic Families in 56-Ball, 0.65-mm Pitch Very Thin Fine-Pitch BGA (Rev. B) (szza029b.htm, 9 KB) 22 May 2002 Abstract	
Power-Up 3-State (PU3S) Circuits in TI Standard Logic Devices (szza033.htm, 9 KB) 10 May 2002 Abstract	
Selecting the Right Texas Instruments Signal Switch (szza030.htm, 9 KB) 07 Sep 2001 Abstract	
Implications of Slow or Floating CMOS Inputs (Rev. C) (scba004c.htm, 9 KB) 01 Feb 1998 Abstract	
Bus-Interface Devices With Output-Damping Resistors Or Reduced-Drive Outputs (Rev. A) (scba012a.htm, 9 KB) 01 Aug 1997 Abstract	

CMOS Power Consumption and CPD Calculation (Rev. B) (scaa035b.htm, 9 KB)

01 Jun 1997 [Abstract](#)

LVC Characterization Information (scba011.htm, 9 KB)

01 Dec 1996 [Abstract](#)

Live Insertion (sdya012.htm, 9 KB)

01 Oct 1996 [Abstract](#)

Input and Output Characteristics of Digital Integrated Circuits (sdya010.htm, 9 KB)

01 Oct 1996 [Abstract](#)

Understanding Advanced Bus-Interface Products Design Guide (scaa029.pdf, 253 KB)

01 May 1996 [Download](#)

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User Guides

Signal Switch Data Book (Rev. A) (scdd003a.pdf, 19732 KB)

14 Nov 2003 [Download](#)

LVC and LV Low-Voltage CMOS Logic Data Book (Rev. B) (scbd152b.pdf, 13291 KB)

18 Dec 2002 [Download](#)

LOGIC Pocket Data Book (scyd013.pdf, 4835 KB)

05 Dec 2002 [Download](#)

Simulation Models

IBIS Model

IBIS Model of SN74LVC125A (Rev. B) (scem013b.ibs, 237 KB)

07 Jun 2002 [ibis](#) / [zip](#)

More Literature

Logic Selection Guide 2005 (Rev. X) (sdyu001x.pdf, 6909 KB)

15 Mar 2005 [Download](#)

Wireless Infrastructure Solutions Guide (2Q2005) (Rev. E) (sstc001e.pdf, 734 KB)

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Design Summary for WCSP Little Logic (Rev. B) (scet007b.pdf, 295 KB)

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Dual- Supply Translation Product Clip (scyb033.pdf, 230 KB)

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Military Semiconductors Selection Guide 2004-2005 (Rev. D) (sgyc003d.pdf, 964 KB)

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SN74LVC1G97 and SN74LVC1G98 Product Clip (Rev. A) (scyb010a.pdf, 253 KB)

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Logic Cross-Reference (Rev. A) (scyb017a.pdf, 2938 KB)

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SN74LVC1G3157 and SNS74LVC2G53 SPDT Analog Switches (scyb014.pdf, 65 KB)

12 Jun 2003 [Download](#)

Standard Linear & Logic for PCs, Servers & Motherboards (scyb005.pdf, 3997 KB)

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STANDARD LINEAR AND LOGIC FOR DVD/VCD PLAYERS (scym001.pdf, 5872 KB)

27 Mar 2002 [Download](#)

Military Low Voltage Solutions (sgyn139.pdf, 103 KB)

04 Apr 2001 [Download](#)

Low-Voltage Logic (LVC) Designer's Guide (scba010.htm, 9 KB)

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