8-Channel, 12-Bit, 40MSPS Analog-to-Digital Converter with Serial LVDS Interface

FEATURES

- **Maximum Sample Rate: 40MSPS**
- **12-Bit Resolution**
- **No Missing Codes**
- **Total Power Dissipation:**
  Internal Reference: 888mW
  External Reference: 822mW
- **CMOS Technology**
- **Simultaneous Sample-and-Hold**
- **70.5dB SNR at 10MHz IF**
- **3.3V Digital/Analog Supply**
- **Serialized LVDS Outputs**
- **Integrated Frame and Bit Patterns**
- **Option to Double LVDS Clock Output Currents**
- **Four Current Modes for LVDS**
- **Pin- and Format-Compatible Family**
- **TQFP-80 PowerPAD™ Package**

APPLICATIONS

- **Portable Ultrasound Systems**
- **Tape Drives**
- **Test Equipment**
- **Optical Networking**

DESCRIPTION

The ADS5270 is a high-performance, 40MSPS, 8-channel analog-to-digital converter (ADC). Internal references are provided, simplifying system design requirements. Low power consumption allows for the highest of system integration densities. Serial LVDS (low-voltage differential signaling) outputs reduce the number of interface lines and package size.

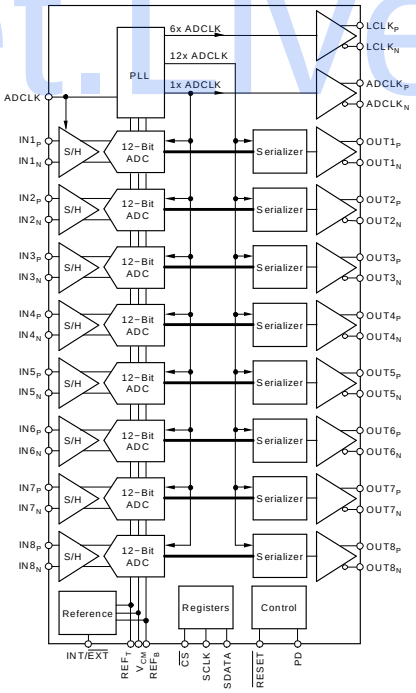
RELATED PRODUCTS

MODEL	RESOLUTION (BITS)	SAMPLE RATE (MSPS)	CHANNELS
ADS5271	12	50	8
ADS5272	12	65	8
ADS5273	12	70	8
ADS5277	10	65	8

An integrated phase lock loop (PLL) multiplies the incoming ADC sampling clock by a factor of 12. This high-frequency LVDS clock is used in the data serialization and transmission process. The word output of each internal ADC is serialized and transmitted either MSB or LSB first. In addition to the eight data outputs, a bit clock and a word clock are also transmitted. The bit clock is at 6x the speed of the sampling clock, whereas the word clock is at the same speed of the sampling clock.

The ADS5270 provides internal references, or can optionally be driven with external references. Best performance can be achieved through the internal reference mode.

The device is available in a TQFP-80 PowerPAD package and is specified over a –40°C to +85°C operating range.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD(2)	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS5270	HTQFP-80	PFP	–40°C to +85°C	ADS5270IPFP	ADS5270IPFP	Tray, 96
					ADS5270IPFPT	Tape and Reel, 250

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Thermal pad size: 4.69mm × 4.69mm (min), 6.20mm × 6.20mm (max).

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage Range, AVDD	–0.3V to +3.8V
Supply Voltage Range, LVDD	–0.3V to +3.8V
Voltage Between AVSS and LVSS	–0.3V to +0.3V
Voltage Between AVDD and LVDD	–0.3V to +0.3V
Voltages Applied to External REF Pins	–0.3V to +2.4V
All LVDS Data and Clock Outputs	–0.3V to +2.4V
Analog Input Pins(2)	–0.3V to min. [3.3V, (AVDD + 0.3V)]
Operating Free-Air Temperature Range, T_A	–40°C to +85°C
Lead Temperature, 1.6mm (1/16" from case for 10s)	+260°C
Junction Temperature	+105°C
Storage Temperature Range	–65°C to +150°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) The DC voltage applied on the input pins should not go below –0.3V. Also, the DC voltage should be limited to the lower of either 3.3V or (AVDD + 0.3V). If the input can go higher than +3.3V, then a resistor greater than or equal to 25Ω should be added in series with each of the input pins. Also, the duty cycle of the overshoot beyond +3.3V should be limited. The overshoot duty cycle can be defined either as a percentage of the time of overshoot over a clock period, or over the entire device lifetime. For a peak voltage between +3.3V and +3.5V, a duty cycle up to 10% is acceptable. For a peak voltage between +3.5V and +3.7V, the overshoot duty cycle should not exceed 1%. Any overshoot beyond +3.7V should be restricted to less than 0.1% duty cycle, and never exceed +3.9V.

RECOMMENDED OPERATING CONDITIONS

	ADS5270			
	MIN	TYP	MAX	UNITS
SUPPLIES AND REFERENCES				
Analog Supply Voltage, AVDD	3.0	3.3	3.6	V
Output Driver Supply Voltage, LVDD	3.0	3.3	3.6	V
REF_T — External Reference Mode	1.825	1.95	2.0	V
REF_B — External Reference Mode	0.9	0.95	1.075	V
REFCM = (REF_T + REF_B)/2 – External Reference Mode(1)		V_{CM} ± 50mV		V
Reference = (REF_T – REF_B) – External Reference Mode	0.75	1.0	1.1	V
Analog Input Common-Mode Range(1)		V_{CM} ± 50mV		V
CLOCK INPUT AND OUTPUTS				
ADCLK Input Sample Rate (low-voltage TTL)	20		40	MSPS
ADCLK Duty Cycle	45		55	%
Low-Level Voltage Clock Input			0.6	V
High-Level Voltage Clock Input	2.2			V
$ADCLK_P$ and $ADCLK_N$ Outputs (LVDS)	20		40	MHz
$LCLK_P$ and $LCLK_N$ Outputs (LVDS)(2)	120		240	MHz
Operating Free-Air Temperature, T_A	–40		+85	°C
Thermal Characteristics:				
θ_{JA}		19.4		°C/W
θ_{JC}		4.2		°C/W

(1) These voltages need to be set to 1.45V ± 50mV if they are derived independent of V_{CM}.
(2) 6 × ADCLK.

ELECTRICAL CHARACTERISTICS

T_{MIN} = –40°C and T_{MAX} = +85°C. Typical values are at T_A = +25°C, clock frequency = maximum specified, 50% clock duty cycle, AVDD = 3.3V, LVDD = 3.3V, –1dBFS, I_{SET} = 56.2kΩ, internal voltage reference, and LVDS buffer current at 3.5mA per channel, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS5270 MIN	ADS5270 TYP	ADS5270 MAX	UNITS
DC ACCURACY						
	No Missing Codes			Tested		
DNL	Differential Nonlinearity	f_{IN} = 5MHz	–0.9	±0.5	+0.9	LSB
INL	Integral Nonlinearity	f_{IN} = 5MHz	–2.0	±0.6	+2.0	LSB
	Offset Error(1)		–0.75		+0.75	%FS
	Offset Temperature Coefficient			±6		ppm/°C
	Fixed Attenuation in Channel(2)			1.5		%FS
	Fixed Attenuation Matching Across Channels			0.01	0.2	dB
	Gain Error/Reference Error(3)	$VREF_T$ – $VREF_B$	–2.5	±1.0	+2.5	%FS
	Gain Error Temperature Coefficient			±20		ppm/°C
POWER REQUIREMENTS(4)						
Internal Reference						
	Power Dissipation	Analog Only (AVDD)		716	760	mW
		Output Driver (LVDD)		172	188	mW
	Total Power Dissipation			888	948	mW
External Reference						
	Power Dissipation	Analog Only (AVDD)		650		mW
		Output Driver (LVDD)		172		mW
	Total Power Dissipation			822		mW
Power-Down		Clock Running		90		mW
REFERENCE VOLTAGES						
$VREF_T$	Reference Top (internal)		1.9	1.95	2.0	V
$VREF_B$	Reference Bottom (internal)		0.9	0.95	1.0	V
V_{CM}	Common-Mode Voltage		1.4	1.45	1.5	V
	V_{CM} Output Current(5)	±50mV Change in Voltage		±2.0		mA
$VREF_T$	Reference Top (external)		1.825	1.95	2.0	V
$VREF_B$	Reference Bottom (external)		0.9	0.95	1.075	V
	External Reference Common-Mode			V_{CM} ± 50mV		V
	External Reference Input Current(6)			1.0		mA

(1) Offset error is the deviation of the average code from mid-code with –1dBFS sinusoid from ideal mid-code (2048). Offset error is expressed in terms of % of full-scale.
(2) Fixed attenuation in the channel arises due to a fixed attenuation in the sample-and-hold amplifier. When the differential voltage at the analog input pins are changed from $–V_{REF}$ to $+V_{REF}$, the swing of the output code is expected to deviate from the full-scale code (4096LSB) by the extent of this fixed attenuation. NOTE: V_{REF} is defined as (REF_T – REF_B).
(3) The reference voltages are trimmed at production so that ($VREF_T$ – $VREF_B$) is within ± 25mV of the ideal value of 1V. This specification does not include fixed attenuation.
(4) Supply current can be calculated from dividing the power dissipation by the supply voltage of 3.3V.
(5) V_{CM} provides the common-mode current for the inputs of all eight channels when the inputs are AC-coupled. The V_{CM} output current specified is the additional drive of the V_{CM} buffer if loaded externally.
(6) Average current drawn from the reference pins in the external reference mode.

ELECTRICAL CHARACTERISTICS (continued)

T_{MIN} = –40°C and T_{MAX} = +85°C. Typical values are at T_A = +25°C, clock frequency = maximum specified, 50% clock duty cycle, AVDD = 3.3V, LVDD = 3.3V, –1dBFS, I_{SET} = 56.2kΩ, internal voltage reference, and LVDS buffer current at 3.5mA per channel, unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADS5270 MIN	ADS5270 TYP	ADS5270 MAX	UNITS
ANALOG INPUT					
Differential Input Capacitance			4.0		pF
Analog Input Common-Mode Range			$V_{CM} \pm 50$		mV
Differential Full-Scale Input Voltage Range	Internal Reference		2.03		V_{PP}
	External Reference		$2.03 \times (VREF_T - VREF_B)$		V_{PP}
Voltage Overload Recovery Time(7)			3.0		CLK Cycles
Input Bandwidth	–3dBFS, 25Ω Series Resistances		300		MHz
DIGITAL DATA INPUTS					
V_{IH} High-Level Input Voltage		2.2			V
V_{IL} Low-Level Input Voltage				0.6	V
C_{IN} Input Capacitance			3.0		pF
DIGITAL DATA OUTPUTS					
Data Format			Straight Offset Binary		
Data Bit Rate		240		480	Mbps
SERIAL INTERFACE					
SCLK Serial Clock Input Frequency				20	MHz

(7) A differential ON/OFF pulse is applied to the ADC input. The differential amplitude of the pulse in its ON (high) state is twice the full-scale range of the ADC, while the differential amplitude of the pulse in its OFF (low) state is zero. The overload recovery time of the ADC is measured as the time required by the ADC output code to settle within 1% of full-scale, as measured from its mid-code value when the pulse is switched from ON (high) to OFF (low).

REFERENCE SELECTION

MODE	INT/$\overline{EXT}$	DESCRIPTION
Internal Reference; FSR = $2.03V_{PP}$	1	Default with internal pull-up.
External Reference; FSR = $2.03 \times (REF_T - REF_B)$	0	Internal reference is powered down. The common-mode voltage of the external reference should be within 50mV of V_{CM}. V_{CM} is derived from the internal bandgap voltage.

AC CHARACTERISTICS

T_{MIN} = –40°C and T_{MAX} = +85°C. Typical values are at T_A = +25°C, clock frequency = maximum specified, 50% clock duty cycle, AVDD = 3.3V, LVDD = 3.3V, –1dBFS, I_{SET} = 56.2kΩ, internal voltage reference, and LVDS buffer current at 3.5mA per channel, unless otherwise noted.

PARAMETER		CONDITIONS	ADS5270			UNITS
			MIN	TYP	MAX	
DYNAMIC CHARACTERISTICS						
SFDR	Spurious-Free Dynamic Range	f_{IN} = 1MHz		89		dBc
		f_{IN} = 5MHz	78	87		dBc
		f_{IN} = 10MHz		85		dBc
		f_{IN} = 20MHz		83		dBc
HD_2	2nd-Order Harmonic Distortion	f_{IN} = 1MHz		95		dBc
		f_{IN} = 5MHz	85	95		dBc
		f_{IN} = 10MHz		90		dBc
		f_{IN} = 20MHz		87		dBc
HD_3	3rd-Order Harmonic Distortion	f_{IN} = 1MHz		89		dBc
		f_{IN} = 5MHz	78	87		dBc
		f_{IN} = 10MHz		85		dBc
		f_{IN} = 20MHz		83		dBc
SNR	Signal-to-Noise Ratio	f_{IN} = 1MHz		70.5		dBFS
		f_{IN} = 5MHz	68	70.5		dBFS
		f_{IN} = 10MHz		70.5		dBFS
		f_{IN} = 20MHz		70.5		dBFS
SINAD	Signal-to-Noise and Distortion	f_{IN} = 1MHz		70		dBFS
		f_{IN} = 5MHz	67.5	70		dBFS
		f_{IN} = 10MHz		70		dBFS
		f_{IN} = 20MHz		70		dBFS
ENOB	Effective Number of Bits	f_{IN} = 5MHz		11.3		Bits
	Crosstalk	5MHz Full-Scale Signal Applied to 7 Channels; Measurement Taken on the Channel with No Input Signal		–90		dBc
IMD3	Two-Tone, Third-Order Intermodulation Distortion	f_1 = 9.5MHz at –7dBFS f_2 = 10.2MHz at –7dBFS		–85		dBFS

LVDS DIGITAL DATA AND CLOCK OUTPUTS

Test conditions at I_O = 3.5mA, R_{LOAD} = 100Ω, and C_{LOAD} = 6pF. I_O refers to the current setting for the LVDS buffer. R_{LOAD} is the differential load resistance between the LVDS pair. C_{LOAD} is the effective single-ended load capacitance between each of the LVDS pins and ground. C_{LOAD} includes the receiver input parasitics as well as the routing parasitics. Measurements are done with a 1-inch transmission line of 100Ω characteristic impedance between the device and the load. All LVDS specifications are characterized, but not parametrically tested at production. LCLKOUT refers to ($LCLK_P$– $LCLK_N$); ADCLKOUT refers to ($ADCLK_P$– $ADCLK_N$); DATA OUT refers to (OUT_P– OUT_N); and ADCLK refers to the input sampling clock.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
DC SPECIFICATIONS(1)						
V_{OH}	Output Voltage High, OUT_P or OUT_N	R_{LOAD} = 100Ω ± 1%; See LVDS Timing Diagram, Page 8	1265	1365	1465	mV
V_{OL}	Output Voltage Low, OUT_P or OUT_N	R_{LOAD} = 100Ω ± 1%	940	1040	1140	mV
$\|V_{OD}\|$	Output Differential Voltage	R_{LOAD} = 100Ω ± 1%	275	325	375	mV
V_{OS}	Output Offset Voltage(2)	R_{LOAD} = 100Ω ± 1%; See LVDS Timing Diagram, Page 8	1.1	1.2	1.3	V
R_O	Output Impedance, Differential	Normal Operation		13		kΩ
R_O	Output Impedance, Differential	Power-Down		20		kΩ
C_O	Output Capacitance(3)			4		pF
$\|\Delta V_{OD}\|$	Change in $\|V_{OD}\|$ Between 0 and 1	R_{LOAD} = 100Ω ± 1%			10	mV
ΔV_{OS}	Change Between 0 and 1	R_{LOAD} = 100Ω ± 1%			25	mV
ISOUT	Output Short-Circuit Current	Drivers Shorted to Ground			40	mA
$ISOUT_{NP}$	Output Current	Drivers Shorted Together			12	mA
DRIVER AC SPECIFICATIONS						
ADCLKOUT Clock Duty Cycle(4)			45	50	55	%
LCLKOUT Duty Cycle(4)			44	50	56	%
Data Setup Time(5)(6)			0.7			ns
Data Hold Time(6)(7)			0.61			ns
LVDS Outputs Rise/Fall Time(8)		I_O = 2.5mA		400		ps
		I_O = 3.5mA	180	300	500	ps
		I_O = 4.5mA		230		ps
		I_O = 6.0mA		180		ps
LCLKOUT Rising Edge to ADCLKOUT Rising Edge(9)			0.74	1.04	1.34	ns
ADCLKOUT Rising Edge to LCLKOUT Falling Edge(9)			0.74	1.04	1.34	ns
ADCLKOUT Rising Edge to DATA OUT Transition(9)			–0.35	0	+0.35	ns

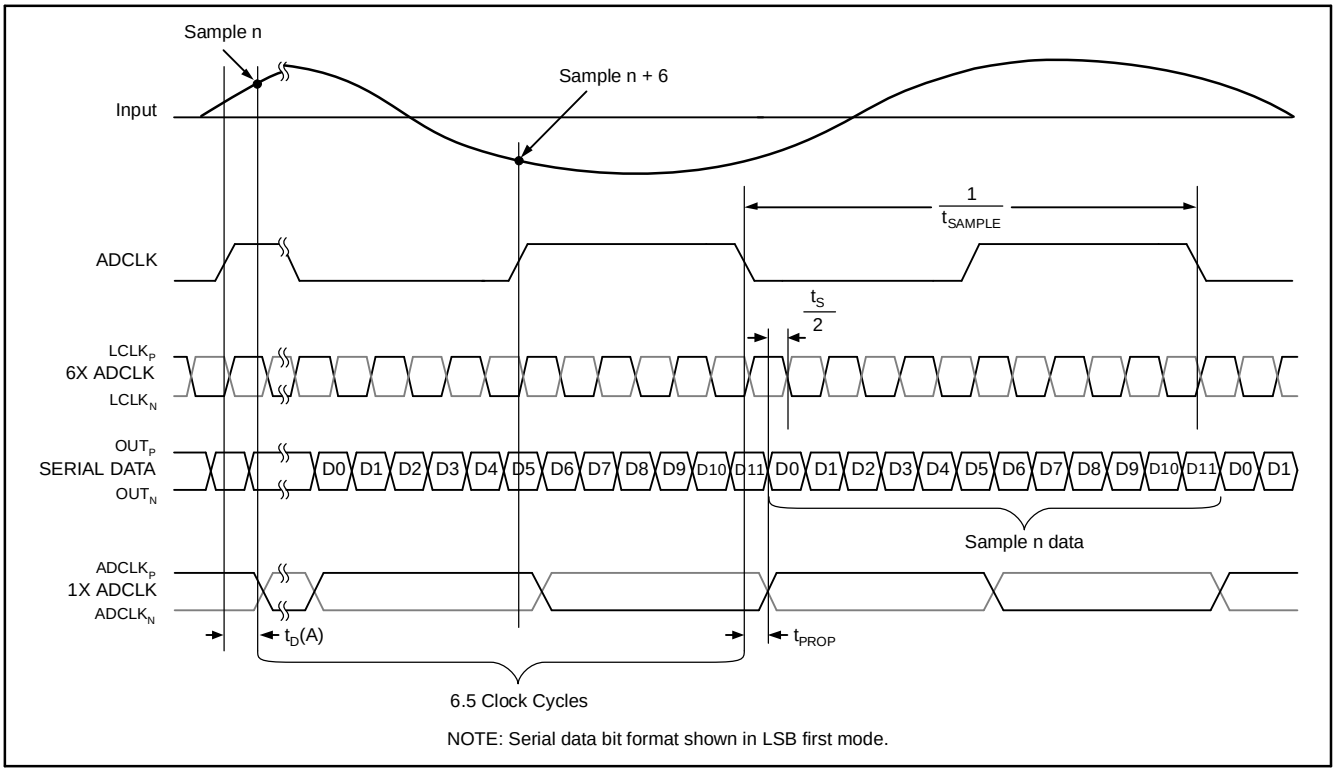
(1) The DC specifications refer to the condition where the LVDS outputs are not switching, but are permanently at a valid logic level 0 or 1.
(2) V_{OS} refers to the common-mode of OUT_P and OUT_N.
(3) Output capacitance inside the device, from either OUT_P or OUT_N to ground.
(4) Measured between zero crossings.
(5) DATA OUT (OUT_P – OUT_N) crossing zero to LCLKOUT ($LCLK_P$ – $LCLK_N$) crossing zero.
(6) Data setup and hold time accounts for data-dependent skews, channel-to-channel mismatches, as well as effects of clock jitter within the device.
(7) LCLKOUT crossing zero to DATA OUT crossing zero.
(8) Measured from –100mV to +100mV on the differential output for rise time, and +100mV to –100mV for fall time.
(9) Measured between zero crossings.

SWITCHING CHARACTERISTICS

T_{MIN} = –40°C and T_{MAX} = +85°C. Typical values are at T_A = +25°C, clock frequency = maximum specified, 50% clock duty cycle, AVDD = 3.3V, LVDD = 3.3V, –1dBFS, internal voltage reference, and LVDS buffer current at 3.5mA per channel, unless otherwise noted.

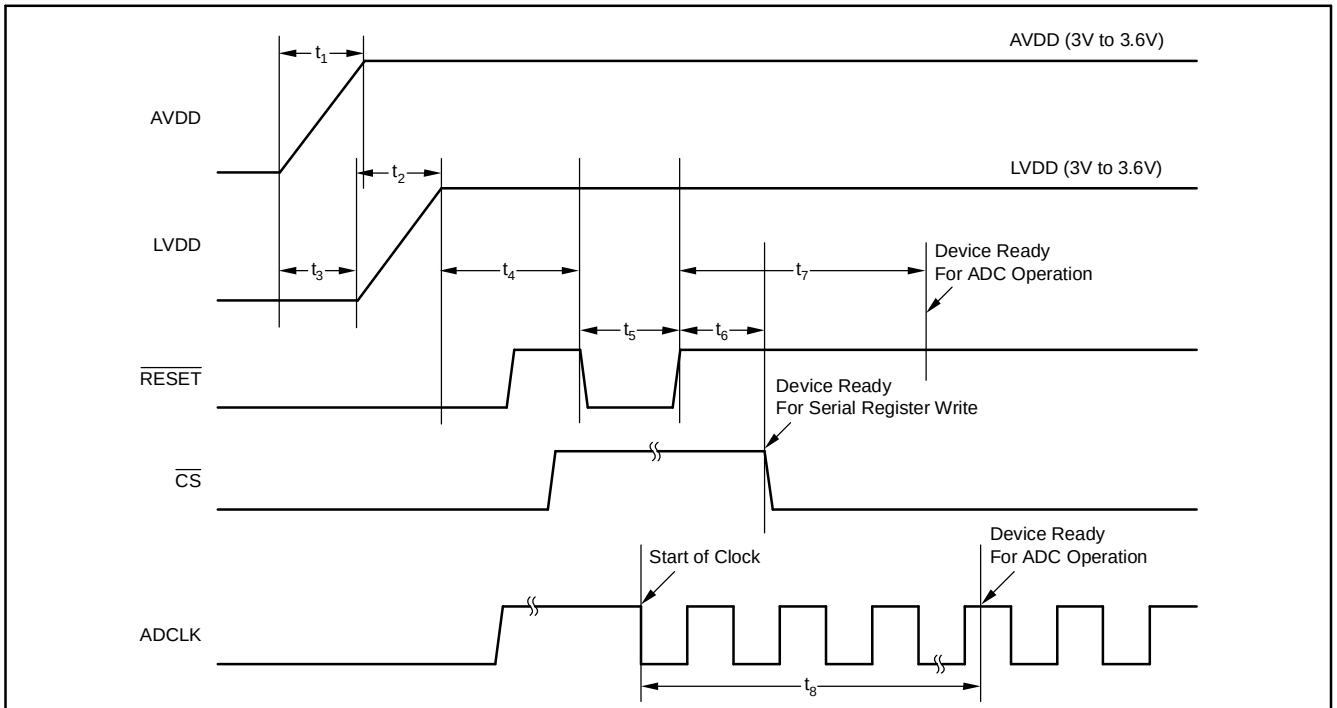
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING SPECIFICATIONS						
	t_{SAMPLE}		25		50	ns
t_D(A)	Aperture Delay		2	4	6.5	ns
	Aperture Jitter (uncertainty)			1		ps rms
t_D(pipeline)	Latency			6.5		Cycles
t_{PROP}	Propagation Delay		3	4.8	6.5	ns

LVDS TIMING DIAGRAM (PER ADC CHANNEL)



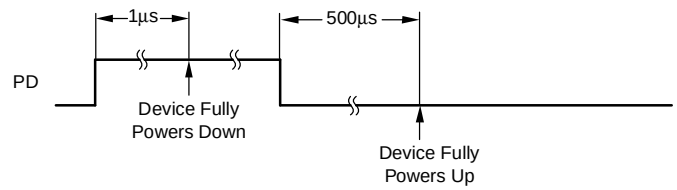
NOTE: Serial data bit format shown in LSB first mode.

RECOMMENDED POWER-UP SEQUENCING AND RESET TIMING



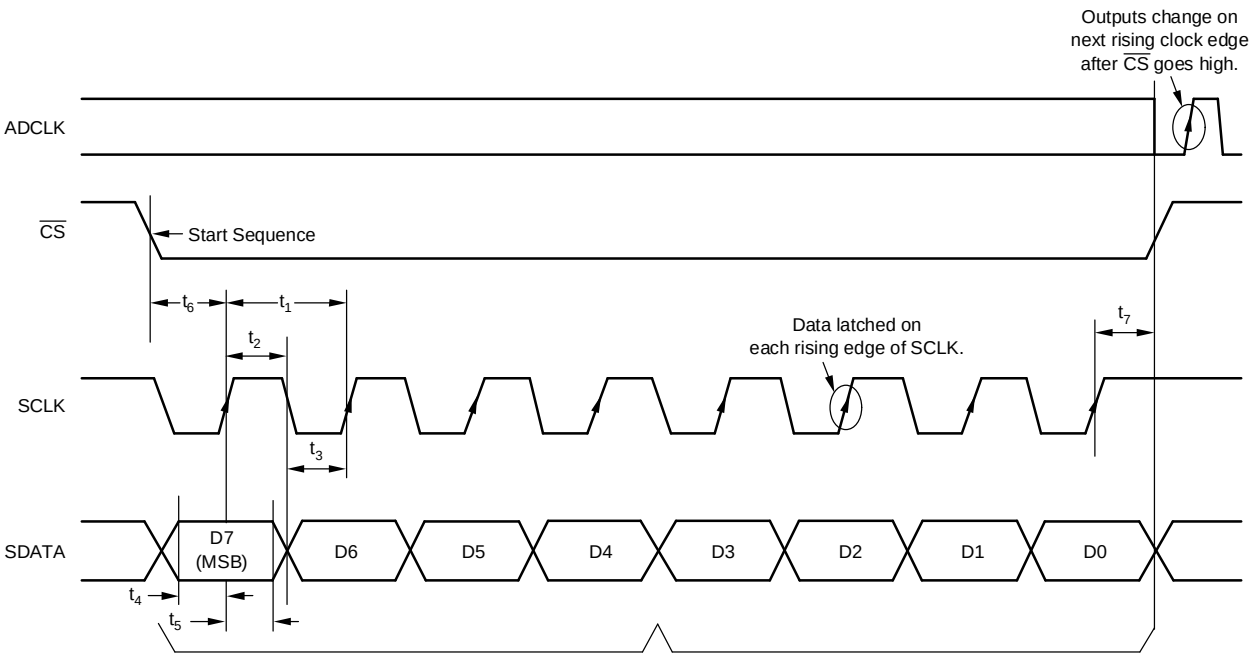
NOTE: 10µs < t_1 < 50ms; 10µs < t_2 < 50ms; −10ms < t_3 < 10ms; t_4 > 10ms; t_5 > 100ns; t_6 > 100ns; t_7 > 10ms; and t_8 > 100µs.

POWER-DOWN TIMING



NOTE: The shown power−up time is based on 1µF bypass capacitors on the reference pins. See the *Theory of Operation* section for details.

SERIAL INTERFACE TIMING



NOTE: Data is shifted in MSB first.

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_1	Serial CLK Period	50			ns
t_2	Serial CLK High Time	20			ns
t_3	Serial CLK Low Time	20			ns
t_4	Data Setup Time	5			ns
t_5	Data Hold Time	5			ns
t_6	$\overline{CS}$ Fall to SCLK Rise	8			ns
t_7	SCLK Rise to $\overline{CS}$ Rise	8			ns

SERIAL INTERFACE REGISTERS

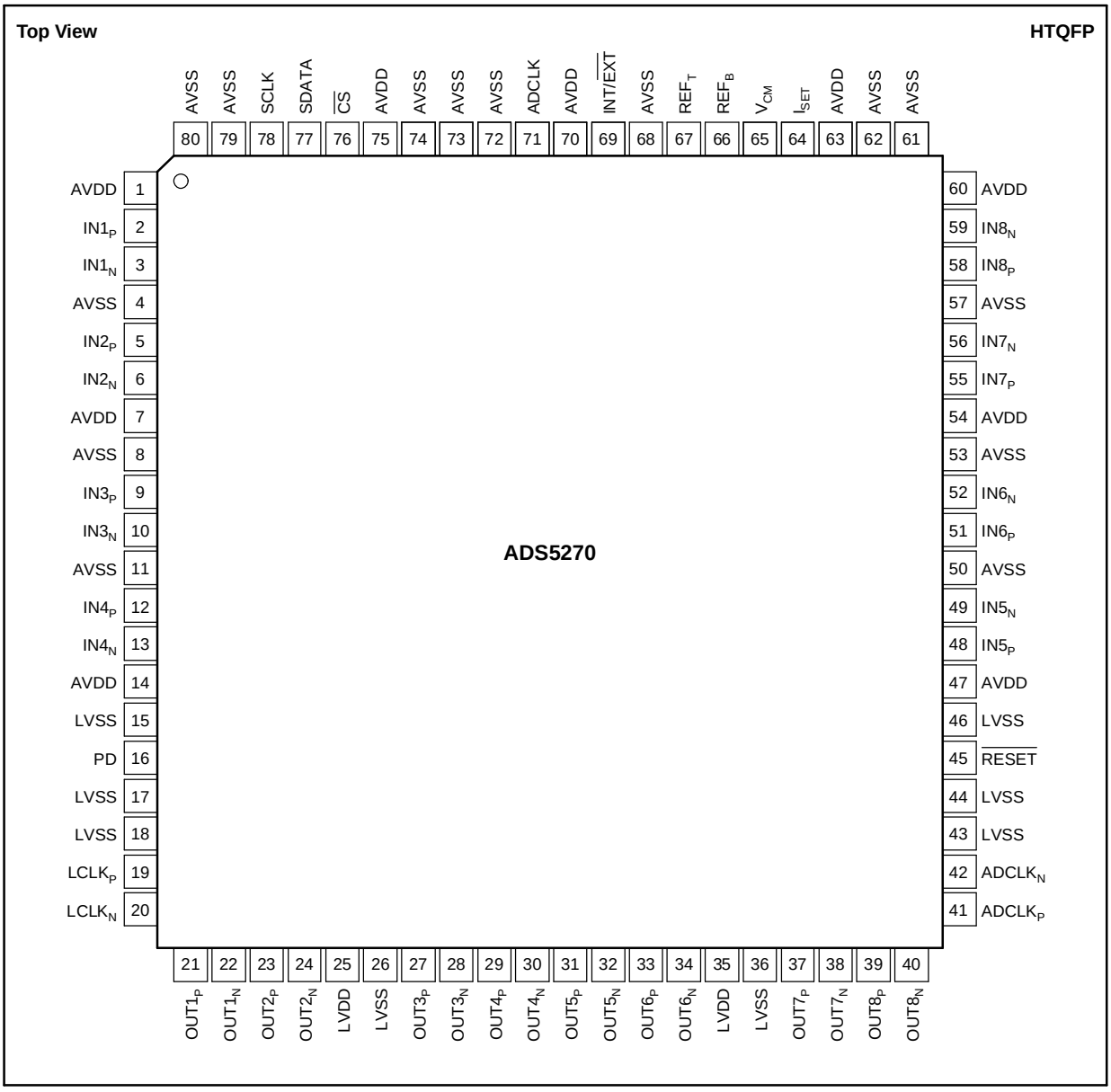
ADDRESS				DATA				DESCRIPTION	REMARKS
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**		
0	0	0	0					**LVDS BUFFERS (Register 0)**	All Data Outputs
				0	0			Normal ADC Output	(default after reset)
				0	1			Deskew Pattern	
				1	0			Sync Pattern	See *Test Patterns*
				1	1			Custom Pattern	
						0	0	Output Current in LVDS = 3.5mA	(default after reset)
						0	1	Output Current in LVDS = 2.5mA	
						1	0	Output Current in LVDS = 4.5mA	
						1	1	Output Current in LVDS = 6.0mA	
0	0	0	1					**CLOCK CURRENT (Register 1)**	
				0	X	X	0	LVDS Clock Output Current	I_{OUT} = 3.5mA (default)
				0	X	X	1	2x LVDS Clock Output Current	I_{OUT} = 7.0mA
0	0	0	1					**LSB/MSB MODE (Register 1)**	
				0	0	X	X	LSB First Mode	(default after reset)
				0	1	X	X	MSB First Mode	
0	0	1	0					**POWER-DOWN ADC CHANNELS (Register 2)**	
				X	X	X	X	Power-Down Channels 1 to 4; D3 is for Channel 4 and D0 for Channel 1	Example: 1010 Powers Down Channels 4 and 2 and Keeps Channels 1 and 3 Active
0	0	1	1					**POWER-DOWN ADC CHANNELS (Register 3)**	
				X	X	X	X	Power-Down Channels 5 to 8; D3 is for Channel 8 and D0 for Channel 5	
								CUSTOM PATTERN (Registers 4–6)	
				D3	**D2**	**D1**	**D0**	Bits for Custom Pattern	See *Test Patterns*
0	1	0	0	X	X	X	X		
0	1	0	1	X	X	X	X		
0	1	1	0	X	X	X	X		

TEST PATTERNS

Serial Output(1)	**LSB**											**MSB**
ADC Output(2)	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11
Deskew Pattern	1	0	1	0	1	0	1	0	1	0	1	0
Sync Pattern	0	0	0	0	0	0	1	1	1	1	1	1
Custom Pattern(3)	D0(4)	D1(4)	D2(4)	D3(4)	D0(5)	D1(5)	D2(5)	D3(5)	D0(6)	D1(6)	D2(6)	D3(6)

(1) The serial output stream comes out LSB first by default.
(2) D11...D0 represent the 12 output bits from the ADC.
(3) D0(4) represents the content of bit D0 of register 4, D3(6) represents the content of bit D3 of register 6, etc.

PIN CONFIGURATION



PIN DESCRIPTIONS

NAME	PIN #	I/O	DESCRIPTION
ADCLK	71	I	Data Converter Clock Input
$ADCLK_N$	42	O	Negative LVDS ADC Clock Output
$ADCLK_P$	41	O	Positive LVDS ADC Clock Output
AVDD	1, 7, 14, 47, 54, 60, 63, 70, 75	I	Analog Power Supply
AVSS	4, 8, 11, 50, 53, 57, 61, 62, 68, 72–74, 79, 80	I	Analog Ground
$\overline{CS}$	76	I	Chip Select; 0 = Select, 1 = No Select
$IN1_N$	3	I	Channel 1 Differential Analog Input Low
$IN1_P$	2	I	Channel 1 Differential Analog Input High
$IN2_N$	6	I	Channel 2 Differential Analog Input Low
$IN2_P$	5	I	Channel 2 Differential Analog Input High
$IN3_N$	10	I	Channel 3 Differential Analog Input Low
$IN3_P$	9	I	Channel 3 Differential Analog Input High
$IN4_N$	13	I	Channel 4 Differential Analog Input Low
$IN4_P$	12	I	Channel 4 Differential Analog Input High
$IN5_N$	49	I	Channel 5 Differential Analog Input Low
$IN5_P$	48	I	Channel 5 Differential Analog Input High
$IN6_N$	52	I	Channel 6 Differential Analog Input Low
$IN6_P$	51	I	Channel 6 Differential Analog Input High
$IN7_N$	56	I	Channel 7 Differential Analog Input Low
$IN7_P$	55	I	Channel 7 Differential Analog Input High
$IN8_N$	59	I	Channel 8 Differential Analog Input Low
$IN8_P$	58	I	Channel 8 Differential Analog Input High
INT/$\overline{EXT}$	69	I	Internal/External Reference Select; 0 = External, 1 = Internal. Weak pull-up to supply.
I_{SET}	64	I/O	Bias Current Setting Resistor of 56.2kΩ to Ground
$LCLK_N$	20	O	Negative LVDS Clock
$LCLK_P$	19	O	Positive LVDS Clock
LVDD	25, 35	I	LVDS Power Supply
LVSS	15, 17, 18, 26, 36, 43, 44, 46	I	LVDS Ground
$OUT1_N$	22	O	Channel 1 Negative LVDS Data Output
$OUT1_P$	21	O	Channel 1 Positive LVDS Data Output
$OUT2_N$	24	O	Channel 2 Negative LVDS Data Output
$OUT2_P$	23	O	Channel 2 Positive LVDS Data Output
$OUT3_N$	28	O	Channel 3 Negative LVDS Data Output
$OUT3_P$	27	O	Channel 3 Positive LVDS Data Output
$OUT4_N$	30	O	Channel 4 Negative LVDS Data Output
$OUT4_P$	29	O	Channel 4 Positive LVDS Data Output
$OUT5_N$	32	O	Channel 5 Negative LVDS Data Output
$OUT5_P$	31	O	Channel 5 Positive LVDS Data Output
$OUT6_N$	34	O	Channel 6 Negative LVDS Data Output
$OUT6_P$	33	O	Channel 6 Positive LVDS Data Output
$OUT7_N$	38	O	Channel 7 Negative LVDS Data Output
$OUT7_P$	37	O	Channel 7 Positive LVDS Data Output
$OUT8_N$	40	O	Channel 8 Negative LVDS Data Output
$OUT8_P$	39	O	Channel 8 Positive LVDS Data Output
PD	16	I	Power-Down; 0 = Normal, 1 = Power-Down
REF_B	66	I/O	Reference Bottom Voltage (2Ω resistor in series with a 0.1µF capacitor to ground)
REF_T	67	I/O	Reference Top Voltage (2Ω resistor in series with a 0.1µF capacitor to ground)
$\overline{RESET}$	45	I	Reset to Default; 0 = Reset, 1 = Normal. Weak pull-down to ground.
SCLK	78	I	Serial Data Clock
SDATA	77	I	Serial Data Input
V_{CM}	65	O	Common-Mode Output Voltage

DEFINITION OF SPECIFICATIONS

Analog Bandwidth

The analog input frequency at which the spectral power of the fundamental frequency (as determined by FFT analysis) is reduced by 3dB.

Aperture Delay

The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs.

Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay.

Clock Duty Cycle

Pulse width high is the minimum amount of time that the ADCLK pulse should be left in logic '1' state to achieve rated performance. Pulse width low is the minimum time that the ADCLK pulse should be left in a low state (logic '0'). At a given clock rate, these specifications define an acceptable clock duty cycle.

Differential Nonlinearity (DNL)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation of any single LSB transition at the digital output from an ideal 1 LSB step at the analog input. If a device claims to have no missing codes, it means that all possible codes (for a 12-bit converter, 4096 codes) are present over the full operating range.

Effective Number of Bits (ENOB)

The ENOB is a measure of converter performance as compared to the theoretical limit based on quantization noise.

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02}$$

Integral Nonlinearity (INL)

INL is the deviation of the transfer function from a reference line measured in fractions of 1 LSB using a *best straight line* or *best fit* determined by a least square curve fit. INL is independent from effects of offset, gain or quantization errors.

Maximum Conversion Rate

The encode rate at which parametric testing is performed. This is the maximum sampling rate where certified operation is given.

Minimum Conversion Rate

This is the minimum sampling rate where the ADC still works.

Signal-to-Noise and Distortion (SINAD)

SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but not including DC.

$$\text{SINAD} = 10\text{Log}_{10}\frac{P_S}{P_N + P_D}$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the full-scale range of the converter.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at DC and the first eight harmonics.

$$\text{SNR} = 10\text{Log}_{10}\frac{P_S}{P_N}$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the full-scale range of the converter.

Spurious-Free Dynamic Range

The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone, Third-Order Intermodulation Distortion

Two-tone IMD3 is the ratio of power of the fundamental (at frequencies f_1 and f_2) to the power of the worst spectral component of third-order intermodulation distortion at either frequency $2f_1 - f_2$ or $2f_2 - f_1$. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the full-scale range of the converter.

TYPICAL CHARACTERISTICS

Typical values are at T_A = +25°C, clock frequency = maximum specified, 50% clock duty cycle, AVDD = 3.3V, LVDD = 3.3V, –1dBFS, I_{SET} = 56.2kΩ, internal voltage reference, and LVDS buffer current at 3.5mA per channel, unless otherwise noted.

SPECTRAL PERFORMANCE

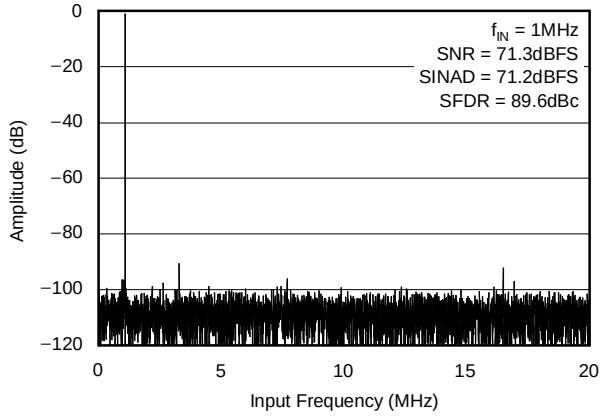


Figure 1.

SPECTRAL PERFORMANCE

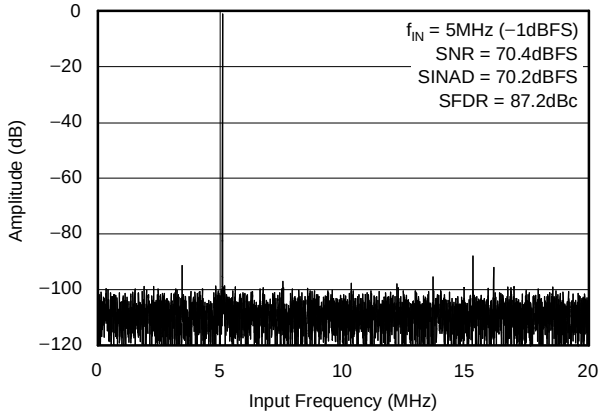


Figure 2.

SPECTRAL PERFORMANCE

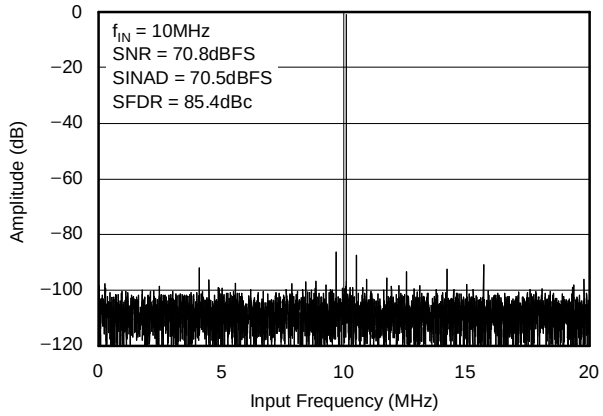


Figure 3.

SPECTRAL PERFORMANCE

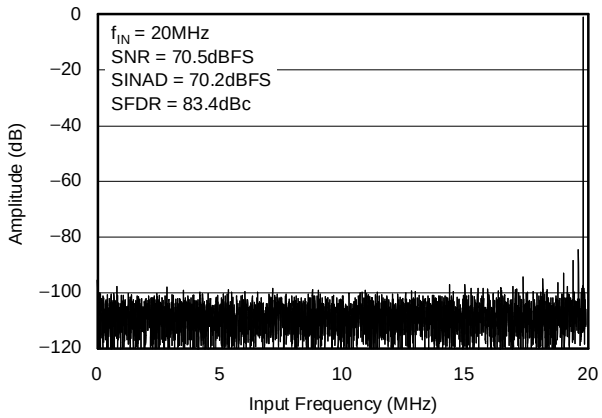


Figure 4.

INTERMODULATION DISTORTION

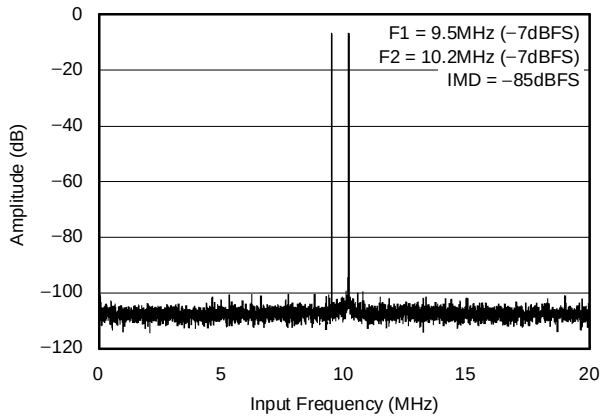


Figure 5.

DIFFERENTIAL NONLINEARITY

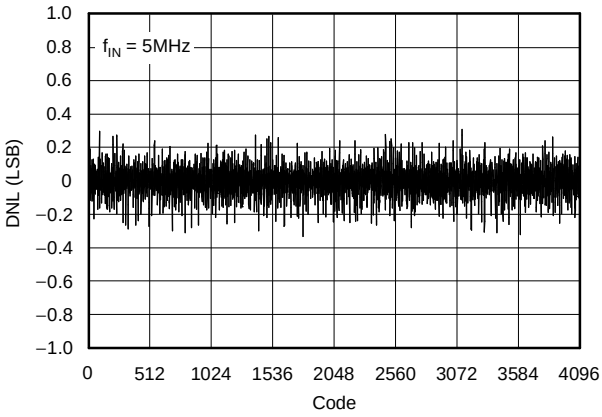


Figure 6.

TYPICAL CHARACTERISTICS (continued)

Typical values are at T_A = +25°C, clock frequency = maximum specified, 50% clock duty cycle, AVDD = 3.3V, LVDD = 3.3V, –1dBFS, I_{SET} = 56.2kΩ, internal voltage reference, and LVDS buffer current at 3.5mA per channel, unless otherwise noted.

INTEGRAL NONLINEARITY

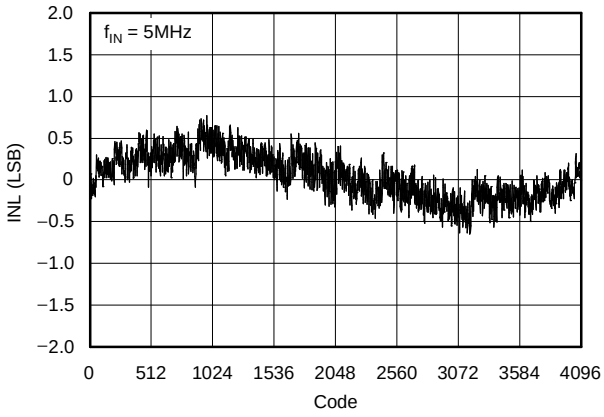


Figure 7.

SWEPT INPUT POWER

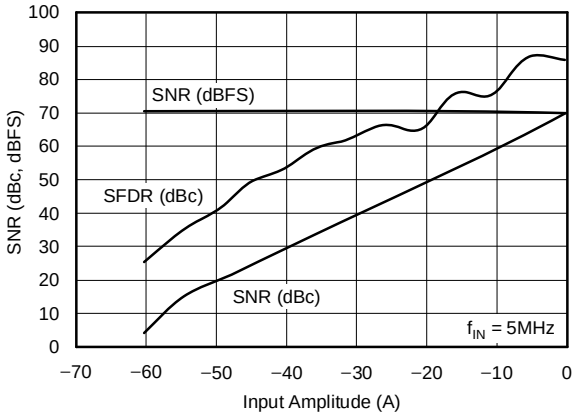


Figure 8.

SWEPT INPUT POWER

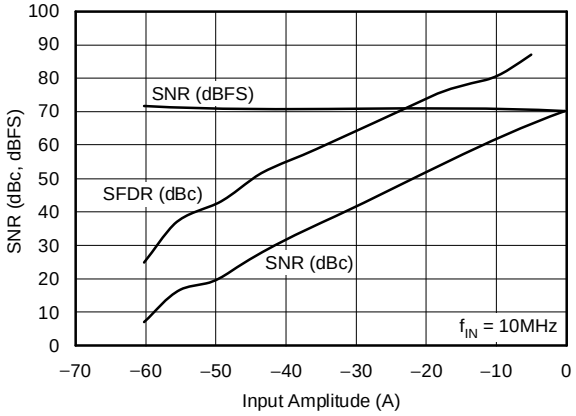


Figure 9.

DYNAMIC PERFORMANCE vs DUTY CYCLE

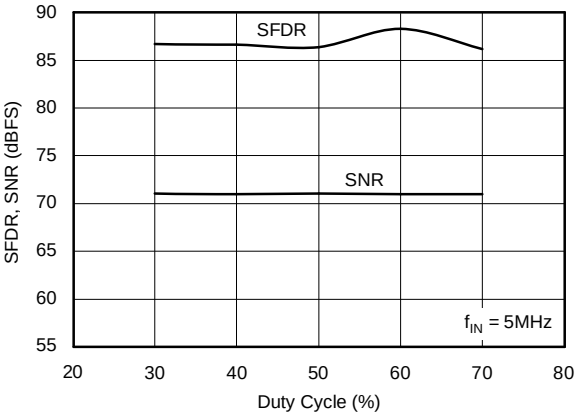


Figure 10.

DYNAMIC PERFORMANCE vs INPUT FREQUENCY

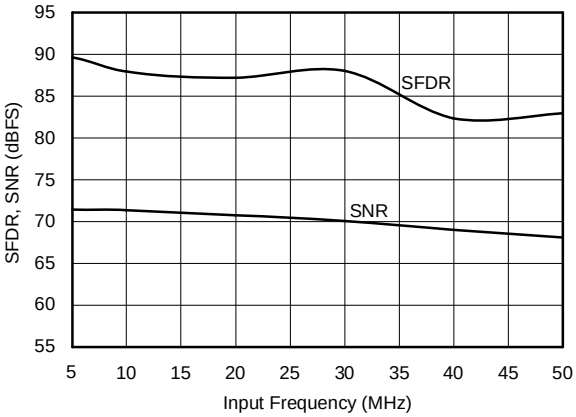


Figure 11.

DYNAMIC PERFORMANCE vs SAMPLE RATE

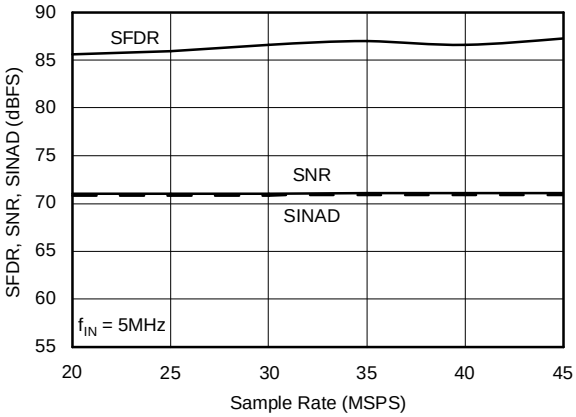


Figure 12.

TYPICAL CHARACTERISTICS (continued)

Typical values are at T_A = +25°C, clock frequency = maximum specified, 50% clock duty cycle, AVDD = 3.3V, LVDD = 3.3V, –1dBFS, I_{SET} = 56.2kΩ, internal voltage reference, and LVDS buffer current at 3.5mA per channel, unless otherwise noted.

DYNAMIC PERFORMANCE vs SAMPLE RATE

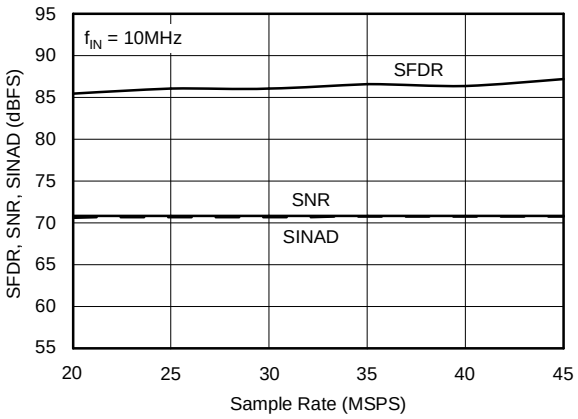


Figure 13.

SUPPLY CURRENT vs SAMPLE RATE

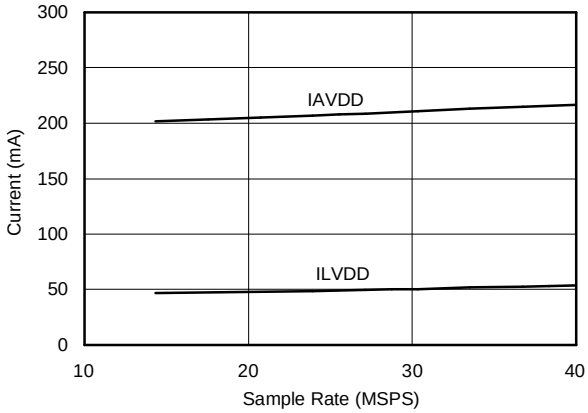


Figure 14.

THEORY OF OPERATION

OVERVIEW

The ADS5270 is an 8-channel, high-speed, CMOS ADC. It consists of a high-performance sample-and-hold circuit at the input, followed by a 12-bit ADC. The 12 bits given out by each channel are serialized and sent out on a single pair of pins in LVDS format. All eight channels of the ADS5270 operate from a single clock referred to as ADCLK. The sampling clocks for each of the eight channels are generated from the input clock using a carefully matched clock buffer tree. The 12x clock required for the serializer is generated internally from ADCLK using a phase lock loop (PLL). A 6x and a 1x clock are also output in LVDS format along with the data to enable easy data capture. The ADS5270 operates from internally generated reference voltages that are trimmed to improve to a high level of accuracy. This feature eliminates the need for external routing of reference lines and also improves matching of the gain across devices. The nominal values of REF_T and REF_B are 1.95V and 0.95V, respectively. These values imply that a differential input of –1V corresponds to the zero code of the ADC, and a differential input of +1V corresponds to the full-scale code (4095 LSB). V_{CM} (common-mode voltage of REF_T and REF_B) is also made available externally through a pin, and is nominally 1.45V.

The ADC employs a pipelined converter architecture consisting of a combination of multi-bit and single-bit internal stages. Each stage feeds its data into the digital error correction logic, ensuring excellent differential linearity and no missing codes at the 12-bit level. The pipeline architecture results in a data latency of 6.5 clock cycles.

The output of the ADC goes to a serializer that operates from a 12x clock generated by the PLL. The 12 data bits from each channel are serialized and sent LSB first. In addition to serializing the data, the serializer also generates a 1x clock and a 6x clock. These clocks are generated in the same way the serialized data is generated, so these clocks maintain perfect synchronization with the data. The data and clock outputs of the serializer are buffered externally using LVDS buffers. Using LVDS buffers to transmit data externally has multiple advantages, such as a reduced number of output pins (saving routing space on the board), reduced power consumption, and reduced effects of digital noise coupling to the analog circuit inside the ADS5270.

The ADS5270 operates from two sets of supplies and grounds. The analog supply/ground set is denoted as AVDD/AVSS, while the digital set is denoted by LVDD/LVSS.

DRIVING THE ANALOG INPUTS

The analog input biasing is shown in Figure 15. The inputs are biased internally using two 600Ω resistors to enable AC-coupling. A resistor greater than 20Ω is recommended in series with each input pin.

A 4pF sampling capacitor is used to sample the inputs. The choice of the external AC-coupling capacitor is dictated by the attenuation at the lowest desired input frequency of operation. The attenuation resulting from using a 10nF AC-coupling capacitor is 0.04%.

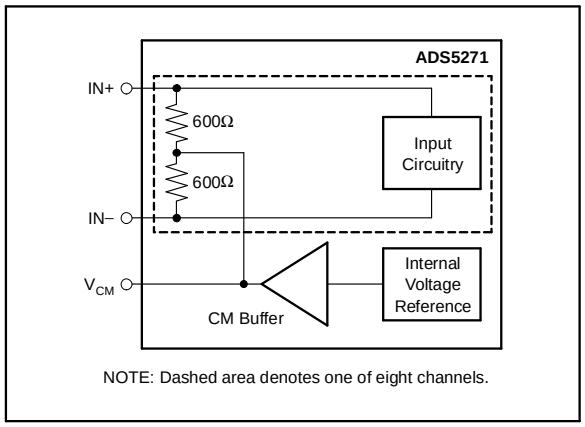


Figure 15. Analog Input Bias Circuitry

If the input is DC-coupled, then the output common-mode voltage of the circuit driving the ADS5270 should match the V_{CM} (which is provided as an output pin) to within ±50mV. It is recommended that the output common-mode of the driving circuit be derived from V_{CM} provided by the device.

Figure 16 shows a detailed RLC model of the sample-and-hold circuit. The circuit operates in two phases. In the sample phase, the input is sampled on two capacitors that are nominally 4pF. The sampling circuit consists of a low-pass RC filter at the input to filter out noise components that might be differentially coupled on the input pins. The next phase is the hold phase wherein the voltage sampled on the capacitors is transferred (using the amplifier) to a subsequent pipeline ADC stage.

INPUT OVER-VOLTAGE RECOVERY

The differential full-scale range supported by the ADS5270 is nominally 2.03V. The ADS5270 is specially designed to handle an over-voltage condition where the differential peak-to-peak voltage can exceed up to twice the ADC full-scale range. If the input common-mode is not considerably off from V_{CM} during overload (less than 300mV around the nominal value of 1.45V), recovery from an over-voltage pulse input of twice the amplitude of a full-scale pulse is expected to be within three clock cycles when the input switches from overload to zero signal. All of the amplifiers in the SHA and ADC are specially designed for excellent recovery from an overload signal.

In most applications, the ADC inputs are driven with differential sinusoidal inputs. While the pulse-type signal remains at peak overload conditions throughout its HIGH state, the sinusoid signal only attains peak overload intermittently, at its minima and maxima. This condition is much less severe for the ADC input and the recovery of the ADC output (to 1% of full-scale around the expected code). This typically happens within the second clock when the input is driven with a sinusoid of amplitude equal to twice that of the ADC differential full-scale range.

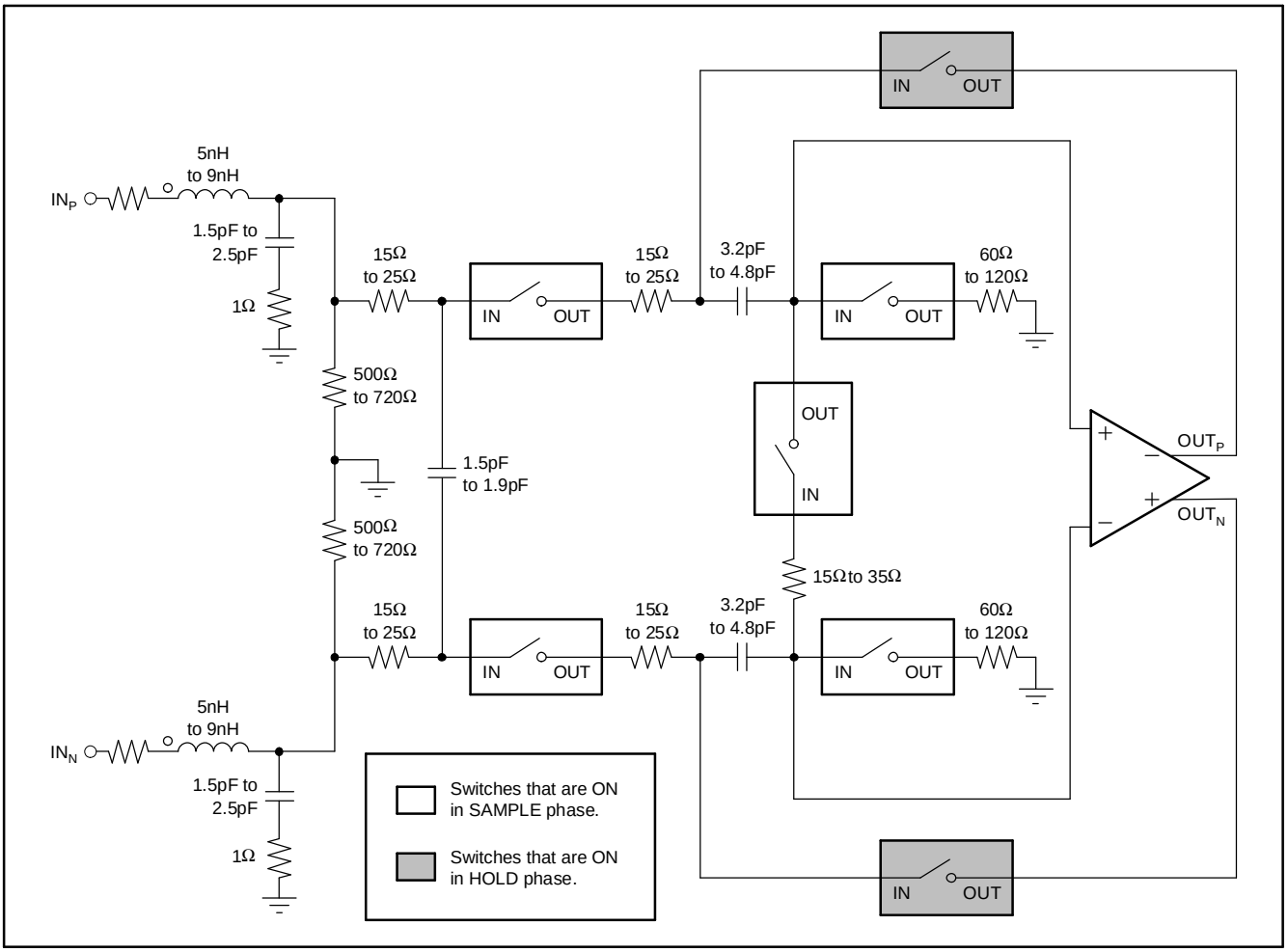


Figure 16. Overall Structure of the Sample-and-Hold Circuit

REFERENCE CIRCUIT DESIGN

The digital beam-forming algorithm relies on gain matching across all receiver channels. A typical system would have about 12 octal ADCs on the board. In such a case, it is critical to ensure that the gain is matched, essentially requiring the reference voltages seen by all the ADCs to be the same. Matching references within the eight channels of a chip is done by using a single internal reference voltage buffer. Trimming the reference voltages on each chip during production ensures the reference voltages are well-matched across different chips.

All bias currents required for the internal operation of the device are set using an external resistor to ground at pin I_{SET}. Using a 56kΩ resistor on I_{SET} generates an internal reference current of 20µA. This current is mirrored internally to generate the bias current for the internal blocks. Using a larger external resistor at I_{SET} reduces the reference bias current and thereby scales down the device operating power. However, it is recommended that the external resistor be within 10% of the specified value of 56kΩ so that the internal bias margins for the various blocks are proper.

Buffering the internal bandgap voltage also generates a voltage called V_{CM}, which is set to the midlevel of REF_T and REF_B, and is accessible on a pin. It is meant as a reference voltage to derive the input common-mode in case the input is directly coupled. It can also be used to derive the reference common-mode voltage in the external reference mode.

When using the internal reference mode, a 2Ω resistor should be added between the reference pins (REF_T and REF_B) and the decoupling capacitor, as shown in Figure 17. If the device is used in the external reference mode, this 2Ω resistor is not required.

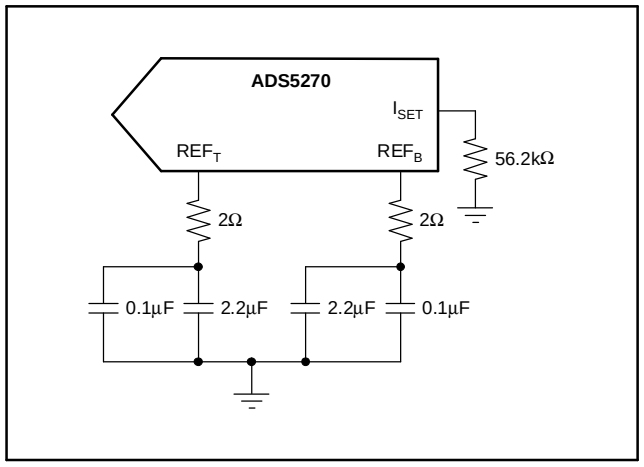


Figure 17. Internal Reference Mode

The device also supports the use of external reference voltages. This mode involves forcing REF_T and REF_B externally. In this mode, the internal reference buffer is tri-stated. Since the switching current for the eight ADCs come from the externally-forced references, it is possible for the performance to be slightly less than when the internal references are used. It should be noted that in this mode, V_{CM} and I_{SET} continue to be generated from the internal bandgap voltage, as in the internal reference mode. It is therefore important to ensure that the common-mode voltage of the externally-forced reference voltages matches to within 50mV of V_{CM}. The state of the reference voltages during various combinations of PD and INT/$\overline{\text{EXT}}$ is shown in Table 1.

Table 1. State of Reference Voltages for Various Combinations of PD and INT/$\overline{\text{EXT}}$

PD	0	0	1	1
INT/$\overline{\text{EXT}}$	0	1	0	1
REF_T	Tri-State	1.95V	Tri-State	Tri-State
REF_B	Tri-State	0.95V	Tri-State	Tri-State
V_{CM}	1.45V	1.45V	Tri-State(1)	Tri-State(1)

CLOCKING

The eight channels on the chip operate from a single ADCLK input. To ensure that the aperture delay and jitter are same for all the channels, a clock tree network is used to generate individual sampling clocks to each channel. The clock paths for all the channels are matched from the source point all the way to the sample-and-hold amplifier. This ensures that the performance and timing for all the channels are identical. The use of the clock tree for matching introduces an aperture delay, which is defined as the delay between the rising edge of ADCLK and the actual instant of sampling. The aperture delays for all the channels are matched to the best possible extent. However, a mismatch of ±20ps (±3σ) could exist between the aperture instants of the eight ADCs within the same chip. However, the aperture delays of ADCs across two different chips can be several hundred picoseconds apart. Another critical specification is the aperture jitter that is defined as the uncertainty of the sampling instant. The gates in the clock path are designed to provide an rms jitter of approximately 1ps.

Ideally, the input ADCLK should have a 50% duty cycle. However, while routing ADCLK to different components onboard, the duty cycle of the ADCLK reaching the ADS5270 could deviate from 50%. A smaller (or larger) duty cycle reduces the time available for sample or hold phases of each circuit, and is therefore not optimal. For this reason, the internal PLL is used to generate an internal clock that has 50% duty cycle. The input sampling instant,

however, is determined by the rising edge of the external clock and is not affected by jitter in the PLL. In addition to generating a 50% duty cycle clock for the ADC, the PLL also generates a 12x clock that is used by the serializer to convert the parallel data from the ADC to a serial stream of bits.

The use of the PLL automatically dictates the minimum sample rate to be about 20MSPS. The PLL also requires the input clock to be free-running. If the input clock is momentarily stopped (for a duration of less than 300ns) then the PLL would require approximately 10μs to lock back to the input clock frequency.

LVDS BUFFERS

The LVDS buffer has two current sources, as shown in Figure 18. OUT_P and OUT_N are loaded externally by a resistive load that is ideally about 100Ω. Depending on whether the data is 0 or 1, the currents are directed in one direction or the other through the resistor. The LVDS buffer has four current settings. The default current setting is 3.5mA, and provides a differential drop of about ±350mV across the 100Ω resistor.

The single-ended output impedance of the LVDS drivers is very high because they are current-source driven. If there are excessive reflections from the receiver, it might be necessary to place a 100Ω termination resistor across the outputs of the LVDS drivers to minimize the effect of reflections. In such a situation, the output current of the LVDS drivers can be increased to regain the output swing.

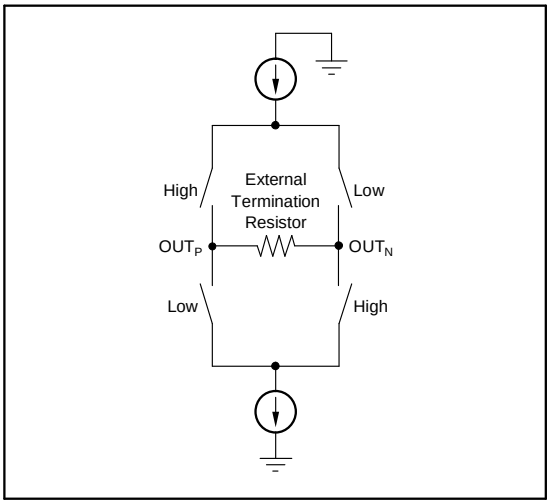


Figure 18. LVDS Buffer

The LVDS buffer gets data from a serializer that takes the output data from each channel and serializes it into a single data stream. For a clock frequency of 40MHz, the data rate output of the serializer is 480Mbps. The data comes out LSB first, with a register programmability that allows it to revert to MSB first. The serializer also gives out a 1x clock and a 6x clock. The 6x clock (denoted as $LCLK_P/LCLK_N$) is meant to synchronize the capture of the LVDS data.

Deskew mode can be enabled as well, using a register setting. This mode gives out a data stream of alternate 0s and 1s and can be used to determine the relative delay between the 6x clock and the output data for optimum capture. A 1x clock is also generated by the serializer and transmitted through the LVDS buffer. The 1x clock (referred to as $ADCLK_P/ADCLK_N$) is used to determine the start of the 12-bit data frame. Sync mode (enabled through a register setting) gives out a data of six 0s followed by six 1s. Using this mode, the 1x clock can be used to determine the start of the data frame. In addition to the deskew mode pattern and the sync mode pattern, a custom pattern can be defined by the user and output from the LVDS buffer. The LVDS buffers are tri-stated in the power-down mode. The LVDS outputs are weakly forced to 1.2V through 10kΩ resistors (from each output pin to 1.2V).

NOISE COUPLING ISSUES

High-speed mixed signals are sensitive to various types of noise coupling. One of the main sources of noise is the switching noise from the serializer and the output buffers. Maximum care is taken to isolate these noise sources from the sensitive analog blocks. As a starting point, the analog and digital domains of the chip are clearly demarcated. AVDD and AVSS are used to denote the supplies for the analog sections, while LVDD and LVSS are used to denote the digital supplies. Care is taken to ensure that there is minimal interaction between the supply sets within the device. The extent of noise coupled and transmitted from the digital to the analog sections depends on the following:

1. The effective inductances of each of the supply/ground sets.
2. The isolation between the digital and analog supply/ground sets.

Smaller effective inductance of the supply/ground pins leads to better suppression of the noise. For this reason, multiple pins are used to drive each supply/ground. It is also critical to ensure that the impedances of the supply and ground lines on board are kept to the minimum possible values. Use of ground planes in the board as well as large decoupling capacitors between the supply and ground lines are necessary to get the best possible SNR from the device.

It is recommended that the isolation be maintained onboard by using separate supplies to drive AVDD and LVDD, as well as separate ground planes for AVSS and LVSS.

The use of LVDS buffers reduces the injected noise considerably, compared to CMOS buffers. The current in the LVDS buffer is independent of the direction of switching. Also, the low output swing as well as the differential nature of the LVDS buffer results in low-noise coupling.

POWER-DOWN MODE

The ADS5270 has a power-down pin, referred to as PD. Pulling PD high causes the device to enter the power-down mode. In this mode, the reference and clock circuitry, as well as all the channels, are powered down. Device power consumption drops to less than 100mW in this mode. In power-down mode, the internal buffers driving REF_T and REF_B are tri-stated and their outputs are forced to a voltage roughly equal to half of the voltage on AVDD. Speed of recovery from power-down mode depends on the value of the external capacitance on the REF_T and REF_B pins. For capacitances on REF_T and REF_B less than 1µF, the reference voltages settle to within 1% of their steady-state values in less than 500µs. Individual channels can also be selectively powered down by programming registers.

The ADS5270 also has an internal circuit that monitors the state of stopped clocks. If ADCLK is stopped for longer than 300ns (or if it runs at a speed less than 3MHz), this monitoring circuit generates a logic signal that puts the device in a partial power-down state. As a result, the power consumption of the device is reduced when ADCLK is stopped. The recovery from such a partial power-down takes approximately 100µs; this is described in Table 2.

RESET

After the supplies have stabilized, it is necessary to give the device an active RESET pulse. This results in all internal registers resetting to their default value of 0 (inactive). Without a reset, it is possible that some registers may be in their non-default state on power-up. This may cause the device to malfunction. When a reset is active, the device outputs '0' code on all channels. However, the LVDS output clocks are unaffected by reset.

LAYOUT OF PCB WITH PowerPAD THERMALLY-ENHANCED PACKAGES

The ADS5270 is housed in an 80-lead PowerPAD thermally-enhanced package. To make optimum use of the thermal efficiencies designed into the PowerPAD package, the printed circuit board (PCB) must be designed with this technology in mind. Please refer to SLMA004 PowerPAD brief *PowerPAD Made Easy* (refer to our web site at www.ti.com), which addresses the specific considerations required when integrating a PowerPAD package into a PCB design. For more detailed information, including thermal modeling and repair procedures, please see the technical brief SLMA002, *PowerPAD Thermally-Enhanced Package* (www.ti.com).

Interfacing High-Speed LVDS Outputs (SBOA104), an application report discussing the design of a simple deserializer that can deserialize LVDS outputs up to 840Mbps, can also be found on the TI web site (www.ti.com).

CONNECTING HIGH-SPEED, MULTI-CHANNEL ADCs TO XILINX FPGAs

A separate application note (XAPP774) describing how to connect TI's high-speed, multi-channel ADCs with serial LVDS outputs to Xilinx FPGAs can be downloaded directly from the Xilinx web site (http://www.xilinx.com).

Table 2. Time Constraints Associated with Device Recovery from Power-Down and Clock Stoppage

DESCRIPTION	TYP	REMARKS
Recovery from power-down mode (PD = 1 to PD = 0).	500µs	Capacitors on REF_T and REF_B less than 1µF.
Recovery from momentary clock stoppage (< 300ns).	10µs	
Recovery from extended clock stoppage (> 300ns).	100µs	

Changes from D Revision (September 2005) to E Revision **Page**

- Changed component image to have TI logo. 1
- Changed X to x (for instance, 12X, 6X, 1X, etc) globally. 1
- Changed ISET to I_{SET} globally. 1
- Changed 56kΩ to 56.2kΩ globally. 1
- Changed fourth bullet of Features section. 1
- Deleted eighth and 12th bullets of Features section. 1
- Changed *Synch* to *Bit* in 11th bullet of Features section. 1
- Added 14th bullet to Features section. 1
- Deleted *parallel* from first paragraph of Description section. 1
- Added Related Products table. 1
- Changed second paragraph of Description section. 1
- Changed order of *PowerPAD TQFP-80* in fourth paragraph of Description section. 1
- Changed front page figure. 1
- Changed structure of Ordering Information table; content remains the same. 2
- Changed placement of second cross reference in Ordering Information table. 2
- Changed first footnote of Ordering Information table. 2
- Changed Absolute Maximum table and footnotes. 2
- Changed Recommended Operating Conditions table and footnotes. 3
- Changed Electrical Characteristics table, conditions, and footnotes. 4
- Changed Electrical Characteristics table, conditions, and footnotes. 5
- Changed Reference Selection table. 5
- Changed AC Characteristics table and conditions. 6
- Changed LVDS table, conditions, and footnotes. 7
- Deleted device name row of Switching Characteristics table. 7
- Changed second and fifth rows of Switching Characteristics table. 7
- Changed unit value of ps to ps rms in third row of Switching Characteristics table. 7
- Changed LVDS timing figure. 8
- Changed Reset timing figure. 8
- Changed Power-Down timing figure. 9
- Changed Serial interface timing figure and table. 9
- Changed Serial Interface Registers table. 10
- Changed Test Patterns table. 10
- Changed pin configuration figure. 11
- Changed Pin Descriptions table. 12
- Changed Typical Characteristics conditions to include T_A = +25°C and I_{SET} = 56.2kΩ. 14
- Changed Figure 1. 14
- Changed Figure 2. 14
- Changed Figure 3. 14
- Changed Figure 4. 14
- Changed Figure 5. 14
- Changed Typical Characteristics conditions to include T_A = +25°C and I_{SET} = 56.2kΩ. 15
- Changed Figure 12. 15
- Changed Typical Characteristics conditions to include T_A = +25°C and I_{SET} = 56.2kΩ. 16
- Changed Figure 13. 16
- Changed Figure 14. 16
- Deleted Figure 15 (Power Dissipation vs Temperature). 16
- Changed figure numbers in Theory of Operation to reflect addition of figure numbers in Typical Characteristics. 17
- Changed 2V to 1.95V, 1V to 0.95V, and 1.5V to 1.45V in first paragraph of *Overview* section in Theory of Operation. 17

- Changed eighth and 12th sentences of first paragraph of *Overview* section in Theory of Operation. 17
- Changed first paragraph of *Driving the Analog Inputs* section of Theory of Operation. 17
- Added second paragraph of *Driving the Analog Inputs* section of Theory of Operation. 17
- Changed Figure 16. 17
- Deleted second paragraph of *Driving the Analog Inputs* section in Theory of Operation. 17
- Added fourth paragraph of *Driving the Analog Inputs* section in Theory of Operation. 18
- Deleted fourth paragraph of *Driving the Analog Inputs* and Figure 17 (Input Circuitry) in Theory of Operation. 18
- Changed Input Over-Voltage Recovery section. 18
- Added Figure 17. 18
- Deleted *heavily* from first sentence of first paragraph of *Reference Circuit Design* section in Theory of Operation. 19
- Changed third paragraph of *Reference Circuit Design* section of Theory of Operation. 19
- Changed fourth paragraph of *Reference Circuit Design* section of Theory of Operation. 19
- Changed Figure 18. 19
- Added last sentence to fifth paragraph of *Reference Circuit Design* section of Theory of Operation and Table 1. 19
- Changed *Clocking* section of Theory of Operation. 19
- Changed *LVDS Buffers* section in Theory of Operation. 20
- Changed *Power-Down Mode* section in Theory of Operation. 21
- Added Table 2. 21
- Deleted *Supply Sequence* section. 21
- Added *Reset* section. 21
- Changed *Layout of PCB with PowerPAD Thermally-Enhanced Packages* section in Theory of Operation. 21
- Added *Connecting High-Speed, Multi-Channel ADCs to XILINX FPGAs* section in Theory of Operation. 21

PACKAGING INFORMATION

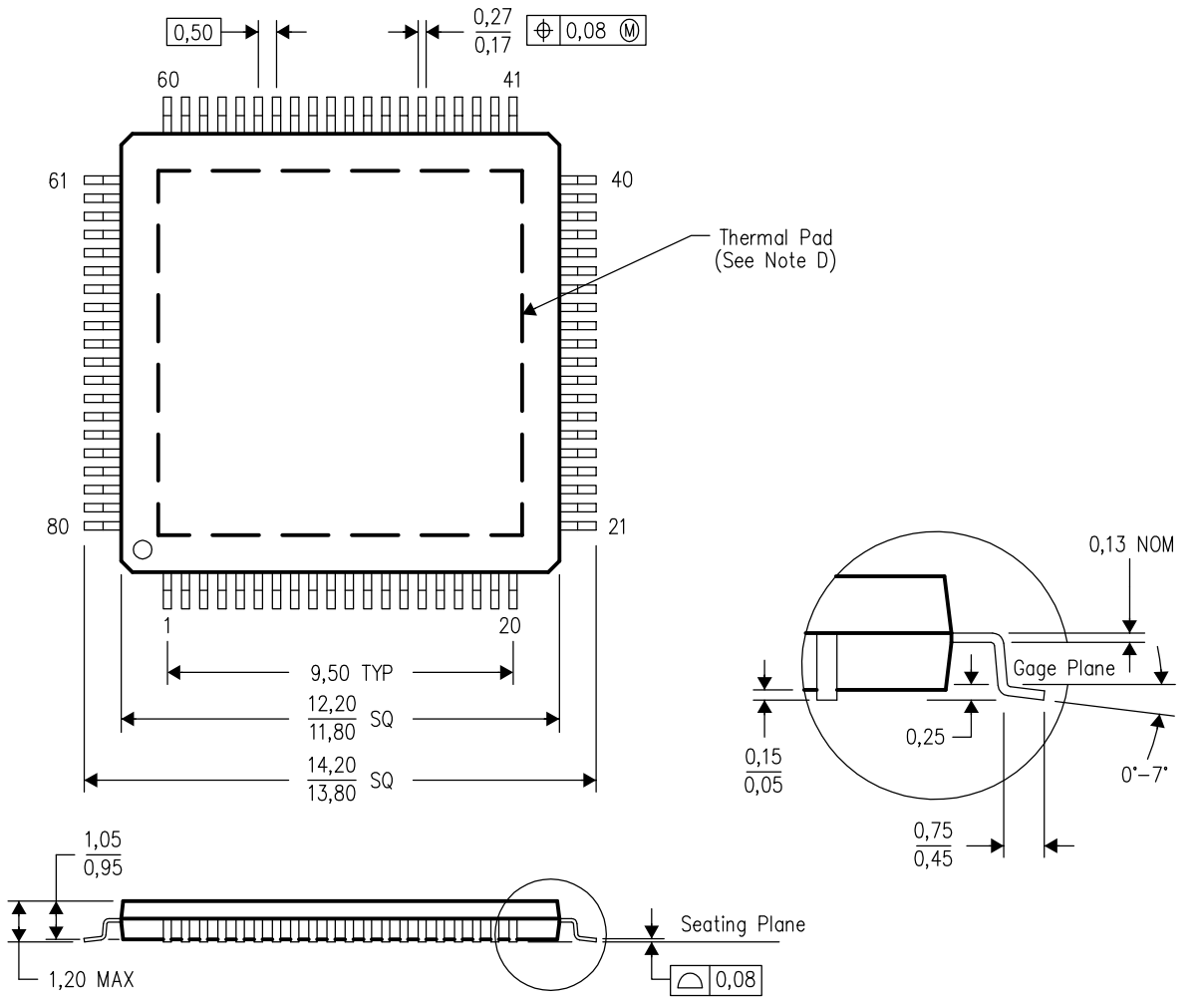
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ADS5270IPFP	ACTIVE	HTQFP	PFP	80	96	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS5270IPFPG4	ACTIVE	HTQFP	PFP	80	96	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS5270IPFPT	ACTIVE	HTQFP	PFP	80	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS5270IPFPTG4	ACTIVE	HTQFP	PFP	80	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

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