36V, Single-Supply, SOT553, Low-Noise OPERATIONAL AMPLIFIER

Check for Samples: OPA171, OPA2171, OPA4171

FEATURES

- **Supply Range: +2.7V to +36V, ±1.35V to ±18V**
- **Low Noise: 14nV/√Hz**
- **RFI Filtered Inputs**
- **Input Range Includes the Negative Supply**
- **Input Range Operates to Positive Supply**
- **Rail-to-Rail Output**
- **Gain Bandwidth: 3MHz**
- **Low Quiescent Current: 475µA per Amplifier**
- **High Common-Mode Rejection: 110dB (typ)**
- **Low Bias Current: 8pA**
- **Industry-Standard Packages:**
  - **8-Pin SOIC**
  - **14-Pin TSSOP**
- ***micro*Packages:**
  - **Single in SOT553**
  - **Dual in VSSOP-8**

APPLICATIONS

- **Tracking Amplifier in Power Modules**
- **Merchant Power Supplies**
- **Transducer Amplifiers**
- **Bridge Amplifiers**
- **Temperature Measurements**
- **Strain Gage Amplifiers**
- **Precision Integrators**
- **Battery-Powered Instruments**
- **Test Equipment**

DESCRIPTION

The OPA171, OPA2171 and OPA4171 (OPAx171) are a family of 36V, single-supply, low-noise operational amplifiers with the ability to operate on supplies ranging from +2.7V (±1.35V) to +36V (±18V). These devices are available in micro-packages and offer good offset, drift, and bandwidth with low quiescent current. The single, dual, and quad versions all have identical specifications for maximum design flexibility.

Unlike most op amps, which are specified at only one supply voltage, the OPAx171 family of op amps are specified from +2.7V to +36V. Input signals beyond the supply rails do not cause phase reversal. The OPAx171 family is stable with capacitive loads up to 300pF. The input can swing 100mV below the negative rail and within 2V of the top rail during normal operation. Note that these devices can operate with full rail-to-rail input 100mV beyond the top rail, but with reduced performance within 2V of the top rail.

The OPA171 is available in SOT553, SOT23-5, and SO-8 packages. The dual OPA2171 comes in VSSOP-8 and SO-8 packages. The quad OPA4171 is offered in TSSOP-14 and SO-14 packages. The OPAx171 series of op amps are specified from –40°C to +125°C.

PRODUCT PREVIEW

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA171	SOT553	DRL	DAP	OPA171AIDRLT	Tape and Reel, 250
				OPA171AIDRLR	Tape and Reel, 4000
	SOT23-5	DBV	OSUI	OPA171AIDBVT	Tape and Reel, 250
				OPA171AIDBVR	Tape and Reel, 3000
	SO-8	D	O171A	OPA171AID	Rail, 75
				OPA171AIDR	Tape and Reel, 2500
OPA2171	VSSOP-8	DCU	OPOC	OPA2171AIDCUT	Tape and Reel, 250
				OPA2171AIDCUR	Tape and Reel, 3000
	SO-8	D	2171A	OPA2171AID	Rail, 75
				OPA2171AIDR	Tape and Reel, 2500
OPA4171	SO-14	D	OPA4171A	OPA42171AID	Rail, 50
				OPA42171AIDR	Tape and Reel, 2500
	TSSOP-14	PW	OPA4171A	OPA42171AIPW	Rail, 90
				OPA42171AIPWR	Tape and Reel, 2000

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or refer to our web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

	OPAx171	UNIT
Supply voltage	+40	V
Input voltage	(V–) – 0.5 to (V+) + 0.5	V
Input differential voltage	TBD	mA
Output short circuit(2)	Continuous	
Operating temperature	–55 to +150	°C
Storage temperature	–65 to +150	°C
Junction temperature	+150	°C
ESD rating: human body model (HBM)	TBD	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Short-circuit to ground, one amplifier per package.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C.**
At T_A = +25°C, V_S = +2.7V to +36V, V_{CM} = V_{OUT} = V_S/2, and R_{LOAD} = 10kΩ to V_S/2,unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA171, OPA2171, OPA4171 MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
Input offset voltage	V_{OS}			0.25	±2	mV
Over temperature					**±2.25**	**mV**
Drift	**dV_{OS}/dT**			**±0.5**	**±2.5**	**µV/°C**
vs power supply	**PSRR**	**V_S = +4V to +36V**		**1**	**±3.0**	**µV/V**
Channel separation, dc		dc		TBD		µV/V
INPUT BIAS CURRENT						
Input bias current	I_B			8	15	pA
Over temperature					**3.5**	**nA**
Input offset current	I_{OS}			4		pA
Over temperature					**3.5**	**nA**
NOISE						
Input voltage noise		f = 0.1Hz to 10Hz		3		μV_{PP}
Input voltage noise density	e_n	f = 100Hz		25		$nV/\sqrt{Hz}$
		f = 1kHz		14		$nV/\sqrt{Hz}$
INPUT VOLTAGE						
Common-mode voltage range(1)	V_{CM}		(V–) – 0.1V		(V+) – 2V	V
Common-mode rejection ratio	**CMRR**	**V_S = +4V to +36V, (V–) – 0.1V < V_{CM} < (V+) – 2V**	**90**	**110**		**dB**
INPUT IMPEDANCE						
Differential				100 || 3		MΩ || pF
Common-mode				250 || 3		GΩ || pF
OPEN-LOOP GAIN						
Open-loop voltage gain	**A_{OL}**	**V_S = +4V to +36V, (V–) + 0.35V < V_O < (V+) – 0.35V**	**110**	**140**		**dB**
FREQUENCY RESPONSE						
Gain bandwidth product	GBP			3.0		MHz
Slew rate	SR	G = +1		1.5		V/µs
Settling time	t_S	To 0.1%, V_S = ±18V, G = +1, 10V step		6		µs
		To 0.01% (12 bit), V_S = ±18V, G = +1, 10V step		12		µs
Overload recovery time		V_{IN} × Gain > V_S		3		µs
Total harmonic distortion + noise	THD+N	G = +1, f = 1kHz, V_O = 3.5V_{RMS}		0.0002		%

(1) The input range can be extended beyond (V+) – 2V up to V+. See the *Typical Characteristics (TBD)* and *Application Information (TBD)* sections for additional information.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (continued)

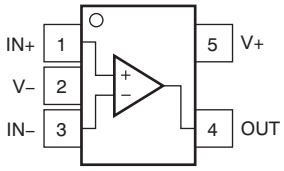
Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C.**
At T_A = +25°C, V_S = +2.7V to +36V, V_{CM} = V_{OUT} = V_S/2, and R_{LOAD} = 10kΩ to V_S/2,unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA171, OPA2171, OPA4171 MIN	TYP	MAX	UNIT
OUTPUT						
Voltage output swing from rail	**V_O**	**R_L = 10kΩ, A_{OL} ≥ 120dB**	**(V–) + 0.35**		**(V+) – 0.35**	**V**
Short-circuit current	I_{SC}			±20		mA
Capacitive load drive	C_{LOAD}		See Typical Characteristics (TBD)			pF
Open-loop output resistance	R_O	f = 1MHz, I_O = 0A		TBD		Ω
POWER SUPPLY						
Specified voltage range	V_S		+2.7		+36	V
Quiescent current per amplifier	I_Q	I_O = 0A		475	595	µA
Over temperature		**I_O = 0A**			**625**	**µA**
TEMPERATURE						
Specified range			–40		+125	°C
Operating range			–55		+150	°C
Thermal resistance	θ_{JA}	SOT-553		250		°C/W
		SOT23-5		250		°C/W
		VSSOP-8		200		°C/W
		SO-8		150		°C/W
		TSSOP-14		100		°C/W
		SO-14		100		°C/W

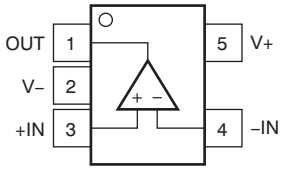
PRODUCT PREVIEW

PIN CONFIGURATIONS

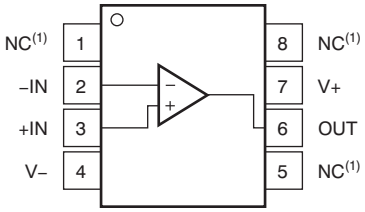
DRL PACKAGE: OPA171
SOT-553
(TOP VIEW)



DBV PACKAGE:OPA171
SOT23-5
(TOP VIEW)

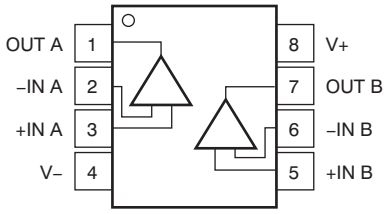


D PACKAGE: OPA171
SO-8
(TOP VIEW)

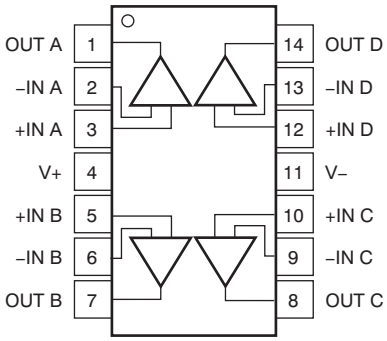


(1) No internal connection.

D AND DCU PACKAGES:OPA2171
SO-8 AND VSSOP-8
(TOP VIEW)



D AND PW PACKAGES:OPA4171
SO-14 AND TSSOP-14
(TOP VIEW)



PRODUCT PREVIEW

PACKAGING INFORMATION

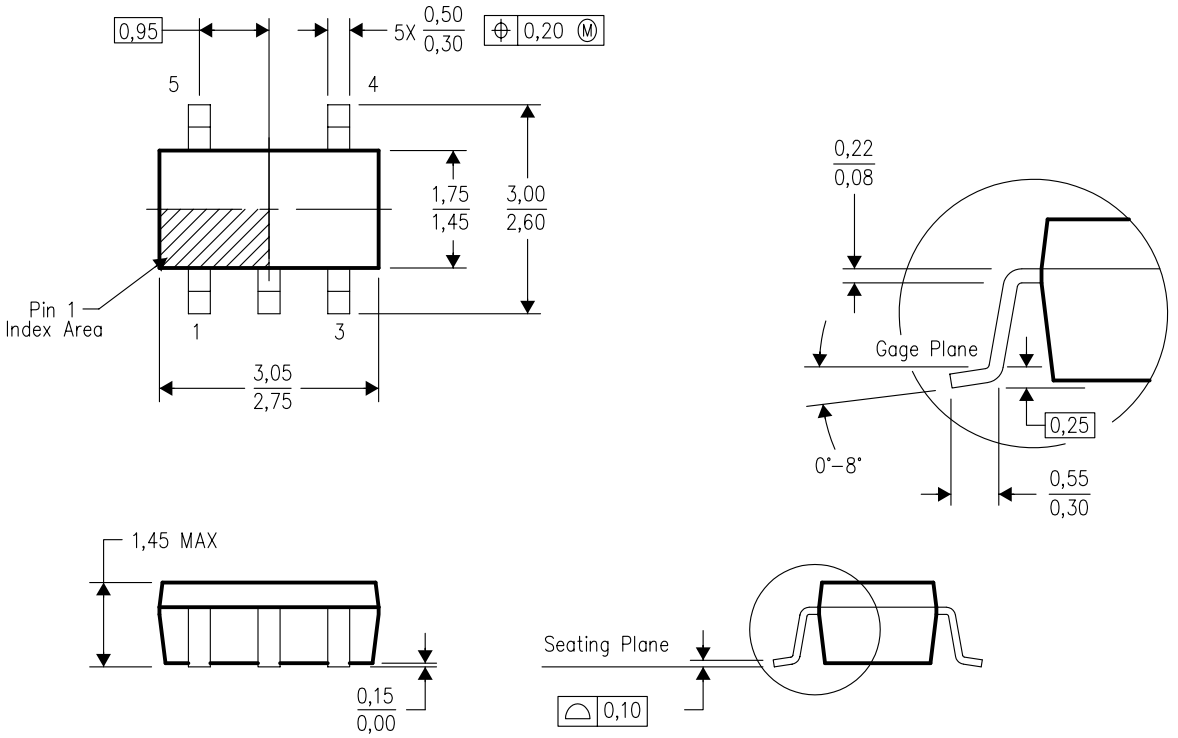
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
OPA171AID	PREVIEW	SOIC	D	8	75	TBD	Call TI	Call TI	Samples Not Available
OPA171AIDBVR	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	Samples Not Available
OPA171AIDBVT	PREVIEW	SOT-23	DBV	5	250	TBD	Call TI	Call TI	Samples Not Available
OPA171AIDR	PREVIEW	SOIC	D	8	2500	TBD	Call TI	Call TI	Samples Not Available
OPA171AIDRLR	PREVIEW	SOT	DRL	5	4000	TBD	Call TI	Call TI	Samples Not Available
OPA171AIDRLT	PREVIEW	SOT	DRL	5	250	TBD	Call TI	Call TI	Samples Not Available

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



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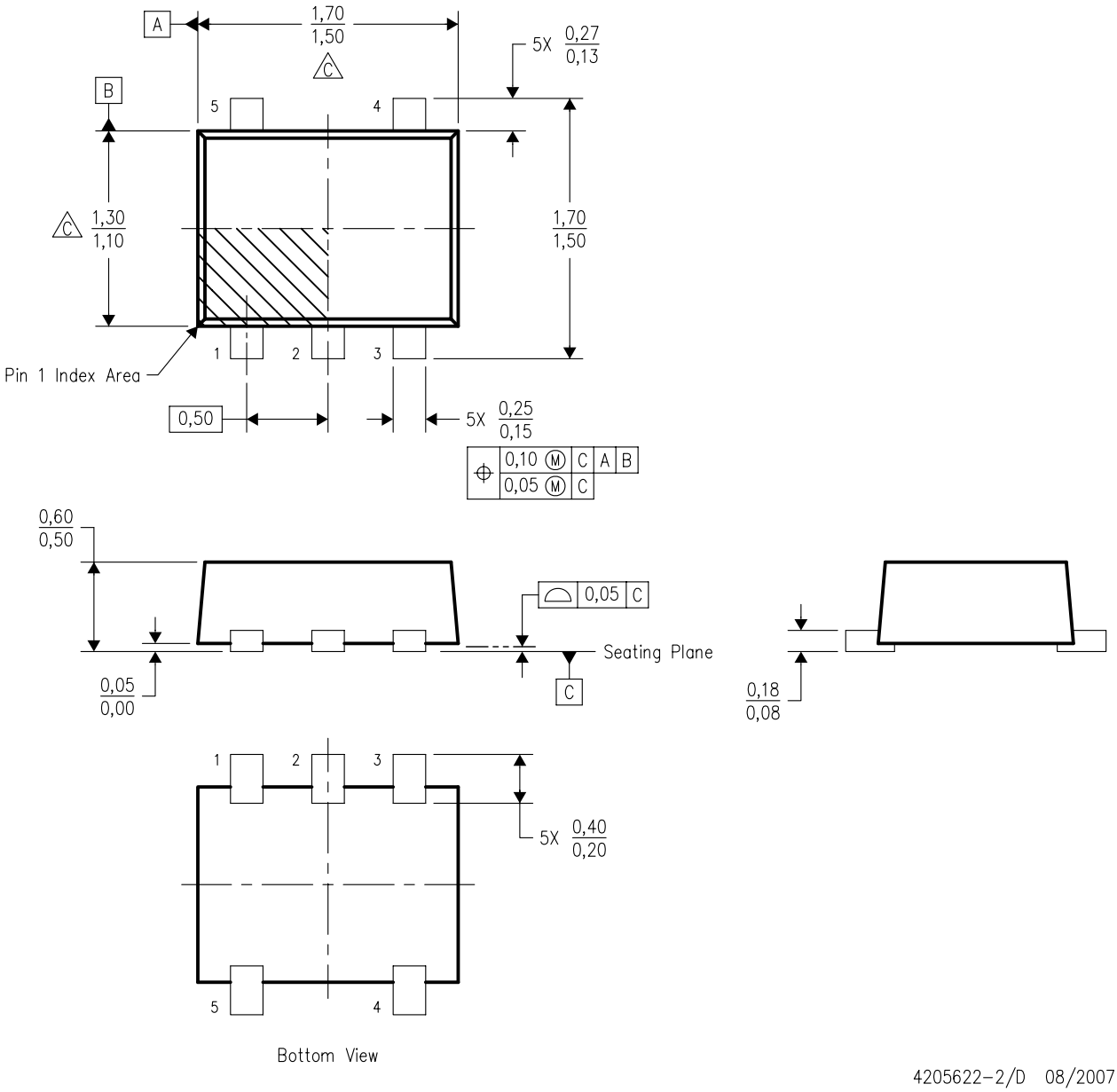
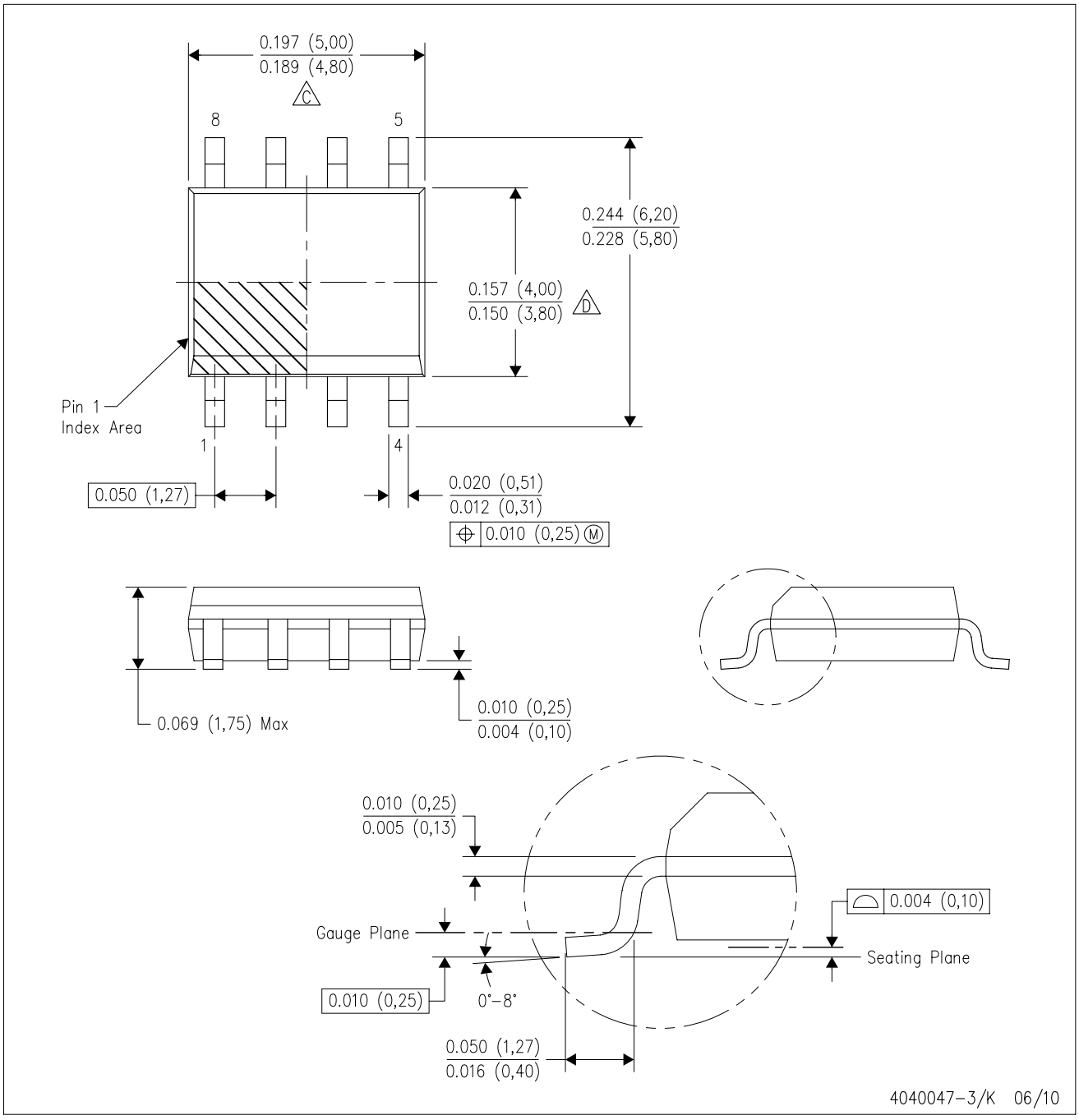
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
D. JEDEC package registration is pending.

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

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