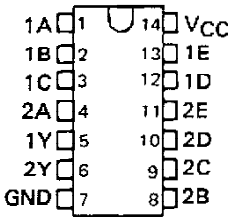
- **Package Options Include Ceramic Chip Carriers and Flat Packages in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

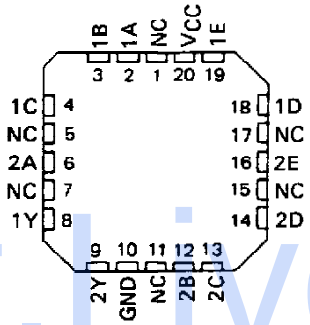
These devices contain two independent 5-input positive-NOR gates. They perform the Boolean function $Y = \overline{A + B + C + D + E}$ in positive logic.

The SN54S260 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74S260 is characterized for operation from 0°C to 70°C.

SN548260 . . . J OR W PACKAGE
SN74S260 . . . D OR N PACKAGE
(TOP VIEW)

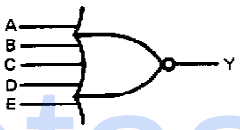


SN54S260 . . . FK PACKAGE
(TOP VIEW)

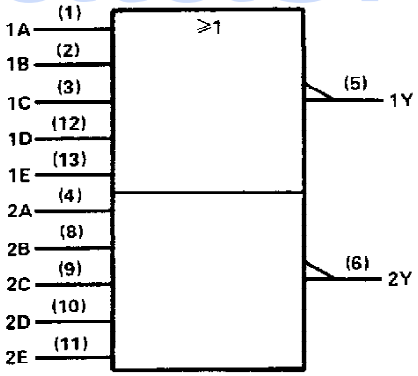


NC – No internal connection

logic diagram (each gate)

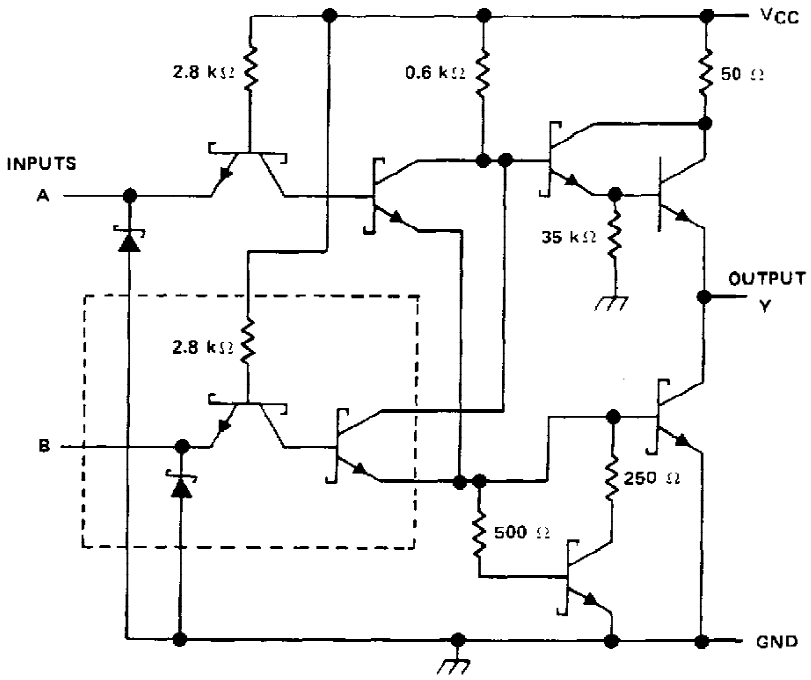


logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

schematic (each gate)



Resistor values shown are nominal.
The portion of the schematic within the dashed-line is repeated for each additional input.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54'	−55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S260			SN74S260			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †			SN54S260			SN74S260			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	V_{IL} = 0.8 V,	I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OL} = 20 mA			0.5			0.5	V
I_I	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	V_{CC} = MAX,	V_{IH} = 2.7 V				50			50	μA
I_{IL}	V_{CC} = MAX,	V_{IL} = 0.5 V				−2			−2	mA
I_{OS}§	V_{CC} = MAX			−40		−100	−40		−100	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V			17	29		17	29	mA
I_{CCL}	V_{CC} = MAX,	See Note 2			26	45		26	45	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.
NOTE 2: One input at 4.5 V, all others at GND.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	R_L = 280 Ω,	C_L = 15 pF		4	5.5	ns
t_{PHL}						4	6	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN54S260J	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SN74S260D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S260DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S260DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S260DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S260N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74S260N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74S260NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SNJ54S260FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54S260J	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SNJ54S260W	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

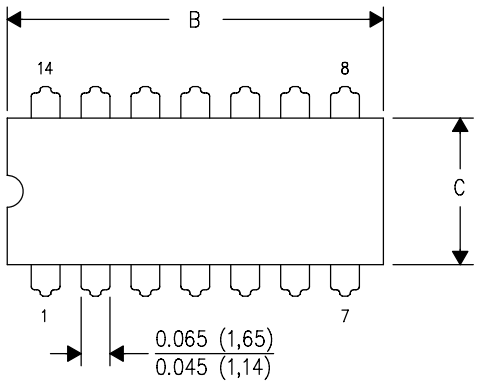
[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

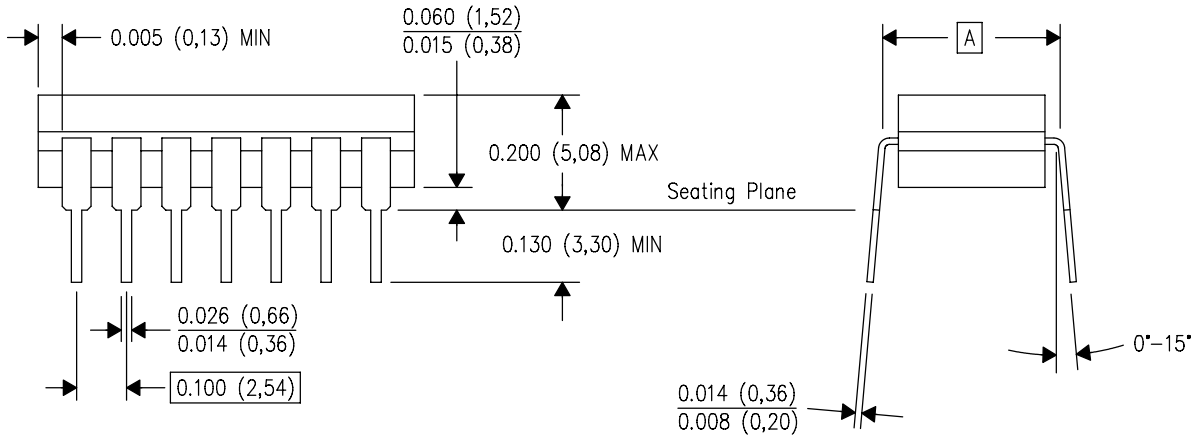
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



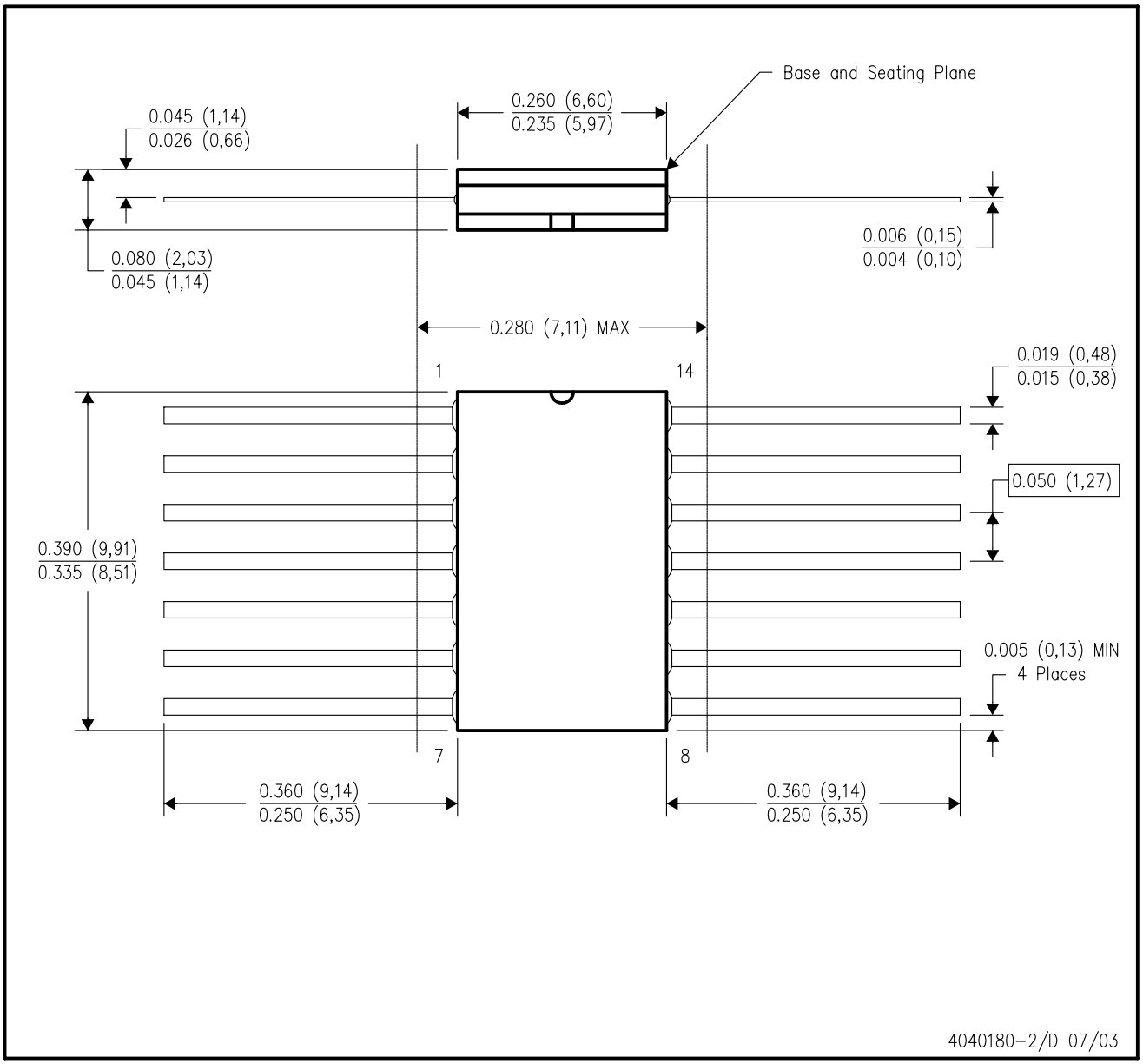
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

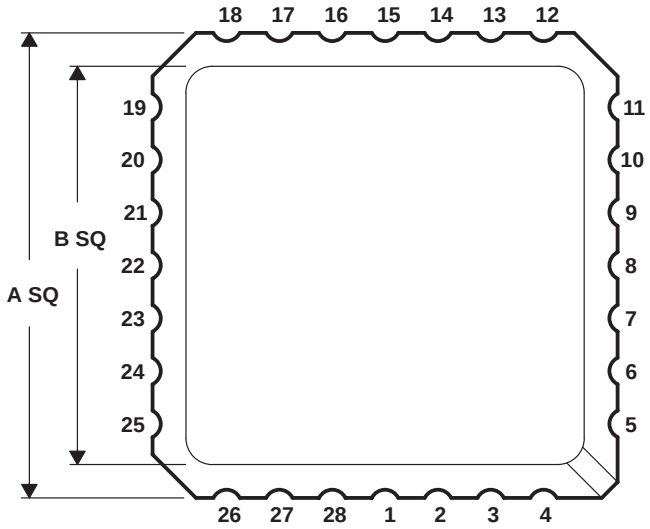
W (R–GDFP–F14) CERAMIC DUAL FLATPACK



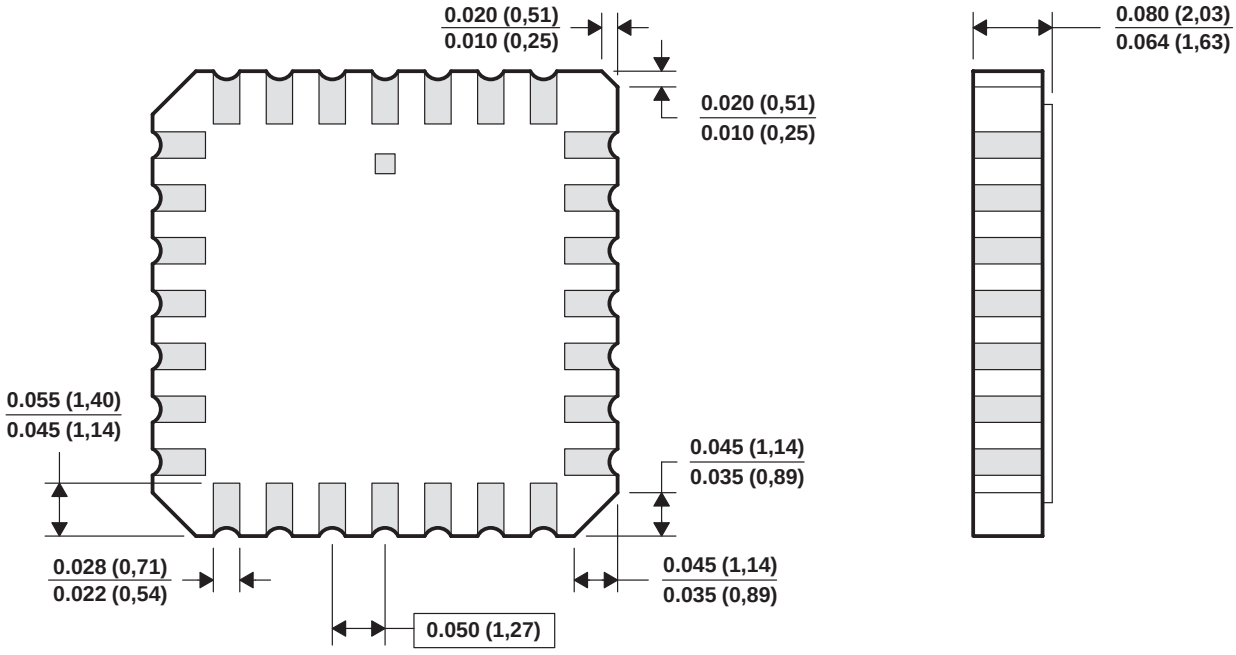
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14 and JEDEC MO–092AB

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



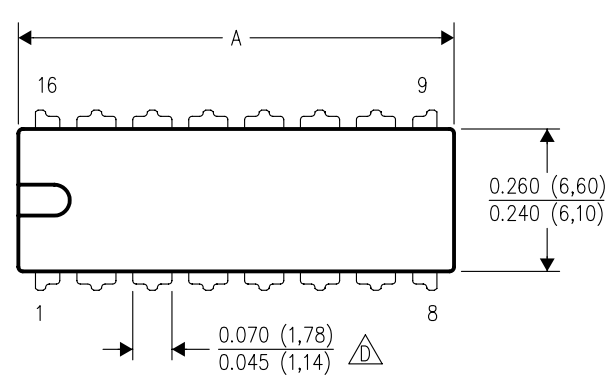
4040140/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

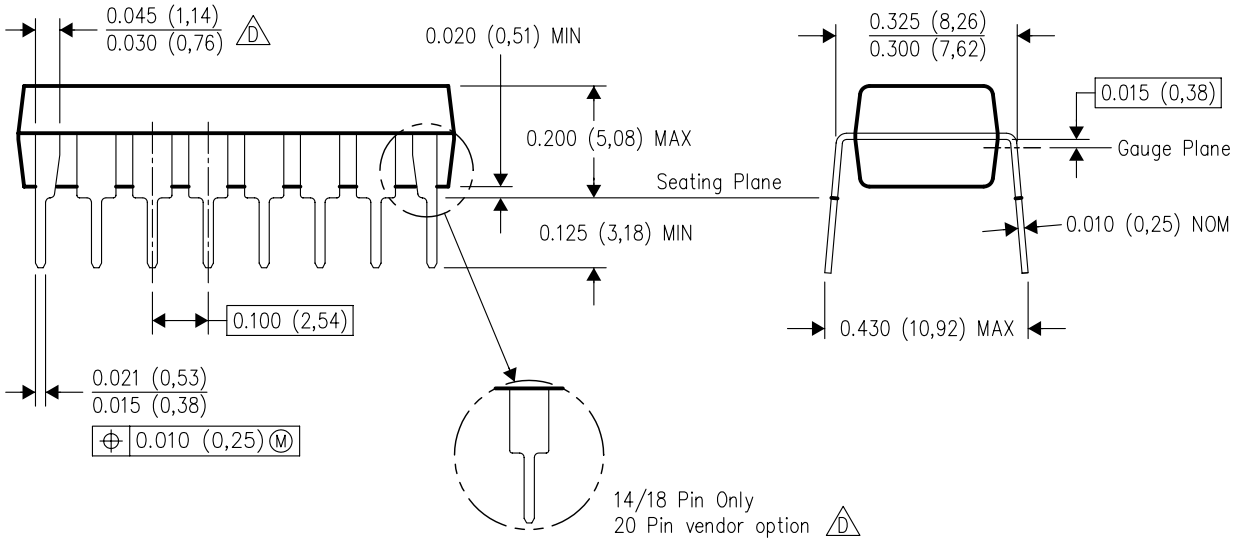
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



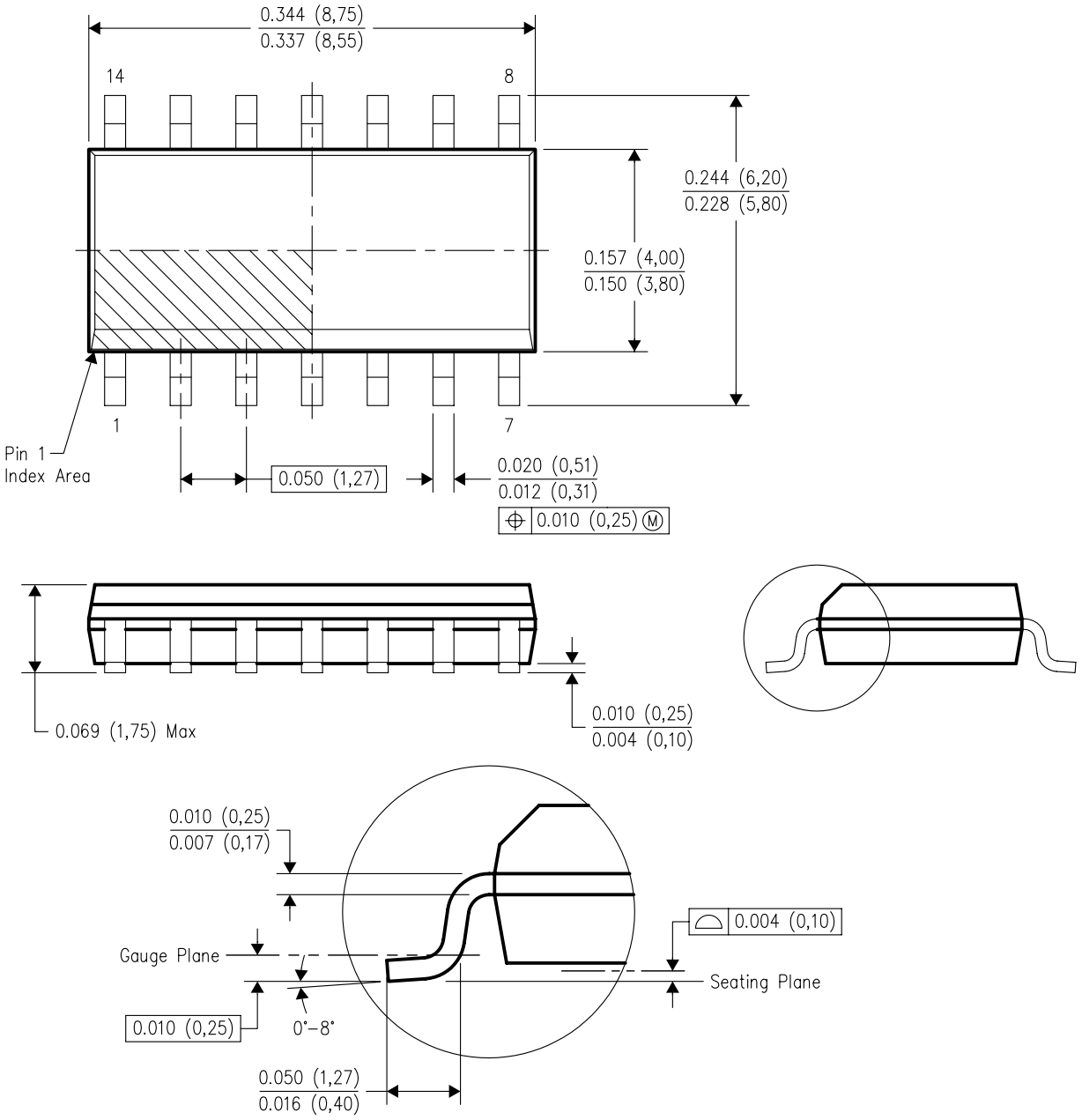
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AB.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

View ROHS Compliant Devices
View RoHS Compliant Devices
clear gif

SN74S260, Status: ACTIVE

Dual 5-input positive-NOR gates

clear gif

Features | Samples | Technical Documents
Quality & Pb-Free Data | Pricing/Packaging | Applications Notes
Related Products | Inventory | Simulation Models
Tools & Software | Symbols/Footprints | Reference Designs

Refine Your Selection
- Logic: NOR Gates

Support
- KnowledgeBase
- Contact Technical Supp
- TI Cross Reference
- Training
- Part Marking Lookup
- Part Number Nomencla

Datasheet

Download Datasheet **Dual 5-Input Positive-NOR Gates** (sn74s260.pdf, 486 KB)
01 Mar 1988 Download

	SN54S260	SN74S260
Voltage Nodes(V)	5	5
Vcc range(V)	4.5 to 5.5	4.75 to 5.25
Input Level	TTL	TTL
Output Level	TTL	TTL
Output Drive(mA)		-1/20
No. of Gates	2	2
Static Current		37
tpd max(ns)		6
	Samples	Samples
	Inventory	Inventory

Product Information

Features

Save this to your personal library

Package Options Include Ceramic Chip Carriers and Flat Packages in Addition to Plastic and Ceramic DIPs
Dependable Texas Instruments Quality and Reliability

Description

These devices contain two independent 5-input positive-NOR gates. They perform the Boolean function Y = A + B + C + D + E\ in positive logic.

The SN54S260 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74S260 is characterized for operation from 0°C to 70°C.

Pricing/Packaging/CAD Design Tools/Samples

			Price	Packaging			CAD Design Tools	Samples
Device	Status	Temp (°C)	Budget Price ($US) | QTY	Industry Standard (TI Pkg) | Pins	Top Side Marking	Standard Pack Quantity	Footprints	Samples
SN74S260D	ACTIVE	0 to 70	1.06 | 1KU	SOIC (D) | 14	View	50	☐	Purchase Samples
SN74S260DE4	ACTIVE	0 to 70	1.06 | 1KU	SOIC (D) | 14	View	50	☐	Purchase Samples
SN74S260DR	ACTIVE	0 to 70	1.06 | 1KU	SOIC (D) | 14	View	2500	☐	Purchase Samples
SN74S260DRE4	ACTIVE	0 to 70	1.06 | 1KU	SOIC (D) | 14	View	2500	☐	Purchase Samples
SN74S260N	ACTIVE	0 to 70	1.06 | 1KU	PDIP (N) | 14	View	25	☐	Purchase Samples
SN74S260N3	OBSOLETE	0 to 70		PDIP (N) | 14	View		☐	Not Available
SN74S260NE4	ACTIVE	0 to 70	1.06 | 1KU	PDIP (N) | 14	View	25	☐	Purchase Samples

Inventory

View all Distributors

Choose a Region

	TI Inventory Status			Reported Distributor Inventory			
SN74S260D	As of 9:04 AM GMT, 29 Nov 2005			As of 9:04 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY | Date	Lead Time	Region	Company	In Stock	Purchase
	0*	300 | 12 Dec	10 Weeks	Asia	P&S	500	
		>10k | 6 Mar					
SN74S260DE4	As of 9:04 AM GMT, 29 Nov 2005			As of 9:04 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY | Date	Lead Time	Region	Company	In Stock	Purchase
	0*	300 | 12 Dec	10 Weeks	None Reported View Distributors			
		>10k | 6 Mar					
SN74S260DR	As of 9:04 AM GMT, 29 Nov 2005			As of 9:04 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY | Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k | 6 Mar	14 Weeks	None Reported View Distributors			
SN74S260DRE4	As of 9:04 AM GMT, 29 Nov 2005			As of 9:04 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY | Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k | 6 Mar	14 Weeks	None Reported View Distributors			
SN74S260N	As of 9:04 AM GMT, 29 Nov 2005			As of 9:04 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY | Date	Lead Time	Region	Company	In Stock	Purchase
	0*	5581 | 16 Dec	10 Weeks	Americas	Newark InOne	258	
		7088 | 28 Dec		Asia	P&S	475	
				Europe	EBV Elektronik	225	
					Spoerle	209	
SN74S260NE4	As of 9:04 AM GMT, 29 Nov 2005			As of 9:04 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY | Date	Lead Time	Region	Company	In Stock	Purchase
	0*	5581 | 16 Dec	10 Weeks	None Reported View Distributors			
		7088 | 28 Dec					

* Our information is updated daily, so please check back with us soon if this does not meet your needs. You may also contact your TI Authorized Distributor, including those listed above, for real time stock information.

** Lead time information is not available at this time. However, our information is updated daily so please check back with us soon. Please contact your preferred TI Authorized Distributor for additional information.

Quality & Lead (Pb)-Free Data

	Product Content				MTBF/FIT Rate
Device	**Eco Plan***	**Lead/Ball Finish**	**MSL Rating/Peak Reflow**	**Details**	**Details**
SN74S260D	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74S260DE4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74S260DR	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74S260DRE4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74S260N	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC	View	View
SN74S260NE4	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC	View	View

* The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please click on the Product Content Details "View" link in the table above for the latest availability information and additional product content details.

If the information you are requesting is not available online at this time, contact one of our Product Information Centers regarding the availability of this information.

Technical Documents

Datasheets

Keep track of what's new

Dual 5-Input Positive-NOR Gates (sn74s260.pdf, 486 KB)
01 Mar 1988 Download

Application Notes

Semiconductor Packing Material Electrostatic Discharge (ESD) Protection (szza047.htm, 9 KB)
08 Jul 2004 Abstract

Shelf-Life Evaluation of Lead-Free Component Finishes (szza046.htm, 9 KB)
24 May 2004 Abstract

Understanding and Interpreting Standard-Logic Data Sheets (Rev. B) (szza036b.htm, 8 KB)
28 May 2003 Abstract

Designing With Logic (Rev. C) (sdya009c.htm, 9 KB)
01 Jun 1997 Abstract

Live Insertion (sdya012.htm, 9 KB)
01 Oct 1996 Abstract

Input and Output Characteristics of Digital Integrated Circuits (sdya010.htm, 9 KB)
01 Oct 1996 Abstract

View Application Notes for NOR GATES

User Guides

LOGIC Pocket Data Book (scyd013.pdf, 4835 KB)
05 Dec 2002 Download

More Literature

Logic Selection Guide 2005 (Rev. X) (sdyu001x.pdf, 6909 KB)
15 Mar 2005 Download

Military Semiconductors Selection Guide 2004-2005 (Rev. D) (sgyc003d.pdf, 964 KB)
10 Aug 2004 Download

Logic Cross-Reference (Rev. A) (scyb017a.pdf, 2938 KB)
07 Oct 2003 Download

View More Literature for NOR GATES