SGS-THOMSON
MICROELECTRONICS

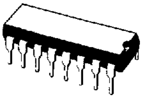
ULN2064B ULN2070B
ULN2066B ULN2074B
ULN2068B ULN2076B

50 V - 1.5 A QUAD DARLINGTON SWITCHES

- OUTPUT CURRENT TO 1.5 A EACH DARLINGTON
- MINIMUM BREAKDOWN 50 V
- SUSTAINING VOLTAGE AT LEAST 35 V
- INTEGRAL SUPPRESSION DIODES (ULN2064B, ULN2066B, ULN2068B and ULN2070B)
- ISOLATED DARLINGTON PINOUT (ULN2074B, ULN2076B)
- VERSIONS COMPATIBLE WITH ALL POPULAR LOGIC FAMILIES

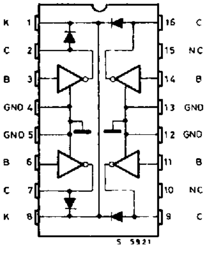
DESCRIPTION

Designed to interface logic to a wide variety of high current, high voltage loads, these devices each contain four NPN darlington switches delivering up to 1.5 A with a specified minimum breakdown of 50 V and a sustaining voltage of 35 V measured at 100 mA. The ULN2064B, ULN2066B, ULN2068B and ULN2070B contain integral suppression diodes for inductive loads have common emitters. The ULN2074B and ULN2076B feature isolated darlington pinouts and are intended for applications such as emitter follower configurations. Inputs of the ULN2064B, ULN2068B and ULN2074B are compatible with popular 5 V logic families and the ULN2066B and ULN2076B are compatible with 6-15 V CMOS and PMOS. Types ULN2068B and ULN2070B include a predriver stage to reduce loading on the control logic.

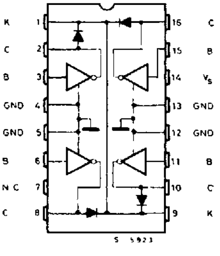


POWERDIP
12 + 2 + 2

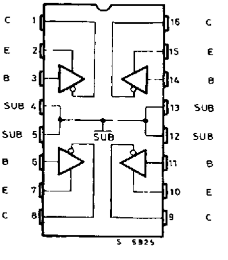
PIN CONNECTIONS (top view) and **ORDER CODES**



ULN2064B
ULN2068B



ULN2068B
ULN2070B

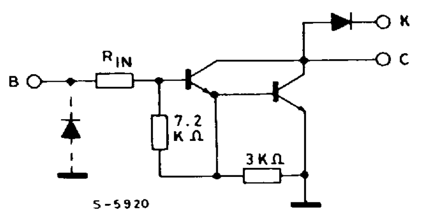


ULN2074B
ULN2076B

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CEX}	Output Voltage	50	V
$V_{CE(sus)}$	Output Sustaining Voltage	35	V
I_o	Output Current	1.75	A
V_I	Input Voltage for **ULN2066B/70B/74B/76B** for **ULN2064B/68B**	30 15	V V
I_I	Input Current	25	mA
V_s	Supply Voltage for **ULN2068B** for **ULN2070B**	10 20	V V
P_{tot}	Power Dissipation : at T_{amb} = 90 °C at T_{amb} = 70 °C	4.3 1	W W
T_{amb}	Operating Ambient Temperature Range	– 20 to 85	°C
T_{stg}	Storage Temperature	– 55 to 150	°C

SCHEMATIC DIAGRAM



ULN2064B : R_{IN} = 35 Ω
ULN2066B : R_{IN} = 3 kΩ

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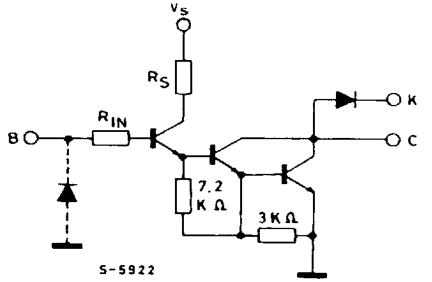
ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig
I_{CEX}	Output Leakage Current	for **ULN2064B – ULN2066B** V_{CE} = 50 V V_{CE} = 50 V T_{amb} = 70 °C			 100 500	 µA µA	1
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	for **ULN2064B – ULN2066B** I_C = 100 mA V_I = 0.4 V	35			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 500 mA I_B = 625 µA I_C = 750 mA I_B = 935 µA I_C = 1 A I_B = 1.25 mA I_C = 1.25 A I_B = 2 mA			1.1 1.2 1.3 1.4	V V V V	3
$I_{I(on)}$	Input Current	for **ULN2064B** V_I = 2.4 V for **ULN2064B** V_I = 3.75 V for **ULN2066B** V_I = 5 V for **ULN2066B** V_I = 12 V	1.4 3.3 0.6 1.7		4.3 9.6 1.8 5.2	mA mA mA mA	4
$V_{I(on)}$	Input Voltage	for **ULN2064B** V_{CE} = 2 V I_C = 1 A V_{CE} = 2 V I_C = 1.5 A for **ULN2066B** V_{CE} = 2 V I_C = 1 A V_{CE} = 2 V I_C = 1.5 A			 2 2.5 6.5 10	 V V V V	5
t_{PLH}	Turn – on Delay Time	0.5 V_I to 0.5 V_O			1	µs	
t_{PHL}	Turn – off Delay Time	0.5 V_I to 0.5 V_O			1.5	µs	
I_R	Clamp Diode Leakage Current	for **ULN2064B – ULN2066B** V_R = 80 V V_R = 80 V T_{amb} = 70 °C			 50 100	 µA µA	6
V_F	Clamp Diode Forward Voltage	I_F = 1 A I_F = 1.5 A			1.75 2	V V	7

Notes : 1 Input voltage is with reference to the substrate (no connection to any other pins) for the ULN2074B and ULN2076B reference is ground for all other types.
2. Input current may be limited by maximum allowable input voltage.

SCHEMATIC DIAGRAM



ULN2068B : R_{IN} = 2.5 kΩ R_s = 900 Ω
ULN2070B : R_{IN} = 11.6 kΩ R_s = 3.4 KΩ

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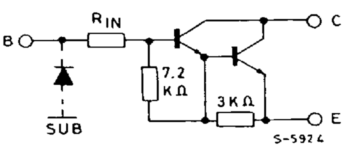
ELECTRICAL CHARACTERISTICS (V_s = 5 V for ULN2068B, V_s = 12 V for ULN2070B, T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig
I_{CEX}	Output Leakage Current	for **ULN2068B – ULN2070B** V_{CE} = 50 V V_{CE} = 50 V T_{amb} = 70 °C			 100 500	 µA µA	1
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	for **ULN2068B – ULN2070B** I_C = 100 mA V_I = 0.4 V	35			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	for **ULN2068B** I_C = 500 mA V_I = 2.75 V I_C = 750 mA V_I = 2.75 V I_C = 1 A V_I = 2.75 V I_C = 1.25 A V_I = 2.75 V for **ULN2070B** I_B = 500 mA V_I = 5 V I_B = 750 mA V_I = 5 V I_B = 1 A V_I = 5 V I_B = 1.25 A V_I = 5 V			 1.1 1.2 1.3 1.4 1.1 1.2 1.3 1.4	 V V V V V V V V	2
$I_{I(on)}$	Input Current	for **ULN2068B** V_I = 2.75 V for **ULN2068B** V_I = 3.75 V for **ULN2070B** V_I = 5 V for **ULN2070B** V_I = 12 V			550 1000 400 1250	µA µA µA µA	4
$V_{I(on)}$	Input Voltage	V_{CE} = 2 V I_C = 1.5 A for **ULN2068B** for **ULN2070B**			 2.75 5	 V V	5
I_s	Supply Current	for **ULN2068B** I_C = 500 mA V_I = 2.75 V for **ULN2070B** I_C = 500 mA V_I = 5 V			 6 4.5	 mA mA	8
t_{PLH}	Turn-on Delay Time	0.5 V_I to 0.5 V_O			1	µs	
t_{PHL}	Turn-off Delay Time	0.5 V_I to 0.5 V_O I_C = 1.25 A			1.5	µs	
I_R	Clamp Diode Leakage Current	for **ULN2068B – ULN2070B** V_R = 50 V V_R = 50 V T_{amb} = 70 °C			 50 100	 µA µA	6
V_F	Clamp Diode Forward Voltage	I_F = 1 A I_F = 1.5 A			1.75 2	V V	7

SCHEMATIC DIAGRAM



ULN2074B : R_{IN} = 350 Ω
ULN2076B : R_{IN} = 3 kΩ

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig
I_{CEX}	Output Leakage Current	for **ULN2074B – ULN2076B** V_{CE} = 50 V V_{CE} = 50 V T_{amb} = 70 °C			 100 500	 µA µA	1
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	for **ULN2074B – ULN2076B** I_C = 100 mA V_I = 0.4 V	35			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 500 mA I_B = 625 µA I_C = 750 mA I_B = 935 µA I_C = 1 A I_B = 1.25 mA I_C = 1.25 A I_B = 2 mA			1.1 1.2 1.3 1.4	V V V V	3
$I_{I(on)}$	Input Current	for **ULN2074B** V_I = 2.4 V for **ULN2074B** V_I = 3.75 V for **ULN2076B** V_I = 5 V for **ULN2076B** V_I = 12 V	1.4 3.3 0.6 1.7		4.3 9.6 1.8 5.2	mA mA mA mA	4
$V_{I(on)}$	Input Voltage	for **ULN2074B** V_{CE} = 2 V I_C = 1 A V_{CE} = 2 V I_C = 1.5 A for **ULN2076B** V_{CE} = 2 V I_C = 1 A V_{CE} = 2 V I_C = 1.5 A			 2 2.5 6.5 10	 V V V V	5
t_{PLH}	Turn-on Delay Time	0.5 V_I to 0.5 V_o			1	µs	
t_{PHL}	Turn-off Delay Time	0.5 V_I to 0.5 V_o			1.5	µs	

TEST CIRCUITS

Figure 1.

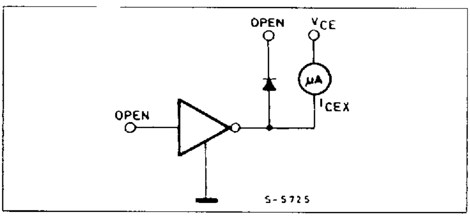


Figure 2.

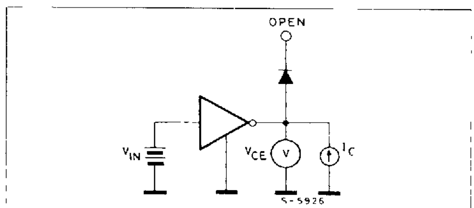


Figure 3.

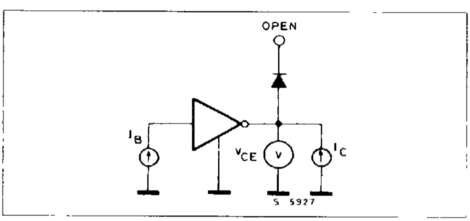


Figure 4.

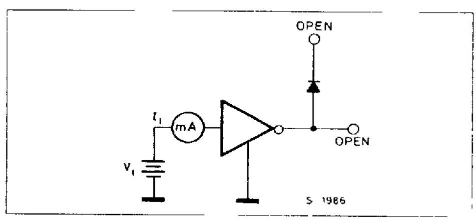


Figure 5.

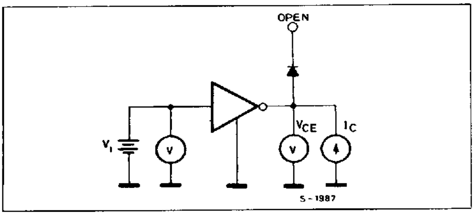


Figure 6.

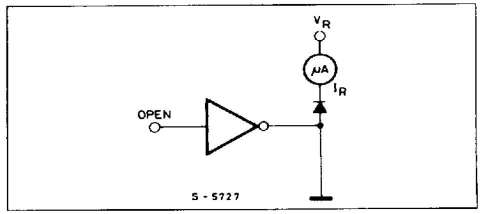


Figure 7.

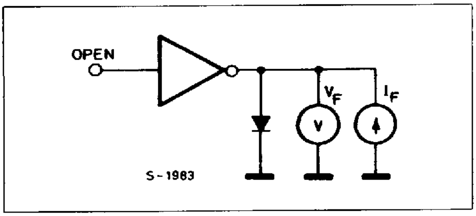


Figure 8.

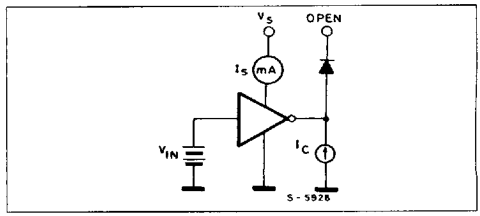


Figure 9 : Input Current as a Function of Input Voltage.

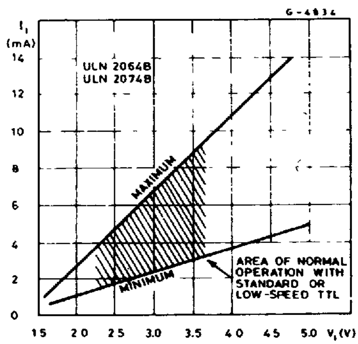


Figure 10 : Input Current as a Function of Input Voltage.

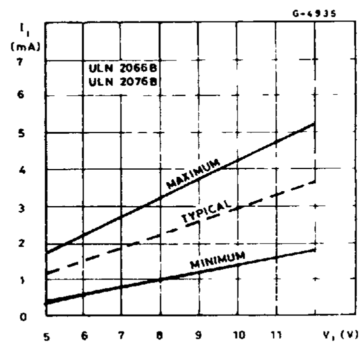
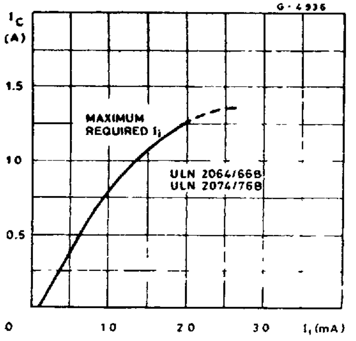


Figure 11 : Collector Current as a Function of Input Current.



TYPICAL APPLICATIONS

Figure 12 : Common-anode LED Drivers.

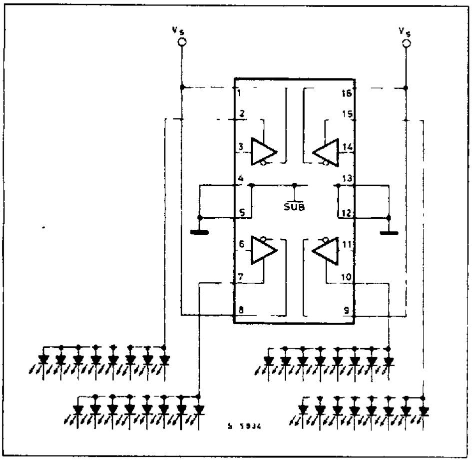
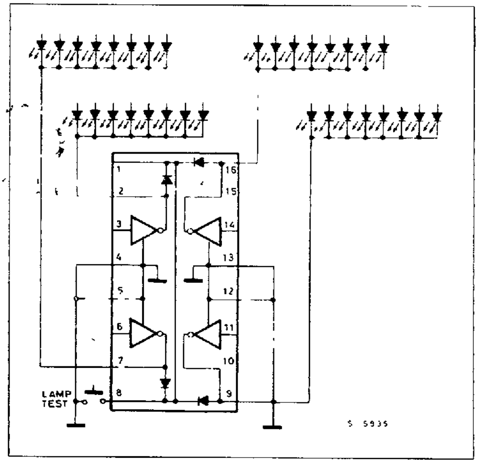


Figure 13 : Common-cathode LED Drivers.



MOUNTING INSTRUCTIONS

The $R_{th\ j\text{-}amb}$ can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 14) or to an external heatsink (Fig. 15).

The diagram of figure 16 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "α" of two equal square copper areas having a thickness of 35 μ (1.4 mils).

During soldering the pins temperature must not exceed 260 °C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 14 : Example of P.C. Board Copper Area which is Used as Heatsink.

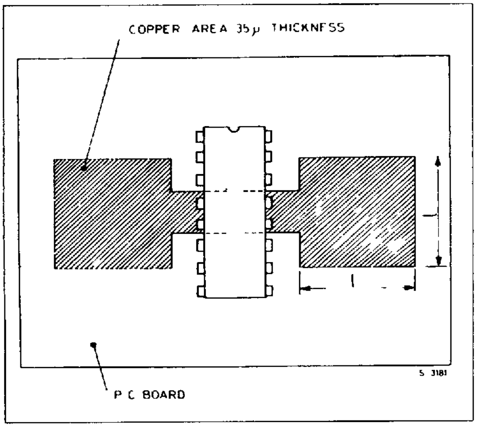


Figure 15 : External Heatsink Mounting Example.

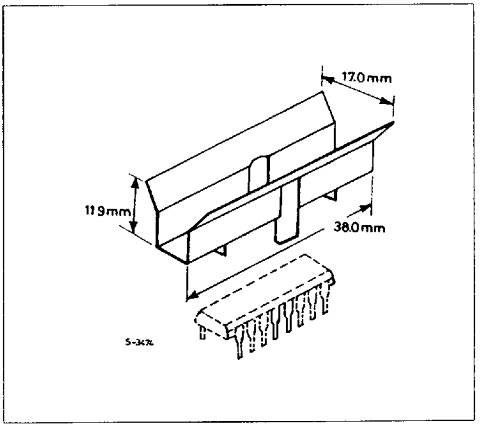


Figure 16 : Maximum Dissipable Power and Junction to Ambient Thermal Resistance vs. Side "α".

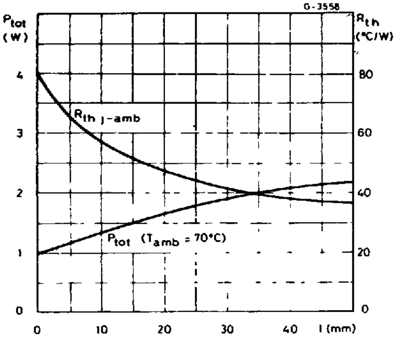


Figure 17 : Maximum Allowable Power Dissipation vs. Ambient Temperature.