Integrated Circuits

The Smart Power ICs and Chip-sets manufactured by IXYS are designed to interface with the company's family of Power MOSFET and IGBT products in order to provide improved performance for a broad range of power conversion and motor control applications.

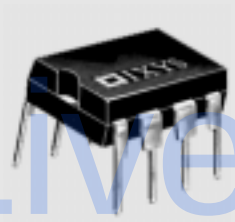
IXYS has focussed on two main areas:

- High/Low Side Driver Integrated Circuits which complement IXYS Power MOSFET and IGBT that offer with either open or closed loop protection of the power devices, such as the IXBD4410 Series.
- PWM Regulator and Controller circuits optimized for specialized power supplies and motor control applications. The device satisfying this need would be the IXDP610 and IXMS150.

Other devices included in the IXYS product range are a series of High Voltage Current Regulators and a Digital Deadtime Generator.

IXYS has an experienced staff of analog, digital and power designers who are teamed together to ensure accurate definition of future generations of integrated solutions to satisfy the needs for the power control, power conversion and motion control markets.

Using the advantages and compatibility of CMOS and IXYS HDMOS™ process, IXYS will continue to integrate functions for power control which are still composed discretely.



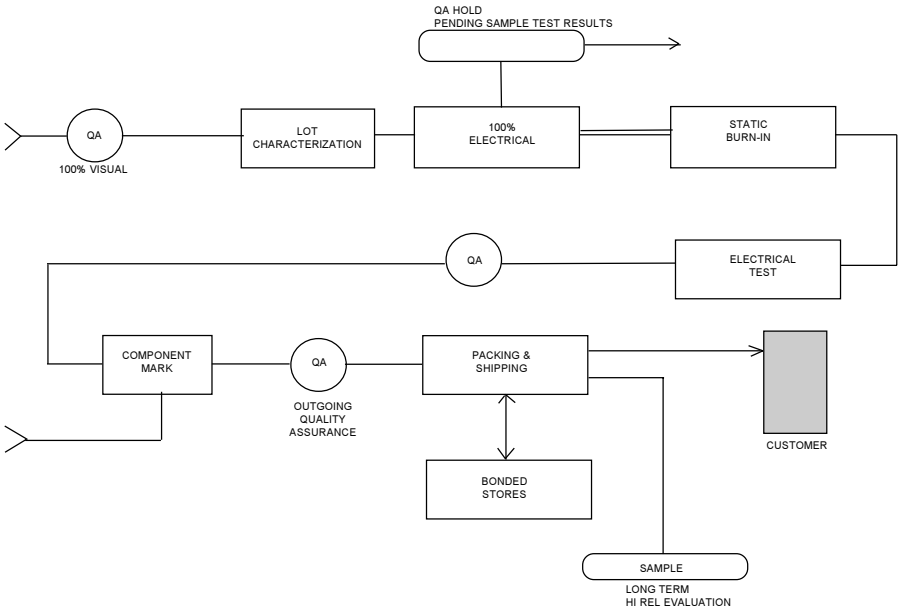
Contents

Quality and Reliability Program

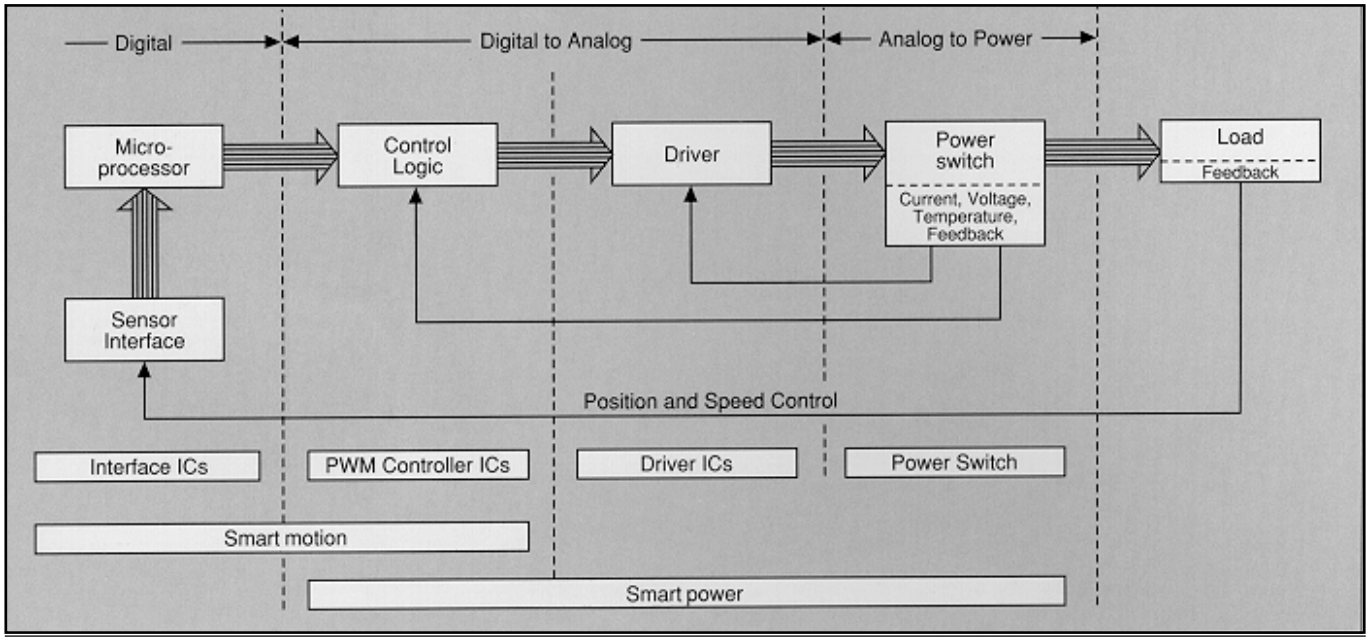
IXYS is committed to the philosophy that quality must be built into a product and not achieved only through inspection. IXYS has designed and implemented a complete Quality and Reliability Program to insure that IXYS' products meet and/or exceed the expectation of our customers.

IXYS' Quality and Reliability Program contains numerous audit points to insure the quality of each process. Stringent electrical tests and numerous environmental tests are run short and long term with samples from all product lots. Only after successful completion of each step in the program will IXYS put its mark on a component. The end result: a superior product for your application requirements.

Production Lot Flow for Motion Control Products



Typical Power Electronic Control System



ISOSMART™ Half Bridge Driver Chipsets

Type	Description	Package	Temperature Range
IXBD4410PI	Full-Feature Low-Side Driver	16-Pin P-DIP	-40 to +85°C
IXBD4411PI	Full-Feature High-Side Driver	16-Pin P-DIP	-40 to +85°C
IXBD4410SI	Full-Feature Low-Side Driver	16-Pin SO	-40 to +85°C
IXBD4411SI	Full-Feature High-Side Driver	16-Pin SO	-40 to +85°C
IXBD4412PI	Basic Low-Side Driver	8-Pin P-DIP	-40 to +85°C
IXBD4413PI	Basic High-Side Driver	8-Pin P-DIP	-40 to +85°C
IXBD4410KIT	Full-Feature Chipset Eval. Kit	PCB	0 to +70°C
IXBD4412KIT	Basic Chipset Evaluation Kit	PCB	0 to +70°C

The IXBD4410/IXBD4411 and the IXBD4412/IXBD4413 ISOSMART™ chipsets are designed to control the gates of two Power MOSFETs, or Power IGBTs, that are connected in a half-bridge (phaseleg) configuration for driving multiple-phase motors, or used in applications that require half-bridge power circuits. The IXBD4410/ IXBD4411 is a full-feature chipset consisting of two 16-Pin-DIP or SO devices interfaced and isolated by two small-signal ferrite pulse transformers. The IXBD4412/IXBD4413 is a basic, low-cost chipset consisting of two 8-Pin-DIP devices interfaced and isolated by a single pulse transformer. The small-signal transformers in both chipsets provide greater than 1200 V isolation.

Even with commutating noise ambients greater than ±50 V/ns and up to 1200 V potentials, these chipsets establish error-free two-way communications between the system ground-reference IXBD4410 resp. IXBD4412 and the inverter output-reference IXBD4411 resp. IXBD4413. They incorporate undervoltage V_{DD} or V_{EE} lockout, and overcurrent or desaturation shutdown to protect the IGBT or Power MOSFET devices from damage.

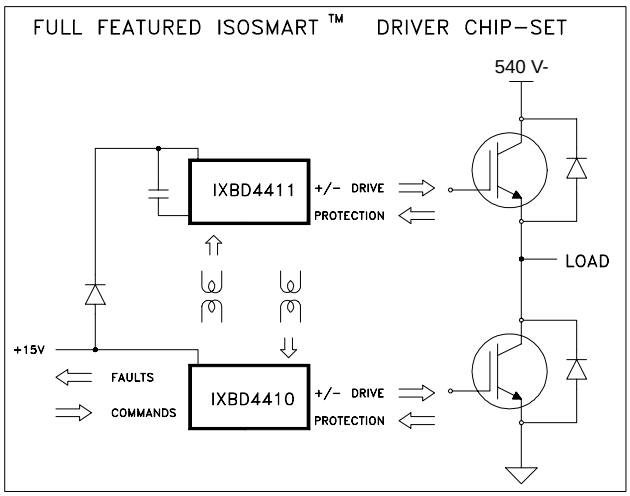
Both chipsets provide the necessary gate drive signals to fully control the grounded-source low-side power device, as well as the floating-source high-side power device. Additionally, the IXBD4410/4411 chipset provides a negative-going, off-state gate drive signal for improved turn-off of IGBTs, or Power MOSFETs, and a system logic-compatible status fault output, $\overline{FLT}$, to indicate overcurrent or desaturation, and undervoltage V_{DD} or V_{EE}. During a status fault, both chipsets keep their respective gate drive outputs off; at V_{EE} for the IXBD4410/4411 and at 0 V for the IXBD4412/4413.

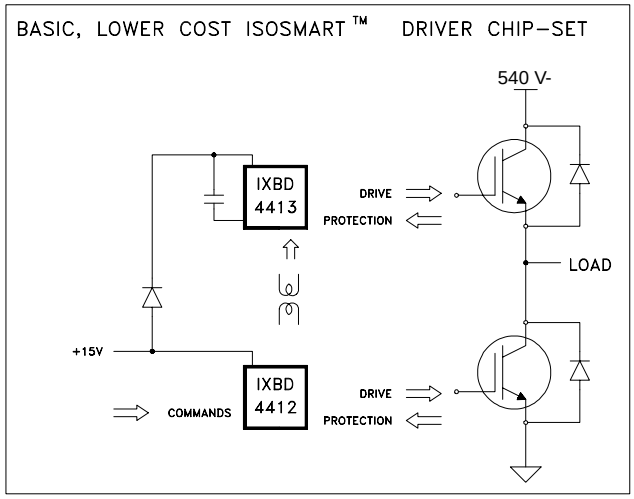
Features

- 1200 V or greater low- to high-side isolation.
- Drives Power Systems Operating on up to 575 V AC mains
- dv/dt immunity of greater than ±50V/ns
- Proprietary low- to high-side level-translation and communication
- On-chip negative gate-drive supply to ensure Power MOSFET or IGBT turn-off
- 5 V logic compatible HCMOS inputs with hysteresis
- Available in either the 16-Pin DIP or the 16-Pin wide-body, small-outline plastic package (IXBD4410/4411)
- 20 ns switching time with 1000 pF load; 100 ns switching time with 10000 pF load
- 100 ns propagation delay time
- 2 A peak output drive capability
- Self shut-down of output in response to over-current or short-circuit
- Under-voltage and over-voltage V_{DD} lockout protection
- Protection from cross conduction of the half bridge
- Logic compatible fault indication from both low and high-side driver (XBD4410/4411).

Applications

- 1- or 3-Phase Motor Controls
- Switch Mode Power Supplies (SMPS)
- Uninterruptible Power Supplies (UPS)
- Induction Heating and Welding Systems
- Switching Amplifiers
- General Power Conversion Circuits





IXYS reserves the right to change limits, test conditions and dimensions.

Symbol	Definition		Maximum Ratings	
V_{DD}/V_{EE}	Supply Voltage	4410/4411	-0.5 ... 24	V
V_{DD}/GND		4412/4413	-0.5 ... 24	V
V_{in}	Input Voltage (INH, INL)		-0.5...V_{DD} +0.5	V
I_{in}	Input Current (INL, INH, IM)		±10	mA
I_o (rev)	Peak Reverse Output Current (OUT)		2	A
P_D	Maximum Power Dissipation		600	mW
T_A	Operating Ambient Temperature		-40 ... 85	°C
T_{JM}	Maximum Junction Temperature		150	°C
T_{stg}	Storage Temperature Range		-55 ... 150	°C
T_L	Lead Soldering Temperature for 10 s		300	°C

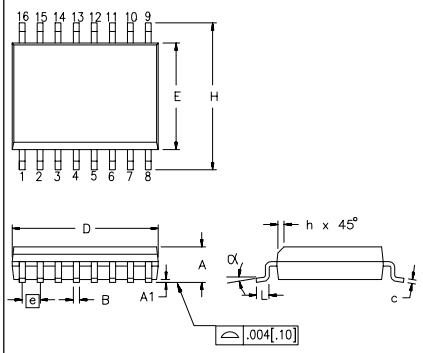
Recommended Operating Conditions

V_{DD}/V_{EE}	Supply Voltage	4410/4411	10 ... 20	V
V_{DD}/GND		4412/4413	10 ... 20	V
V_{DD}/LG			10 ... 16.5	V
L_{GH}/L_{GI}	Maximum Common Mode dv/dt		±50	V/ns

Symbol	Definition/Condition (T_A = 25°C, V_{DD} = 15 V, unless otherwise specified)	Characteristic Values min.	typ.	max.	
INL, INH Inputs (referred to LG)					
V_{t+}	Positive-Going Threshold	3.65			V
V_{t-}	Negative-Going Threshold			1	V
V_{ih}	Input Hysteresis		1		V
I_{in}	Input Leakage Current/V_{in}=V_{DD} or LG	-1		1	µA
C_{in}	Input Capacitance		10		pF
Open Drain Fault Output (referred to LG for 4410/4411)					
V_{oh}	HI Output/R_{pu} = 10 kΩ to V_{DD}	V_{DD}-0.05			V
V_{ol}	LO Output/I_o = 4 mA		0.3	0.5	V
OUT Output (referred to LG)					
V_{oh}	HI Output/I_o = -5 mA	V_{DD}-0.05			V
V_{ol}	LO Output/I_o = 5 mA		V_{EE}+0.05		V
R_o	Output HI Res./I_o = -0.1 A		3	5	Ω
R_o	Output LO Res./I_o = 0.1 A		3	4	Ω
I_{pk}	Peak Output Current/C_L = 10 nF	1.5	2		A
IM Input (referred to KG for 4410/4411 and to LG for 4412/4413)					
V_{t+}	Positive-Going Threshold	0.24	0.3	0.45	V
C_{in}	Input Capacitance		10		pF
R_s	Shorting Device Output Resistance	50	75	100	Ω
VEE Supply (referred to LG for 4410/4411)					
V_{EE}	Output Voltage/I_o = 1 mA, C_o = 1 µF	-5	-6.5	-7.5	V
I_{out}	Output Current/V_{out} = 0.70 • V_{EE}	-20	-25		mA
f_{inv}	Inverting Frequency		600		kHz
V_{EEF}	Undervoltage Fault Indication	-3		-4.8	V

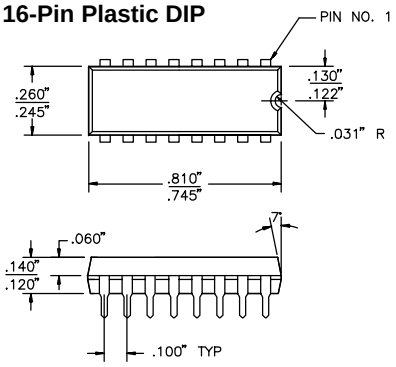
Dimensions in inch (1" = 25.4 mm)

16-Pin SO

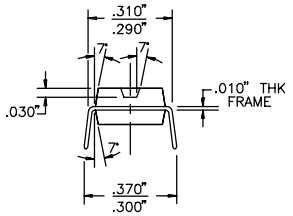


SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.093	.104	2.35	2.65
A1	.004	.012	.10	.30
B	.013	.020	.33	.51
C	.009	.013	.23	.32
D	.398	.413	10.10	10.50
E	.291	.299	7.40	7.60
e	.050 BSC		1.27 BSC	
H	.394	.419	10.00	10.65
h	.010	.029	.25	.75
L	.016	.050	.40	1.27
α	0°	8°	0°	8°

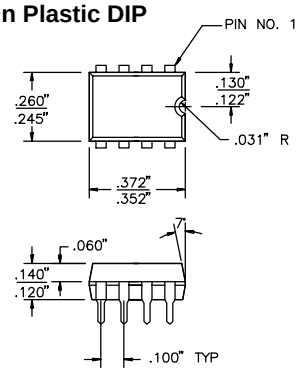
16-Pin Plastic DIP



Cross view for both packages



8-Pin Plastic DIP



Symbol	Definition/Condition		Characteristic Values (T_A = 25°C, V_{DD} = 15 V, unless otherwise specified) min.	typ.	max.	
V_{DD} Undervoltage Lockout						
V_{uv}	Drop Out		9.5	10.5	11.5	V
V_{uh}	Hysteresis		0.1	0.15	0.3	V
Quiescent Power Supply Current						
I_{DD}	V_{DD} Current/V_{in}=V_{DD} or LG, I_o = 0				20	mA
INL and INH Inputs (Fig. 1a - 1c)						
$t_{d(on)}$	Turn-on delay time; 4410/4412	C_L =1nF		110	175	ns
t_r	Rise time;	C_L =10 nF		70	100	ns
		C_L =1 nF		15	20	ns
$t_{d(off)}$	Turn-off delay time 4410/4412	C_L =1nF		70	150	ns
t_f	Fall time	C_L =10nF		70	150	ns
		C_L =1nF		15	20	ns
$t_{dlh(off)}$	4410/4412 Turn-on delay time vs. 4411/4413 Turn-off delay time	C_L =1nF		60	150	ns
$t_{dlh(on)}$	4410/4412 Turn-on delay time vs. 4411/4413 Turn-off delay time	C_L =1nF		60	150	ns
Fault Output Delay for any Fault Conditions (4410/4411)						
t_{FLT}	$\overline{FLT}$ Delay/R_{pu} = 2 kΩ	C_L = 20 pF		200	300	ns
Overcurrent Protection Delay						
t_{oc}	Driver-Off delay time	C_L = 1 nF		200	300	ns

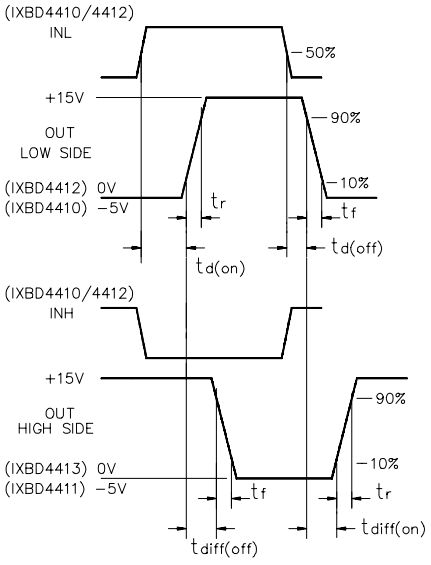


Fig. 1c: Output signal waveform

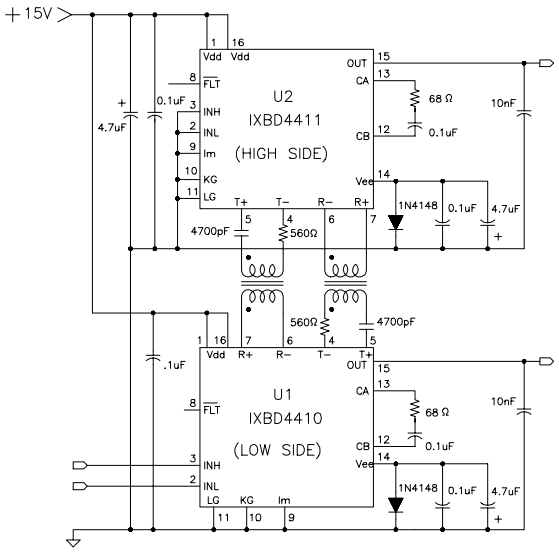


Fig. 1a: IXBD4410/4411 Switching time test circuit

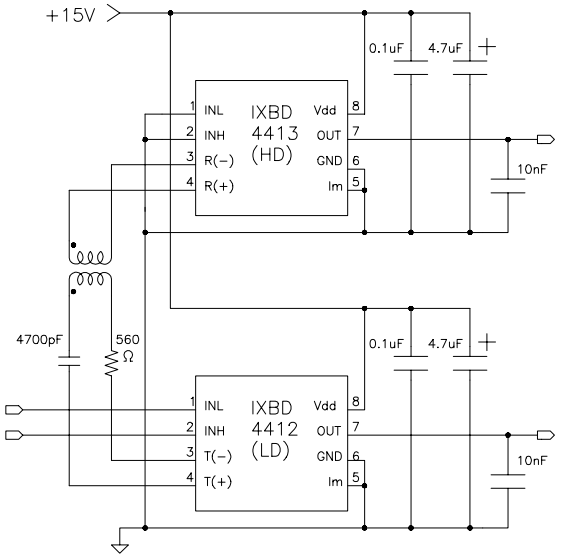


Figure 1b: IXBD4412/4413 Switching time test circuit

Chipset Overview

The ISOSMART™ chipsets are pairs of integrated circuits providing isolated high- and low-side drivers for phaseleg motor control, or any other application which utilizes a half bridge, 2- or 3-phase drive configuration. They consist of two drive control inputs (INL and INH) for two Power-MOSFET/IGBT gate-drive outputs. Both inputs operate from a common ground, and are activated by HCMOS compatible logic levels. The low-side output operates near input ground, while the high-side output operates from a floating ground that is nominally the source connection of the high-side phaseleg power device. Both outputs typically provide 2 A of transient current drive for fast switching of the phaseleg power device.

IXBD4410/IXBD4411

The full featured ISOSMART™ driver chipset incorporates a IXBD4410 as the low-side driver (Fig. 3) and a IXBD4411 as the high-side driver (Fig. 2). When input "INL" is set to a positive logic level, the low-side gate output goes high (turns on); when "INH" is set to a positive logic level, the high-side gate drive output goes high. The high-side IC is isolated from the low-side IC by a magnetic barrier, across which the turn on/off signal is transmitted to the high-side gate drive. In the case of the IXBD4410/4411 chipset, the IXBD4411 fault signal is also transmitted back to the IXBD4410 driver. This isolation only depends on the low cost communications transformer, which is designed to withstand 1200 V or more.

There are two magnetic transmission channels between the low- and high-side IC's for bi-directional communication (IXBD4410/4411). One sends a signal from the low-side IXBD4410 IC up to the high-side IXBD4411 IC, and the other sends a signal back from the high-side to the low-side IC. The signal that is sent up controls the IXBD4411 gate-drive output. The signal sent from the IXBD4411 back to the IXBD4410 indicates a high-side fault has occurred (overcurrent, or under-voltage of the high-side +power supplies). This is detected at the IXBD4410 driver and sets "$\overline{\text{FLT}}$" pin low, to indicate the high-side fault. The fault signal that is returned from the IXBD4411 is strictly for status; any gate-drive shutdown because of a high-side fault is done

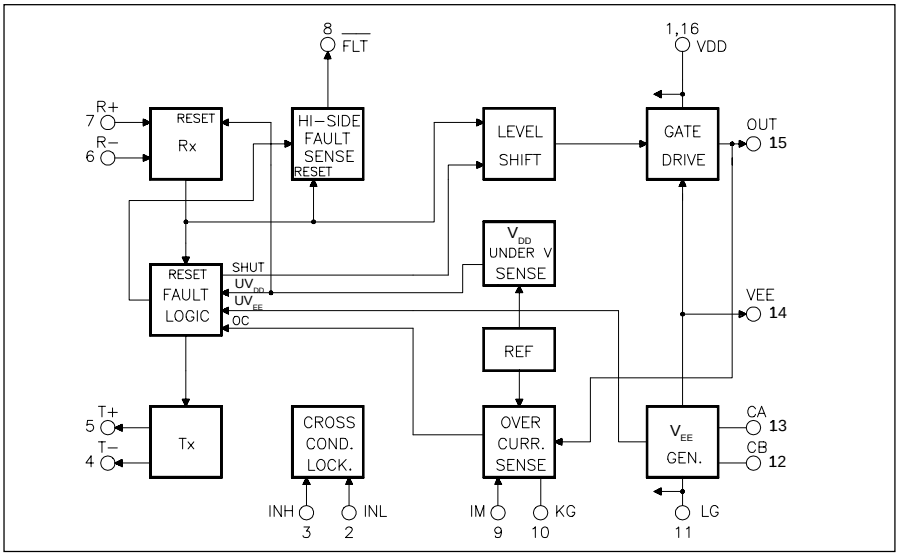


Fig. 2: IXBD4411, high-side driver block diagram

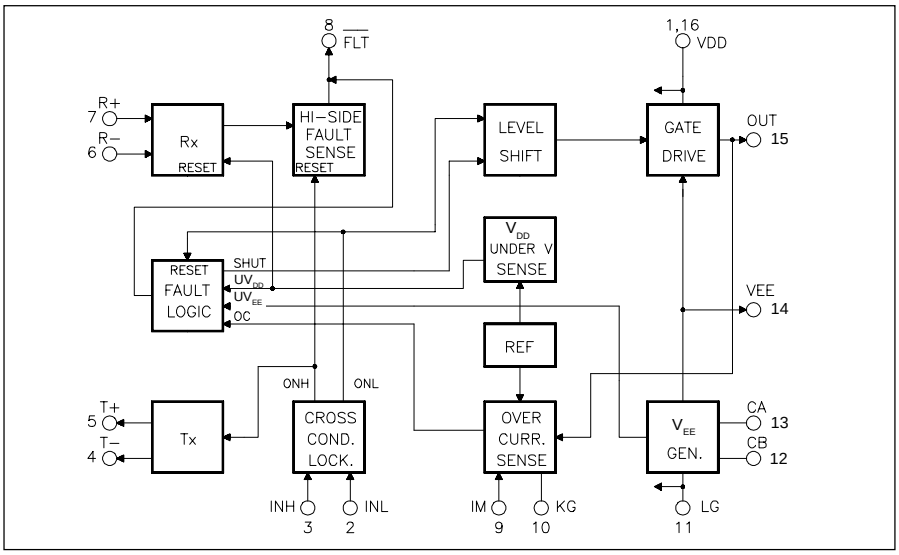


Fig. 3: IXBD4410, low-side driver block diagram

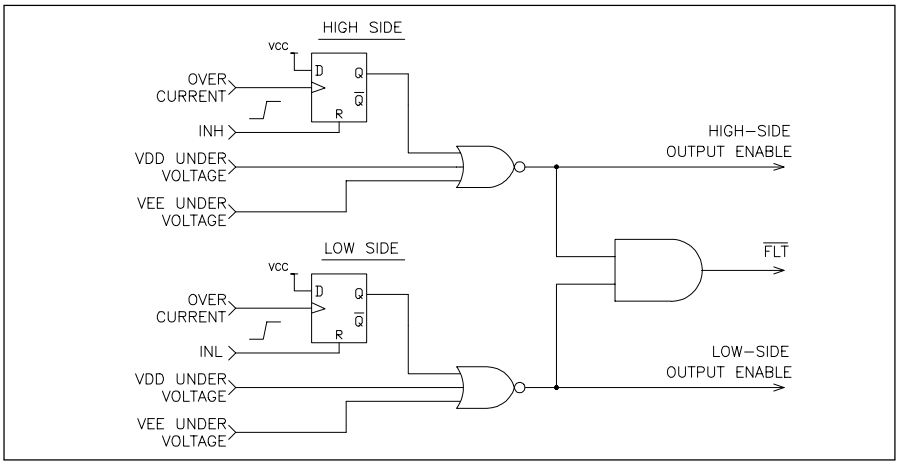


Fig. 4: Logic representation of IXBD4410 $\overline{\text{FLT}}$ signal

locally within the high-side IXBD4411. The IXBD4411 gate-drive will turn-off the power device whenever an overcurrent or under voltage condition arises. The overcurrent sensing is active only while the gate driver output is "high" (on). The overcurrent fault condition is latched and is reset on the next INH gate input positive transition. The $\overline{FLT}$ (pin 8) of the IXBD4411 is not used and should be grounded.

The low-side IXBD4410 driver provides an output pin 8 ($\overline{FLT}$) to indicate a high-side (IXBD4411) **or** a low-side (IXBD4410) fault. This output pin is an "open-drain" output. The IXBD4410 low-side driver fault indications are similar to the IXBD4411 high-side driver indications as outlined above. A "graphic" logic diagram of the chipset's $\overline{FLT}$ function is presented in Fig.4. Note that this diagram presents the logic of this function at the "low-side" IXBD4410 driver and is not the actual circuit. It describes the combined logic of the "fault logic" and "hi-side fault sense" blocks in both the IXBD4410 and IXBD4411 as shown in Fig. 2 and 3.

IXBD4412/IXBD4413

The basic, lower cost ISOSMART™ chipset consists of a pair of 8 Pin P-DIP ICs: IXBD4412 (low-side driver) and the IXBD4413 (high-side driver). It operates similarly to the IXBD4410/4411 pair, but does not include the negative drive or the fault indications option. This pair requires only a single magentic isolated transmission channel.

The most efficient method of providing power for the high-side driver is by bootstrapping. This method is illustrated in the functional drawing on page 4 and in the application example (Fig. 6 and 9) by diode D1 and capacitor C1. Using this method, the power is drawn through a high-voltage diode onto a reservoir capacitor whenever the floating high-side ground returns to near the real ground of the low-side driver; when the high-side gate is turned on, and the floating ground moves towards a higher potential, the bootstrapping diode back-biases, and the high-side driver draws its power solely from the reservoir capacitor. Power may also be provided via any isolated power supply (usually an extra secondary on the system housekeeping supply switching transformer).

Both the IXBD4410 and IXBD4411 contain on-board negative charge pumps to provide negative gate drive, which ensures turn-off of the high- or low-side power device in the presence of currents induced by power device Miller capacitance or from inductive ground transients. These charge pumps provide -5 V relative to the local driver ground when V_{DD} is at +15 V, and at rated average currents of 25 mA. The charge pump requires two external capacitors (C7 and C11 in Fig. 6). The charge pump frequency is nominally 600 kHz. The charge pump clock is turned off whenever the difference between the V_{DD} and V_{EE} supplies exceed 20 V, to prevent exceeding the breakdown rating of the IC.

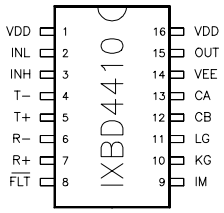
Both the IXBD4410 and IXBD4411 drivers possess two local grounds each, a common logic ground, and "Kelvin" ground. The Kelvin ground and logic grounds are first connected directly to each other, and then to the Kelvin-source of the power device for accurate over-current measurement in the presence of inductive transients on the power device source terminal.

Power MOSFET or IGBT overcurrent sensing utilizes an on -chip comparator with a typical 300 mV threshold. In a typical application, the current mirror pin of the Power MOSFET or IGBT is connected to a grounded, low-value resistor, and to the overcurrent comparator input on the high- or low-side driver. The comparator will respond typically within 150 ns to an overcurrent condition to shutdown the driver output. The power switches could be protected also by desaturation detection (see Fig. 6, 7 and 9).

To assure maximum protection for the phaseleg power devices, the chipset incorporates the following Power MOSFET and IGBT protection circuits:

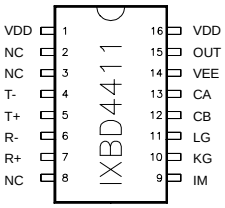
- Power device overcurrent or desaturation protection. The IXBD4410/4411 or 4412/4413 will turn off the driven device within 150 ns of sensing an output overcurrent, or desaturation condition.
- Gate-drive lockout circuitry to prevent cross conduction (simultaneous conduction of the low- and high-side phaseleg power devices), either under normal operating conditions or when a fault occurs.
- During power-up, the chipset's gate-drive outputs will be low (off), until the voltage reaches the under-voltage trip point.
- Under-voltage gate-drive lockout on the low- and/or high- side driver whenever the respective positive power supply falls below 9.5 V typically.
- Under-voltage gate-drive lockout on the low- and high- side driver whenever the respective negative power supply rises above -3 V typically (IXBD4410/4411).

Pin Description
IXBD4410 (Low-Side Driver)



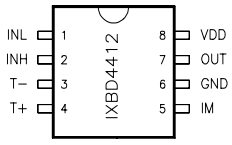
Sym.	Pin	Description of IXBD 4410/4411
VDD	1 16	Positive power supply.
INL **NC**	2	Logic input signal referenced to LG (logic ground). In the IXBD4410. A "high" to this pin turns on its gate drive output and resets its fault logic. A "low" to this pin turns off the gate drive output. In the IXBD4411 this pin is not used and should be connected to its ground (LG). **N**o **C**onnection (IXBD 4411)
INH **NC**	3	Logic input signal referenced to LG (logic ground). In the IXBD4410, this signal is transmitted to the IXBD4411 "high-side" driver through pins 4 and 5 (T- and T+). A "high" to this pin turns on the IXBD4411 gate drive output and resets its fault logic. A "low" to this pin turns off the IXBD4411 gate drive output. In the IXBD4411 this pin is not used and should be connected to its ground (LG). **N**o **C**onnection (IXBD 4411)
T- **T+**	4 5	Transmitter output complementary drive signals. Direct drive of the low signal transformer, which is connected to the receiver of the chipset's companion device. In the IXBD4410, this signal transmits the on/off command to its companion IXBD4411. In the IXBD4411, this signal transmits the fault indication to its companion IXBD4410 driver.
R- **R+**	6 7	Receiver input complementary signal. Directly connected to the low signal transformer, which is driven by the chipset's companion device. In the IXBD4410, this input receives the fault indication from its companion IXBD4411 driver. In the IXBD4411, this input receives the on/off command from its companion IXBD4410 driver.

Pin Description
IXBD4411 (High-Side Driver)



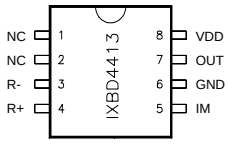
Sym.	Pin	Description of IXBD 4410/4411
$\overline{\text{FLT}}$ NC	8	Low/high side fault output. In the IXBD4410, this output indicates a fault condition of either device of the chipset. A "high" indicates no fault, A "low" indicates that either overcurrent, V_{DD} or V_{EE} under-voltage occurred. In case of overcurrent, this output will remain active "low" until the next input cycle of the respective driver. In case of under-voltage, this output will remain "low" until the proper voltage is restored. The IXBD4411 does not have a $\overline{\text{FLT}}$ output,and its pin 8 should be tied to LG **N**o **C**onnection (IXBD 4411)
IM	9	Current sense or desaturation detection input. This input is active only while the OUT pin is "high" (on). When the OUT pin is "low" (off) this input is pulled to ground through a 70 Ω resistor. Any voltage at this pin above the threshold of .3 V typical, will turn the output (pin 15) off. This pin is used for power device overcurrent protection.
KG	10	Kelvin ground. This ground is used as Kelvin connection for overcurrent or desaturation sensing.
LG	11	Logic and power ground.
CB	12	Capacitor terminals for negative charge pump (V_{EE}); "+" terminal is CB (pin 12).
CA	13	
VEE	14	Negative supply terminal.
OUT	15	Gate drive output. In the IXBD4410 this output responds to the INL signal. A "high" at INL will turn it on ("high"), a "low" will turn it off ("low"). In the IXBD4411, this output responds to the transmitted signal from the companion IXBD4410. A "high" at INH of the IXBD4410 drives will turn it on ("high"). A "low" will turn it off ("low"). This output will turn off ("low") also in response to any fault condition.

Pin Description
IXBD4412 (Low-Side Driver)



Sym.	Pin	Description of IXBD 4412
INL	1	Logic input signal referenced to GND. A "high" to this pin turns on the gate drive output and resets the fault logic. A "low" to this pin turns off the gate drive output.
INH	2	Logic input signal referenced to GND. A "high" to this pin is transmitted to the "high-side" driver (IXBD4413), turns on the "high-side" gate drive output and resets its fault logic. A "low" to this pin is transmitted to the "high-side" driver (IXBD4413) and turns off its gate drive output.
T-	3	Transmitter output comple-mentary signal. Direct drive of the low signal transformer, which is connected to the receiver of the companion IXBD4413 "high-side" driver. This signal transmits the on/off command to the companion driver.
T+	4	
IM	5	Current sense or desaturation detection input. This input is active only while the OUT pin is "high" (on). When the OUT pin is "low" (off) this input is pulled to ground through a 50 Ω resistor. Any voltage at this pin, above the threshold of 0.3 V typical, will turn the output (pin 7) off. This pin is used for power device overcurrent protection.
GND	6	Logic and power ground.
OUT	7	Gate drive output. This output responds to the INL signal. A "high" at INL will turn it on ("high"), A "low" will turn it off ("low"). Any fault condition will also turn this output off ("low").
VDD	8	Positive power supply.

Pin Description
IXBD4413 (High-Side Driver)



Sym.	Pin	Description of IXBD 4413
NC	1	Not used. Connect to GND (pin 6).
NC	2	Not used. Connect to GND (pin 6).
R-	3	Receiver input complementary signal. Directly connected to the low signal transformer, which is driven by the companion IXBD4412 "low-side" driver. This input receives the on/off command from its companion "low-side" IXBD4412 driver.
R+	4	
IM	5	Current sense or desaturation detection input. This input is active only while the OUT pin is "high" (on). When the OUT pin is "low" (off) this input is pulled to ground through a 70 Ω resistor. Any voltage at this pin, above the threshold of 0.3 V typical, will turn the output (pin 7) off. This pin is used for power device overcurrent protection.
GND	6	Logic and power ground.
OUT	7	Gate drive output. This output responds to the transmitted signal from the companion IXBD4412 "low-side" driver. A "high" at INH of the "low-side" driver (IXBD4412) will turn this output on ("high"), A "low" will turn off ("low"). Any fault condition will also turn this output off ("low").
VDD	8	Positive power supply.

Application

The IXBD4410/4411 or IXBD 4412/ 4413 chipset devices are specifically designed as MOS-gated transistor drivers in half-bridge power converters, 1- and 3-phase motor controls, and UPS applications. The phaseleg PWM command is normally generated by previous (user provided) circuitry. It must be decomposed into two separate logic signals, one for the high-side and one for the low-side power transistors, with appropriate deadtime for each state transition. The deadtime insures non-overlapping conduction even if the turn-on and turn-off delay times of the power devices are unequal. The minimum deadtime should be greater than t_{dlh}. A separate circuit, or an IC device like the IXYS deadtime generator IXDP630, can be used to perform this function. The ISOSMART™ chipset family of devices do not generate deadtime, although there is an internal lockout that prohibits one device form being commanded "on" before the other is commanded "off". This simplifies start-up and shutdown protection circuitry, preventing logic error during power-up from turning on both high-and low-side transistors simultaneously.

Negative V_{EE} Charge Pump Circuit Design

The on-chip V_{EE} generator provided in the IXBD4410/4411 generates a negative power supply, regulated at 20 V below the positive V_{DD} rail. (Note: this circuit is not present in the lower-cost IXBD4412/4413 chipset).If V_{DD} is +10 V, V_{EE} will be -10 V. If V_{DD} is +15 V, V_{EE} will be -5 V. This negative drive potential in the off-state is either desirable or required in many instances. When switching a clamped inductive load (Fig. 5), the turn-on of Q2 will commutate the freewheeling diode around Q1. Whether this diode is intrinsic (as in a MOSFET) or extrinsic (IGBT or bipolar), its reverse recovery is critical to proper circuit operation.

At high turn-on di/dt in Q2, and near its rated voltage, the recovery of D1 can get quite "snappy" (the di/dt in the second half of the recovery process, after the diode has begun to recover its blocking capability, can get very large), creating a very high dv/dt across Q1. This dv/dt is impressed across the Miller capacitance of Q1, forcing a large

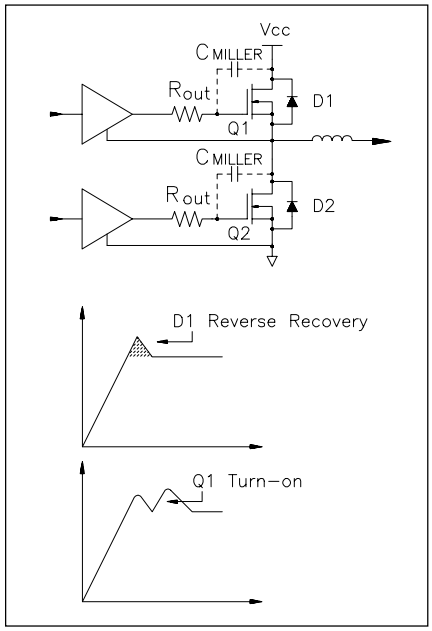


Fig. 5: Switching a clamped inductive load

current to flow out the gate terminal of the device. If this current pulse causes a high enough voltage drop across the output impedance of the gate drive circuit, R_{out}, Q1 will be turned on.

The Q1 conduction in every instance Q2 is turned on (and Vice Versa), aside from degrading efficiency, can lead to catastrophic failure of both power transistors. At high temperature, where the -6 to -7 mV/°C temperature coefficient of IGBT/MOSFET threshold reduces the voltage required to create a failure, this problem is even more likely to occur. In an industrial module package (e.g.: a 150 A/1200 V IGBT phaseleg module), the series inductance contributed by the long gate leads and connectors further complicate the design.

In a heavily snubbered converter, or in a power supply design with low transformer leakage inductance, the design problem is relatively simple and negative drive is seldom required. In these applications, the IXBD4412/4413 is adequate. However, in a modern snubberless or lightly snubbered converter design, it is important to keep the gate drive impedance high enough during transistor turnoff to limit the reapplied dv/dt (the transistor is its own 'active' snubber). This is always important for EMI control, and in the case of IGBT may be required to achieve the necessary RBSOA. At the same time, it is mandatory to keep the off-state gate drive impedance very low to assure the transistor remain off during induced dv/dt (including diode recovery dv/dt). In some instances, it is simply not possible to satisfy both criteria with 0 V applied in the off-state. In these cases the IXBD4410/4411 with V_{EE} negative bias generator must be used.

The internal V_{EE} generator is a charge pump circuit. Referring to Fig. 6, an external charge pump capacitor is required between the CA and CB

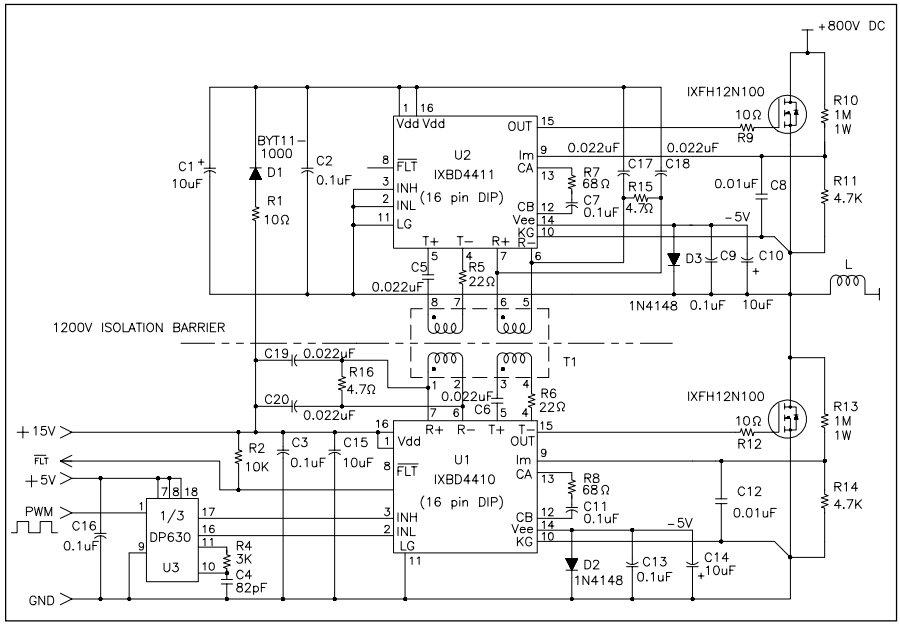


Fig. 6: IXBD4410/4411 Detailed one phase circuit with dead time generator IXDP 630

terminals (C7, C11), and an output reservoir capacitor between V_{EE} and GND (C10, C14). A 0.1 µF charge pump capacitor (C7, C11) is recommended. The voltage regulation method used in the IXBD4410/4411 allows a 1 to 2 V ripple frequency depends on the size of the V_{EE} output reservoir capacitor (C10, C14) and the average load current. The minimum recommended output reservoir (C10, C14) is 4.7 µF tantalum, or 10 µF if aluminium electrolytic construction is chosen. Note that this reservoir capacitor is in addition to a good quality high frequency bypass capacitor (0.1 µF) that should be placed from VEE to GND (C9, C13).

A small resistor in series with the charge pump capacitor, (R7, R8) reduces the peak charging currents of the charge pump. A value or 68 Ω or greater is recommended, as illustrated in the applications example in Fig. 6.

Current Sense / Desaturation Detection Circuit

All members of the ISOSMART™ driver family provide a very flexible overcurrent/short circuit protection capability that works with both standard three-terminal power transistors, and with 4- and 5-terminal current sensing power devices. Overcurrent detection is accomplished as illustrated in Fig. 7a (for a current mirror power device) and Fig. 7b (for a standard three terminal power transistor). Desaturation detection is accomplished with the same internal circuits by measuring the voltage across the power transistor in the on-state with an external resistor divider (Fig. 7c).

The IM input trip point V_{TIM}, typically 300 mV, is referenced to the Kelvin ground pin KG.

Current Mirror MOSFET and IGBT allow good control of peak let-thru currents and excellent short circuit protection when combined with the ISOSMART™ driver family of devices. The sense resistor is chosen to develop 300 mV at the desired peak transistor current, assuming a mirror ration of 1400:1, and a trip point of 30 A is desired:

R_s = 300 mV • 1400/30 A = 14 Ω
(use 15 Ω CC).

It is important to realize that C_{oss} per unit area of the mirror cells is much

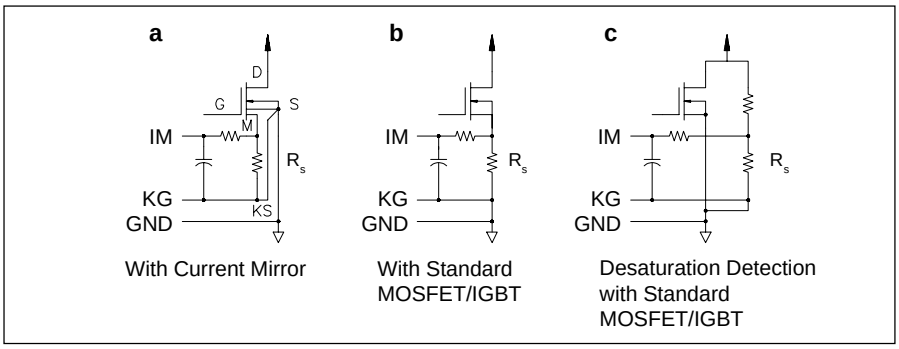


Fig. 7: Alternative overcurrent protection circuits

larger that C_{oss} per unit area of the bulk of the chip (due to periphery effects). This causes a large transient current pulse at the mirror output whenever the transistor switches (C • dv/dt currents), which can cause false overcurrent trigger. The RC filter indicated in Fig. 7a will eliminate this problem.

Standard three-terminal MOSFET and IGBT devices (in discrete as well as modern industrial single transistor and phaseleg modules) can also be protected from short circuit with the ISOSMART™ driver family devices. In discrete device designs, where the source/emitter terminal is available, overcurrent protection with an external power resistor can be implemented. The resistor is placed in series with the device emitter, with the full device current flowing through it (Fig. 7b). The sense resistor is again selected to develop 300 mV at the desired peak transistor current, assuming a trip point of 30 A is desired:

R_s = 300 mV / 30 A = 10 mΩ
(use 10 mΩ, non-inductive current sense resistor).

It is important to recognize that "non-inductive" is a relative term, especially when applied to current sense resistor construction and characterization. There is always significant series inductance inserted with the sense resistor, and L • di/dt voltage transients can cause false overcurrent trigger.

The RC filter indicated in Figure 7b will eliminate this problem. Choosing the RC pole at the current sense resistor RL zero should exactly compensate for series inductance. Because the exact value is not normally known (and can vary depending on PC layout and component lead dress) this is not normally a good idea. Usually, the RC time constant should be two to ten times longer than the suspected RL time constant.

Desaturation detection as in Figure 7c is probably the most common method of short circuit protection in use today. While not strictly an "overcurrent" detector, if the power transistor gain, and consequently short circuit let-thru current, is well controlled (as with modern MOSFET and IGBT) this methodology offers very effective protection.

Both the IXBD4410/4411 one-phase (half-bridge) circuits in Fig. 6 and the IXBD4412/4413 circuit in Fig. 9 uses desaturation detection. In Fig. 6, the voltage across the two Power MOSFET devices (or IGBTs) are monitored by two sets of voltage-divider networks, R10 and R11 for the high-side gate driver, and R13 and R14 for the low-side gate driver. The dividers are set to trip the IM input comparators when either Power MOSFET device V_{DS} exceeds a reasonable value, perhaps 50 V (usually a value of 10 % of the nominal DC bus voltage works well). R10 or R13 are chosen to tolerate the applied steady state DC bus voltage at an acceptable power dissipation. Dielectric withstand capability, power handling, temperature rise, and PC board creep and strike spacings, must all be carefully considered in the design of the voltage-divider networks.

In the off-state, the voltage across the Power MOSFET device may go as high as the DC bus potential. To keep this normal condition from setting the internal fault flip-flop of the IXBD4410 or the IXBD4411, an internal CMOS switch is turned on and placed across IM and KG pins shorting them together. This effectively discharges C8 or C12 in Fig. 6 and maintains zero potential with respect to KG at IM.

When the command arrives to switch on the Power MOSFET device, the CMOS switch shorting IM to KG is turned off. The driven Power MOSFET device is switched on approximately 100 ns to 1 µs later, and with typical load conditions, its drain-to-source potential, V_{DS}, may take an additional 10 µs of delay to collapse to the normal on-state voltage level. To prevent false triggering due to this, C8 or C12 in parallel combination with R10 and R11, or R13 and R14, delays the IM input signal. During this turn-on interval, the voltageacross C8 or C12 will rise until the Power MOSFET device finally comes on and pulls the voltage across C8 or C12 back down. If the MOSFET device load circuit is shorted, its V_{DS} voltage cannot callapse at turn-on. In this case, the voltage across C8 or C12 rises rapidly until it reaches 300 mV, tripping the fault flip-flop and shutting down the driver output. At the same time, C8 or C12 must be kept small enough that the added delay does not slow down the detection of a short circuit event so much that the Power MOSFET device fails before the driver realizes that it is in trouble. The desaturation detection circuit in Fig. 9 functions identically to the one in Fig. 6 as just described. Current limit or desaturation detection is latched, and reset on a cycle-by-cycle basis with the rising edge of the respective input command.

Three Phase Motor Controls

Fig. 8 is a block diagram of a typical 3-phase PWM voltage-source inverter motor control. The power circuit consists of six power switching transistors with freewheeling diodes around each of them. The control function may be performed digitally by a microprocessor, microcontroller, DSP chip, or user custom IC; or it may be performed by a PC board full of random logic and analog circuits. In any of these cases, the PWM command for all six power transistors is generated in one circuit, and this circuit is usually referred to system ground potential - the bottom terminal of the power bridge.

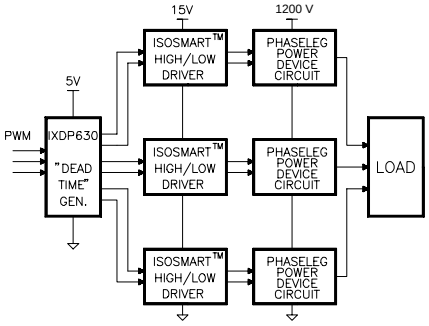


Fig. 8: Typical 3-phase motor control system block diagram

The ISOSMART™ family of drivers is the interface between the world of control logic and the world of power, 5 V input logic commands precisely control actions at high voltage and current (1200 V and 100 A in a typical application). Fig. 6 is a detailed schematic of one phase of three 3-phase motor control, showing the interconnection of the IXBD4410/4411 and its associated circuitry.

This application utilizes the full feature set of the IXBD4410/4411 family of devices in a 460 V~ line operated inverter. In situations that would not benefit from the negative gate drive, and do not require the fault status output, the IXBD4412/4413 chipset may prove adequate. Fig. 9 is a complete schematic of one phase of a 3-phase inverter using the lower cost IXBD4412/4413 chipset. Notice the reduction in total parts count. With the smaller 8-pin packages of the devices themselves, the IXBD4412/4413 chipset offers a 70 % reduction in PC board real estate for a modest reduction in feature set compared to the IXBD4410/4411 devices.

PCB Layout Considerations

The IXBD4410/4411 or IXBD4412/4413 is intended to be used in high voltage, high speed, high dv/dt applications.

To ensure proper operation, great care must be taken in laying out the printed circuit board. The layout critical areas include the communication links, current sense, gate drive, and supply bypassing.

The communication path should be as short as possible. Added inductance disturbs the frequency response of the signal path, and these distortions may cause false triggering in the receiver. The transformer should be placed between the two ICs with the orientation of one IC reversed (Fig. 10).

Capacitance between the high- and low-side should be minimized. No signal trace should run underneath the communication path, and high- and low-side traces should be separated on the PCB. The dv/dt of the high-side during power stage switching may cause false logic transitions in low-side circuits due to capacitive coupling.

The low signal pulse transformer provides the isolation between high-and

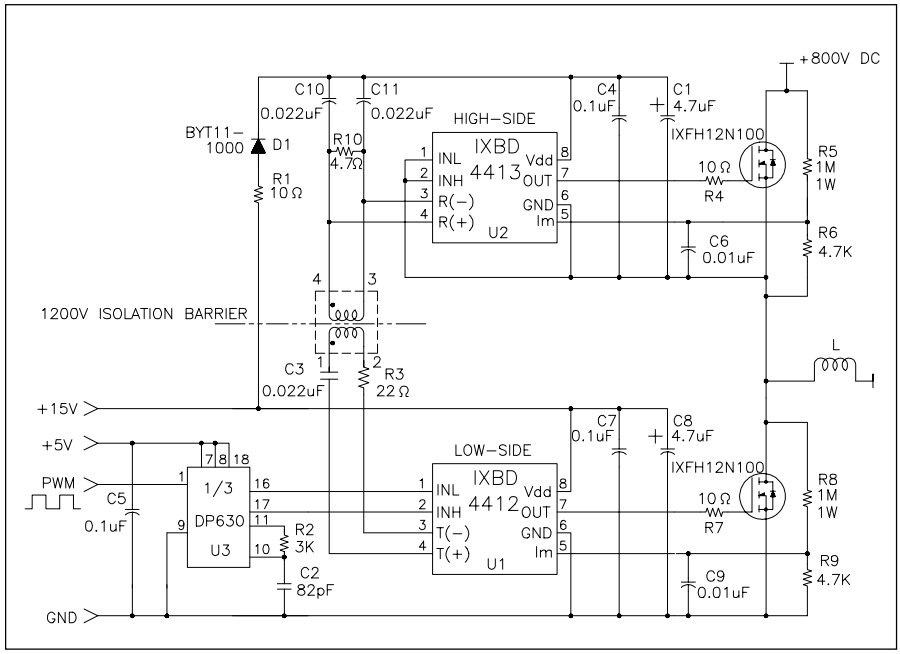


Fig. 9: Lower cost IXBD4412/4413 single phase circuit with deadtime generator IXDP630

low-side circuits. For 460 V~ line operation, a spacing of 4 mm is recommended between low- and high-side circuits, and a transformer HIPOT specification of at least 1500 V~ is required. This creep spacing is usually adequate to control leakage currents on the PCB with up to 1200 V~ applied after 10 to 15 years of accumulated dust and particulates in a standard industrial environment. In other environments, or at other line voltages, this spacing should be appropriately modified.

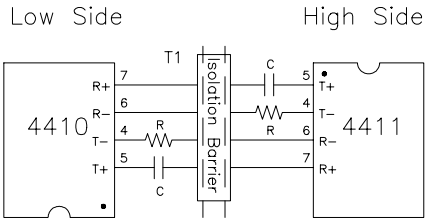


Fig. 10: Suggested IC Orientation

The current sense/desaturation detect input is noise sensitive. The 300 mV trip point is referred to the KG (Kelvin ground) pin, and the applied signal must be kept as clean as possible, A filter is recommended, preferably a monolithic ceramic capacitor placed as close to the IC as possible directly between IM and KG. To preserve maximum noise immunity, the KG pin should first be connected directly to the LG pin, and the pair then sent directly to the power transistor source/emitter terminal, or (if a desaturation detection circuit is used) to the bottom of the divider resistor chain.

All supply pins must be bypassed with a low impedance capacitor (preferably monolithic ceramic construction) with minimum lead length. The output driver stage draws 2 A (typical) currents during transitions at di/dt values in excess of 100 A/µs. Supply line inductance will cause supply and ground bounce on the chip that can cause problems (logic oscillations and, in severe cases, possible latchup failure) without proper bypassing. These bypass elements are in addition to the reservoir capacitors required for the negative Vee supply and the high-side bootstrapped supply if these features are used.

Power Circuit Noise Considerations

In a typical transistor inverter, the output MOSFET may switch on or off with di/dt >500 A/µs. Referring to Fig.11 and assuming that the MOSFET source terminal has a one inch path on the PCB to system ground, a voltage as high as V = 27 nH • 500 A/µs = 13.5 V can be developed. If the MOSFET switched 25 A, the transient will last as long as (25/500) µs or 50 ns, which is more than the typical 6 or 7 ns propagations or of a 74HC series gate.

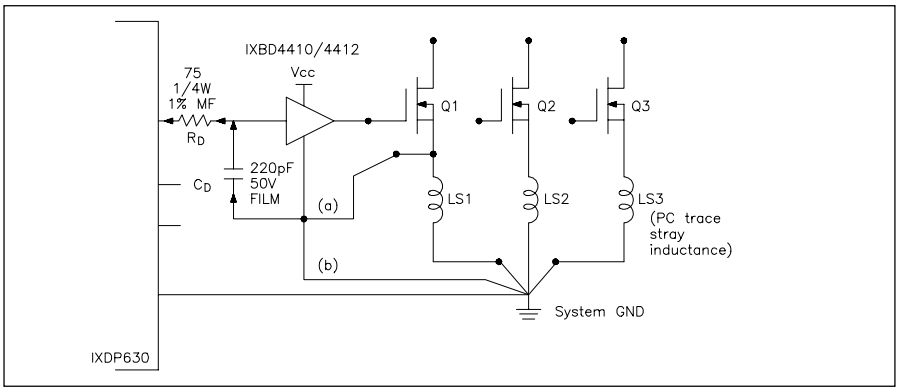


Fig. 11: Potential layout problems that create functional problems

Fig. 11 illustrates an example layout problem. The power circuit consists of three power transistors (MOSFETs in this example). With the ISOSMART™ gate driver chipset grounded as in option (b) in Fig. 11, the communication path from the IXDP630 will operate without errors. The PC trace induced voltages are not common with the digital path, so the input of the gate driver will not see or respond to them.

Unfortunately, the MOSFET will not operate properly. The voltage induced across LS1 when Q1 is turned on, acts as source degeneration, modifying the turn-on behavior of the MOSFET. If LS1= 27 nH, and V_{CC} is 15 V (assuming the gate plateau of the MOSFET is 6 V), the di/dt at turn-on will be regulated by the driver/MOSFET/LS1 loop to about 200 A/µs; quite a surprise when your circuit requires 500 A/µs to operate correctly.

It is possible to make use of this behavior to create a turn-on or turn-off di/dt limiter (perhaps to snub the upper free wheeling diode reverse recovery). While possible, this is normally not desirable or practical where two or more transistors are controlled. Equalizing the parasitic impedances of three traces while positioning the transistors next to their heat sink and meeting UL/VDE voltage spacings is just too difficult.

Grounding the gate driver as in option (a) in Fig. 11 solves the MOSFET turn on problem by eliminating LS1 from the source feedback loop. Now, unfortunately, the gate driver will oscillate every time it is turned on or off. As the IXDP630 output goes "high", the gate drive output follows (after its propagation delay) and the MOSFET starts to conduct. The voltage transient induced across LS1 (V = LS1 • di/dt) raises the local ground (point a) until it exceeds V_{oh} (630) - V_{il} (4410/4412) and the driver (after its propagation delay) turns the MOSFET off. Now the MOSFET current falls, V(LS1) drops, point (a) drops to system ground (or slightly below), and the driver detects a "1" at its input. After its propagation delay, it again turns the MOSFET on, continuing the oscillation for one more cycle.

To eliminate this problem, a ground level transformation circuit must be added, that rejects this common mode transient. The simplest is a de-coupling circuit, also illustrated in Fig. 11. The capacitor voltage (on C_d) remains constant while the transient voltage is dropped across R_d and the driver detects no input transition, eliminating the oscillation. This circuit does add significantly to turn-on and turn-off delay time, and cannot be used if the transient lasts longer than the allowable delays. Delay times must be considered in selection of system dead time.

The most complex (and most effective) method of eliminating the effects of transients between grounds is isolation.

Optocouplers and pulse transformers are the most commonly used isolation techniques, and work very well in this case. The IXDP630/631 has been specifically designed to directly drive a high speed optocoupler like the Hewlett Packard HCPL22XX family or the General Instrument 740L60XX optologic family. These optos are especially well suited to motor control and power conversion equipment due to their very high common mode dv/dt rejection capabilities.

Transformer Considerations

The transformer is the communication link and isolation barrier between the high- and low-side ICs. The high-side gate and fault signals are transmitted through the transformer while maintaining the proper isolation. The transmitter signal is in the form of a square wave, but the receiver responds only to the logic edges. This allows for much smaller transformer designs, since a 10 kHz switching frequency does not require a 10 kHz pulse transformer.

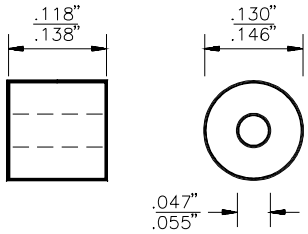


Fig. 12: Ferrite bead dimensions

The recommended transformer for this ISOSMART™ driver chipset is fabricated using a very small ferrite shield bead (see Fig. 12), onto which a six-turn primary and a two-turn secondary winding of 36 AWG magnet wire are made. The two windings are segment wound to achieve primary-to-secondary isolation of up to 2500 V~. The six-turn primaries are connected to the respective IXBD4410/4411 transmitter outputs and the two-turn secondaries are connected to their respective receiver inputs.

The nominal electrical specifications of the transformer are as follows:

- Open circuit inductance (100 kHz; 20 mV): 3 µH
- Interwinding capacitance: 2 pF
- Primary leakage inductance: 0.1 µH
- Turns ratio: 6:2
- Primary-to-secondary isolation (1min): 1500 V~
- Core permeability (μ_i): 125

The recommended ferrite bead is Fair Rite Products' part number 2661000101. It is manufactured by:

Fair-Rite Products Corp.
Wallkill, NY
Phone: (914) 895-2055

Several transformer manufacturers have produced custom transformers for the IXBD4410/4411 and IXBD 4412/4413 chip set, to the above specifications:

1) 12 Pin DIP outline-
   Part Number 500 - 1914
   BH Electronics
   Buinsville, MN
   Phone: (612) 894-9690

2) 8 Pin DIP outline-
   Part Number 23Z129
   Fil-Mag
   San Diego, CA
   Phone: (619) 569-6577

3) Transformer, type 23Z119 for IXBD 4412/4413 and 23Z129 for IXBD 4410/4411
   FEE,
   Rodgau/Germany
   Phone: +49-6106-2011
   Fax: +49-6106-24286

As seen in the application drawings (Fig. 6, 9 and 13) a coupling capacitor (22 nF) and a damping resistor (22 Ω) are added in series with the primary side of the transformer. The capacitor will control the small amount of energy needed to transfer the signal to the companion driver. The resistor will control the damping of the signal and limit the peak transmitter output current. The receiver is designed to operate over a wide common mode input range. To reduce noise pickup, the receiver has ±250 mV of input hysteresis.

If the signal is being distorted at the transmitter, the transmitter is probably running into current limit. A decrease in the coupling capacitance or an increase in the damping resistance should solve this problem. The receiver operates over a wide input range. The minimum amplitude for one side of the receiver is about 1 V and a maximum of about 3 V. It is critical that there be no overshoot on the transformer secondary waveform. Each signal should be slightly overdamped. If significant overshoot exists, the received signal may be logically inverted. An increase of the damping resistor will solve this problem.

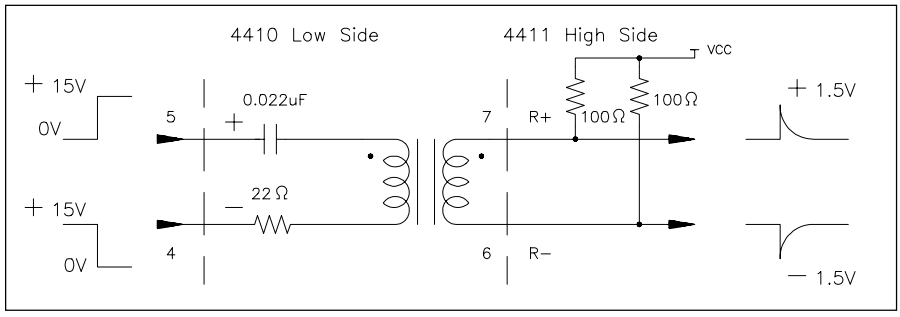


Fig. 13: Transmitter/Receiver Waveforms

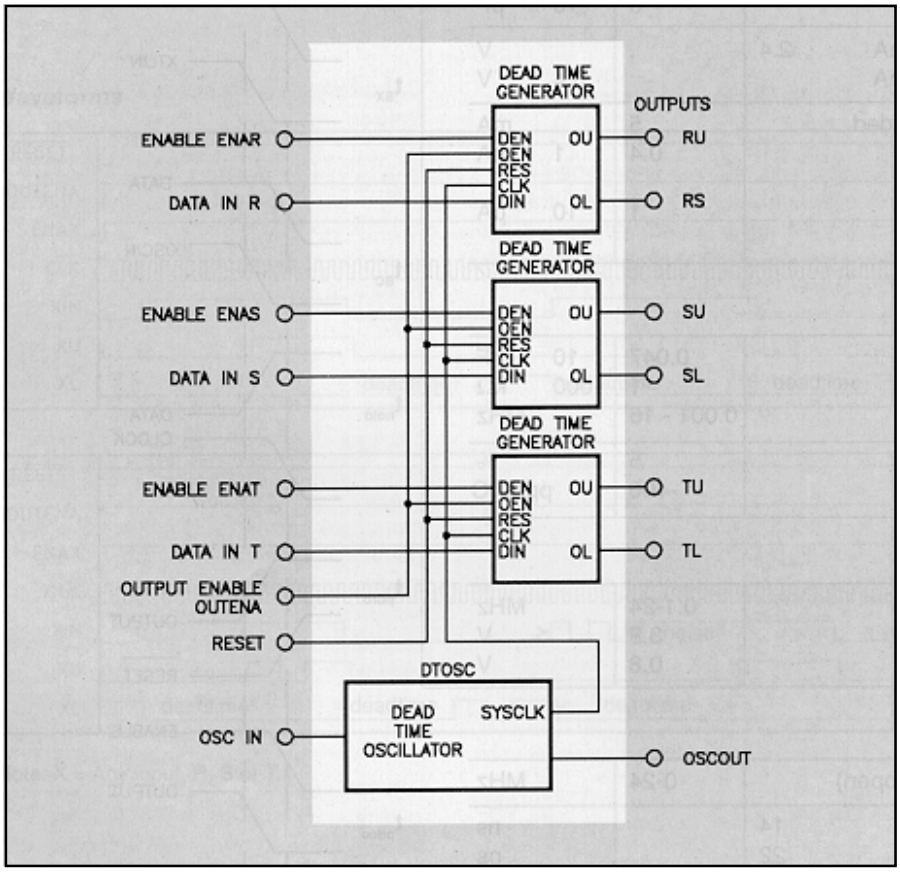
Inverter Interface and Digital Deadtime Generator for 3-Phase PWM Controls

Type	Package	Configuration	Temp. Range
IXDP630 PI	18-Pin Plastic DIP	RC Oscillator	-40°C to +85°C
IXDP631 PI	18-Pin Plastic DIP	Crystal Oscillator	-40°C to +85°C

This 5 V HCMOS integrated circuit is intended primarily for application in three-phase, sinusoidally commutated brushless motor, induction motor, AC servomotor or UPS PWM modulator control systems. It injects the required deadtime to convert a single phase leg PWM command into the two separate logic signals required to drive the upper and lower semiconductor switches in a PWM inverter. It also provides facilities for output disable and fast overcurrent and fault condition shutdown.

In the IXDP630, deadtime programming is achieved by an internal RC oscillator. In the IXDP631, programming is achieved by use of a crystal oscillator. An alternative for both the IXDP630/631 is with an external clock signal. Because of its flexibility, the IXDP630/631 is easily utilized in a variety of brushed DC, trapezoidally commutated brushless DC, hybrid and variable reluctance step and other more exotic PWM motor drive power and control circuit designs.

Block Diagram IXDP 630/IXDP 631



Features

- 5 V HCMOS logic implementation maintains low power at high speed
- Schmitt trigger inputs and CMOS logic levels improve noise immunity
- Simultaneously injects equal dead-time in up to three output phases
- Replaces 10-12 standard SSI/MSI logic devices
- Allows a wide range of PWM modulation strategies
- Directly drives high speed optocouplers

Applications

- 1- and 3- Phase Motion Controls
- 1- and 3- Phase UPS Systems
- General Power Conversion Circuits
- Pulse Timing and Waveform Generation
- General Purpose Delay and Filter
- General Purpose Three Channel "One Shot"

IXYS reserves the right to change limits, test conditions and dimensions.

Symbol	Definition	Maximum Ratings min.	max.	
V_{CC}	Supply Voltage	-0.5	7	V
V_{IN}	DC Input Voltage	-0.5	V_{CC} + 0.5	V
I_{IN}	DC Input Current	-1	1	mA
V_0	DC Output Voltage	0.5	V_{CC} + 0.5	V
I_0	DC Output Current	-25	25	mA
T_{stg}	Storage Temperature	-55	150	°C
T_L	Lead Soldering (max. 10 s)		300	°C

Recommended Operating Conditions

V_{CC}	Supply Voltage	4.5	5.5	V
T_J	Operating Temperature	-40	85	°C
I_0	Output Current	-8	8	mA
f_{OSC}	Oscillator Frequency	0.001	16/24	MHz

Symbol	Definition/Condition	Characteristic Values min.	typ.	max.	
V_{t+}	Input Hi Threshold	3.6	2.7		V
V_{t-}	Input Lo Threshold		1.6	0.8	V
V_{HYS}	Hysteresis		1.1		V
I_{in}	Input Leakage Current	-10		10	µA
C_{in}	Input Capacitance		5	10	pF
V_{oh}	Output High Voltage I_o = -8 mA	2.4			V
V_{ol}	Output Low Voltage I_o = 8 mA			0.4	V
I_{CC}	Supply Current Outputs Unloaded		5		mA
I_{CCQ}	Quiescent Current Outputs Unloaded IXDP630		0.4	1	mA
I_{CCQ}	Quiescent Current Outputs Unloaded IXDP631		1	10	µA

DP630 Oscillator Section

C_{OSC}	Capacitor (RCIN to GND)	0.047	10	nF
R_{OSC}	Resistor (OSCOUT to RCIN)	1	1000	kΩ
f_{OSC}	Frequency Range	0.001 - 16		MHz
	Initial Tolerance ($f_{OSC} \leq$ 1MHz)	5		%
	Temperature Coefficient	-400		ppm/°C

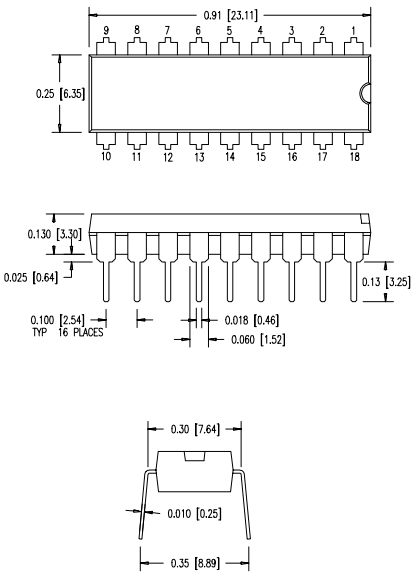
DP631 Oscillator Section

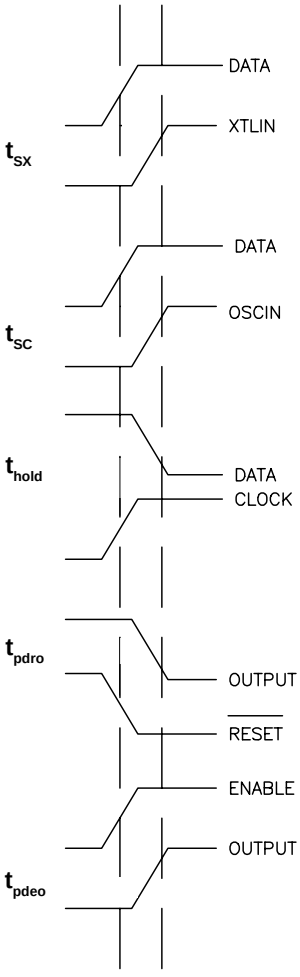
f_{OSC}	Frequency Range	0.1-24		MHz
V_{INH}	Oscillator Thresholds (IXTLIN)	3.9		V
V_{INL}		0.8		V

External Oscillator

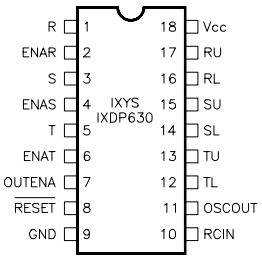
f_{IN}	Frequency Range (ODCOUT open)		0-24		MHz
t_{sx}	Set Up Time DATA-to-XTLIN	14			ns
t_{sc}	Set Up Time DATA-to-OSCIN	22			ns
t_{hold}	Hold Time CLOCK-Data	0			ns
t_{pdro}	Propagation Delay RESET-to-OUTPUT		15	20	ns
t_{pdeo}	Propagation Delay ENABLE-to-OUTPUT		8	16	ns

Dimensions in inch (1" = 25.4 mm)
16-Pin Plastic DIP

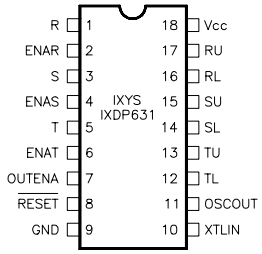




Pin Description IXDP630



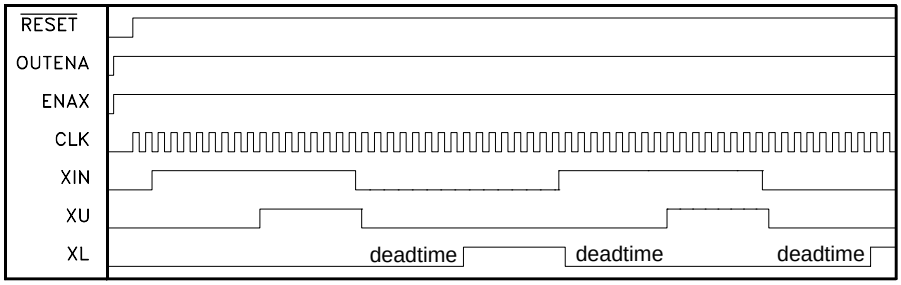
Pin Description IXDP631



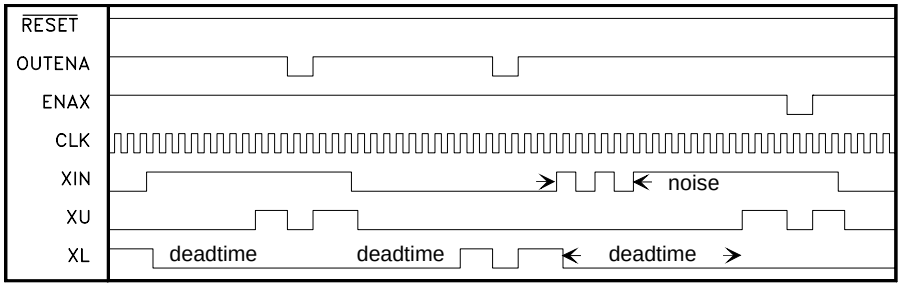
Sym.	Pin	Description
R S T	1 3 5	R, S and T are the three single-phase inputs. Each input is expanded into two outputs to generate non-overlapping drive signals, RU/RL, SU/SL, and TU/TL. The delay from the falling edge of one line to the rising edge of the other is a function of the clock.
ENAR ENAS ENAT	2 4 6	High logic input will enable the outputs, as set by the proper input phase. The ENA (R,S,T) signals control the drive output lines. A low logic input will force both controlled outputs to a low logic level
OUT ENA	7	High logic level will enable all outputs to their related phase. The OUTENA simultaneously controls all outputs. Low input logic level will inhibit all outputs (low).
$\overline{\text{RESET}}$	8	The $\overline{\text{RESET}}$ signal is active low. When a logic low $\overline{\text{RESET}}$ is applied, all outputs will go low. After releasing the $\overline{\text{RESET}}$ command within the generated delay, the outputs will align with the phase input level after the programmed delay internal.

Sym.	Pin	Description
GND	9	CIRCUIT GROUND - 0 Volts
RCIN or XTLIN	10	The first node of the clock network. For the IXDP630, the RC input is applied to RCIN. For the IXDP 631, the crystal oscillator is applied to XTLIN. If an external clock is to be supplied to the chip it should be connected to this pin.
OSC OUT	11	This is the output node of the oscillator. It is connected indirectly to the RCIN or XTLIN pins when using the internal oscillator as described in the applications information. It is not recommended for external use.
TL TU SL SU RL RU	12 13 14 15 16 17	After the appropriate delay, the external drive outputs (R,S, T) U are in phase with their corresponding inputs; (R,S, T) L are the complementary outputs.
V_{CC}	18	Voltage Supply +5 V ± 10 %

Waveforms



This diagram shows the normal operation of the IXDP630/631 after the $\overline{\text{RESET}}$ input is released. The DEADTIME is the 8 Clock periods between XU and XL when both XU and XL are a "0". The length of the DEADTIME is fixed at 8 times the period of CLK.



The diagram shows OUTENA and ENAX asynchronously forcing the XU Output and the XL Output to the off state. OUTENA will force all three channels to the off state. ENAX (where X is one of the three channels) will only force the XU and XL Outputs of that channel to the off state. Note that because ENAX is asynchronous with respect to the internal clock and deadtime counters, when ENAX goes HI whatever state the deadtime counter was in immediately propagates to the output. This figure also shows that noise at the XIN input will be filtered before the XU Output or XL Output will become active, which may extend the deadtime.

Note: X = Any input, R, S or T.

Application Information

Basic Operation

The IXDP630/631 Deadtime Generators are intended to simplify the implementation of a single- or three-phase digitally controlled power conversion circuit. It replaces one to three digital event counters (timer/counters) in a microcontroller or DSP implementation of a motor control, UPS or other power system. In most cases these timers are at a premium. They must be used to calculate pulse width on one to three independent modulators, set interrupt service times, generate a real-time clock, handle communications timing functions, etc.

The input command on the R, S and T inputs is first synchronized with the internal oscillator. When an input changes state, the on output is switched off, and after a deadtime of exactly 8 clock periods, the complimentary output is switched on. For example, if input R is hi, output RU is hi. At the first rising edge of CLK out after input R is brought low, the RU output goes low. After exactly 8 more clock periods the RL output goes high. This injected delay is the deadtime.

This method of synchronizing is utilized to guarantee that the deadtime is always exactly the same (to the accuracy of the CLK frequency). This can be very important in certain applications. Unbalanced deadtime creates an offset in the PWM output stage transfer function, and can cause saturation of the induction machine control or the driven transformer if not corrected within a few cycles.

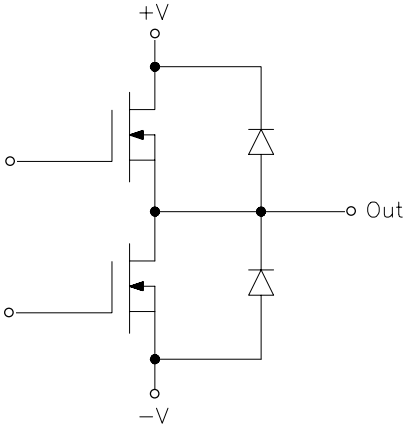


Fig. 1: Totem Pole configuration of transistor switches; reason for deadtime requirements

Deadtime in power circuits

Why is deadtime required?

Fig. 1 is typical of a switching power conversion equipment output stage. It has two (or typically more) switches. A simple logic error - turning a transistor on at the wrong instant - can cause catastrophic failure in the right (or **wrong**) circumstances.

In normal operation, when the state of the output totem pole must change, the conducting transistor is turned off. Then, after a delay (usually called the deadtime), the other transistor is turned on. The delay is added to ensure that there is no possibility of both transistors conducting at the same time (this would cause a short circuit of the DC link - a "shoot through" - and would likely fail both transistors in a few microseconds).

When the control logic commands a switch to change to the off state, several parasitics may delay/modify this command. The propagation delay of the control logic and gate drive buffer, td (off) of the power transistor, storage time (for bipolars) or tail time (for IGBTs), voltage rise and current fall times, etc., may be significant.

Problems Caused by Excessive Deadtime

If a little is good, a lot should be better - except with deadtime. Unfortunately, deadband in the switching output stage causes a nonlinearity in the power circuit transfer function that may be difficult for the control loop to remove. Fig. 2 illustrates the problem. The switching period T is:

$T = t_1 + t_2 + DT$

t_1 is the time Q1 is commanded on, t_2 is the time Q2 is commanded on, and DT is the deadtime. Assuming continuous condition, and with current in the direction of I_{L1}:

$t_{hi} = t_1 + DT$
$t_{lo} = t_2$

With current in the direction of I_{L2}:

$t_{hi} = t_1 + DT$
$t_{lo} = t_2 + DT.$

The change in "apparent duty cycle" is then twice the deadtime (2DT). If deadtime is 5% of the cycle period, the duty cycle, as load current crosses zero, instantly changes by 10 %. This is a significant nonlinearity that causes zero crossing distortions in load current and voltage that must be removed by the feedback loop around the PWM stage. If these nonlinearities get large enough, the loop may not have the gain or the speed to remove them. This may cause problems in the behavior of the end product that are unacceptable. Zero crossing distortion in the current of a microstepped step motor, for example, causes very serious position errors, velocity ripple, and audible noise in operation - all undesirable.

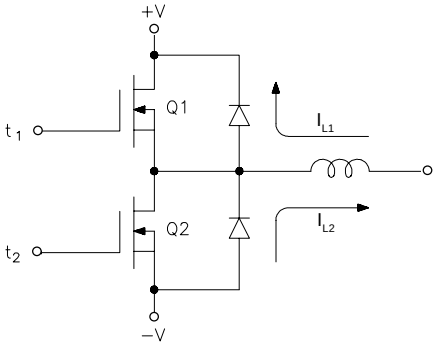


Fig. 2: Problems caused by excessive deadtime.

Calculating Appropriate Deadtime Values

The designer must determine, under worst case conditions, the absolute maximum delay between the logic off command and the actual cessation of transistor conduction. This includes all appropriate stages of logic, transistor storage and delay times, etc. It is very important to include special effects due to the switch technology chosen. Storage time of a bipolar transistor with constant base drive can vary 10:1 as collector current varies (storage time increases dramatically at low collector current, such as at light load). These effects must be considered when determining "worst case" delay time requirements. A power circuit must not only work at full rated load, but must not fail under light or no load conditions.

A delay of at least this time (plus a guardband) must be injected in the command to the series transistor so as to absolutely prohibit its turn-on during this interval.

Selecting Components for a Specific Requirement

Deadtime in the IXDP630/631 is exactly 8 clock periods: DT= 8/fclk. Once the worst case (minimum) deadtime has been determined (from Power switching component manufacturer data sheets, drive circuit analysis, breadboard measurements, etc.) the clock frequency is calculated: fclk(max) = 8/ DT(min).

This is the highest allowable clock frequency, including the effects of initial accuracy, tolerance, temperature coefficient, etc. When choosing oscillator components, special attention to resistor and capacitor construction is mandatory.

Oscillator Design

There are two versions of the deadtime generator. They have distinctly different internal oscillator designs to serve different application. In either case, however, the internal oscillator can be disabled by simply leaving its external components off. An HCMOS compatible clock up to 24 MHz can be fed directly into the RCIN or XTLIN pin.

IXDP630 RC Oscillator Design

The IXDP630 uses a Schmitt trigger inverter oscillator (Fig. 3). Two external components, R_{OSC} and C_{OSC}, determine the clock frequency and consequently the deadtime. This design allows a significant cost reduction over a standard crystal oscillator, but entails a trade-off in frequency accuracy. The initial accuracy and drift are a function of the external component tolerance and temperature coefficients, supply voltage, and IXDP630 internal parameters. At frequencies under 1 MHz, assuming the external components were perfect, the IXDP630 would introduce an initial accuracy error of 5 %, and a temperature dependence of -400 ppm. The shift in frequency over the V_{CC} range 4.5 V to 5.5 V is typically less than 5 %.

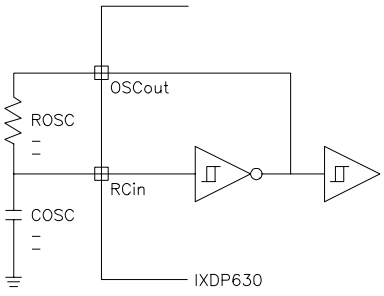


Fig. 3: IXDP630 internal Schmitt Trigger inverter oscillator (R_{OSC}, C_{OSC} are external)

At higher frequencies and with resistor values below 1 kΩ, the IXDP630 internal parameters become more influential factors. This results in greater frequency variation from one device to another, as well as with temperature and supply voltage variations. If high accuracy is a requirement, the IXDP631 with a crystal oscillator would be the better choice.

Oscillator frequency vs. Rosc and Cosc is shown in Fig. 4. For an analytical method of setting the oscillator, the design equation is for operation below 1 MHz approximately:

$$f_{OSC} \approx \frac{0.95}{Cosc\ Rosc}$$

For operation above 1 MHz,

$$f_{OSC} \approx \frac{0.95}{Cosc\ (Rosc+30) + 3 \bullet 10^{-8}}$$

IXDP631 Precision Crystal Oscillator Design

The IXDP631 uses a more common standard internal crystal oscillator design. For proper operation the crystal must be of the parallel resonant type, resonating at the crystal's fundamental frequency. Fig. 5 illustrates the recommended oscillator configuration. Note the external components required. The capacitors are needed to achieve the calibrated crystal frequency (their value is determined by the crystal manufacturer), and the resistor is necessary to assure that the circuit starts in every case. While the circuit will **usually** operate without these extra parts, this is not recommended.

The crystal oscillator in the IXDP631 is significantly more accurate than the RC oscillator in the IXDP630. The total tolerance (including effects of initial accuracy, temperature, supply voltage, drift, etc.) is better than ±100 ppm. This improves the accuracy and repeatability of the desired deadtime, but at the added expense of a crystal.

Which version is appropriate for your application? That depends on how you are willing to trade off component cost for deadtime accuracy.

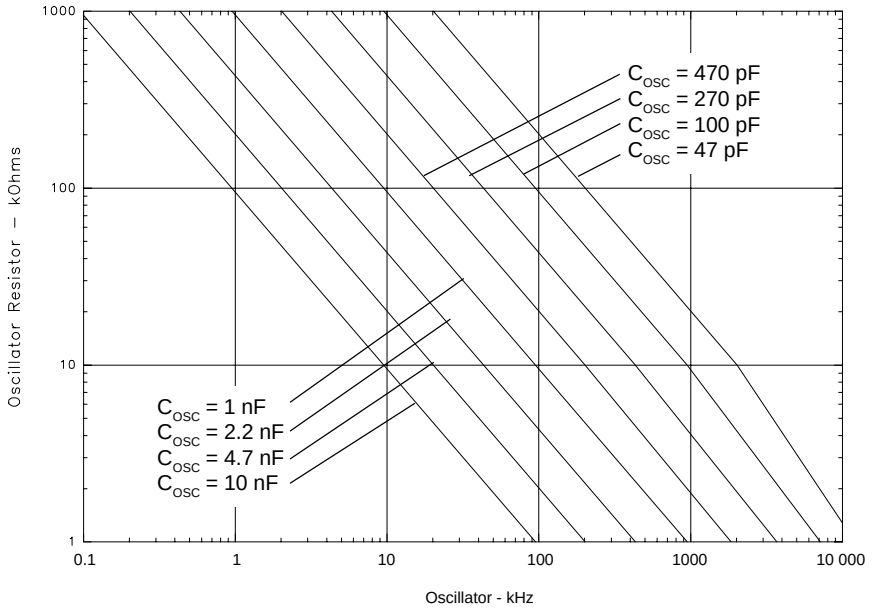


Fig. 4. Oscillator frequency component selection for IXDP630.

IXDP630 RC Oscillator Component Details

The IXDP630 oscillator has only two external components. Rosc should be a precision, high frequency resistor. The material used in carbon composition resistors is hydroscopic (it absorbs water), causing resistors above 100 kΩ to 1 MΩ to change value with relative humidity. This is on top of initial tolerance and temperature coefficient deviations, and so is not recommended. Instead, precision metal film or carbon film resistor construction is preferred, with initial tolerances of 1 % and better with temperature coefficients of ±100 ppm.

The construction of Cosc is also critical to circuit operation. Cosc should be a good quality monolithic ceramic (single or multilayer) or a metallized polypropylene timing capacitor. If ceramic technology is chosen, be sure to consider temperature coefficient and tolerance. It is the minimum capacitor value that is critical, not the part number rated capacitance. A Z5U ceramic has an initial tolerance of +80/-20 %, and a temperature variation of +30/-80 % over temperature. An X7R is ±10 % initial tolerance, ±10 % over temperature. An NPO is ±5 % initial tolerance, ±5 % over temperature (although tighter selections are readily available in NPO).

If film technology is chosen, polypropylene is one of the best choices. Tolerances down to 1 % and 2 % are standard and temperature coefficient is ±100 ppm.

The layout of the external components is also critical. The components should be as close to the device as possible, minimizing stray capacitance and inductance.

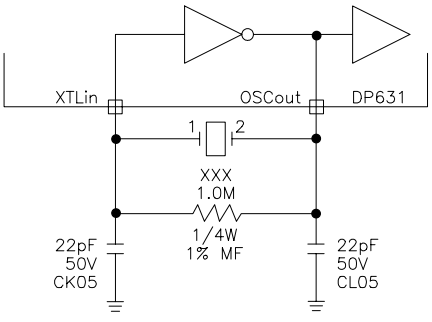


Fig. 5. Recommended Crystal Oscillator Components

IXDP631 Crystal Oscillator Component Details

The IXDP631 oscillator requires three external passive components, in addition to the crystal. The crystal is chosen with a frequency below fclk (min). The capacitors and resistor (illustrated earlier in Fig. 5) follow rules similar to the RC oscillator option. The resistor should be metal or carbon film, although its accuracy and stability do not significantly affect oscillator frequency accuracy. The capacitors should be monolithic ceramic construction (CK05, or similar) with X7R or better characteristics.

Grounding, Interfacing and Noise Immunity

Due to the very high level of currents that are switched at high speed in a typical motor control power circuit, voltage transients (V = L • di/dt) can cause serious problems. Fast digital circuits respond to transients instead of legitimate inputs, disturbing inverter operation or causing outright failure.

Bypassing and Decoupling

As with any high speed logic component, the IXDP630/631 should be bypassed with a good quality (monolithic ceramic or film) capacitor designed specifically for bypass application. Decoupling is normally not required. The IXDP630 does not generate sufficient supply line current ripple to be a significant noise source when properly bypassed, and it is capable of rejecting normal supply line noise.

Logic Levels

All inputs to the IXDP630 and IXDP631 (except XTLIN on the IXDP631) are HCMOS Schmitt Trigger compatible. On the IXDP631, the XTLIN pin is different because the crystal oscillator circuit cannot tolerate a Schmitt input. The hysteresis inherent in Schmitt Trigger inputs greatly improves the reliability of digital communications. It can reject ground bounce of up to 2 V, and induced voltages in digital signal traces of 1 V.

Power Circuit Noise Generation

In a typical transistor inverter, the output MOSFET may switch on or off with di/dt ≥ 500A/µs. Referring to Fig. 6, and assuming that the MOSFET Source Terminal has a 1 inch path on the PCB to system ground, a voltage as high as 13.5 V can be developed:

V = 27 nH • 500A/µs = 13.5 V

If the MOSFET switches 25 A, the transient will last as long as (25/500) µs or 50 ns, which is much more than the typical 6 or 7 ns propagation delay of a 74 HC series gate.

Caution: *If one set of digital circuits is tied to system ground, and one to local ground, it is clear that such a transient would cause spurious outputs. In an inverter, the consequences of such an error could be catastrophic. Turning a transistor on at the wrong time could easily cause it to explode, with the potential for equipment damage and operator injury -- clearly undesirable.*

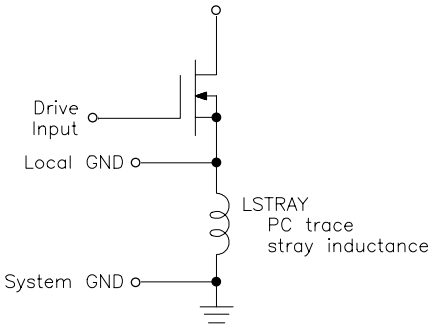


Fig. 6. Power circuit noise generation

Methods of Correcting these Problems

The first step is to use a logic family with inherent noise immunity. Standard TTL (or any of its derivatives, including 74HCT CMOS) is a poor choice because of the logic levels these families employ. In particular, V_{OL}, V_{IL} are too close to ground to reject the levels of ground noise common to power circuits. 74HC logic is significantly superior, and the older 4000 series CMOS is even better. Unfortunately, in modern motor controls, especially those that employ microprocessors, the speeds of the 4000 series CMOS are no longer adequate. In most cases 74HC logic is the only viable alternative.

Layout

The second, and most important step is the printed circuit board (PCB) layout. The PCB is a very important component in any power circuit, and there is a

tendency to leave it off the schematic. During the layout process, the engineer must consider each and every connection from the standpoint of its contribution to system operation. How sensitive is it? What noise producing lines are routed near it? What transients can occur between circuits tied to each end of this trace...? With few exceptions, modern autorouters cannot deal with these requirements. If autorouters are used, they produce layouts that will not function.

Remember that the IXDP630/631 is the interface between the control circuits and the power circuits. Nowhere else on the PCB are these problems more likely to occur. Nowhere else will one need to pay more attention. Fig. 7 illustrates an example layout problem. The power circuit consists of three

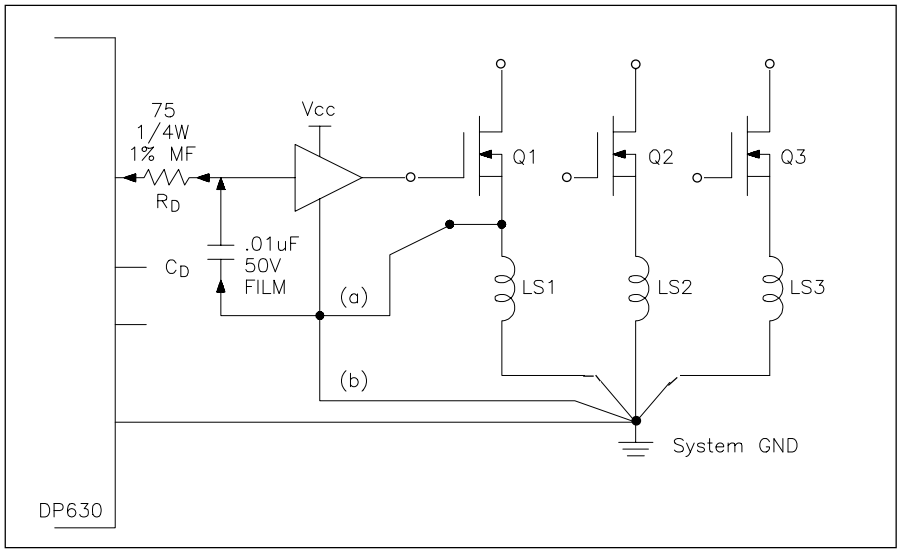


Fig. 7. Potential layout problems that create functional problems.

power transistors (MOSFETs in this example) controlled by a common digital IC (the IXDP630). With the gate drive amplifier (a discrete circuit or possibly an IC driver like the IXBD4410) grounded as in option (b), the communication path from the IXDP630 will operate without errors. The PC trace induced voltages are not common with the digital path so the input of the gate drive buffer will not see or respond to them. Unfortunately, the MOSFET will not operate properly. The voltage induced across L_{S1} when Q1 is turned on, acts as source degeneration, modifying the turn-on behavior of the MOSFET. If L_{S1} = 27 nH, and V_{CC} is 12 V (assuming the gate plateau of the MOSFET is 6 V), the di/dt at turn-on will be regulated by the driver/MOSFET/L_{S1} loop to about 200 A/µs - quite a surprise when your circuit requires 500 A/µs to operate correctly.

It is possible to make use of this behavior to create a turn-on or turn-off di/dt limiter (perhaps to snub the upper freewheeling diode reverse recovery). While possible, this is normally not desirable or practical where two or more transistors are controlled. Equalizing the parasitic impedances of three traces while positioning the transistors next to their heat sink and meeting UL/VDE voltage spacings is just too difficult.

Grounding the gate drive buffer as in option (a) solves the MOSFET turn on problem by eliminating L_{S1} from the Source feedback loop. Now, unfortunately, the gate driver will oscillate every time you turn it on or off. As the IXDP630 output goes high, the gate driver output follows (after its propagation delay) and the MOSFET starts to conduct. The voltage transient induced across L_{S1} (V = Ls1/di/dt) raises the local ground (point a) until it exceeds V_{oh} (630)-V_{il} (gate buffer) and the buffer (after its prop. delay) turns the MOSFET off. Now the MOSFET current falls, V(Ls1) drops, point (a) drops to (or slightly below) system ground, and the buffer detects a "1" at its input. After its propagation delay, it again turns the MOSFET on, continuing the oscillation for one more cycle.

To eliminate this problem, a ground level transformation circuit must be added that rejects this common mode transient. The simplest is a decoupling circuit, also illustrated in Fig. 7. The capacitor voltage (on C_d) remains constant while the transient voltage is dropped across R_d and the buffer detects no input transition, eliminating the oscillation. This circuit does add significantly to turn-on and turn-off delay time, and cannot be used if the transient lasts as long as these delays are allowed to extend. Delay times must be considered in selection of system deadtime.

It is also important to consider the layout of the bypass capacitor as well as the oscillator components in order to keep these as close to the device as possible.

Isolation

The most complex (and most effective) method of eliminating the effects of transients between grounds is isolation. Optocouplers and pulse transformers are the most commonly used isolation techniques, and work very well in this case. The IXDP630/631 has been specifically designed to directly drive a high speed optocoupler like the Hewlett Packard HCPL22XX family or the General Instrument 740L60XX optologic family. These optos are especially well suited to motor control and power conversion equipment due to their very high common-mode dv/dt rejection capabilities.

The major problem associated with using an optocoupler in a power circuit is its common-mode dv/dt capability. When a lower transistor is turned on, its Collector (or Drain) is pulled to ground very quickly. The optocoupler that drives the upper transistor has its local output stage referenced to the Emitter (Source) of this upper device, which is tied to the Collector of the lower device. As this node moves, the dv/dt between here and input circuit common is impressed across the upper optocoupler. This causes displacement currents to flow in sensitive nodes in the optical receiver circuitry, and may cause false triggering of the output. Always pay strict attention to the manufacturer's recommended dv/dt ratings - exceeding them could be disastrous.

High Voltage Current Regulators

Current Regulator	BV_{DS} min. V	$I_{D(P)}$ typ. mA	TO-220 AB	TO-251 AA	TO-252 AA
Non switchable regulators	350	10 20 35	**IXCP 10M35** **IXCP 20M35** **IXCP 35M35**	**IXCU 10M35** **IXCU 20M35** **IXCU 35M35**	**IXCY 10M35** **IXCY 20M35** **IXCY 35M35**
Switchable regulators	350	10	**IXCP 10M35S**	**IXCU 10M35S**	**IXCY 10M35S**
	450	10	**IXCP 10M45S**	**IXCU 10M45S**	**IXCY 10M45S**

Pin connections
1 = No Connection or CTL (Control for switchable regulator)
2 = 4 = (+) Pos. Term., 3 = (-) Neg. Term.

Features
- Extremely stable current characteristics 50 ppm/K
- Minimum of 350/450 V breakdown
- Easily configured for bi-directional current sourcing
- 40 W continuous dissipation
- International standard packages JEDEC TO-220, TO-251 and TO-252
- On/Off switchable current source

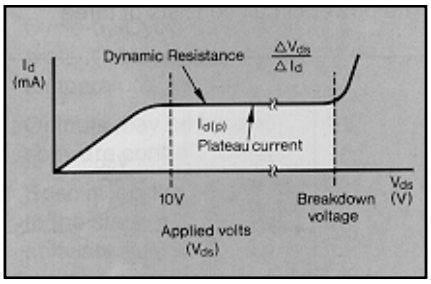


Fig. 3 Current regulator characteristics

Applications
- Start-up circuits for SMPS
- PABX current sources
- Telephone line terminations in PABXs and modems
- Highly stable voltage sources
- Surge limiters and protection (DC and AC)
- Instantaneously reacting indestructible fuses
- Waveform synthesizes
- Soft start-up circuits

Non switchable regulators

This is a family of extremely stable, high voltage current regulators. The temperature stability is based on a threshold compensation technique and uses IXYS' most recently developed high voltage process. The complete family will be capable of providing other intermediate current levels which can be programmed on-chip during the manufacturing phase.

Specific applications are current sourcing in PABX applications, telephone line terminations, surge protection and voltage supply protection. Two devices in a back-to-back configuration will give bi-directional operation. Specific bi-directional applications would be series surge protection and soft start-up applications from AC mains.

Switchable regulators

The IXYS Switchable Current Regulator with its 350/450 V minimum breakdown capability, is intended as a current source for off-line applications, such as switched mode power supply start-up circuits, where shutting the regulator down on demand is required to reduce standby power consumption. For additional design flexibility, the regulated current level can be reduced to values below nominal by adding a single resistor in series with the negative terminal.

Nomenclature of Current Regulators

IXCU 10M45S (Example)

IX	IXYS
C	Current Regulator
	Package style
P	TO-220 AB
U	TO-251 AA
Y	TO-252 (D-PAK)
10	Current Rating, 10 = 10 mA
M	Current Level A = Amps, M = mA, U = µA
45	Voltage rating, 45 = 450 V
S	Switchable regulator

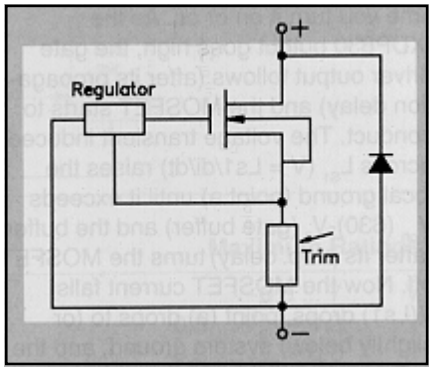


Fig. 1 Block diagram of non switchable regulator

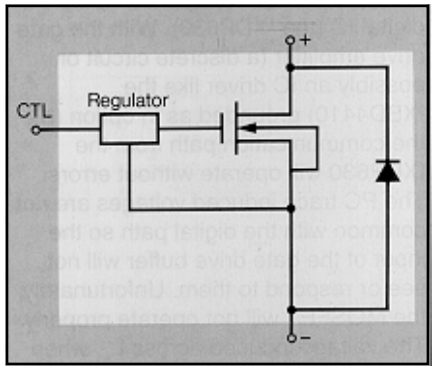


Fig. 2 Block diagram of switchable regulator

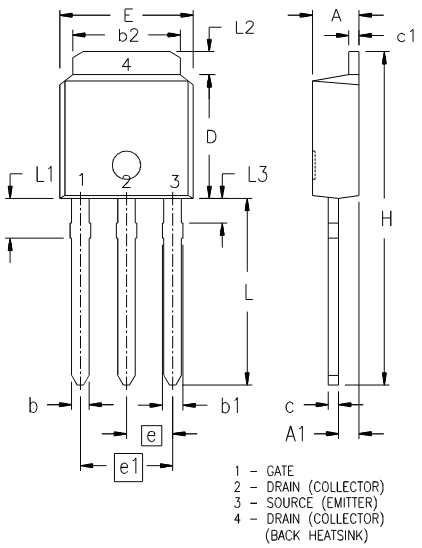
Non Switchable Current Regulators

Symbol	Definition	Maximum Ratings	
V_{DS}	Drain Source Voltage	+350	V
P_D	Power Dissipation (T_C = 25°C)	40	W
I_{RM}	Maximum Reverse Current	1	A
T_J	Junction Operating Temperature	-55 to +150	°C
T_{stg}	Storage Temperature	-55 to +150	°C
T_L	Temperature for soldering (max. 10 s)	260	°C
M_D	Mounting torque with screw M3 (TO-220)	0.45/4	Nm/lb.in.
	with screw M3.5 (TO-220)	0.55/5	Nm/lb.in.

Symbol	Definition/Condition			Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
BV_{DS}	Breakdown voltage at operating current level	10M35 20M35 35M35	I_D = 20mA* I_D = 35mA* I_D = 50mA*	350			V
$I_{D(P)}$	Plateau Current	10M35 20M35 35M35	V_{DS} = 10 V	7 15 29	10 20 35	13 25 41	mA mA mA
$\Delta I_{D(P)}/\Delta T$	Plateau Current Shift with Temperature		V_{DS} = 10 V		50		ppm/K
$\Delta V_{DS}/\Delta I_{D(p)}$	Dynamic Resistance	10M35 20M35 35M35	V_{DS} = 10 V	20 10 6			kΩ kΩ kΩ
R_{thJC}	Thermal Resistance junction-to-case					3.1	K/W
R_{thJA}	Thermal Resistance junction-to-ambient,					80	K/W
						100	K/W

* Pulse test to limit power dissipation to within device capability.

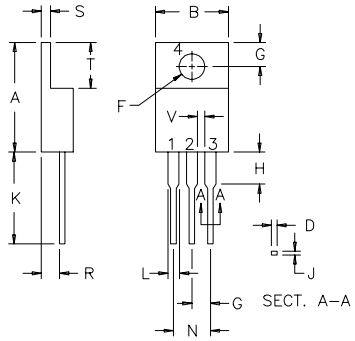
TO-251 AA



SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.086	.094	2.19	2.38
A1	.035	.045	0.89	1.14
b	.025	.035	0.64	0.89
b1	.030	.045	0.76	1.14
b2	.205	.215	5.21	5.46
c	.018	.023	0.46	0.58
c1	.018	.023	0.46	0.58
D	.235	.245	5.97	6.22
E	.250	.265	6.35	6.73
e	.090 BSC		2.28 BSC	
e1	.180 BSC		4.57 BSC	
H	.670	.700	17.02	17.78
L	.350	.380	8.89	9.65
L1	.075	.090	1.91	2.28
L2	.035	.050	0.89	1.27
L3	.045	.060	1.15	1.52

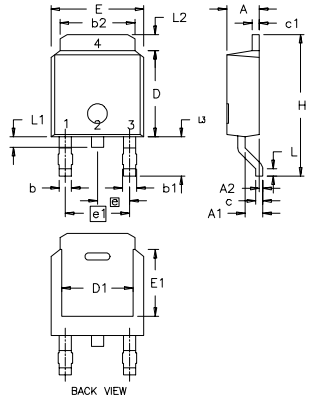
Notes:
1. This drawing meets all dimensions requirement of JEDEC outlines TO-251AA.
2. All metal surface are solder plated except trimmed area.

TO-220 AB



Dim.	Millimeter Min.	Millimeter Max.	Inches Min.	Inches Max.
A	14.23	16.51	.560	.650
B	9.66	10.66	.380	.420
C	3.56	4.82	.140	.190
D	0.64	0.89	.025	.035
F	3.54	4.06	.139	.161
G	2.29	2.79	.090	.110
H	–	6.35	–	.250
J	0.51	0.76	.020	.030
K	12.70	14.73	.500	.580
L	1.15	1.77	.045	.070
N	4.83	5.33	.190	.210
Q	2.54	3.42	.100	.135
R	2.04	2.49	.080	.115
S	0.64	1.39	.025	.055
T	5.85	6.85	2.30	2.70
V	1.15	–	.045	–

TO-252 AA (D-PAK)



Dim.	Millimeter Min.	Millimeter Max.	Inches Min.	Inches Max.
A	2.19	2.38	0.086	0.094
A1	0.89	1.14	0.035	0.045
A2	0	0.13	0	0.005
b	0.64	0.89	0.025	0.035
b1	0.76	1.14	0.030	0.045
b2	5.21	5.46	0.205	0.215
c	0.46	0.58	0.018	0.023
c1	0.46	0.58	0.018	0.023
D	5.97	6.22	0.235	0.245
D1	4.32	5.21	0.170	0.205
E	6.35	6.73	0.250	0.265
E1	4.32	5.21	0.170	0.205
e	2.28 BSC		0.090 BSC	
e1	4.57 BSC		0.180 BSC	
H	9.40	10.42	0.370	0.410
L	0.51	1.02	0.020	0.040
L1	0.64	1.02	0.025	0.040
L2	0.89	1.27	0.035	0.050
L3	2.54	2.92	0.100	0.115

Switchable Current Regulators

Symbol	Test Condition		Maximum Ratings	
V_{AKR}	T_J = 25°C to 150°C	10M35S	350	V
		10M45S	450	V
V_{AGR}	T_J = 25°C to 150°C	10M35S	350	V
V_{AGR}		10M45S	450	V
V_{GK}			±20	V
I_D	T_C = 25°C		-0.3	A
P_D	T_C = 25°C		40	W
T_J			-55 ... +150	°C
T_{stg}			-55 ... +150	°C
T_L	Temperature for Soldering (max. 10 s)		260	°C
M_D	Mounting torque with screw M3 (TO-220)		0.45/4	Nm/lb.in.
	with screw M3.5 (TO-220)		0.55/5	Nm/lb.in.

Symbol	Test Condition		Characteristic Values (T_J = 25°C unless otherwise specified) min.	typ.	max.	
V_{AKR}	R_K = 300 Ω, (Fig. 4)	10M35S	350			V
		10M45S	450			V
$I_{D(P)}$	V_D = 10 V; R_K = 300 Ω; (Fig. 5)		7	10	15	mA
$V_{G(off)}$	I_D = 100 µA; V_D = 300 V	10M35S	-5			V
	I_D = 100 µA; V_D = 400 V	10M45S	-5			V
	Fig. 4					
I_{DV}	V_D= 300 V; V_{GK} = -10 V	10M35S			25	µA
	V_D= 400 V; V_{GK} = -10 V	10M45S			25	µA
	Fig. 4					
dv/di	Dynamic resistance; V_D= 10 V		10			kΩ
	R_K = 300 Ω; (Fig. 4)					
R_{thJC}	Thermal Resistance junction-to-case				3.1	K/W
R_{thJA}	Thermal Resistance junction-to-ambient,	TO-220			80	K/W
		TO-252			100	K/W

Pin connections

1 = G, Control terminal
2 = 4 = A (+), Positive terminal
3 = K (-), Negative terminal

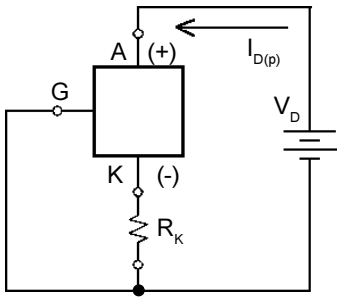


Fig. 4 Resistor "R_K" in series with negative pin to achieve different current levels

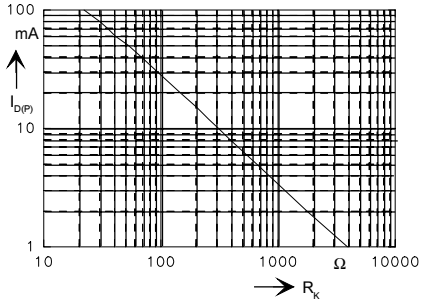


Fig. 5 Plateau current versus external resistance

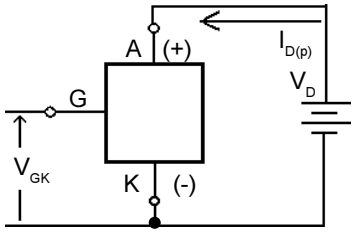


Fig. 6 Current regulator controlled by V_G

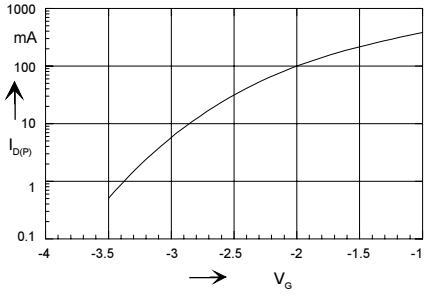


Fig. 7 Plateau current versus applied input voltage

Application examples with switchable regulator

Start-up Circuit

An often overlooked area in switch mode power supply (SMPS) designs is the start-up circuit (or housekeeping supply). A good start-up circuit should be inexpensive, require little space, be non-complex and should not lower the overall efficiency of the power supply. To maximize efficiency, it should switch off when the supply is in operation.

Fig. 8a shows a simple start-up circuit for a universal 96 to 264 V~ SMPS. Here R1, a 15 W/11 kΩ dropping resistor, provides the initial 10 mA or greater supply current required by the SMPS control IC. This circuit will consume up to 12.4 W of additional power, all of which must be dissipated and which reduces the overall SMPS design efficiency. Depending on the application, additional air space should be provided to adequately cool R1 and avoid damaging heat sensitive components.

Fig. 8b shows an SMPS start-up circuit using I1, the IXCP 10M45S switchable current regulator and M1, a 2N7000P MOSFET, to switch I1 on and off. Only during the first 10 ms to 20 ms of SMPS start-up does I1 need to be on to supply up to 10 mA, which is set by R1 = 300 Ω. It is commanded off during all other times. The additional average power dissipation due to this start-up circuit during normal operation, ie after M1 has turned I1 off, is proportional to the square of the voltage across R2.

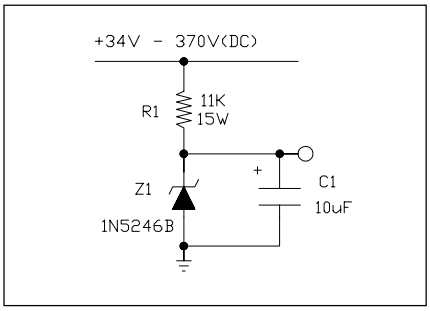


Fig. 8a Standard start-up circuit for SMPS

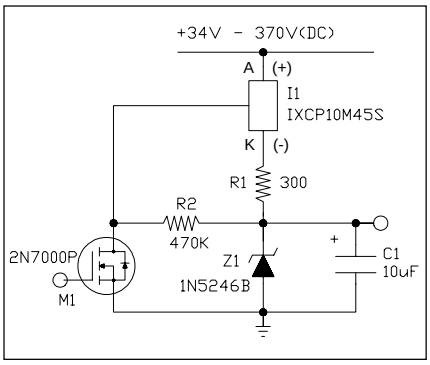


Fig. 8b SMPS start-up circuit using IXCP 10M45S

This approximately 0.5 mW, assuming V = 16 V and R2 = 470 kΩ. As such, minimal heat build-up will occur in the IXCP 10M45S, eliminating potential problems to heat sensitive components.

Any reduction in power dissipation in the start-up circuit translates directly into improved SMPS efficiency. Even though there may be more components required in Fig. 8b versus Fig. 8a, the absence of a heat generating component will serve to increase overall packing density and improve PCB layout flexibility.

Simple Off Line Power Supply with the IXCP 10M45S

In Fig. 9, the IXCP 10M45S, IC1, extends the input voltage range of a 5 V linear voltage regulator IC2, a 78L05 for example, to allow it to work off of 110 to 230 V~ mains. In fact, any three terminal linear regulator rated less than 50 mA (100 mA off 110 V mains) from 5 V to 22 V will work in this application. Assume that the rectified voltage across C2 is sufficiently positive to allow the output of 78L05 to supply I_L to the load with a regulated 5 V. Under steady state conditions the current output of IC1 (-) just matches the current input of IC2 (IN) with no current flow into or out of C2. Assume the current demanded by the load is such that I_L goes down. This will cause IC2 (IN) current to also go down resulting in excess current output from IC1 (-). This excess current will charge C2, resulting in IC1 (-) terminal voltage becoming more positive, which then reduces the IC1 output current until it matches the IC2 (IN) input current. If the current demanded by the load goes up increasing I_L, the IC2 (IN) input current will also go up. C2 will initially source the additional current by discharging itself. The reduction in C2 voltage causes IC1 (-) terminal to become more negative with respect to IC1 and results in IC1 output current increase. In steady state, IC1 will provide exactly the current required by IC2 - no more and no less. Note that IC1 must be heat sink since its average power dissipation is approximately peak input mains voltage multiplied by the output regulator current.

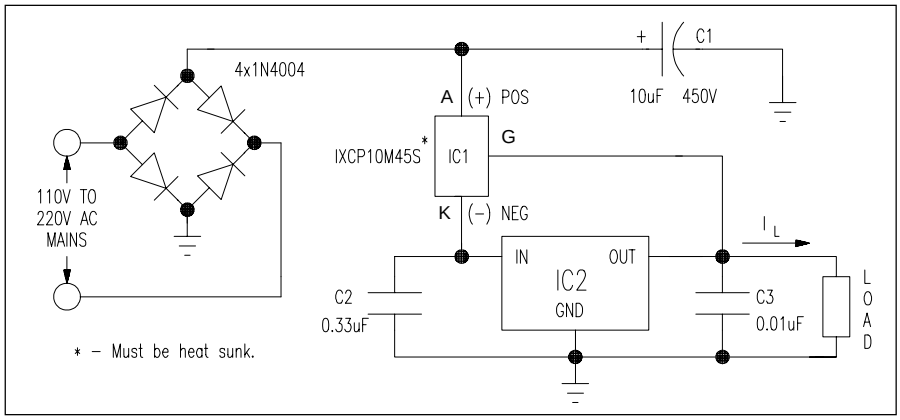


Fig. 9 Use of IXCP 10M45A to extend input voltage range to low voltage current regulators

Other Application

Current Regulator as a Current Source in PABXs

Telephone instruments need to take power from the telephone line when they are taken "off" hook; i.e., when the telephone is physically lifted by the user. The power is sourced for the PABX end, and in most cases, this is achieved by applying a differential DC voltage to the telephone lines via substantially sized inductors.

These inductors provide a very low resistance to the DC applied voltage while simultaneously presenting a high impedance to audio signals appearing on the line and ensuring that the signal is not routed to the voltage source under operating line conditions.

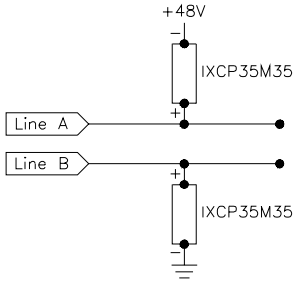


Fig. 10 Using two matched IXCP35M35 current regulators as current sources.

In addition to the inductor, some other components are generally necessary.

For example the IXCP35M35 current regulator could provide a cost-effective equivalent function in a single package. The IXCP35M35 has a 35 mA nominal value and is capable of acting as a constant current source for the line. It has a high dynamic impedance to AC signals under normal conditions when the DC operating voltage across it is greater than several volts. Although this device operates at a 35 mA nominal current, other current levels could be supplied to the end user.

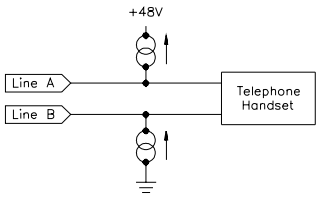


Fig. 11 PABX current sourcing with two current sources for longitudinal balance

Two current sources are needed, one in the "A" line and one in the "B" line. Their characteristics must have a high degree of matching. This provides the longitudinal balance that is needed. Longitudinal imbalance between the two lines will mean that there is likely to be unwanted pickup across the phone terminals. The circuit of Fig. 11 shows the two current sources in a PABX line. Applied voltage is around -48 V.

As well as longitudinal balance, each source must present a certain impedance value to AC speech signals on each line. The use of two current sources would provide an attractive cost-effective solution to PABX current

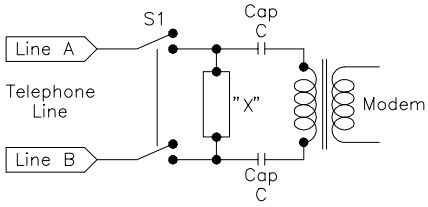


Fig. 12 Modem link-telephone line "X" is the line termination

sourcing applications (Fig. 11). The devices have a 350 V breakdown capability and can be utilized with voltage supplies substantially greater than -48 V, if required.

The 350 V capability also allows an extension of this current source approach to embrace other specific functions in a PABX system.

The important aspect of the current sources in the A and B lines is that the degree of matching should be high. The design of the current regulator embraces these features.

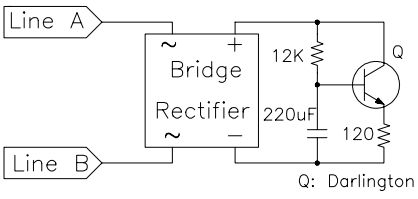


Fig. 13 Example of line terminating circuit

Devices can be matched to 0.1 mA at the operating voltage level by a combination of on-chip trimming at the pre-assembly stage or by a binning procedure during electrical test.

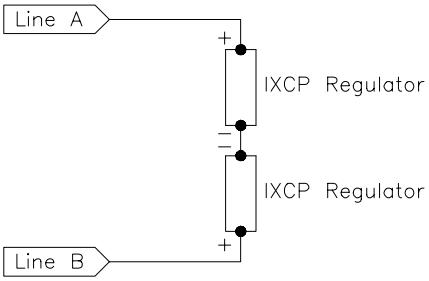


Fig. 14 Two current Regulators placed back-to-back

Telephone Line Termination

Fig. 12 shows a simple schematic of a modem interface in a telephone line at the subscriber end. Block "X" consists of a circuit which provides the end of line termination characteristics that are required.

Different countries may require different characteristics. The termination must provide specific DC characteristics as well as provide the dynamic impedance necessary between the A and B lines.

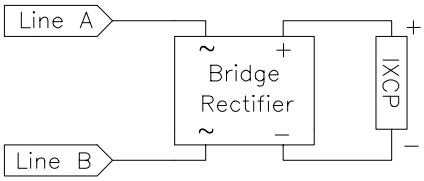


Fig. 15 Bi-directional Regulator (one package)

To input information into the line, switch SI will have to close. This initially means that ringing voltage will be imposed across the termination "X". Therefore, it not only has to provide the terminating characteristics under normal data transmission but has to be capable of withstanding the initially applied differential ringing voltage of the line when the switch SI is closed.

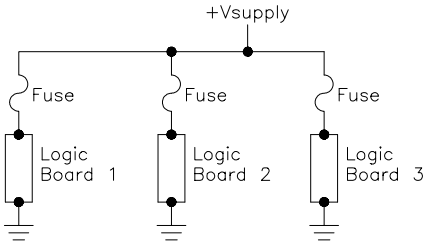


Fig. 16 Normal fusing links in series with each board

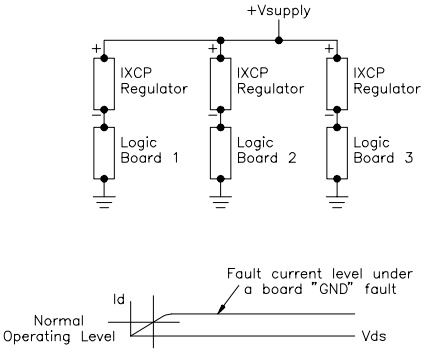


Fig.17 Low cost current regulators instead of fuses

The differential line voltage can be either polarity, therefore "X" also needs to cater for this potential bi-directionally.

An existing solution is illustrated in Fig. 13, an end-of-line termination in some countries. Fig. 14 and 15 show alternate solutions using the IXCP regulators.

Instantaneous "Fuse"

Another application would be protection against sudden voltage "droops" on voltage supply lines to logic cards in computing systems, resulting from one component suddenly shorting to ground. Normal fusing networks will draw considerable current during the time it takes for the fuse to clear. This could cause a sufficient dip in power rail voltage to cause malfunctions of the other logic cards, even with fast-blow fuses (Fig. 16). The current regulator in series with the logic card restricts the current to its own operating level (Fig. 17). Therefore the voltage supply does not become overloaded and the regulator remains intact.

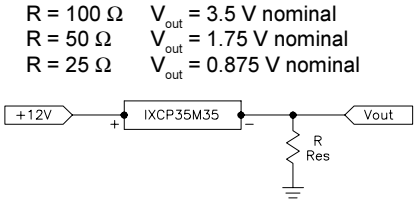


Fig. 18 Simple voltage source with high stability

The current regulator thus provides an "instantaneous fusing" function. When the logic component is replaced, the regulator to normal functioning mode.

The obvious advantages to having this regulator as fuse substitute are:

- Prevents a "dip" in the power supply during a fault condition
- Regulator remains intact
- Can be easily tied in with logic to indicate a "down state" board

Highly Stable Voltage Sources

An obvious application would be to use the current regulator as a source of a highly stable current to produce a stable voltage reference (Fig. 18). This would be effectively independent of temperature and a low cost approach. A high voltage reference is also possible, thanks to their high breakdown voltages.

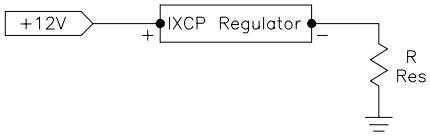


Fig. 19 DC surge suppression

DC and AC Overvoltage Suppression

The regulator can be used as a voltage surge suppressor. The device is again connected in series with the lead (Fig. 19) and would normally operate at a current level lower than the plateau (Fig. 20A). Any incoming voltage surge (Fig. 20b) less than the breakdown voltage of the regulator will be clamped by the IXCP regulator to voltage less than the plateau current times the effective resistance of the load.

Waveform Pattern Generation

Using a pair of matched current regulators, very linear and symmetrical waveforms can be generated. The temperature-stable characteristics of

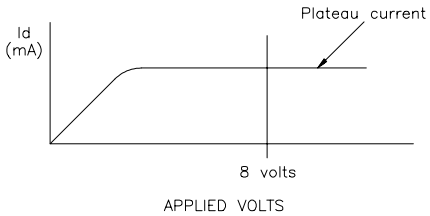


Fig. 20A DC surge suppression

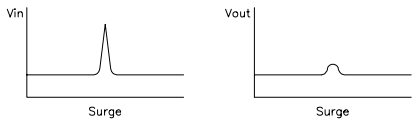


Fig. 20B Incoming surge/output surge across load

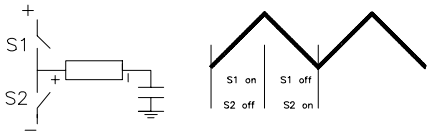


Fig. 21 Use of IXCP current regulators to generate linear waveforms.

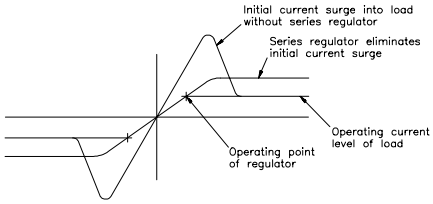


Fig. 22 Soft start on AC mains using a regulator in series with a load.

the current regulator provide a high degree of linearity and repeatability. Basically the circuit consists simply of one current regulator, two switches, and one capacitor (Fig. 21).
Switch S2 would be on the ground side and would operate from low voltage logic. Switch S1 would be driven from an isolated driver. With matched regulators, the upward and downward slopes match any requirement as dictated by the control logic timing.

Soft Start-Up Circuits

Here the regulator characteristic will clamp initial current surges which can occur when power is initially applied to a load. The device, with its 350 V capability could, for example, be used with a DC power supply or with AC mains to limit the initial high in-rush of current into lamp filaments, thereby increasing the filament life several times. It could, therefore, be used effectively in the lighting display and transportation lighting industries.

Testing & Handling Recommendations

- For initial assessment of the parts where the customer may test the device characteristics in free air without heat sinking, the continuous power dissipation should be kept within 1.5 W at ambient of 25°C. (R_{thJA} = 80 K/W for TO-220, and R_{thJA} = 100 K/W for TO-252))
- Normal electrostatic handling precautions for MOS devices should be adhered to.

Bus Compatible Digital PWM Controller, IXDP 610

Description

The IXDP610 Digital Pulse Width Modulator (DPWM) is a programmable CMOS LSI device which accepts digital pulse width data from a microprocessor and generates two complementary, non-overlapping, pulse width modulated signals for direct digital control of switching power bridge. The DPWM is designed to be operated under the direct control of a microprocessor and interfaces easily with most standard microprocessor and microcomputer buses. The IXDP610 is packaged in an 18-Pin slim DP.

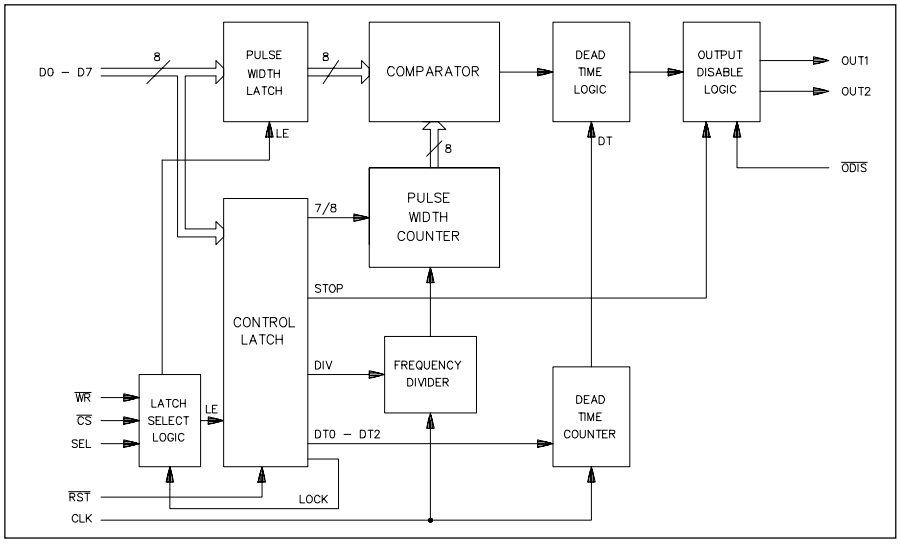
The PWM waveform generated by the IXDP610 results from comparing the output of the Pulse Width counter to the number stored in the Pulse Width Latch (see below). A programmable "dead-time" is incorporated into the PWM waveform. The Dead-Time Logic disables both outputs on each transition of the Comparator output for the required dead-time interval.

The output stage provides complementary PWM output signals capable of sinking and sourcing 20 mA at TTL voltage levels. The Output Disable logic can be activated either by software or hardware. This facilitates cycle-by-cycle current-limit, short-circuit, over-temperature, and desaturation protection schemes.

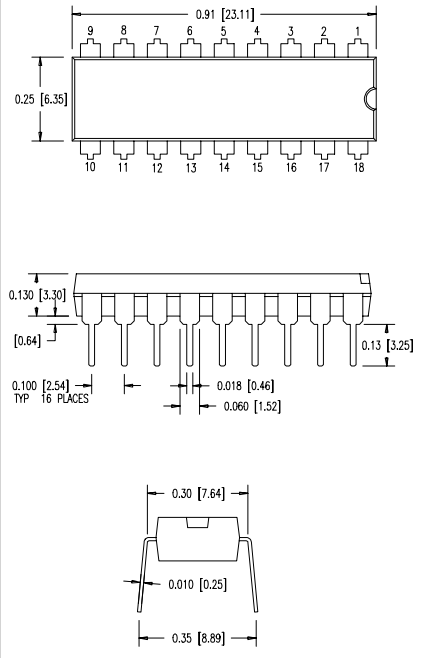
The IXDP610 is capable of operating at PWM frequencies from zero to 300kHz; the dead-time is programmable from zero to 14 clock cycles (0 to 11 % of the PWM cycle), which allows operation with fast power MOSFETs, IGBTs, and bipolar power transistors. A trade-off between PWM frequency and resolution is provided by selecting the counter resolution to be 7-bit or 8-bit. The 20 mA output drive makes the IXDP610 capable of directly driving opto isolators and Smart Power devices. The fast response to pulse width commands is achieved by instantaneous change of the outputs to correspond to the new command. This eliminates the one-cycle delay usually associated with other digital PWM implementations.

Features

- Microcomputer bus compatible
- Two complementary outputs for direct control of a switching power bridge
- Dynamically programmable pulse width ranges from 0 to 100 %
- Two modes of operation: 7-bit or 8-bit resolution
- Switching frequency range up to 300 kHz
- Programmable Dead-time Counter prevents switching overlap
- Cycle-by-Cycle disable input to protect against over-current, over-temperature, etc.
- Outputs may be disabled under software control
- Special locking bit prevents damage to the stage in the event of a software failure
- 18-pin slim DIP package



Dimensions in inch and mm
18-Pin Slim DIP



Symbol	Definition		Maximum Ratings	
V_{CC}	Supply voltage		-0.3 ... 7	V
V_{IN}	Input voltage		-0.3 ... V_{CC} + 0.3	V
V_{out}	Output voltage		-0.3 ... V_{CC} + 0.3	V
P_D	Maximum power dissipation		500	mW
T_{stg}	Storage temperature range	Industrial	-40 ... 125	°C
		Military	-65 ... 150	°C

Symbol	Definition	Maximum Ratings Industrial min.	max.	Military min.	max.	
	Operating Range					
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
T_A	Operating free air temperature	-40	85	-55	+150	°C

Symbol	Definition/Condition		Characteristic Values (Over operating range, unless otherwise specified) min.	typ.	max.	
$V_{IH(CMOS)}$	Input High Voltage	$\overline{ODIS}$	3.8		V_{CC} +0.3	V
$V_{IL(CMOS)}$	Input Low Voltage	$\overline{ODIS}$	-0.3		1.2	V
V_H	Input Hysteresis	$\overline{ODIS}$	0.3	0.5		V
V_{OH}	Output High Voltage	OUT1 I_{OH} = -20 mA OUT2	2.4			V
V_{OL}	Output Low Voltage	OUT1 I_{OL} = 20 mA OUT2			0.4	V
$V_{IH(TTL)}$	Input High Voltage	All Inputs Except $\overline{ODIS}$	2.0		V_{CC} +0.3	V
$V_{IL(TTL)}$	Input Low Voltage	All Inputs Except $\overline{ODIS}$	-0.3		0.8	V
I_{LI}	Input Leakage Current	All Inputs $0 < V_I < V_{CC}$	-10	-0.1	10	µA
I_{CC}	Power Supply Current	f_{CLK} = 5 MHz $V_{IH} = V_{CC}$ or 0		3.5	10	mA

Symbol		Definition/Condition	Characteristic Values (T_A = 25°C, V_{CC} = 5 V ± 10 %, C1 = 50 pF)	Industrial -40...85°C		Military -55...125°C		
No. see Fig. 3-6			typ.	min.	max.	min.	max.	
1	t_{AVWL}	SEL Stable to $\overline{WR}$ Low		5		5		ns
2	t_{WHAX}	SEL Stable after $\overline{WR}$ High		10		10		ns
3	t_{SLWL}	$\overline{CS}$ Low to $\overline{WR}$ Low		5		5		ns
4	t_{WHSH}	$\overline{CS}$ High after $\overline{WR}$ High		5		5		ns
5	t_{WLWH}	$\overline{WR}$ Pulse Width	8	20		20		ns
6	t_{DVWH}	Data Valid to $\overline{WR}$ High		5		5		ns
7	t_{WHDX}	Data Held after $\overline{WR}$ High	10	20		20		ns
8	f_{CLK}	Clock Frequency	50	0	38.5 ①	0	33 ①	MHz
9	t_{CLCH}	Clock Pulse Duration Low	10	13		15		ns
	t_{CHCL}	High	10	13		15		ns
10	t_{CHOV}	CLK to Output when Writing to PW latch	25		50		60	ns
11	t_{ODLOL}	$\overline{ODIS}$ Low to Output Low	20	50		60		ns
12	t_{WHOL}	$\overline{WR}$ High to Output Low When Writing $\overline{Stop}$ to the Control latch	30		60		80	ns
13	t_{RLRH}	$\overline{RST}$ Low Time		50		60		ns

Numbers in the Fig. 3 to 6 corresponding to the time values on the bottom left of this page.

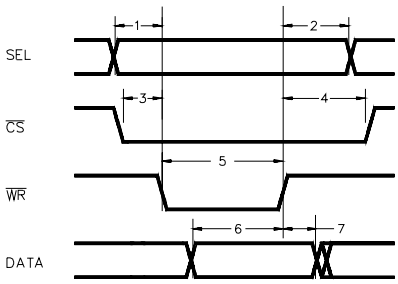


Fig. 3 Write operation timing diagram

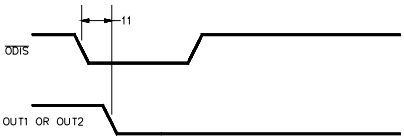


Fig. 4 Output disable to outputs off timing

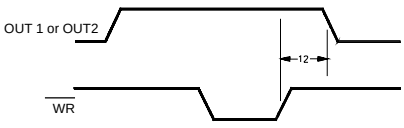


Fig. 5 Stop to outputs off timing

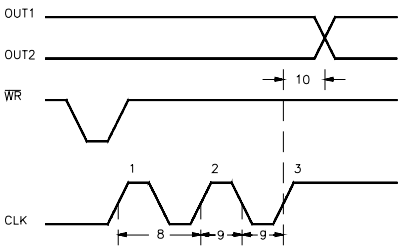
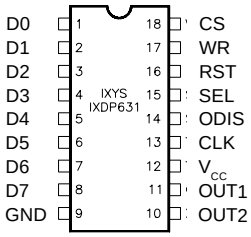


Fig. 6 CLOCK to output when writing to PW latch

① Extended frequency range parts are also available.
② Output will change 3 rising CLOCK edges after $\overline{WR}$ (see Fig. 6)

Pin Description IXDP 610



Sym. Pin Description

D0 D1 D2 D3 D4 D5 D6 D7	1 2 3 4 5 6 7 8	DATA BUS - the data bus on the IXDP610 is configured for input only. Data to be written to the IXDP610 is placed on data lines D0 through D7 during a microprocessor write cycle. Data is accepted by the IXDP610 when CHIP SELECT is low and the WRITE input goes from a low to a high state. The SELECT input determines whether the data written to the IXDP610 will go to the Control latch or to the Pulse Width latch. D0 is the least significant bit and D7 is the most significant bit.
GND	9	CIRCUIT GROUND
OUT2 OUT1	10 11	COMPLEMENTARY OUTPUTS these two outputs provide the complementary PWM signals. The base period or cycle time of these outputs is determined by the CLOCK and the control latch.
V_{CC}	12	POWER SUPPLY (5 V ± 10 %)
CLK	13	CLOCK - the frequency of this input determines the PWM base frequency. CLK also drives the internal state machines. It has no effect on any data bus transactions.
$\overline{ODIS}$	14	$\overline{OUTPUT\ DISABLE}$ - asserting this Schmitt trigger input forces the complementary outputs to be immediately disabled (OUT1 and OUT2 are forced low). The complementary outputs will remain low as long as long as this input is asserted, and for the duration of the PWM cycle in which $\overline{OUTPUT\ DISABLE}$ goes from low to high; i.e., the complementary outputs are not re-enabled until the beginning of the next PWM cycle, and then only if $\overline{OUTPUT\ DISABLE}$ and the $\overline{Stop}$ bit in the Control latch are not asserted.
SEL	15	SELECT-this input determines whether data written into the IXDP610 goes to the internal Pulse Width (PW) latch or to the Control latch. A zero on this input (low voltage) directs data to the PW latch; a one on this input (high voltage) directs data to the Control latch.
$\overline{RST}$	16	$\overline{RESET}$-this asynchronous, active low input disables the outputs, chooses 8-bit count mode in the PWM counter, sets the clock to be "divided by 1", clears Lock bit, and sets the dead-time counter to 7. Asserting $\overline{RESET}$ writes a 01000111 binary to the Control latch. Asserting $\overline{RESET}$ is the only way in which the Lock bit in the control latch can be cleared. Writes to the control latch that occur after the lock bit has been set to a one, can only modify the $\overline{Stop}$ bit. Any writes to the control latch, while the $\overline{RESET}$ input is asserted, are ignored. $\overline{RESET}$ also clears the PW latch.
$\overline{WR}$	17	$\overline{WRITE}$-a low-to-high transition on this input, when $\overline{CHIP\ SELECT}$ is low, causes data to be written to the selected IXDP610 latch. If $\overline{SELECT}$ is low, the data is written to the pulse width latch. If $\overline{SELECT}$ is high, the data is written to the control latch.
$\overline{CS}$	18	$\overline{CHIP\ SELECT}$ - this active low input enables the $\overline{WRITE}$ input so that data may be written into the IXDP610 latch selected by the $\overline{SELECT}$ input.

Nomenclature of Digital PWM Controller

IXDP 610 P I _ (Example)

IX — IXYS

DP 610 — Digital PWM Controller

Package Type
P — 18-Pin Plastic DIP

Temperature Range
I — Industrial (-40 to 85°C)
M — Military (-55 to 125°C)

– Optional Processing
Blank = Standard
B = Burn-in

Description

Introduction

The IXDP610 is a digital PWM controller. It simplifies the interface between a microprocessor and a switching power bridge by providing to a microprocessor the means to directly control the average voltage across a load (DC motor, etc.). Since the IXDP610 generates two complementary PWM control signals, there is no need for Digital to Analog Converters (DACs), Sawtooth Generators, and Analog Comparators. OUT1 and OUT2 can directly drive the buffers to the power transistors.

Use of the IXDP610 in a DC servo system is depicted in the system block diagram shown in Fig. 1. The IXDP610 receives digital data from the microprocessor and converts the data to a pair of complementary PWM signals that can be used to control the average voltage across a DC servo motor. A Shaft Encoder Peripheral Interface (SEPI) IC converts incremental encoder signals to a binary number so the microprocessor can monitor and complete the control of the DC servo motor.

It is possible to generate PWM control signals in software with a dedicated microprocessor or microcontroller. This has the limitation, however, of very low switching frequencies (<5 kHz) and significant software overhead. By using the IXDP610 to handle the generation of the PWM control signals, a microprocessor can handle several PWM channels and the PWM control signals can switch at relatively high rates (up to 300 kHz). Servicing the IXDP610 is a simple as writing an 8-bit number to the Pulse Width latch whenever a change in duty cycle is desired. This is analogous to writing data to a DAC.

Programmable dead-time

Because the IXDP610 is a digital IC, and is programmable, it is possible to tailor the dead-time period (defined as t_{DT} in Fig. 2). IXDP610's programmable dead-time feature is difficult to duplicate in the equivalent analog system. The control of a switching bridge usually involves a process of alternating the "on-time" of two power switches connected in series between a high-voltage and a low-voltage. For example, the H-bridge of Fig. 3 can be operated by turning the upper left and lower right transistors on and leaving the two remaining transistors off, during the first half of the PWM cycle. In the second half of the cycle, the upper right and lower left transistors are on and the remaining two are off. During the

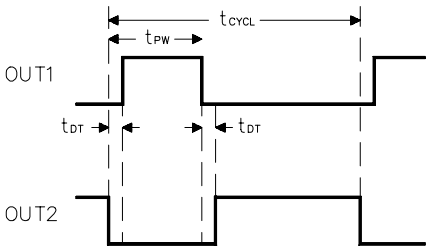


Fig. 2 PWM Cycle Time and Dead-Time Definition

transition, between the first half and the second half of the PWM cycle, there is a very short period of time when both the upper transistor and the lower transistor in a leg could be on. If both transistors are on, for this short period of time, they will effectively short the high voltage supply to ground-this is an undesirable situation.

The IXDP610's programmable dead-time feature prevents this situation by guaranteeing that both transistors in a leg are off for a minimum of time during a transition (the dead-time period). Since the dead-time is programmable, it can be tailored to the specific application. It can be short for high-speed MOSFETs and longer for IGBTs.

Protection circuitry

The IXDP610 has several features that facilitate protection of the power devices being controlled. The $\overline{\text{ODIS}}$ pin is an input that can be driven by external hardware under emergency shutdown conditions, such as over-current and over-temperature. The $\overline{\text{Stop}}$ bit, in the Control latch, provides a mechanism through which the software can indefinitely disable the complementary outputs. $\overline{\text{ODIS}}$ and $\overline{\text{Stop}}$ perform similar functions, they provide a means to protect the power devices from measurable system hazards such as over-current, over-voltage, over-temperature etc.

Software runaway is a system hazard that is difficult or impossible to measure. The Lock bit, in the Control latch, can be used to protect the system from software runaway and/or errors. Setting the Lock bit prevents subsequent writes to the Control latch from having any affect on the IXDP610's operating parameters. Setting the Lock bit does not prevent one from asserting the $\overline{\text{Stop}}$ bit. Once the Lock bit is set, it is impossible to modify critical parameters, such as the dead-time delay or the PWM waveform resolution.

Control latch

The Control latch is composed of eight bits that determine the IXDP610's operating parameters. Those bits are summarized in Table 2.

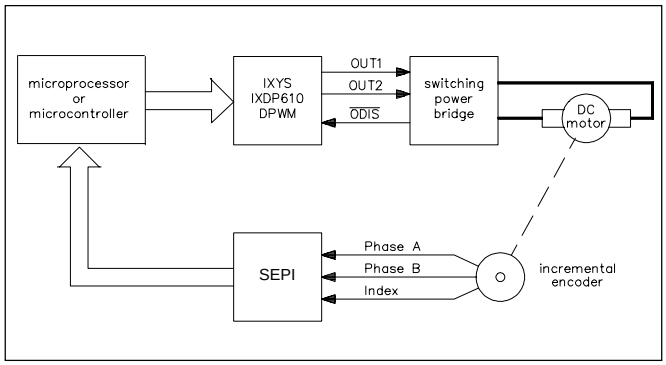


Fig. 1 Basic System Configuration

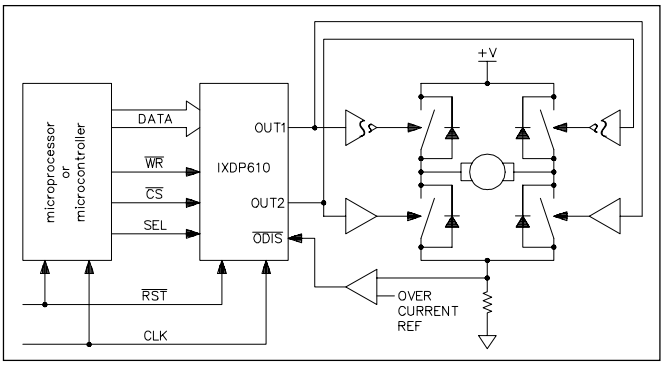


Fig. 3 IXDP610 to DC Servo Motor Full Bridge Block Diagram

SEL	$\overline{CS}$	$\overline{WR}$	Resulting Function
X	1	X	No Action
0	0		Load D0-D7 into PW latch
1	0		Load D0-D7 into Control Latch

Table 1 Bus Transaction Truth Table

Dead-time counter bits - these three bits determine the dead-time period, as defined by Fig. 2. Dead-time is that period of time when both OUT1 and OUT2 are low. Any binary number from 000 through 111 is valid. Thus, eight different dead-time periods can be programmed. DT0 is the least significant bit and DT2 is the most significant bit. A 000 binary means no dead-time and a 111 means maximum dead-time. Each dead-time count corresponds to two CLOCK periods. For instance, if a binary three (3) is programmed into the dead-time bits, the dead-time will be six external CLOCK cycles long.

The dead-time is provided to aid in preventing switch overlap. The Dead-time Counter delays turning on the switch connected to OUT1 until the switch connected to OUT2 has had sufficient time to turn off; the complement is also true, the dead-time counter delays turning on the switch connected to OUT2 until the switch connected to OUT1 has had sufficient time to turn off. Since the dead-time counter is programmable, the user can optimize the dead-time delay to suit their specific application.

In a typical PWM cycle (refer to Fig. 2) two dead-time periods will occur. One follows the turnoff of OUT2. The dead-time counter is triggered by an output turning off. During a dead-time period, both outputs are guaranteed to be off (no dead-time periods occur during 0 % and 100 % duty-cycle states). The dead-time period overlaps the ontime of an output, therefore, it shortens the on-time without affecting the base PWM cycle time. A dead-time period is only inserted if an output changes from high to low (on to off). Thus, if a PWM duty cycle is chosen such that an output would be on for a period of time equal to or less than one dead-time period, the switch associated with that output will not be turned on during the PWM cycle. In this special case, one will observe only dead-time period per PWM cycle time, rather than the two dead-time periods shown in Fig. 2.

Lock bit - writing a one to this bit prevents further writes to all bits in the control latch, except the $\overline{Stop}$ bit. Thus, a one should not be written to this bit until the IXDP610 has been programmed. Those writes that follow a one being written to the Lock bit have no effect on D0 through D6. The locking feature provided by this bit prevents modification of the control latch due to a software error, thereby helping prevent damage to the bridge being controlled by the IXDP610. Asserting the $\overline{RESET}$ pin is the only method by which the lock bit can be cleared.

Divide bit - this bit sets the frequency of the internal PWM clock. Writing a one to this bit causes the external CLOCK to be divided by two before being presented to the PW counter. Writing a zero to this bit results in no division of the external CLOCK before it is presented to the PW counter ("divide by one"). The Divide bit has no affect on the dead-time Counter.

Resolution bit - writing a zero to this bit chooses 7-bit counter resolution, while writing a one chooses 8-bit PWM counter resolution. Choosing 7-bit resolution doubles the achieveable PWM base frequency at the expense of decreased duty cycle resolution. The combination of the Divide bit and the Resolution bit provides the user with three different PWM base periods for a given external CLOCK frequency. A $\overline{RESET}$ programs the IXDP610 to operate in the 8-bit resolution mode.

When the IXDP610 is programmed in 8-bit mode, the PWM base period is equal to 256 PWM clock cycles. In 7-bit mode the PWM base period is equal to 128 PWM clock cycles. A PWM clock cycle is equal to one external CLOCK period when the Divide bit in the control latch is a zero and is equal to two external CLOCK periods when the Divide bit is a one.

The following formula can be used to determine the PWM base period:

If (($\overline{7}$/8 bit = 0) And (DIV bit = 0))
PWM base period CLOCK period x 128

else If (($\overline{7}$/8 bit = 0) And (DIV bit = 1))
PWM base period = CLOCK period x 256

else If (($\overline{7}$/8 bit = 1) And (DIV bit = 0))
PWM base period = CLOCK period x 256

else If (($\overline{7}$/8 bit = 1) And (DIV bit = 1))
PWM base period = CLOCK period x 512

The Pulse Width number that is written to the Pulse Width latch represents the high time of OUT1 (the low time of OUT2). The Dead-time Counter decreases the on-time (output high) of an output by one dead-time period (t_{DT}). See Fig. 2 and the description of the dead-time bits in the Control latch to determine the duration of one dead-time period.

Stop bit - writing a zero to this bit immediately disables the complementary outputs (OUT1 and OUT2 are forced to zero). As long as this bit is a zero, the complementary outputs will be disabled. This bit is not affected by the Lock bit. This bit is equivalent in function to the $\overline{OUTPUT\ DISABLE}$ input. The outputs will not be re-enabled until the start of the PWM period which has both the $\overline{Stop}$ bit and the $\overline{OUTPUT\ DISABLE}$ input set to ones.

PW latch - The binary number written to the PW latch represents the duty cycle of the complementary PWM outputs. Percent duty cycle is defined as follows: (assuming zero dead-time)

For OUT1:

$$\%\ \text{duty cycle} = \frac{\text{time at 1}}{\text{PWM cycle time}} \times 100$$

For OUT2:

$$\%\ \text{duty cycle} = \frac{\text{time at 0}}{\text{PWM cycle time}} \times 100$$

"PWM cycle time" is t_{CYCLE} in Fig. 2.

Control Bits	Name	Description
bit 0	DT0	for setting the dead-time period, all combinations are valid,
bit 1	DT1	0 is no dead-time delay and 7 is maximum dead-time.
bit 2	DT2	
bit 3		not used, reserved; always write a zero to this bit
bit 4	Lock	setting this bit prevents further access to all bits in the Control latch, except the $\overline{Stop}$ bit.
bit 5	DIV	determines frequency of the internal PWM clock.
bit 6	$\overline{7}$/8	chooses between 7-bit and 8-bit resolution.
bit 7	$\overline{Stop}$	disables (turns off) the complementary outputs.

Table 2 Control Latch Bits

The Resolution bit in the Control latch determines whether the number in the PW latch has 7 significant bits or 8 significant bits. The following formulae can be used to determine the resulting PWM waveform's duty cycle:

For 7-bit mode operation:

$$\% \text{ duty cycle} = \frac{\text{PW number}}{128} \times 100$$

For 8-bit mode operation:

$$\% \text{ duty cycle} = \frac{\text{PW number}}{256} \times 100$$

The formulae are valid for all PW numbers except those at the extremes.

PW Number (binary)				Resulting Duty
7-Bit Resolution		8-Bit Resolution		Cycle %
0000	0000	0000	0000	0.0
0000	0001	0000	0001	0.0
	--	0000	0010	0.78125
	--	0000	0011	1.171875
0000	0010	0000	0100	1.5625
	--	0000	0101	1.953125
0000	0011	0000	0110	2.34375
	--	0000	0111	2.734375
0000	0100	0000	1000	3.125
	:		:	:
	:		:	:
	:		:	:
0100	0000	1000	0000	50.0
	:		:	:
	:		:	:
	:		:	:
0111	1101	1111	1010	97.65625
	--	1111	1011	98.046875
0111	1110	1111	1100	98.4375
	--	1111	1101	98.828125
	--	1111	1110	99.21875
0111	1111	1111	1111	100.0
1XXX	XXXX		--	100.0

Table 3: Duty Cycle as a Function of PW Number

The following table illustrates the resulting percent duty cycle for several PW numbers. (The complete table would have 256 entries, those entries that have been omitted can be calculated using the above formulare.)

The PWM duty cycle byte can be written to at any time. If the outputs are disabled by either the $\overline{\text{Stop}}$ bit in the Control latch or the $\overline{\text{OUTPUT DISABLE}}$ input, writing to the PWM duty cycle byte will have no effect on the outputs. When the outputs are re-enabled, the duty cycle will be determined by the last byte written to the PWM duty cycle byte.

Application Information

Introduction

The IXDP610 is a digital PWM controller intended for use with general-purpose microprocessors and microcontrollers. Therefore, it is important to understand how the microprocessor hardware and software interacts with and affects the operation of the IXDP610. On the following pages one will find discussions of some of the most important hardware and software interface issues. Among these issues are the hardware interface, how to choose the IXDP610's clock, initialization of the DPWM, the effect of the dead-time on the duty cycle, and the response of the IXDP610 to changes in the Pulse Width latch number. The following pages should be studied carefully by both the hardware and the software designer.

The IXDP610 can be interfaced with virtually any microprocessor or microcontroller. Some interface examples are shown below.

8051 to IXDP610 Interface

Fig. 4 is an example of how the IXDP610 can be interfaced with an Intel 8051 microcontroller. The interface is very simple and is ideally suited for servo motor control applications. The 11.059 MHz clock allows one to use the 8051's built-in serial communication hardware at any standard baud rate. At this clock frequency, the IXDP610 can be configured for a 21.6 kHz switching frequency and a dead-time between zero and 1.26 µs, which is adjustable in 180 ns steps.

8088 to IXDP610 Interface

Fig. 5 is just one example of how the IXDP610 can be interfaced with the Intel 8088 microprocessor. Using a 5 MHz clock (15 MHz crystal) the IXDP610 can be configured for a 19.53 kHz switching frequency. The deadtime can be adjusted between 0 and 2.8 µs, in 400 ns steps. This configuration is ideally suited for driving DC servo motor amplifiers that use MOSFET, IGBT, or bipolar transistors.

Frequency and dead-time considerations

Typical applications for the IXDP610 include full and half bridge systems. Shown in Fig. 3 is a full bridge system. The programmable dead-time feature of the IXDP610 aids in preventing shorts in the power bridge and allows use of either fast MOSFETs or slower IGBTs and bipolar transistors. Table 4 shows some of the PWM frequency and dead-time combinations that can be obtained with the IXDP610. The various options shown in the table are selected by varying the CLK frequency and the Divide and $\overline{7}$/8 bit in the

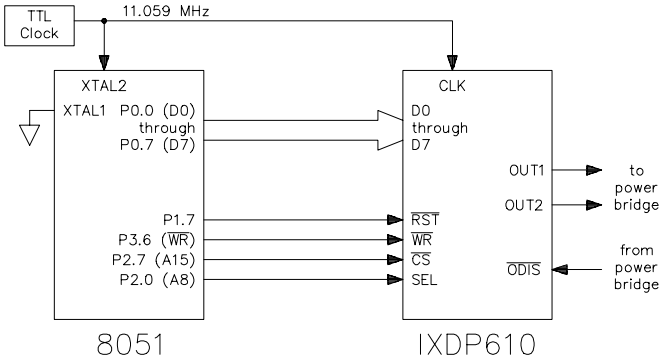


Fig. 4 8051 to IXDP610 Interface

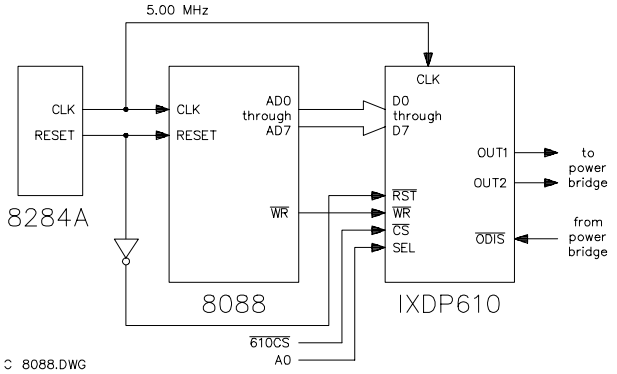


Fig. 5 8088 to IXDP610 Interface

IXDP610's Control latch. The "%" columns express the dead-time as a percent of the PWM cycle time.

If a zero is written to the $\overline{7}$/8 bit the IXDP610 is programmed for 7-bit resolution, writing a one programs the IXDP610 for 8-bit resolution. If a one is written to the Divide bit, the external clock (CLK) is divided by two before being presented to the Pulse Width counter; a zero in the Divide bit passes CLK directly to the Pulse Width Counter with no division of the frequency. For a given CLK frequency one can select three different PWM frequencies: CLK/128, CLK/256, and CLK/512. (CLK/256 can be selected for either 7-bit or 8-bit resolution.

Software Considerations

Initialization and the Lock Bit

After power-up, the IXDP610 should be reset via the $\overline{RST}$ input. Doing so will guarantee the initial state of the DPWM and effectively write a 01000111 binary to the Control latch. Thus, after asserting $\overline{RST}$, the IXDP610 is set to the following state:

- $\overline{Stop}$ is asserted, disabling OUT1 and OUT2
- 8-bit resolution is selected
- CLK is divided by one (not divided by two)
- Lock bit is “UNLOCKED”
- Dead-time Counter is set for maximum dead-time.

Asserting $\overline{RST}$ is the only means by which the Lock bit can be “unlocked". The lock bit must be cleared in order to write to all other bits in the Control latch, except the $\overline{Stop}$ bit.

The IXDP610 does not undergo an internal reset on power-up; therefore, it is recommended that the system reset be connected to the DPWM, as in Fig. 5. If one wishes to allow software control over the $\overline{RST}$ input, they should “OR” the system reset and an I/O bit together, so the DPWM has a known state following system reset. Before initializing the Control latch, one should first write a valid number to the Pulse Width latch (i.e., a number that results in 0 V applied to the load). Asserting $\overline{RST}$ clears the Pulse Width latch.

During a write to the Control latch, all bits can be modified simultaneously, including the Lock bit. Thus, only one write is necessary to set the dead-time: 1) assert the Lock bit; 2) choose the Divide bit state; 3) choose the resolution. In most applications it is not necessary to change the dead-time bit, the Divide bit, or the $\overline{7}$/8 bit “on the fly”. Therefore, it is recommended that the Lock bit be asserted during initialization of the Control latch. Setting the Lock bit guarantees that a software runaway will not modify the state of the dead-time bit, thereby preventing an accidental short of the bridge. If the $\overline{RST}$ input is accessible to the software (via an I/O bit, spare chip select, etc.), the hardware associated with asserting the $\overline{RST}$ input should be designed to minimize the possibility of resetting the IXDP610 in the event of a software runaway, since asserting the $\overline{RST}$ input clears the Lock bit, allowing modification of the DPWM's Control latch.

Software Overflow Protection

In many applications, the Pulse Width number written by the microprocessor to the IXDP610’s Pulse Width latch is the result of closed-loop numeric calculations. Depending on the algorithm used, the calculated PWM number may be susceptible to overflow, i.e. the calculated PWM number could be larger than the available 8-bits (or 7-bits) provided in the Pulse Width latch. If this is the case, it is important that the software checks for overflow conditions before writing a number to the Pulse Width latch. Following is an example assuming 8-bit resolution:

if (PWM__num < 0), check for underflow, PWM__num = 0, set to minimum limit

else if (PWM__num > 255), check for overflow, PWM__num = 255; set to maximum limit

Effect of Dead-time on Duty Cycle

The IXDP610 has been designed to generate PWM signals that range from 0 % to 100 %, inclusive. When zero dead-time has been selected (by writing 000 to the dead-time bits) the duty cycle of a PWM cycle can be determined by using the formulae shown on page 32/33. Fig. 6 illustrates the effect that a nonzero dead-time has on the PWM waveform.

The dead-time feature built into the IXDP610 guarantees that both OUT1 and OUT2 remain off for the duration of the dead-time period. A dead-time period occurs each time either OUT1 or OUT2 turns off; the dead-time period overlaps the on-time of an output (see Fig. 6c). Thus, if the desired duty cycle is such that the on-

PWM Frequency kHz	Dead-time Options						CLK MHz	$\overline{7}$/8 bit	DIV bit
	Min.		Step		Max.				
	%	µs	%	µs	%	µs			
300	0	0	1.56	0.052	10.9	0.363	38.4	0	0
200	0	0	1.56	0.078	10.9	0.547	25.6	0	0
100	0	0	0.78	0.078	5.5	0.547	25.6	1	0
100	0	0	1.56	0.156	10.9	1.094	12.8	0	0
50	0	0	0.39	0.078	2.7	0.547	25.6	1	1
50	0	0	0.78	0.156	5.5	1.094	12.8	1	0
50	0	0	0.78	0.156	5.5	1.094	12.8	0	1
50	0	0	1.56	0.312	10.9	2.188	6.4	0	0
20	0	0	0.39	0.195	2.7	1.367	10.24	1	1
20	0	0	0.78	0.391	5.5	2.734	5.12	1	0
20	0	0	0.78	0.391	5.5	2.734	5.12	0	1
20	0	0	1.56	0.781	10.9	5.469	2.56	0	0
5	0	0	0.39	0.781	2.7	5.469	2.56	1	1
5	0	0	0.78	1.562	5.5	10.94	1.28	1	0
5	0	0	0.78	1.562	5.5	10.94	1.28	0	1
5	0	0	1.56	3.125	10.9	21.88	0.64	0	0

Table 4. Sample PWM Frequency and Dead-time Options

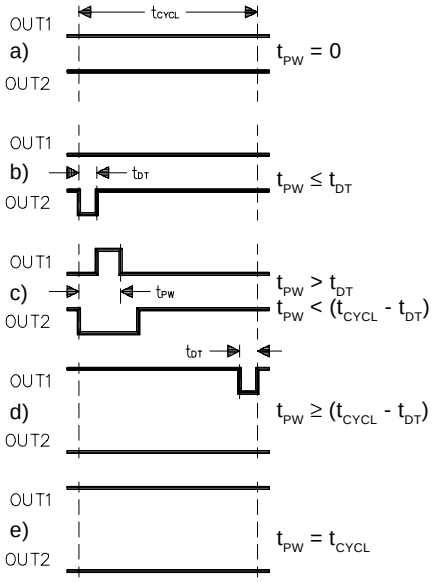


Fig. 6 Effect of Nonzero Dead-time on PWM Waveform

time of an output is less than one dead-time period, the output will not turn on. This is shown in Fig. 6b and 6d. Therefore, the commanded duty cycle and the actual duty cycle may differ slightly, especially at extreme duty cycle values.

Additionally, the dead-time can have an effect on the voltage applied to the load by the switching power bridge; the exact effect is a function of the direction of the current in the bridge and the architecture of the bridge. One should try and choose the smallest dead-time that will work with the given switch configuration.

Fig. 6.a and 6.e illustrate the two duty cycle extremes, 0 % and 100 %. In these two instances there will never by a dead-time period, regardless of the value programmed in the dead-time bits, because neither output ever turns off. Fig. 6b and 6d have only one dead-time period inserted in each PWM cycle. In Fig. 6b the desired ontime of OUT1 is less than the one dead-time period, therefore OUT1 can never turn on. The same is true for OUT2 in Fig. 6d. Fig. 6c is the normal situation, where both outputs turn on and off during one PWM cycle and, as a result, two dead-time periods are inserted.

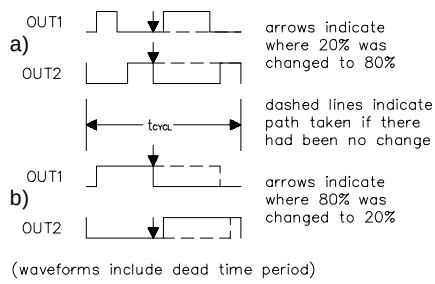


Fig. 7 Effect of Changing the Duty Cycle during a PWM Cycle

Response to a Change in the Pulse Width Number

One can change the Pulse Width number at any time. It is not necessary to synchronize writes to the Pulse Width latch with the CLK or the PWM cycle period. The IXDP610 responds to the new Pulse Width number three clock cycles after the Pulse Width latch is loaded (3 CLK cycles after $\overline{WR}$ goes high). Thus, OUT1 and OUT2 will immediately reflect the new Pulse Width number. The IXDP610 does not wait until the next PWM cycle to implement a change in the Pulse Width number. (See Fig. 7).

The resulting duty cycle is somewhere between the old and the new duty cycle. The exact value of the resulting duty cycle depends on when the Width Latch is loaded (3 CLK cycles after $\overline{WR}$ goes high). Thus, OUT1 and OUT2 will immediately reflect the new Pulse Width number. The IXDP610 does not wait until the next PWM cycle to implement a change in the Pulse Width number.

Fig. 7a shows what happens when the Pulse Width number is changed from 20 % to 80 % near the middle of the PWM cycle. Fig. 7b shows the reverse situation.

The resulting duty cycle is somewhere between the old and the new duty cycle. The exact value of the resulting duty cycle depends when the Width latch is loaded (3 CLK cycles after $\overline{WR}$ goes high). Thus, OUT1 and OUT2 will immediately reflect the new Pulse Width number. The IXDP610 does not wait until the next PWM cycle to implement a change in the Pulse Width number.

High Performance Dual PWM Microstepping Controller

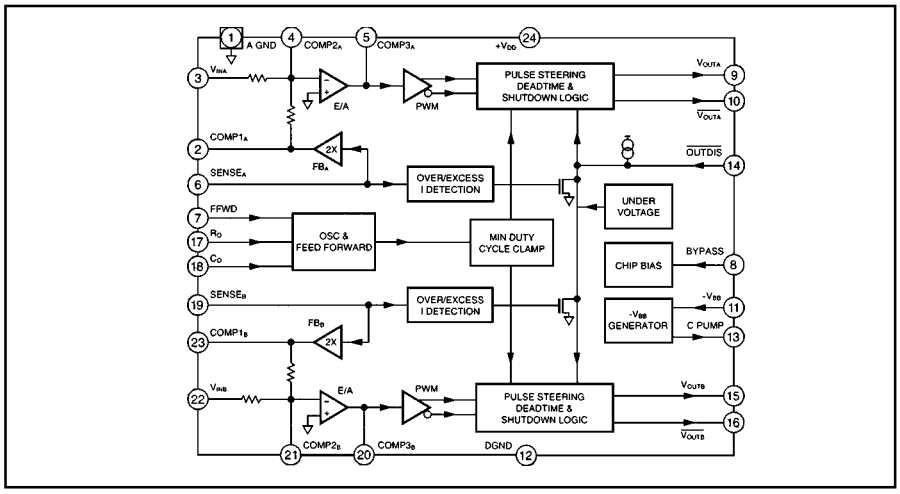
Type	Package	Temperature Range
IXMS150 PSI	24-Pin Skinny DIP	-40°C to +85°C

The IXMS150 is a high performance monolithic 2-channel PWM controller. Implemented in CMOS, the low power IXMS150 precisely controls the current in each of two separate power H-bridge drivers using unique sampling and signal processing techniques. Each channel contains an error amplifier, PWM, feedback amplifier, and protection circuitry. Protection features include over/excess current shutdown, min/max duty cycle clamp, under voltage lockout, dead time insertion, and a shutdown input for over-temp or other external fault circuitry. Other features include a common oscillator, feedforward circuit for motor supply compensation, and an onchip negative bias generator.

The IXMS150 has been optimized for microstep control of two phase step motors. Due to its high level of accuracy, the IXMS150 will allow a designer to implement a control system with a resolution in excess of 250 microsteps per step, or 50,000 steps per revolution with a 200 step per revolution step motor. The IXMS150 greatly improves positioning accuracy and virtually eliminates low speed velocity ripple and resonance effects at a fraction of the cost of a board level microstepping system.

Other applications which the IXMS150 is designed for include control of two single-phase (DC) motors or control of synchronous reluctance motors. The IXMS150 is ideal for robotics, printers, plotters, and x-y tables and can facilitate the construction of very sophisticated positioning control systems while significantly reducing component cost, board space, design time and systems cost.

Block diagram of IXMS 150



Symbol	Definition	Max. Ratings	
V_{DD}	Supply voltage	-0.3...15	V
	Operating range	10.8...13.2	V
	Common-mode-range	-15...15	V
	Differential Input voltage ①	±30	V
V_{IN}	Input voltage ①	-15...15	V
V_O	Output voltage	-0.3...V_{DD}+0.3	V
P_D	Maximum power dissipation	500	mW
T_A	Ambient temperature range	-40...85	°C
T_{stg}	Storage temperature range	-55...125	°C

① Input voltage may not exceed either supply rail by more than 0.3 V at any time.
IXYS reserves the right to change limits, test conditions and dimensions.

Features

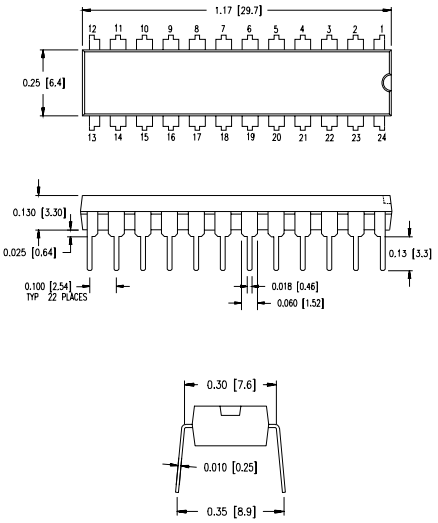
- Two complete, synchronous PWMs
- Command input range ±2.0 V full scale
- ±0.625 V full scale current feedback signal
- 1% gain matching between channels without external trim
- 1.6% gain linearity
- Feedforward to compensate for motor supply variations
- Only one sense resistor per H-bridge needed
- Onboard two level current limiting
- Undervoltage lockout assures proper behavior on power up and power down
- Enable input for external over temperature or fault circuit input
- Duty cycles limited for AC coupled gate drive
- Wide range of built in dead time.
- On board negative power supply generator
- Single +12 V supply operation
- 24-pin DIP package

Applications

- Full, half quarter, or microstepping 2-phase step motor position controller
- Dual DC servo motor torque controller
- Solenoid actuator force controller
- General 2-channel current-commanded PWM control

Symbol	Definition/Condition			Characteristic Values (V_{DD} = 12 V, T_A = 25°C unless otherwise specified) min.	typ.	max.	
Oscillator							
f_{OSC}	Frequency	C_o		10		400	kHz
$V_{A(p-p)}$	Amplitude		FFWD = OPEN		7		V
Z_{OUT}	Output Impedance		± I_{OUT} = 400 µA		2.5		mΩ
	Resistance Range	R_o		15		100	kΩ
	Capacitance Range	C_o		100		2000	pF
Feed Forward							
V_{FFWD}	Feedforward Voltage		FFWD = Open		3.5		V
Z_{INFF}	Impedance to AGND			25	45		kΩ
Analog Inputs							
V_{FS}	Input FullScale	V_{INA} V_{INB}	DC			±2	V
Z_{IN1}	V_{IN} to $Comp_2$ Impedance		DC	20	32		kΩ
Z_{IN2}	$Comp_1$ to $Comp_2$ Impedance		DC	12	20		kΩ
Sense Inputs		$SENSE_A$					
V_{SENSE}	Full Scale Input	$SENSE_B$	DC			±0.625	V
Z_{INS}	Input Impedance		DC	100	200		kΩ
Protection Circuit		$SENSE_A$					
V_{OV-1}	Over Current Voltage	$SENSE_B$		0.8	0.95	1.0	V
t_{OV-1}	Reset Pulse Width			0.5	1		µs
V_{EX-1}	Excess Current Voltage			3.45	3.6	3.75	V
t_{EX-1}	Reset Pulse Width				300		ns
Under Voltage							
V_{UV}	Minimum V_{DD}	$\overline{OUTDIS}$		7.5	8	8.5	V
I_{IH}	Input High Current		V_{IH} = 11.5 V		100		µA
I_{IL}	Input Low Current		V_{IL} = 0.5 V		1.8		mA
Outputs							
V_{OH}	Output High Voltage	V_{OUTA}, $\overline{V_{OUTA}}$	I_{OH} = -10 mA	8.0	11.2		V
V_{OL}	Output Low Voltage	V_{OUTB}, $\overline{V_{OUTB}}$	I_{OL} = 10 mA		0.8	1.1	V
t_r	Rise Time		C_L = 100 pF		35	50	ns
t_f	Fall Time		C_L = 100 pF		35	50	ns
T_{DT}	Dead-Time		C_o = 180 pF	200	300	450	ns
T_{MIN}	Minimum Pulse Width		C_p = 30 pF	0.6	0.8	1.5	µs
VBB Generator							
V_{BBmin}	Minimum Negative Bias	V_{BB}	$\overline{OUTDIS}$ = V_{DD}	-1.4	-1.9		V
V_{BB}	Negative Bias Voltage		I_{OUT} = -3 mA	-2.1	-2.4		V
V_{REG}	Load Regulation		f_{OSC} = 100 kHz		60		mV
V_{OH}	Output High Volt.	C_{PUMP}	I_{OH} = -10 mA		11.2		V
V_{OL}	Output Low Volt.		I_{OL} = 32 mA		0.8		V
Supply							
I_{DD1}	Idle Current	V_{DD}	V_{IN} = 0		16	26	mA
I_{DD2}	Operating Current		f_{OSC} = 100 kHz		15	45	mA
V_{BYPASS}	Bypass Voltage	BYPASS		5.9		16.1	V
Z_{INBP}	Impedance to AGND			9	16		kΩ

Dimensions in inch (1" = 25.4 mm)
24-Pin Skinny DIP



Pin Description IXMS 150

Sym.	Pin	Description
AGND	1	Analog Ground
COMP	2 4 5 20 21 23	Analog Compensation (see application notes for recommendations).
VIN	3 22	Analog Input: The analog input range is ± 2 V. A low output im pedance voltage source should drive these pins. The input is greater than 20 kΩ.
SENSE	6 19	Analog Sense: Each of the phases sense resistors are connected to these pins. Input range is +0.625 V.
FFWD	7	FFWD, for Motor High Voltage Compensation: A voltage on this pin sets the oscillator amplitude. Input range = 0.9-4 V (see application notes for recommendations).
BY-PASS	8	Filter Cap: A capacitor on this pin provides filtering to the internal bias network.
VOUT	9 10 15 16	Output Stage: To drive buffered power MOSFET H-Bridge.
VBB	11	Negative Bias Generator Output: For internal use by the IXMS 150.
DGND	12	Digital Ground
CPUMP	13	Charge Pump Capacitor: Used by the internal Negative Bias Generator.
$\overline{\text{OUTDIS}}$	14	Digital ENABLE input and STATUS output: Forcing this pin low causes pins 9, 10, 15, and 16 to go low, disabling the H-bridge. When uses as an output, a low state on this pin indicates an over current, excess current, or insufficient $+V_{DD}$ or V_{BB} error condition.
R_O, C_O	17 18	Oscillator Frequency and Dead-time set: Independent adjustment can be made to the oscillator frequency and dead-time (see applications notes).
VDD	24	Positive Supply Voltage

* Pin numbers in parantheses are associated with channel B.

Nomenclature of Dual PWM Microstepping Controller

IXMS 150 PS I (Example)

IX — IXYS

MS 150 — Dual PWM Controller

Package Type

PS — Plastic Skinny DIP

Temperature Range

I — Industrial

Functional Description

Introduction

The IXMS150 is designed with monolithic CMOS technology. The IC is primarily intended for use with two-phase step motors in the microstepping mode but may also be used for control of two DC motors, audio amplifiers, or any application requiring two synchronized PWMs. The IXMS150 simultaneously controls the currents in each of two separate H-bridges. This device utilizes both analog and digital functions.

The IC has five fundamental sections: (1) oscillator and feedforward circuitry, (2) analog section for control of the motor currents, (3) a protection network to protect the H-bridges and the motor from abnormal conditions, (4) the digital PWM logic for the control signals, and (5) the power supply section which includes a negative bias generator.

Oscillator

The IXMS150 contains an internal oscillator which is controlled by adjusting the values of R_O and C_O. These two components determine the switching frequency, amount of dead time, and the minimum pulse width at output pins 9, 10, 15 and 16. The minimum and maximum values of R_O and C_O are given in the Electrical Characteristics.

The oscillator also sets the frequency of the charge pump circuit in the internal negative bias generator (V_{BB}). At lower frequencies (<40 kHz) the value of CPUMP must be increased to assure proper operation.

Feedforward Compansation

In all fixed frequency PWM control systems open loop gain, motor current slew rate, and motor current ripple are proportional to the motor supply voltage. Gain variations due to supply voltage changes complicate the design of such systems and restrict their bandwidth to the minimum worst case condition. For this reason, an advanced adaptive compensation scheme is built-in using a feedforward technique. This feature has been designed such that open loop gain is inversely proportional to the voltage applied to the FFWD pin, normally a fraction of the motor supply. As a result, open loop gain can be made independent of the high voltage supply and system bandwidth can be maximized.

Analog Section

The analog section of each channel of the IXMS150 consists of a signal processor and an error amplifier. The signal processor is required since the voltage developed across the sense resistor often contains transients associated with the switching characteristics of the power devices. These transients need to be properly filtered for the system to operate with the desired degree of precision. Because of this, the IXMS150 uses proprietary analog and digital signal processing techniques that sense the true average phase currents. Since this requires only one sense resistor per H-bridge it avoids mismatches in charge/discharge currents associated with two sense resistor per H-bridge topologies.

The instantaneous difference between the motor current and the control input is integrated via the E/A amp and fed to the PWM comparator to generate the appropriate signals for the H-bridges. External compensation of the input and sense signals is provided for via the comp1, comp2 and comp3 pins.

Protection Circuitry

The IC has a two-level Over/Excess Current protection circuit. Maximum current is represented as 0.625 V at the SENSE input. If the SENSE voltage exceeds 0.9 volts for more than one microsecond, the switching outputs (VOUT) and $\overline{\text{OUTDIS}}$ will be forced low. This represents a current that is 40 % beyond full scale. If the SENSE voltage exceeds 3.6 V, these outputs will be forced low immediately. This represents a current that is 500% beyond full scale. The time delay on the lower level of overcurrent avoids erroneous shutdowns as a result of noise spikes that are coupled from the motor's H-bridges. Note that the threshold voltages cited here assume a supply of +12 V.

Undervoltage Lockout

A third protection mechanism is the Under-Voltage Lockout. It assures proper behavior on power-up and power-down and avoids high power dissipation in the H-bridge due to insufficient gate voltage. It uses a zener for reference and has a trip point set at 8 V. It will also check to make sure there is sufficient negative bias to insure proper operation. This is typically -1.6 V. OUTDIS will be held low by the UV Lockout circuit until V_{BB} and V_{DD} reach these values.

Output Disable Feature

To enable external over-temperature protection, the output disable pin ($\overline{\text{OUTDIS}}$) is available on the IXMS150. When pulled low this disables the output by forcing all output pins low. The same output disable input pin is also used as a status output. When it is pulled low by the internal circuitry it indicates an error condition such as undervoltage (V_{DD}), insufficient negative bias voltage (V_{BB}) or over/excess current. This can be used as a status indicator in smart systems.

PWM Section

The PWM comparator generates two complementary signals based on the output of the error amplifier. Dead-time is then added which is adjusted by the selection of the external oscillator capacitor. There is also a minimum duty cycle clamp circuit that allows the use of an AC coupled H-bridge.

Supply Section

The main power supply (V_{DD}) is applied to pin 24. This is typically +12 V. Internal bias circuitry presents a $V_{DD}/2$ reference voltage at pin 8, BYPASS. A 0.1 µF capacitor should be connected from pin 8 to analog ground for noise immunity.

Negative Bias Generator

The IXMS150 samples both positive and negative voltages at the motor sense feedback resistor. In addition, since errors in the input current around zero are a major contributor to microstep positioning error, the input control range is bipolar and specified as ±2 V full scale. For these reasons it is desirable to have both positive and negative power supplies. In order to enable single 12 V supply operation, a negative voltage generator and regulator are built into the IC. This is a charge pump circuit whose frequency is that of the onboard oscillator. It utilizes an external pair of capacitors and diodes to generate a negative bias equal to $-V_{DD}/5$ or approximately -2.4 V for V_{DD} = 12 V.

Application Information

Introduction

The advantages of step motors are well known. They may be operated in an open loop fashion, the accuracy of which is mostly dependent on the mechanical accuracy of the motor. They move in quantized increments (steps) which lends them easily to digitally controlled motion systems. In addition, their drive signals are square wave in nature and are therefore easily generated with relatively high efficiency due to their ON/OFF characteristics.

But step motors are not free of problems. Their large pulse drive waveforms create mechanical forces which excite and aggravate the mechanical resonances in the system. These are load dependent and difficult to control since step motors have very little damping of their own. At resonance a step motor system is likely to lose synchronization and therefore skip or gain a step. Being an open loop system, this would imply loss of position information and would be unacceptable. A common method of solving this problem is to avoid the band of resonance frequencies altogether, but this might put severe limitations on system performance. Steppers have 200 steps per revolution or 1.8 degrees per step. The highest resolution commercially available steppers have 400 steps per revolution or 0.9 degrees per step.

Microstepping Mode

One way to circumvent the problems associated with step motors while still retaining their open loop advantages is to use them in the microstepping mode. In this mode each of the steps is subdivided into smaller steps or “microsteps". Applying currents to both phases of the motor creates a torque phaser which is proportional to the vector sum of both currents. When the phasor completes one “turn” (360 electrical degrees), the motor moves exactly four full steps or one torque cycle. Similarly, when that phasor moves 22.5 electrical degrees the motor will move (22.5/90) • 100 = 25 % of a full step. Thus the position of the motor is determined by the angle of the torque phasor. When used with an appropriate motor a positioning accuracy of 2 % of a full step can be achieved, equaling 0.036 degrees for a 200 full steps per revolution motor. In this manner the motor can be positioned to any arbitrary angle. A common way to control the angle of the torque phasor is by applying to the motor’s phases two periodic waveforms shifted by 90 electrical degrees.

Let the phase current equations be:

$i_A = I_O \bullet \cos \theta e$ (1)
$i_B = I_O \bullet \sin \theta e$ (2)

Note that θe is the electrical position.

The resulting torque generated by the corresponding phases would then be:

$T_A = K_0 \bullet i_A = K_0 \bullet I_0 \bullet \cos \theta e$ (3)
$T_B = K_0 \bullet i_B = K_0 \bullet I_0 \bullet \sin \theta e$ (4)

where K_0 is the torque constant of the motor. Substituting Eqs. (1), (2) into (3), (4) and doing vector summation the resulting total generated torque measured on the motor shaft is given by:

$T_g = K_0 \bullet I_0$ (5)

Note that in this case we have zero torque ripple.

Using this technique one can theoretically achieve infinite resolution with any step motor. Since the drive current waveforms are sinusoidal instead of square, the step to step oscillations are eliminated and the associated velocity ripple. This greatly improves performance at low rotational speeds and helps avoid resonance problems. In an actual application, the extent to which these things are true depends on how the two sinusoidal reference waveforms are generated.

Seemingly we have lost the quantized motion feature of a stepper when used in this mode. This can be regained by defining the term microsteps per step. Each full step is subdivided into microsteps by applying to the motor’s phases those intermediate current levels for which their vector sum tracks the circle of Fig. 2 and divides the full step (90 electrical degrees) into the require number of microsteps. An example of the required phase currents for full step and four microstep per step operation are shown in Fig. 1 and 2 respectively.

Phase Current Matching Requirements

Assuming microstepping is being used for resolution improvement and not as a resonance avoidance technique, a step motor can be selected knowing the torque needed, its specified step

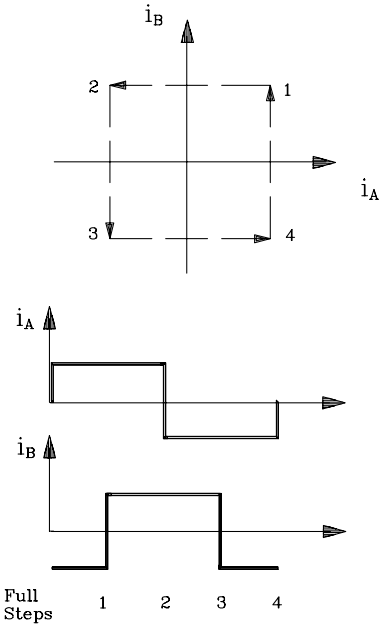


Fig. 1 Full Step Drive Waveforms

accuracy, and the required resolution or the number of microsteps per step. Next, one must determine the accuracy required of the phase currents to maintain the accuracy of the complete system. Equations (1) - (4) clearly indicate that errors in the absolute value or phase of the phase currents will impact positioning accuracy. Another observation is that by keeping the ratio of the phase currents i_A/i_B constant, errors in their value will result

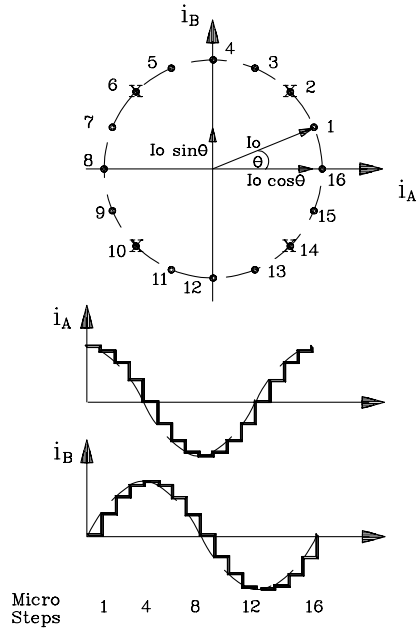


Fig. 2 Four Microstep per Step Drive Waveforms

in torque value errors but no positioning errors. The question is, what is the upper bound on the current errors in order to keep the position error within some given angle $\Delta\theta$.

Referring to Fig. 3, assume the required currents i_A, i_B are given by Equations (1), (2) respectively such that their vector sum points to position P. Let the phase currents vary by a small amount such that their vector sum lies within a circle centered at point P and having the radius i, as indicated in Fig. 3.

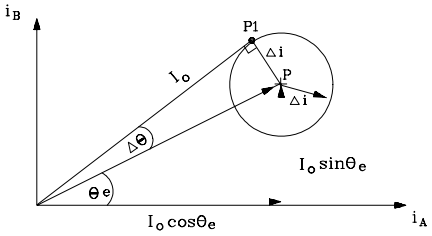


Fig. 3 Effect of Current Errors on Position

If follows that the worst case position error occurs for the cases where the vector sum is tangent to the circle such as point P_1, at which:

$$\tan(\Delta\theta) = \Delta i / I_0 \qquad (6)$$

For instance, to keep position error to less than 1% of a full step, the electrical angular error would be:

$$\Delta\theta = 0.01 \bullet 90° = 0.9° \qquad (7)$$

This is assuming there are 90 electrical degrees for a full step. Therefore total current error must be:

$$i/I_0 = \tan(\Delta\theta) = 0.016 \text{ or } 1.6\ \%) \qquad (8)$$

Thus the current error must be kept to less than 1.6 % of full scale or peak current at each phase for 1% maximum position error. This upper bound on error includes all error sources such as zero offset errors and full scale matching errors. Another interesting observation is that in the vicinity of a full step (i.e., $\theta e = 0$), the phase having the bigger impact on position error is the one carrying the smaller current through it. This has a strong impact on input waveform generation.

Input waveform generation

It has been shown that the two input signals, VIN_A and VIN_B, are sinusoidal and 90° out of phase. This may be accomplished by using two look-up

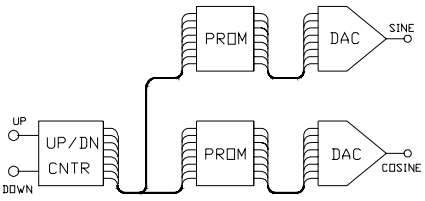


Fig. 4 Simple Reference Waveform Generator

tables stored in ROM and two DACs per Fig. 4. An up/down counter may be used to generate the appropriate address locations for the ROMs and the data outputs used to control the DACs. The user then need only supply up or down pulses to the counter to control the IXMS150 and hence the motor.

In higher performance systems a microprocessor may be used in place of the counter and the ROMs. The micro can perform the look-up function and calculate the appropriate system responses, velocity profiles, etc. necessary for total system operation. An example of this configuration is shown in Fig. 5.

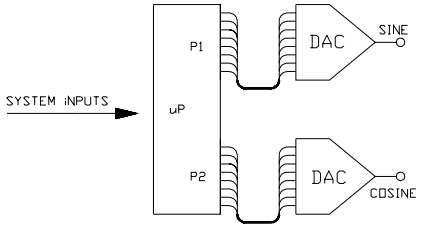


Fig. 5 Microprocessor Based Referenced Waveform Generator

Current Sensing Considerations

Most commercially available monolithic PWM controllers monitor and control the peak of the phase current by comparing the voltage across the sense resistor with a ramp voltage. This approach assumes that the ripple current is fixed in amplitude. Results shown later clearly indicate the variation of the ripple current with frequency. But even in fixed frequency systems the ripple current is directly proportional to the motor supply voltage and to the back EMF voltage of the motor. Ripple current is not insignificant compared to the full scale current and therefore cannot be neglected in a precision system. In addition, there are transients associated with the turn on and turn off characteristics of the power devices in the H-bridge that must be properly filtered if the system is to operate with the desired degree of precision.

This presents a significant engineering challenge that has been solved by IXYS's design team. Using proprietary analog and digital signal processing techniques, IXYS has developed a control system that measures the true average phase currents. Requiring only one sense resistor per H-bridge, this technique avoids errors due to mismatches in charge/discharge currents associated with using one sense resistor on each leg of the H-bridge. This improves system performance as well as minimizing component count. The sense resistor for each H-bridge should be selected based on the required peak motor current:

$$R_S = 0.625\ V/I_{mpk} \qquad (9)$$

The voltage developed across this resistor is then applied to the corresponding sense input for each H-bridge.

Negative bias Generator

One of today's cost cutting trends is to minimize the number of power supplies, implying single supply operation for the control section. Yet the current feedback and reference inputs are bipolar signals. Level shifting has been used for the reference input in the past, but that can not be easily done for the feedback signal without impacting accuracy or efficiency. In practice one finds that in order to generate true zero voltage having low impedance drive there must be a negative power supply. Otherwise there will be a tradeoff sacrificing accuracy for simpler system design.

For these reasons the approach selected by IXYS was different. Taking advantage of our CMOS design, we opted to build into the chip a negative bias generator. This does put stringent demands on noise coupling but results in the most flexible system having the highest possible accuracy. The built in charge pump circuit requires two capacitors and two diodes to be added externally. The recommended component values for an oscillator frequency of 100 kHz are given below.

C1 = 0.047 µF
C2 = 100 µF
D1 = D2 = 1N4148
Note: $V_{BB} = -(V_{DD}/5)$

Use the formula
C2 = 100 µF · 100 kHz/f_{OSC}
for other frequencies.

With V_{DD} = 12 V and an oscillator frequency of 100 kHz, the bias generator should be able to source 3 mA at -2.4 V using these component values. This capability may be used to power other external circuitry as long as there is sufficient remaining negative bias to allow the IXMS150 to operate properly.

Impact of PWM Frequency on System Operation

PWM switching frequency has a pronounced effect on ripple current through the motor windings, the resulting eddy current losses in the motor, and system efficiency. As expected, motor current ripple goes down as frequency increases and therefore losses resulting from ripple currents are also reduced. Switching frequency also impacts losses in the power stage. These losses are associated with the energy necessary to turn on and off the power MOSFETs and are proportional to the switching frequency. In addition, the switching frequency has a limiting effect on maximum current loop bandwidth and therefore system bandwidth and therefore system bandwidth and maximum motor velocity.

Oscillator

The oscillator block diagram is shown in Fig. 6.

The frequency is set by the values of R_O and C_O:

$$f_{OSC} = 1/R_O \bullet (C_O + C_P)) \qquad (10)$$

Note: C_P is a 38 pF (typ.) internal parasitic capacitor.

Feedforward

The amplitude of the oscillator waveform and overall system gain are modulated by the voltage applied to the feedforward pin (FFWD). This is nominally 3.5 V which should be divided down from the motor high voltage supply. This will allow system bandwidth to be maximized by making overall system gain inversely proportional to the motor supply voltage. Refer to Fig. 7 for an example of how feedforward is connected to the motor supply. It is recommended that a filter capacitor be connected from FFWD to AGND to filter noise spikes from the motor supply. Its value should be chosen so that the time constant of the capacitor and the parallel combination of R_{ff1} and R_{ff2} is such that switching noise will be filtered but not variations in the motor supply such as 120 Hz ripple, etc.

Minimum Pulse Width

The minimum output pulse width can also be modified by adjusting the oscillator capacitor C_O. The relationship is:

$$t_{pw(min)} = R_{mp} \bullet (C_O + C_p) \qquad (11)$$

Note: R_{mp} is a 3.6 kΩ (typ.) internal resistor, and C_p is a 38 pF (typ.) internal parasitic capacitor.

Dead Time

Dead time is adjusted via the external oscillator capacitor C_O. There is an internal resistor in the dead time circuit as well. The relationship is:

$$t_{DT} = R_{DT} \bullet (C_O + C_p) \qquad (12)$$

Note: R_{DT} is a 1.4 kΩ (typ.) internal resistor and C_p is a 38 pF (typ.) internal parasitic capacitor.

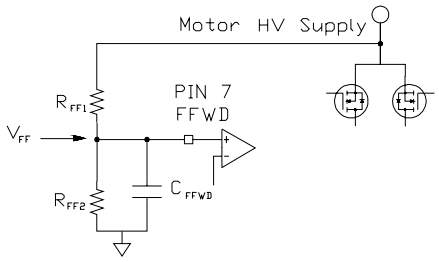


Fig. 7 Feedforward Connection Diagram

Motor Slew Rate Limitations

The maximum motor velocity in a microstepping application is determined by the maximum rate of change of the phase currents. Once this limit is reached the system is “slew rate limited,” at which point the peak undistorted phase current times the frequency of the input command is a fixed value. The theoretical limit for the maximum di/dt of the phase currents is determined by the motor supply voltage and the inductance of the motor:

$$di/dt\ (max) = V_{HV}/L_m \qquad (13)$$

The limit does not take into account the back EMF of the motor, the bandwidth of the current loop driving the motor, or the minimum pulse width. The motor’s back EMF will tend to reduce the voltage applied across the motor windings, effectively reducing the maximum slew rate. The bandwidth of the current loop must also be high enough so as not to degrade system performance.

Non-Circulating Operating Mode

The IXMS150 is designed to control an H-bridge in the non-circulating mode. The equivalent circuit for an H-bridge is shown in Fig. 8. In the non-circulating

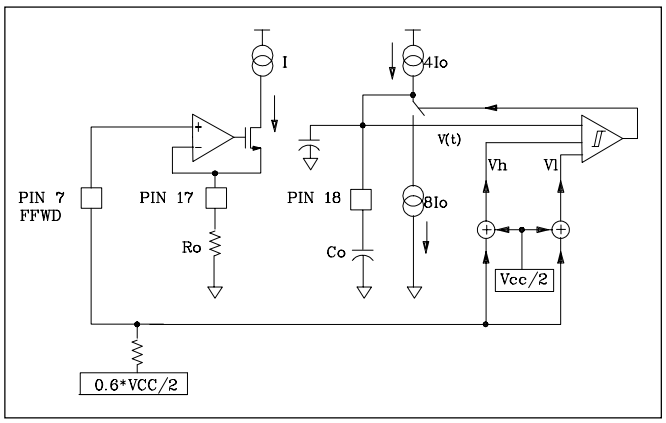


Fig. 6a: Oscillator Block Diagram

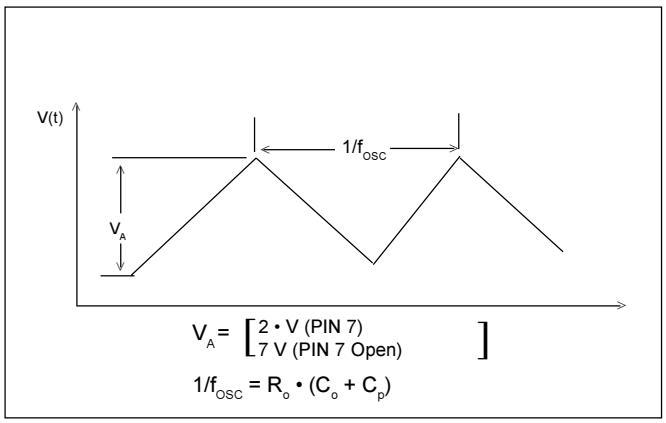


Fig. 6b: Oscillator Waveform Diagram

mode, either SW1 and SW4 are on ($V_m = V_{HV}$) or SW2 + SW3 are on ($V_m = -V_{HV}$). By appropriately controlling the duty cycle of SW1//4 vs. SW2/3, the average motor voltage can be controlled such that:

$V_{m(avg)} = 2 \bullet V_{HV}$ (0.5-DUTY)

Note: DUTY is defined as the duty cycle of V_{OUTA}.
The IXMS150 can now regulate the motor coil current by commanding the voltage level and polarity required.

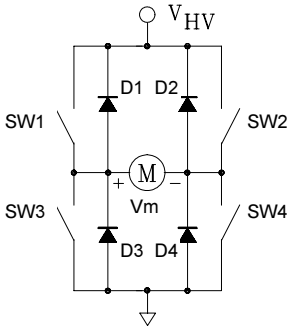


Fig. 8 Simplified H-Bridge Diagram

The Power Stage:
An AC Coupled H-Bridge

Fig. 9 shows the power driver selected for this application. Two of these are required to drive the two phase step motor. This circuit uses two N-channel and two P-channel power MOSFETs as opposed to an all N-channel architecture. The drawback of using P-channel transistors is that they are larger and therefore more expensive than similarly rated N-channel devices. But the advantages are much simplified drive and level shifting circuitry. This results in a lower component count and therefore higher reliability. It also lends itself easily to hybridization. Other advantages of this topology are: a) the high efficiency associated with level shifting by AC coupling since no power is dissipated in the capacitors, and b) the same circuit can be used for motor applications ranging from 12 V to several hundred volts, the only modification being appropriately rated power transistors and coupling capacitors.

A limitation of this circuit is that it cannot be used at duty cycle extremes. This would require one input to be continuously low while the other is continuously high. Eventually the coupling capacitors (C1, C2) would charge up to a voltage that would no longer fully enhance the MOSFETs, with the top two transistors (Q2, Q4) being destroyed due to excessive power dissipation. Therefore one has to limit the duty cycle excursions. The solution selected by IXYS limits the minimum output pulse-width to 0.5 ms, which translates to a duty cycle range of 5 % to 95 % when operating at 100 kHz, or wider at lower frequencies. There is a penalty of slightly limiting the maximum slew rate to (1-2 • Min Duty) of the unrestricted case, which translates to 90 % of the unrestricted maximum slew rate for 100 kHz operation.

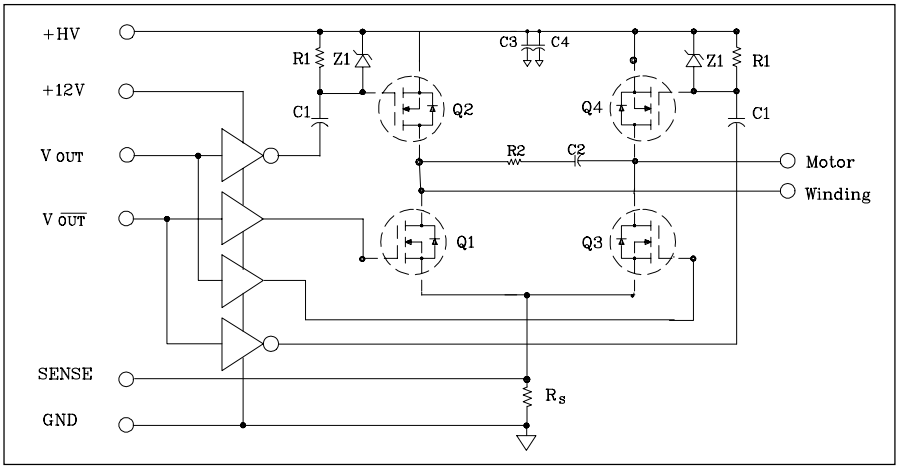


Fig. 9 AC Coupled H-Bridge Diagram

Loop Compensation Information

When used with the appropriate power stage, each channel of the IXMS150 acts as a closed loop transconductance amplifier. As such, it must be properly compensated to guarantee stable operation with a particular motor. The basic elements involved in the current loop are illustrated in Fig. 11a. Referring to Fig. 11b, the loop gain for this system (the product of the forward and feedback gain terms) can be expressed as:

$$G_{loop}(s) = G_{e/a}(s) \bullet K_{pwm} \bullet G_m(s) \bullet G_i(s) \quad (14)$$

where

$G_{e/a}(s)$ = error amplifier gain
K_{pwm} = cascade of pwm and output H-bridge gain
$G_m(s)$ = cascade of motor winding impedance and H-bridge parasitic resistance
$G_i(s)$ = current sense resistor and sampling amplifier gain

The value of each of these terms can be determined from the Laplace transform diagram in Fig. 11b:

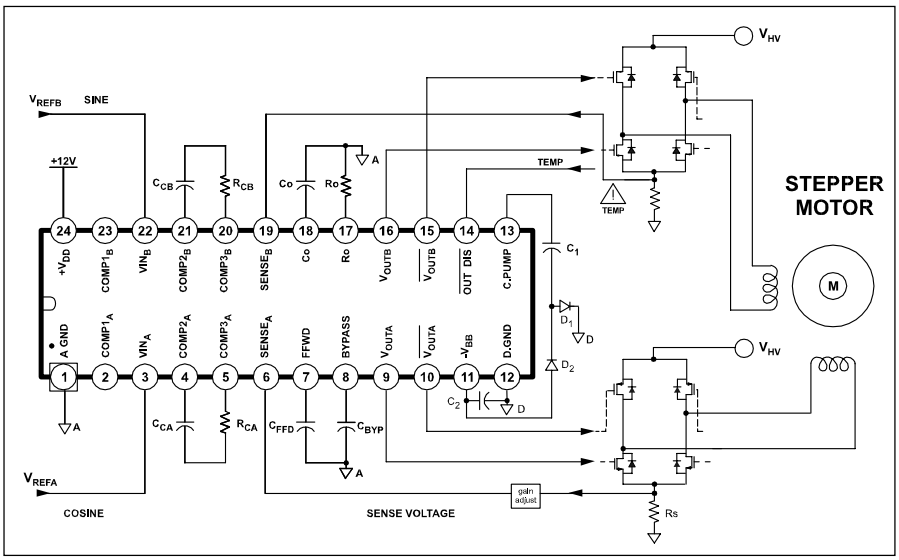


Fig. 10a Simplified Microstepping System

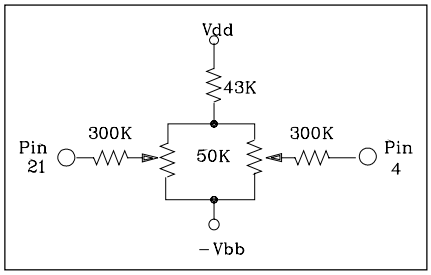


Fig. 10b Input Offset Adjust Circuit

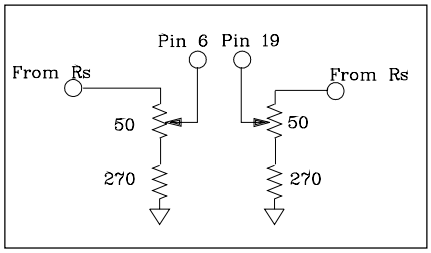


Fig. 10c Gain Adjust Circuit

$G_{e/a}(s) = (1 + sRC)/(sR_2C)$ (15)

$K_{pwm} = 2 \bullet V_{HV}/V_A$ (16)

$G_m(S) = 1/(sL_m + R_m + R_{sw} + R_s)$ (17)

$G_i(s) = 2 \bullet R_s$
(ignoring sampling effects) (18)

where:

R, C = external compensation components

R_2 = internal input resistor, typically 20 kΩ

V_{HV} = motor high voltage power supply

V_A = oscillator amplitude, typically 7 V

L_m = motor inductance

R_m = motor winding resistance

R_{sw} = power switch resistance

R_s = sense resistor

It is very important that the motor inductance value used in the analysis is not the value on the manufacturer's data sheet but rather the value observed in actual operation. The PWM action causes high frequency effects that can change the apparent small signal inductance significantly. These effects are dependent upon voltage as well as current and frequency. It is best to measure the observed current ripple at the motor supply voltage and switching frequency you expect to use and calculate the actual motor inductance using:

$$L_m = V_{HV}/((2 \bullet F_{osc})(I_{max}-I_{min})) \quad (19)$$

It is also important to note that both R_m and R_{sw} are temperature dependent. The motor winding resistance can increase by as much as 30 % at high temperatures, and if FETs are used as power devices, R_{sw} can increase to 2.2 times its value at room temperature.

Substituting equations 15 through 18 into equation 14 gives the expanded loop gain equation (eq. 20):

$$G_{loop}(s) = \frac{(1+sRC) \bullet 2Vhv \bullet 1 \bullet 2Rs}{sR_2C \bullet V_A \bullet (sL_m+R_m+R_s+R_{sw})}$$

which can be written as (eq.21):

$$G_{loop}(s) = \frac{4 \bullet V_{HV} \bullet R_s}{V_A(R_m+R_s \bullet R_{sw})} \bullet \frac{(1+RC)}{(sR_2 \bullet C)\,[1+sL_m/R_m+R_s+R_{sw})]}$$

Therefore the poles and zeros of the system are:

pole at DC, with a 0dB intercept of:

$4V_{HV}R_s/[V_AR_2C(R_m + R_s + R_{sw})]$

zero at 1/(R • C)

pole at $(R_m + R_s + R_{sw}) / L_m$

A simple Bode analysis can be performed to provide the necessary information to guarantee the stability of the loop. A stable system will result when the gain crossover occurs at a point where the loop phase shift is less than -180 degrees. The gain crossover point is defined as the frequency where the magnitude of $G_{loop}(s) = 1$ (0dB).

The Bode plot will show two figures of merit that give an indication of the behavior of the closed loop system, gain margin and phase margin. Gain margin is the amount of loop signal attenuation at the point where the loop phase has reached -180 degrees. It is a qualitative measure of how susceptible the loop is to noise outside its bandwidth. Phase margin is the amount of

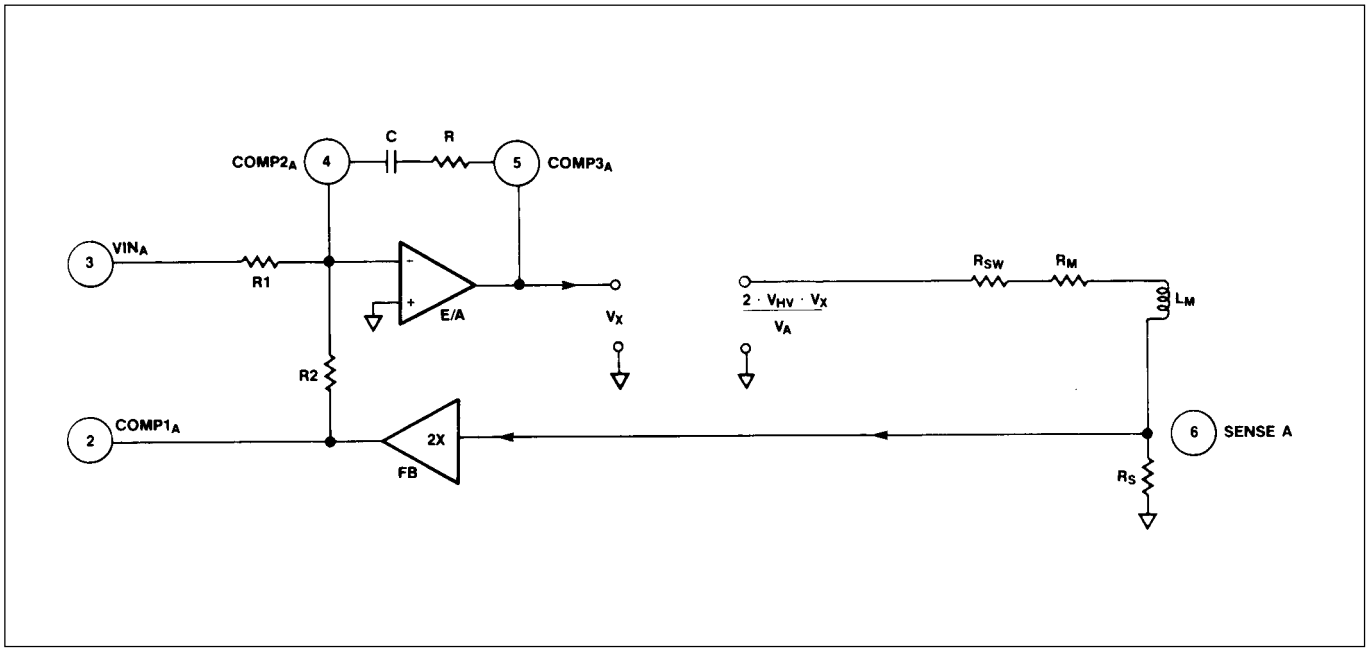


Fig. 11a Loop Compensation Block Diagram

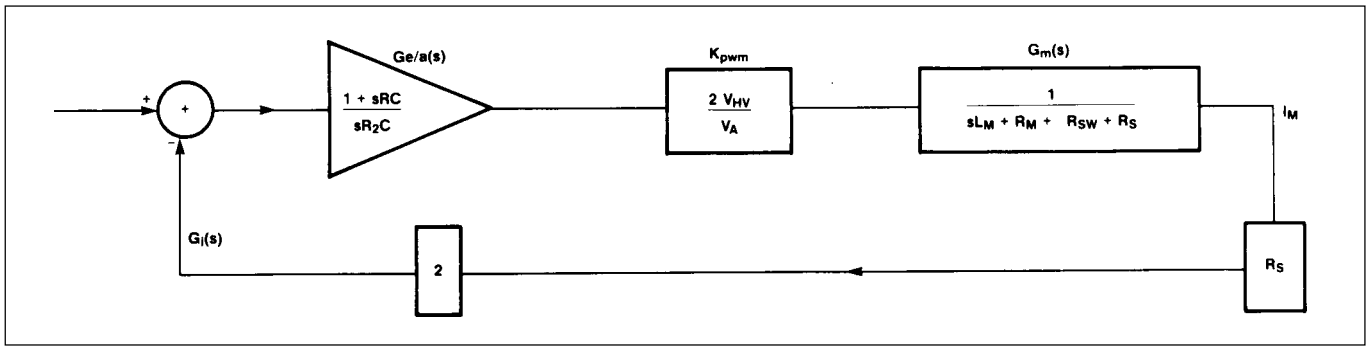
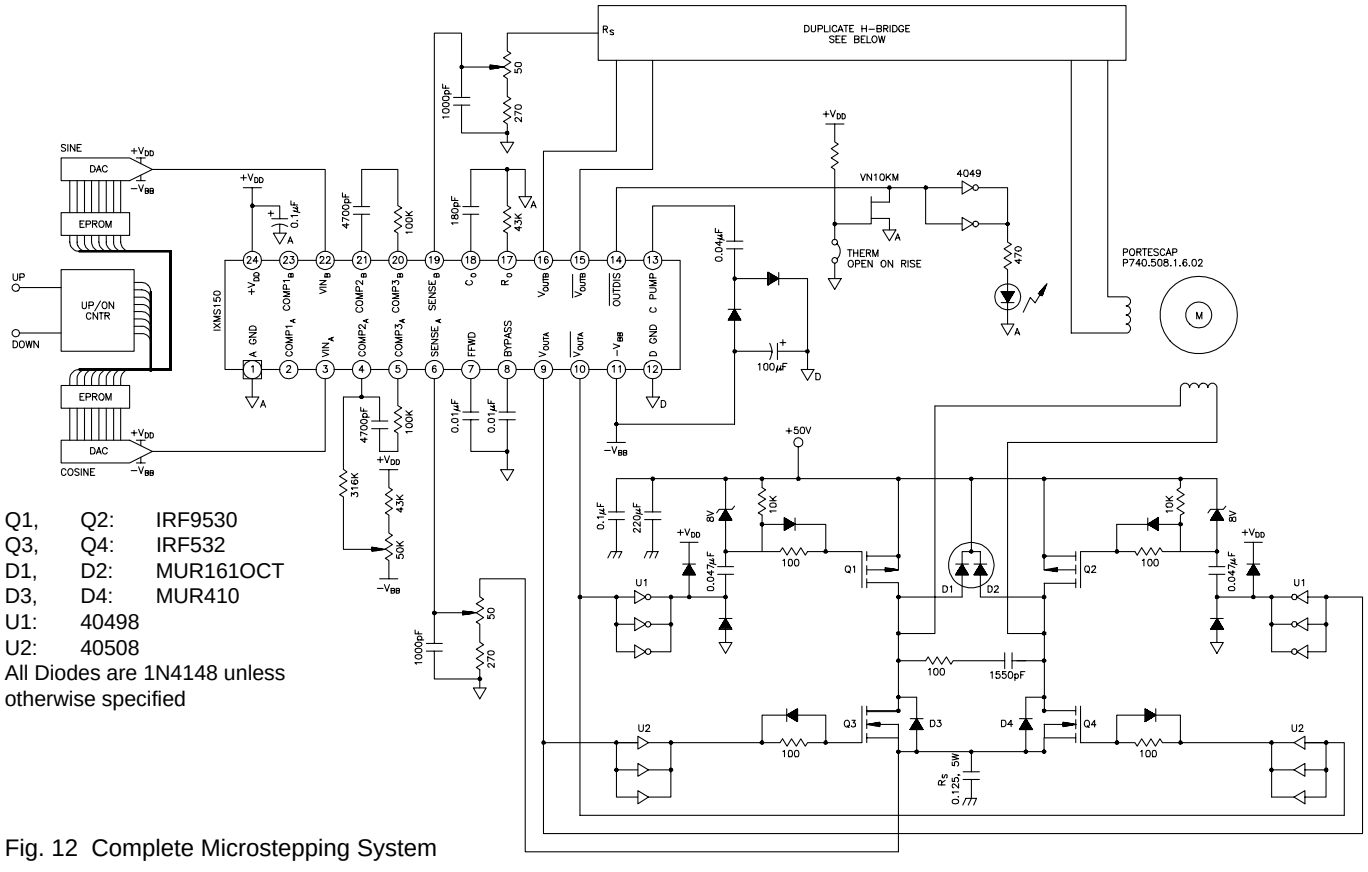


Fig. 11b Simplified laplace transform for stability analysis

phase shift left (i.e., 180 - (loop phase)) at the gain crossover. This number gives the most intuitive feeling for how the loop will respond to perturbations and variations in system parameters. Theoretically, a system with 1 degree of phase margin is stable. However, a step input to a system with small phase margin will cause an underdamped, ringly response or an oscillation that dies out after a long time.

In a step motor, this overshoot and ring in the current waveform is unacceptable. As the phase margin of a system is increased, the response to a step input slows down and the ringing is decreased. The response becomes more damped. In a practical system, the minimum acceptable phase margin is about 30 degrees. More than 90 degrees slows the system response with no significant improvement in stability. 60 degrees is usually considered optimal, if no other constraints exist.

In a PWM motor drive amplifier, there are several additional constraints that apply. Because the levels of voltage and current being switched are so high, synchronous noise appears everywhere and can degrade system performance. It is common to see apparent instabilities that are simply loop amplification of subharmonic switching transient noise. It is important to maintain at least 60 degrees of phase margin and to maintain as much gain margin as is practical. The PWM comparator delays, power stage gate drive delays, and the sampling technique used to generate the current feedback signal also account for significant phase delays when the switching frequency is high, or when the excitation approaches the switching frequency. For these reasons it is usually advisable to design for a calculated 60 to 90 degree phase margin because of the importance of the effects not accounted for in the linearized circuit model.



Q1, Q2: IRF9530
Q3, Q4: IRF532
D1, D2: MUR161OCT
D3, D4: MUR410
U1: 40498
U2: 40508
All Diodes are 1N4148 unless otherwise specified

Fig. 12 Complete Microstepping System