MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

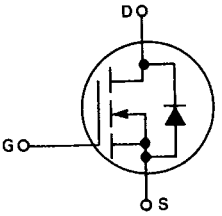
IRF530
IRF531
IRF532
IRF533

N-CHANNEL ENHANCEMENT-MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

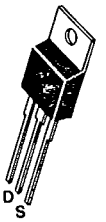
These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

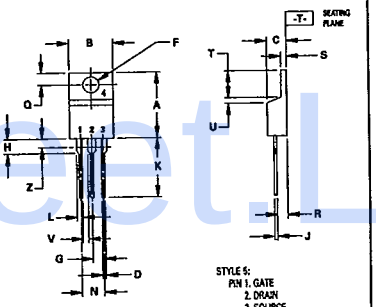
- Silicon Gate for Fast Switching Speeds
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™



Part Number	V_{DS}	$r_{DS(on)}$	I_D
IRF530	100 V	0.18 Ω	14 A
IRF531	60 V	0.18 Ω	14 A
IRF532	100 V	0.25 Ω	12 A
IRF533	60 V	0.25 Ω	12 A





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	IRF 530	IRF 531	IRF 532	IRF 533	Unit
Drain-Source Voltage	V_{DSS}	100	60	100	60	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	100	60	100	60	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Continuous Drain Current T_C = 25°C	I_D	14	14	12	12	Adc
Continuous Drain Current T_C = 100°C	I_D	9.0	9.0	8.0	8.0	Adc
Drain Current — Pulsed	I_{DM}	56	56	48	48	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6				Watts W/°C
Operating and Storage Temperature Range	T_J,T_{stg}	−55 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 1.67 62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300	°C

See the MTM12N10 Designer's Data Sheet for a complete set of design curves for this product.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA)	IRF530,532 IRF531,533	$V_{(BR)DSS}$	100 60	— —	— —	Vdc
Zero Gate Voltage Drain Current (V_{GS} = 0 V, V_{DS} = Rated V_{DSS}) (V_{GS} = 0 V, V_{DS} = 0.8 Rated V_{DSS}, T_C = 125°C)		I_{DSS}	— —	— —	0.25 1.0	mAdc
Forward Gate-Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)		I_{GSSF}	—	—	100	nAdc
Reverse Gate-Body Leakage Current (V_{GS} = −20 V, V_{DS} = 0)		I_{GSSR}	—	—	−100	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μA)		$V_{GS(th)}$	2.0	—	4.0	Vdc
On-State Drain Current (V_{DS} = 25 V, V_{GS} = 10 V)	IRF530,531 IRF532,533	$I_{D(on)}$	14 12	— —	— —	Adc
Static Drain-Source On-Resistance (V_{GS} = 10 V, I_D = 8.0 A)	IRF530,531 IRF532,533	$r_{DS(on)}$	— —	— —	0.18 0.25	Ohm
Forward Transconductance (V_{DS} = 15 V, I_D = 8.0 A)		g_{FS}	4.0	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	—	800	pF
Output Capacitance		C_{oss}	—	—	500	
Reverse Transfer Capacitance		C_{rss}	—	—	150	
SWITCHING CHARACTERISTICS* (T_J = 100°C)						
Turn-On Delay Time	V_{DD} = 36 V, I_D = 8.0 A Z_o = 15 Ω	$t_{d(on)}$	—	—	30	ns
Rise Time		t_r	—	—	75	
Turn-Off Delay Time		$t_{d(off)}$	—	—	40	
Fall Time		t_f	—	—	45	

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	2.3	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance	
Reverse Recovery Time		t_{rr}	360	ns

INTERNAL PACKAGE INDUCTANCE (TO-220)

	Symbol	Min	Typ	Max	Unit
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L_d	— —	3.5 4.5	— —	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad.)	L_s	—	7.5	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0 %.

FIGURE 1 — SWITCHING TEST CIRCUIT

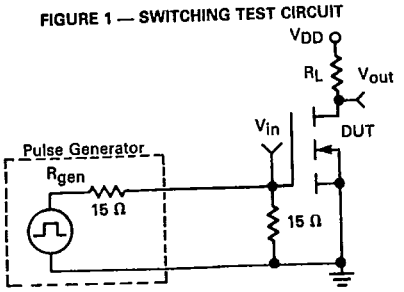


FIGURE 2 — SWITCHING WAVEFORMS