19-2941; Rev 1; 6/07

Low-Voltage, CMOS Analog Multiplexers/Switches

General Description

The MAX4581L/MAX4582L/MAX4583L are low-voltage, CMOS analog ICs configured as an 8-channel multiplexer (MAX4581L), two 4-channel multiplexers (MAX4582L), and three single-pole/double-throw (SPDT) switches (MAX4583L).

These CMOS devices operate with a +2V to +12V single supply. Each switch can handle rail-to-rail analog signals. Off-leakage current is only 2nA at +25°C.

All digital inputs have 0.8V to 2.0V logic thresholds to ensure TTL/CMOS-logic compatibility when using a +12V supply.

Applications

Audio and Video Signal Routing

Data-Acquisition Systems

Communications Circuits

Automotive

DSL Modem

Features

- **+3V Logic-Compatible Inputs (V_{IH} = 2.0V, V_{IL} = 0.8V)**
- **Guaranteed On-Resistance: 80Ω with +12V Supply**
- **Guaranteed 4Ω On-Resistance Match Between Channels**
- **Guaranteed Low Off-Leakage Current: 2nA at +25°C**
- **Guaranteed Low On-Leakage Current: 2nA at +25°C**
- **+2V to +12V Supply Operation**
- **TTL/CMOS-Logic Compatible**
- **Low Crosstalk: -96dB (MAX4582L)**
- **High Off-Isolation: -90dB**
- **Tiny 4mm × 4mm Thin QFN Package**
- **Pin Compatible with Industry-Standard 74HC4051/74HC4052/74HC4053 and MAX4051/MAX4052/MAX4053**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX4581LESE	-40°C to +85°C	16 Narrow SO
MAX4581LEEE	-40°C to +85°C	16 QSOP
MAX4581LETE	-40°C to +85°C	16 TQFN-EP* (4mm x 4mm)

Ordering Information continued at end of data sheet.

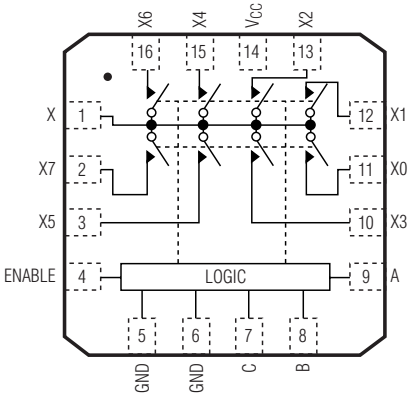
**EP = Exposed pad.*

Pin Configurations/Functional Diagrams

TOP VIEW

MAXIM

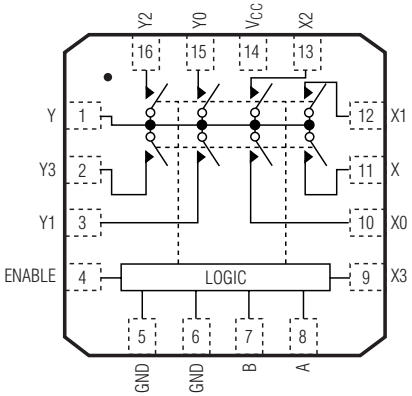
MAX4581L



THIN QFN

MAXIM

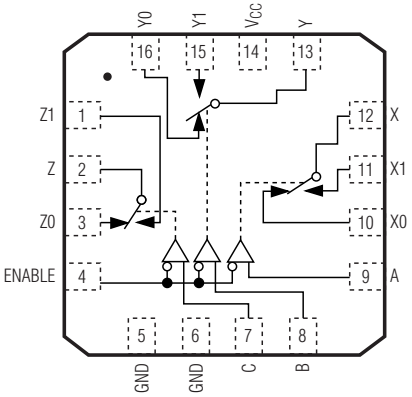
MAX4582L



THIN QFN

MAXIM

MAX4583L



THIN QFN

PIN CONFIGURATIONS/FUNCTIONAL DIAGRAMS CONTINUED AT END OF DATA SHEET.

Low-Voltage, CMOS Analog Multiplexers/Switches

ABSOLUTE MAXIMUM RATINGS

(All Voltages Referenced to GND, Unless Otherwise Noted.)
V_{CC} .....-0.3V to +13V
Voltage At Any Pin (Note 1) .....(GND - 0.3V) to (V_{CC} + 0.3V)
Continuous Current into Any Terminal .....±20mA
Peak Current X_, Y_ or Z_
(pulsed at 1ms, 10% duty cycle) .....±40mA
ESD per Method 3015.7 .....>2000V

Continuous Power Dissipation (T_A = +70°C)
16-Pin Narrow SO (derate 8.7mW/°C above +70°C) ...696mW
16-Pin QSOP (derate 8.3mW/°C above +70°C).....667mW
16-Pin Thin QFN (derate 16.9mW/°C above +70°C) .1349mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Voltages exceeding V_{CC} or GND on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +12V ±5%, $V_{\_H}$ = 2.0V, $V_{\_L}$ = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP (NOTE 3)	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	V_X, V_Y, V_Z			-40°C to +85°C	0		V_{CC}	V
Switch On-Resistance	R_{ON}	V_{CC} = 11.4V; I_X, I_Y, I_Z = 1mA; V_X, V_Y, V_Z = 10V		+25°C		50	80	Ω
				-40°C to +85°C			100	
Switch On-Resistance Match Between Channels	ΔR_{ON}	V_{CC} = 11.4V; I_X, I_Y, I_Z = 1mA; V_X, V_Y, V_Z = 10V (Note 4)		+25°C		1	4	Ω
				-40°C to +85°C			5	
Switch On-Resistance Flatness	$R_{FLAT(ON)}$	V_{CC} = 11.4V; I_X, I_Y, I_Z = 1mA; $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 1.5V, 6V, 10V (Note 5)		+25°C		5	12	Ω
				-40°C to +85°C			15	
X_, Y_, Z_ Off-Leakage	$I_{X\_(OFF)}$, $I_{Y\_(OFF)}$, $I_{Z\_(OFF)}$	V_{CC} = 12.6V; $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 1V, 10V; V_X, V_Y, V_Z = 10V, 1V (Note 6)		+25°C	-2		+2	nA
				-40°C to +85°C	-10		+10	
X, Y, Z Off-Leakage	$I_{X(OFF)}$, $I_{Y(OFF)}$, $I_{Z(OFF)}$	V_{CC} = 12.6V; $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 1V, 10V; V_X, V_Y, V_Z = 10V, 1V (Note 6)	MAX4581L	+25°C	-2		+2	nA
				-40°C to +85°C	-100		+100	
			MAX4582L/ MAX4583L	+25°C	-2		+2	
				-40°C to +85°C	-50		+50	
X, Y, Z On-Leakage	$I_{X(ON)}$, $I_{Y(ON)}$, $I_{Z(ON)}$	V_{CC} = 12.6V; V_X, V_Y, V_Z = 10V, 1V (Note 6)	MAX4581L	+25°C	-2		+2	nA
				-40°C to +85°C	-100		+100	
			MAX4582L/ MAX4583L	+25°C	-2		+2	
				-40°C to +85°C	-50		+50	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +12V ±5%, $V_{\_H}$ = 2.0V, $V_{\_L}$ = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP (NOTE 3)	MAX	UNITS
DIGITAL I/O (INH, ADD_)								
Logic Input High Threshold	V_{AH}, V_{BH}, V_{CH}, V_{ENABLE_H}			-40°C to +85°C		1.5	2.0	V
Logic Input Low Threshold	V_{AL}, V_{BL}, V_{CL}, V_{ENABLE_L}			-40°C to +85°C	0.8	1.5		V
Input Current High	I_{AH}, I_{BH}, I_{CH}, I_{ENABLE_H}	V_A, V_B, V_C, V_{ENABLE} = 2.0V		+25°C	-1		+1	µA
Input Current Low	I_{AL}, I_{BL}, I_{CL}, I_{ENABLE_L}	V_A, V_B, V_C, V_{ENABLE} = 0.8V		+25°C	-1		+1	µA
SWITCH DYNAMIC CHARACTERISTICS								
Enable Turn-On Time	t_{ON}	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 10V, R_L = 300Ω, C_L = 35pF, Figure 1		+25°C		100	200	ns
				-40°C to +85°C			200	
Enable Turn-Off Time	t_{OFF}	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 10V, R_L = 300Ω, C_L = 35pF, Figure 1		+25°C		40	100	ns
				-40°C to +85°C			150	
Address Transition Time	t_{TRANS}	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 10V, R_L = 300Ω, C_L = 35pF, Figure 2		+25°C		90	200	ns
				-40°C to +85°C			200	
Break-Before-Make Time	t_{BBM}	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 10V, R_L = 300Ω, C_L = 35pF, Figure 3		-40°C to +85°C		20		ns
Charge Injection (Note 7)	Q	C_L = 1nF, R_S = 0Ω, V_S = 0V, Figure 4		+25°C		0.5		pC
Input Off-Capacitance	$C_{X\_(OFF)}$, $C_{Y\_(OFF)}$, $C_{Z\_(OFF)}$	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 0V, f = 1MHz, Figure 5		+25°C		4		pF
Output Off-Capacitance	$C_{X(OFF)}$, $C_{Y(OFF)}$, $C_{Z(OFF)}$	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 0V, f = 1MHz, Figure 5	MAX4581L	+25°C		18		pF
			MAX4582L			10		
			MAX4583L			6		
Output On-Capacitance	$C_{X(OFF)}$, $C_{Y(OFF)}$, $C_{Z(OFF)}$	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 0V, f = 1MHz, Figure 5	MAX4581L	+25°C		25		pF
			MAX4582L			17		
			MAX4583L			12.5		

Low-Voltage, CMOS Analog Multiplexers/Switches

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +12V ±5%, $V_{\_H}$ = 2.0V, $V_{\_L}$ = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3)

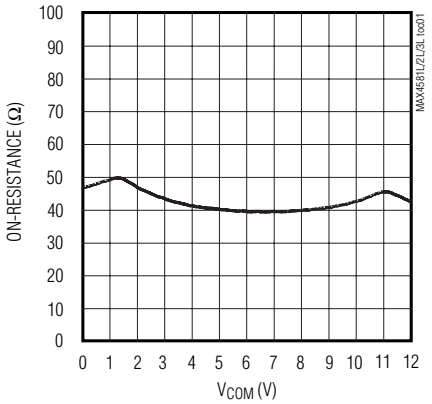
PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP (NOTE 3)	MAX	UNITS
Off-Isolation	V_{ISO}	R_L = 50Ω, f = 1MHz (Figure 7)	+25°C		-90		dB
Channel-to-Channel Crosstalk	V_{CT}	R_L = 50Ω, f = 1MHz (Figure 7)	+25°C		-96		dB
Total Harmonic Distortion	THD	R_L = 600Ω, $V_{X\_}$ or $V_{Y\_}$ or $V_{Z\_}$ = $5V_{P-P}$, f = 20Hz to 20kHz	+25°C		0.02		%
POWER SUPPLY							
Power-Supply Range	V_{CC}			2		12.6	V
Power-Supply Current	I_{CC}	V_{CC} = 12.6V; V_A, V_B, V_Z, V_{ENABLE} = V_{CC} or 0V	+25°C	-1		+1	µA
			-40°C to +85°C	-10		+10	

Note 2: Thin QFN packages are production tested at T_A = +85°C. Limits over temperature are guaranteed by design.
Note 3: The algebraic convention used in this data sheet is where the most negative value is the minimum column.
Note 4: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.
Note 5: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.
Note 6: Leakage parameters are 100% tested at the maximum-rated hot operating temperature and guaranteed by design at T_A = +25°C.
Note 7: Guaranteed by design, not production tested.

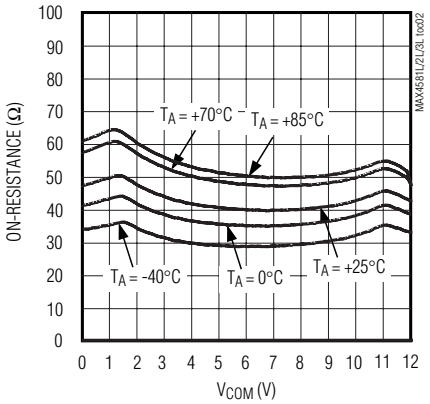
Typical Operating Characteristics

(V_{CC} = 12V, V_{EN} = GND, T_A = +25°C, unless otherwise noted.)

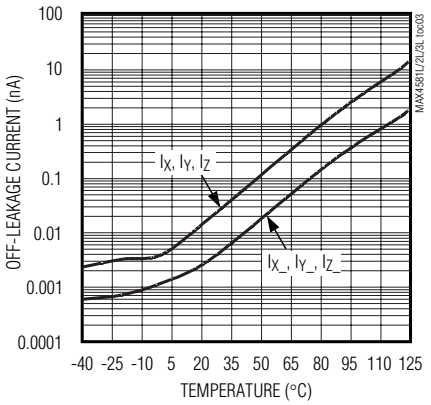
ON-RESISTANCE vs. V_{COM}



ON-RESISTANCE vs. V_{COM}



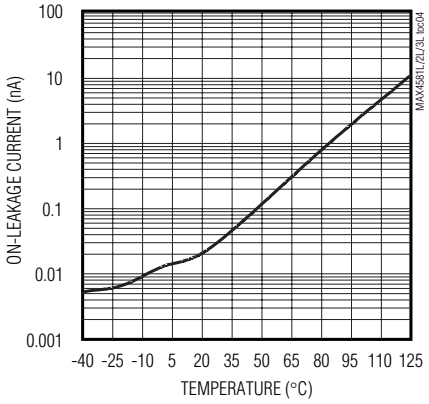
OFF-LEAKAGE CURRENT vs. TEMPERATURE



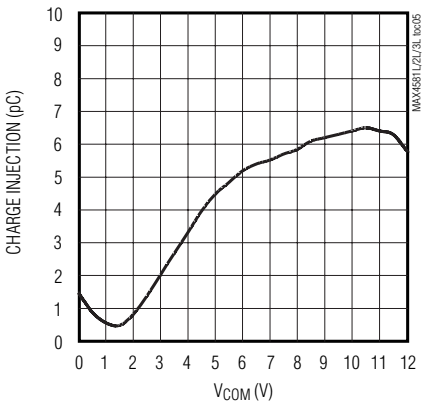
Typical Operating Characteristics (continued)

(V_{CC} = 12V, V_{EN} = GND, T_A = +25°C, unless otherwise noted.)

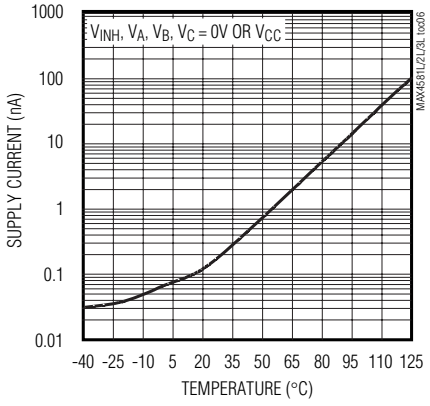
ON-LEAKAGE CURRENT vs. TEMPERATURE



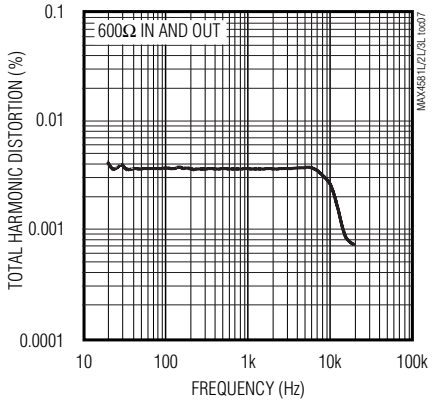
CHARGE INJECTION vs. V_{COM}



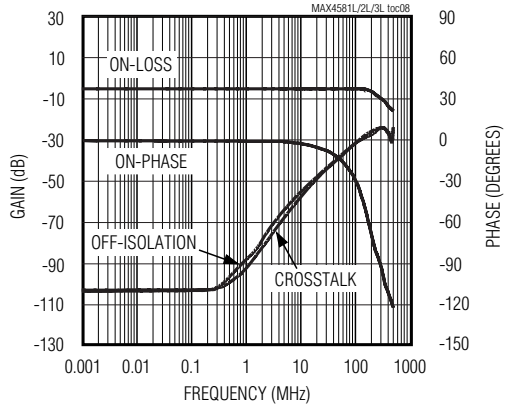
SUPPLY CURRENT vs. TEMPERATURE



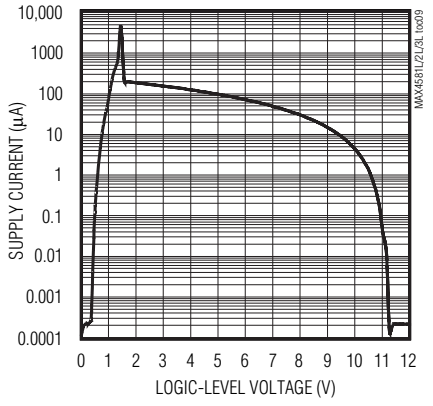
TOTAL HARMONIC DISTORTION vs. FREQUENCY



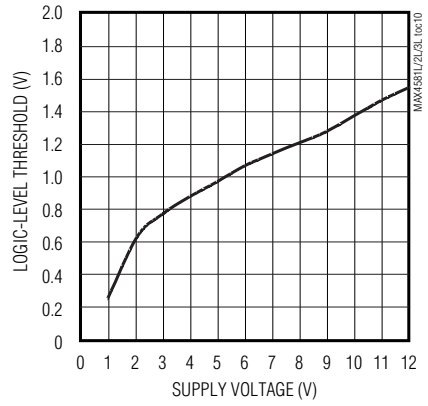
FREQUENCY RESPONSE



SUPPLY CURRENT vs. LOGIC-LEVEL VOLTAGE



LOGIC-LEVEL THRESHOLD vs. SUPPLY VOLTAGE



Low-Voltage, CMOS Analog Multiplexers/Switches

Pin Description

PIN						NAME	FUNCTION
MAX4581L		MAX4582L		MAX4583L			
SO/QSOP	QFN	SO/QSOP	QFN	SO/QSOP	QFN		
1, 2, 4, 5, 12–15	2, 3, 10–13, 15, 16	—	—	—	—	X0–X7	Analog Switch Inputs 0–7
3	1	13	11	14	12	X	Analog Switch X Output
6	4	6	4	6	4	Enable	Digital Enable Input. Drive enable low or connect to GND for normal operation.
7, 8	5, 6	7, 8	5, 6	7, 8	5, 6	GND	Ground. Connect to digital ground. (Analog signals have no ground reference; they are limited to V_{CC}.)
9	7	—	—	9	7	C	Digital Address C Input
10	8	9	7	10	8	B	Digital Address B Input
11	9	10	8	11	9	A	Digital Address A Input
16	14	16	14	16	14	V_{CC}	Positive Analog and Digital Supply Voltage Input. Bypass with a 0.1µF capacitor to GND.
—	—	11, 12, 14, 15,	9, 10, 12, 13	—	—	X0–X3	Analog Switch X Inputs 0–3
—	—	1, 2, 4, 5	2, 3, 15, 16	—	—	Y0–Y3	Analog Switch Y Inputs 0–3
—	—	3	1	15	13	Y	Analog Switch Y Output
—	—	—	—	13	11	X1	Analog Switch X Normally Open Input
—	—	—	—	12	10	X0	Analog Switch X Normally Closed Input
—	—	—	—	1	15	Y1	Analog Switch Y Normally Open Input
—	—	—	—	2	16	Y0	Analog Switch Y Normally Closed Input
—	—	—	—	3	1	Z1	Analog Switch Z Normally Open Input
—	—	—	—	5	3	Z0	Analog Switch Z Normally Closed Input
—	—	—	—	4	2	Z	Analog Switch Z Output
—	EP	—	EP	—	EP	Exposed Pad	Bottom of QFN package only. Contains an exposed pad that must be connected externally to V_{CC}.

Note: *Input and output pins are identical and interchangeable. Any may be considered an input or output; signals pass equally well in both directions.*

Detailed Description

The MAX4581L/MAX4582L/MAX4583L are low-voltage, CMOS analog ICs that operate from a single supply of +2V to +12V. The MAX4581L is configured as an 8-channel multiplexer, the MAX4582L as two 4-channel multiplexers, and the MAX4583L as three single-pole/double-throw (SPDT) switches. These devices can handle rail-to-rail analog signals with only 2nA of off-leakage current at +25°C.

The MAX4581L/MAX4582L/MAX4583L are TTL/CMOS-logic compatible with 0.8V to 2.0V logic thresholds for all digital inputs when operating from a +12V supply.

Applications Information

Power-Supply Considerations

The MAX4581L/MAX4582L/MAX4583Ls' construction is typical of most CMOS analog switches. The supply input, V_{CC}, is used to power the internal CMOS switches and sets the limit of the analog voltage on any switch. Reverse ESD protection diodes are internally connected between each analog signal pin and both V_{CC} and GND. If any analog signal exceeds V_{CC} or goes below GND, one of these diodes conducts. During normal operation, these reverse-biased ESD diodes leak, causing the only current drawn from V_{CC} or GND. Virtually all the analog leakage current comes from the ESD diodes. Although the ESD diodes on a given signal pin are identical, and therefore fairly well balanced, they are reverse biased differently by either V_{CC} or GND and the analog signal. This means that leakage varies as the analog signal varies. The difference in the two diodes' leakage to V_{CC} and GND constitutes the analog signal-path leakage current. Because there is no connection between the analog signal paths and GND, all analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. Because of this, both sides of a given switch can show leakage currents of either the same or opposite polarity.

V_{CC} and GND power the internal logic and logic-level translators, and set both the input and output logic limits. The logic-level translators convert the logic levels into switched V_{CC} and GND signals to drive the gates of the analog switches. This drive signal is the only connection between the logic supplies (and signals) and the analog supplies. The logic-level thresholds are TTL/CMOS compatible when V_{CC} is +12V.

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices. Always sequence V_{CC} first, followed by the logic inputs and analog signals.

Pin Nomenclature

The MAX4581L/MAX4582L/MAX4583L are pin compatible with the industry-standard 74HC4051/74HC4052/74HC4053 and the MAX4051/MAX4052/MAX4053.

Table 1. Truth Table/Switch Programming

ENABLE INPUT	SELECT INPUTS			ON SWITCHES		
	C*	B	A	MAX4581L	MAX4582L	MAX4583L
H	X	X	X	All switches open	All switches open	All switches open
L	L	L	L	X–X0	X–X0, Y–Y0	X–X0, Y–Y0, Z–Z0
L	L	L	H	X–X1	X–X1, Y–Y1	X–X1, Y–Y0, Z–Z0
L	L	H	L	X–X2	X–X2, Y–Y2	X–X0, Y–Y1, Z–Z0
L	L	H	H	X–X3	X–X3, Y–Y3	X–X1, Y–Y1, Z–Z0
L	H	L	L	X–X4	X–X0, Y–Y0	X–X0, Y–Y0, Z–Z1
L	H	L	H	X–X5	X–X1, Y–Y1	X–X1, Y–Y0, Z–Z1
L	H	H	L	X–X6	X–X2, Y–Y2	X–X0, Y–Y1, Z–Z1
L	H	H	H	X–X7	X–X3, Y-Y3	X–X1, Y–Y1, Z–Z1

X = *Don't care.*

**C not present on MAX4582L.*

Note: *Input and output pins are identical and interchangeable. Either may be considered an input or output; signals pass equally well in either direction.*

Low-Voltage, CMOS Analog Multiplexers/Switches

Test Circuits/Timing Diagrams

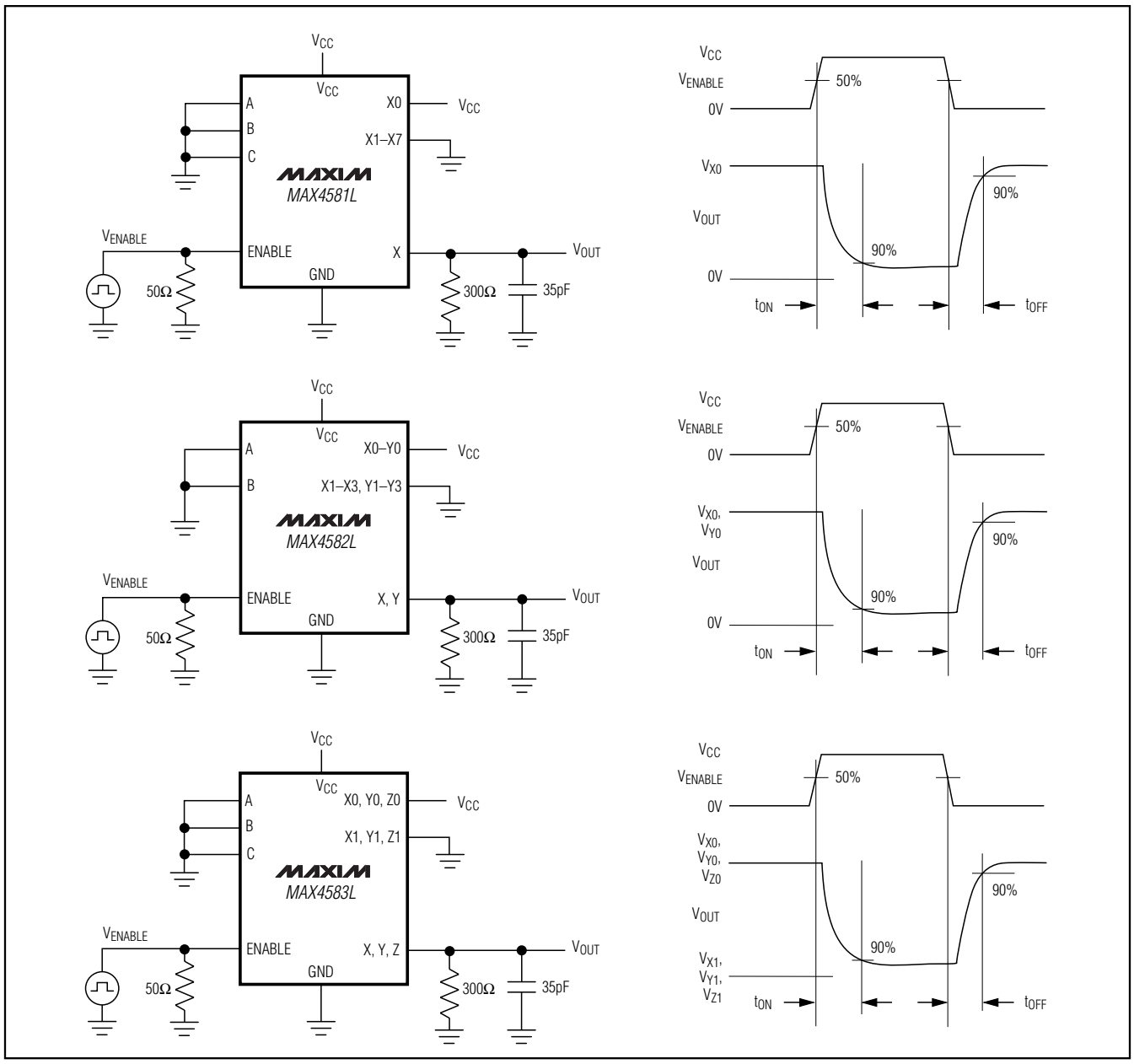


Figure 1. Enable Switching Times

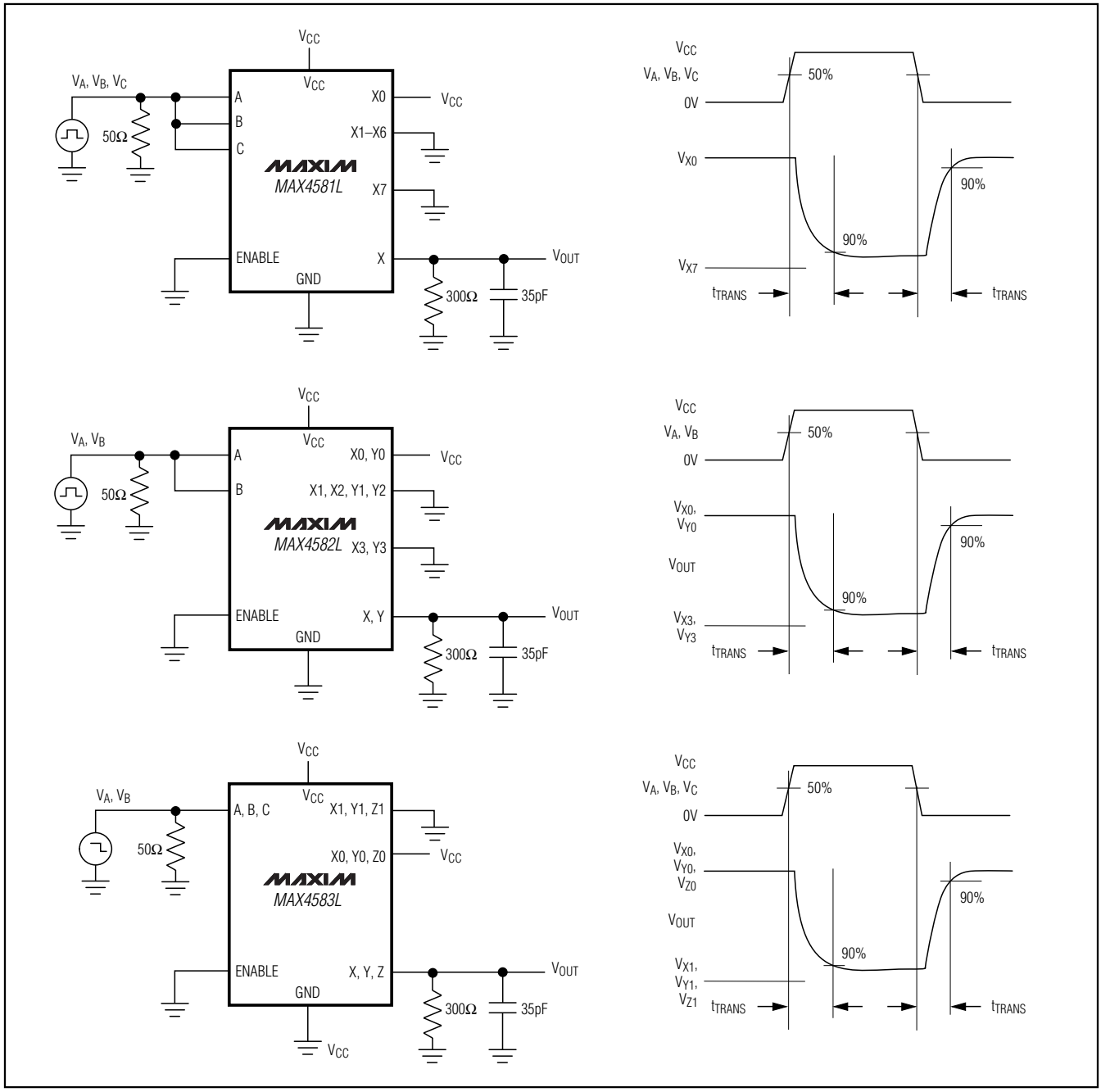


Figure 2. Address Transition Time

Low-Voltage, CMOS Analog Multiplexers/Switches

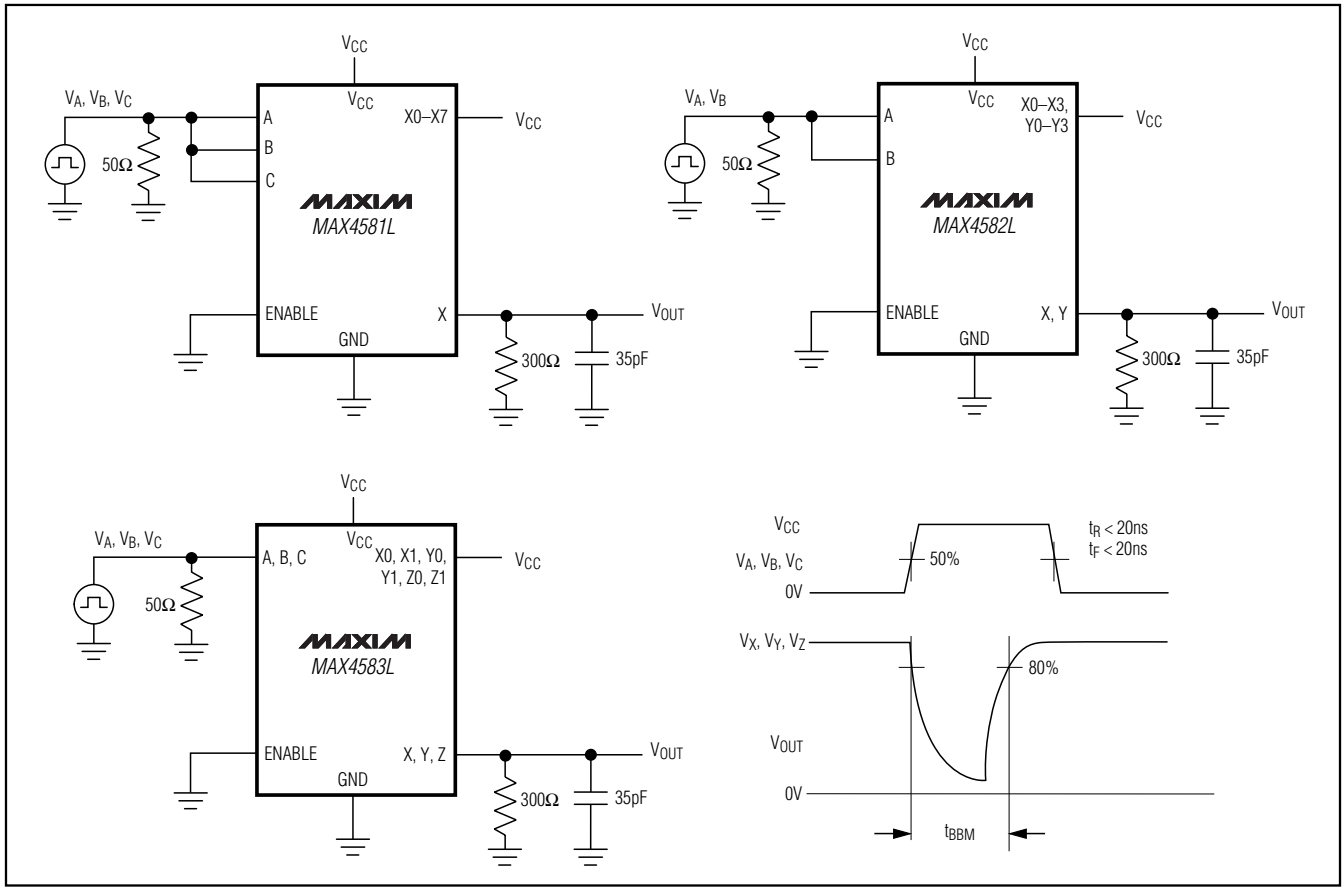


Figure 3. Break-Before-Make Interval

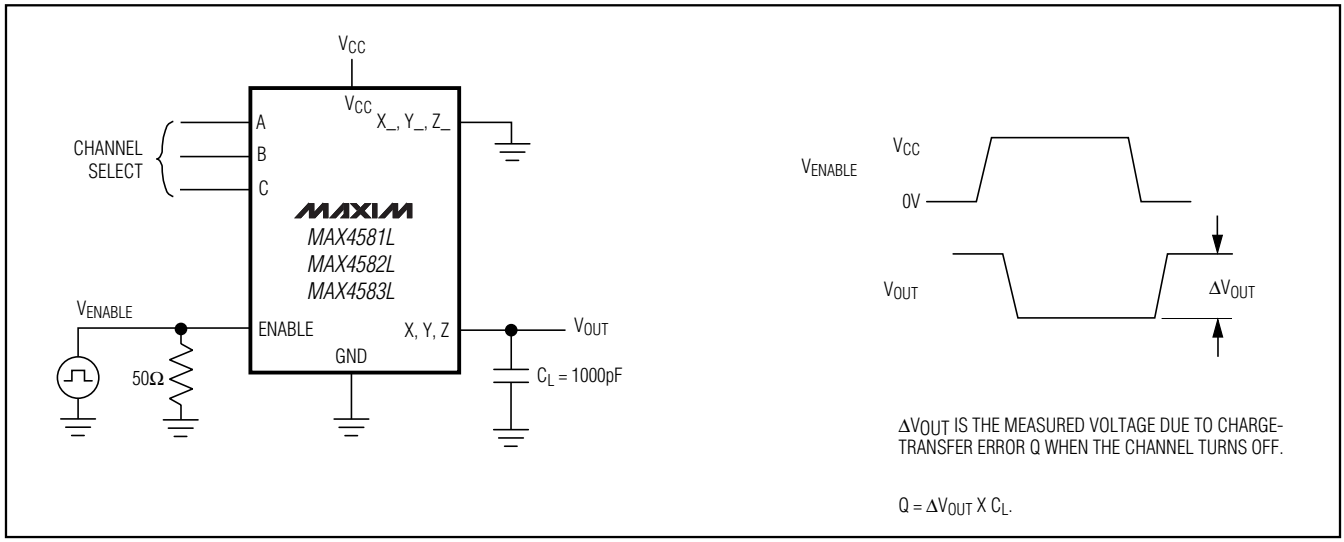


Figure 4. Charge Injection

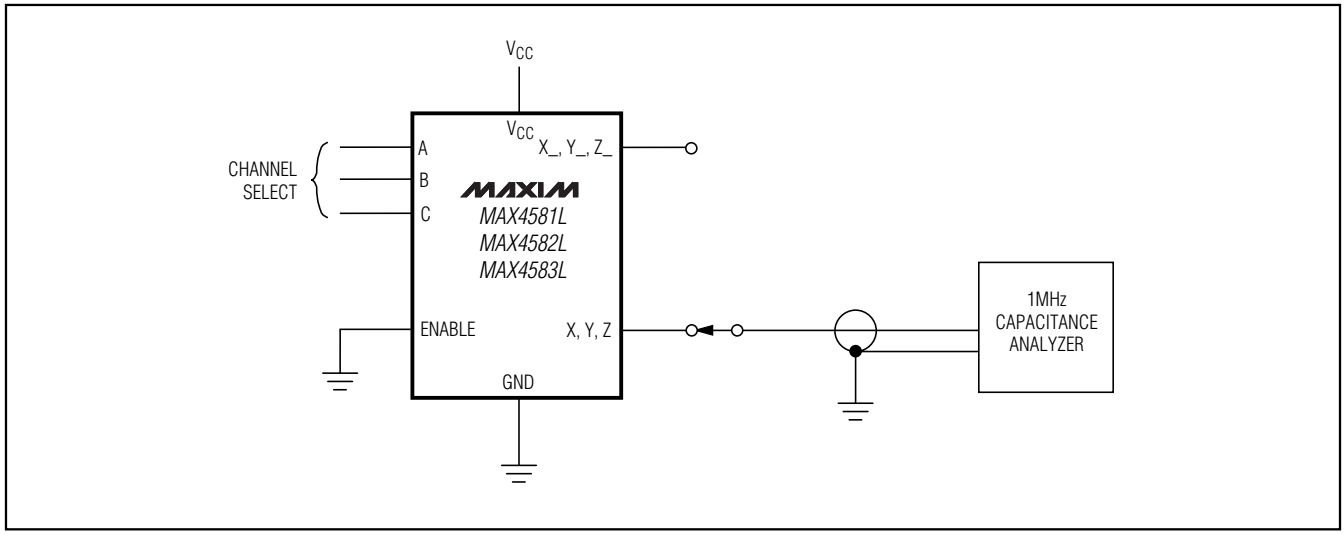
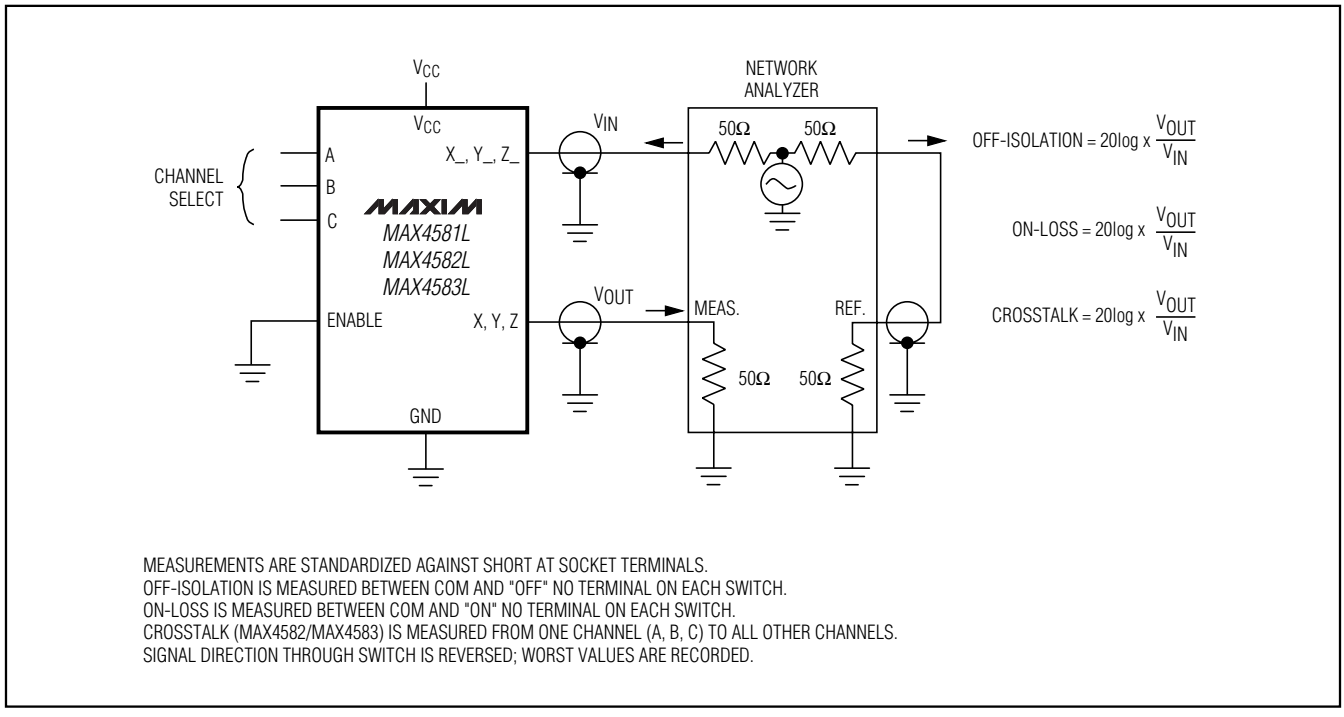


Figure 5. NO/COM Capacitance



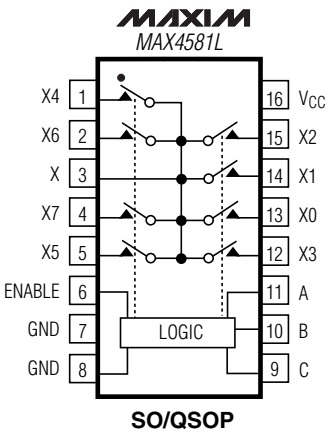
MEASUREMENTS ARE STANDARDIZED AGAINST SHORT AT SOCKET TERMINALS.
OFF-ISOLATION IS MEASURED BETWEEN COM AND "OFF" NO TERMINAL ON EACH SWITCH.
ON-LOSS IS MEASURED BETWEEN COM AND "ON" NO TERMINAL ON EACH SWITCH.
CROSSTALK (MAX4582/MAX4583) IS MEASURED FROM ONE CHANNEL (A, B, C) TO ALL OTHER CHANNELS.
SIGNAL DIRECTION THROUGH SWITCH IS REVERSED; WORST VALUES ARE RECORDED.

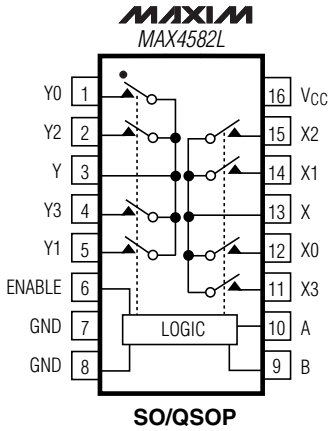
Figure 6. Off-Isolation, On-Loss, and Crosstalk

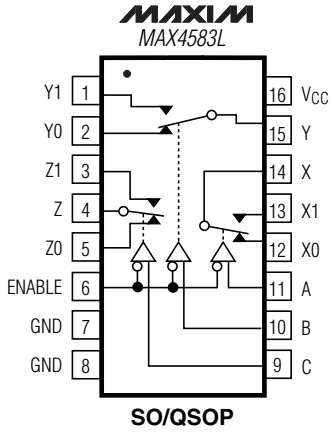
Low-Voltage, CMOS Analog Multiplexers/Switches

Pin Configurations/Functional Diagrams (continued)

TOP VIEW







Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
MAX4582LESE	-40°C to +85°C	16 Narrow SO
MAX4582LEEE	-40°C to +85°C	16 QSOP
MAX4582LETE	-40°C to +85°C	16 TQFN-EP* (4mm x 4mm)
MAX4583LESE	-40°C to +85°C	16 Narrow SO
MAX4583LEEE	-40°C to +85°C	16 QSOP
MAX4583LETE	-40°C to +85°C	16 TQFN-EP* (4mm x 4mm)

**EP = Exposed pad.*

Chip Information

TRANSISTOR COUNT: 219

PROCESS: CMOS

Revision History

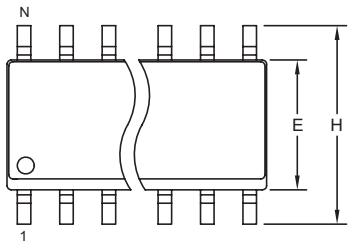
Pages changed at Rev 1: 1, 6, 12, 16

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

SOICN .EPS

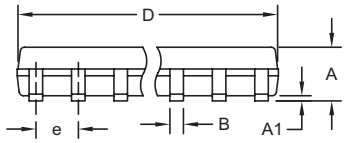
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27



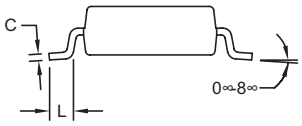
TOP VIEW

VARIATIONS:

	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE:

PACKAGE OUTLINE, .150" SOIC

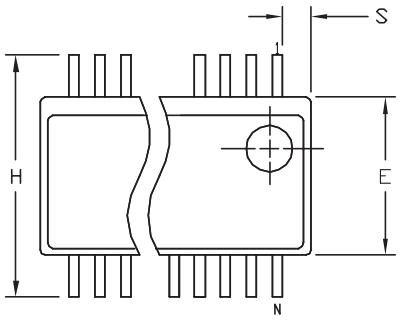
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0041	B	1/1

Low-Voltage, CMOS Analog Multiplexers/Switches

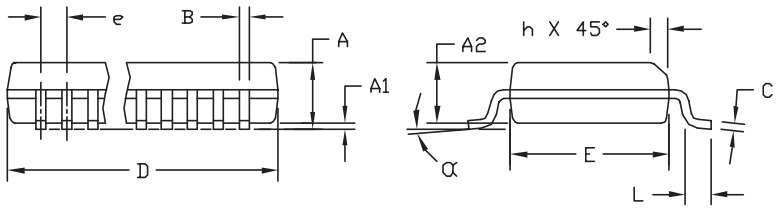
Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

QSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.053	.069	1.35	1.75
A1	.004	.010	.102	.254
A2	.049	.065	1.245	1.651
B	.008	.012	0.20	0.30
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°



VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AB
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AD
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AE
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AF
S	.0250	.0300	0.635	0.762		

NOTES:
1). D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2). MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3). CONTROLLING DIMENSIONS: INCHES.
4). MEETS JEDEC MO137.

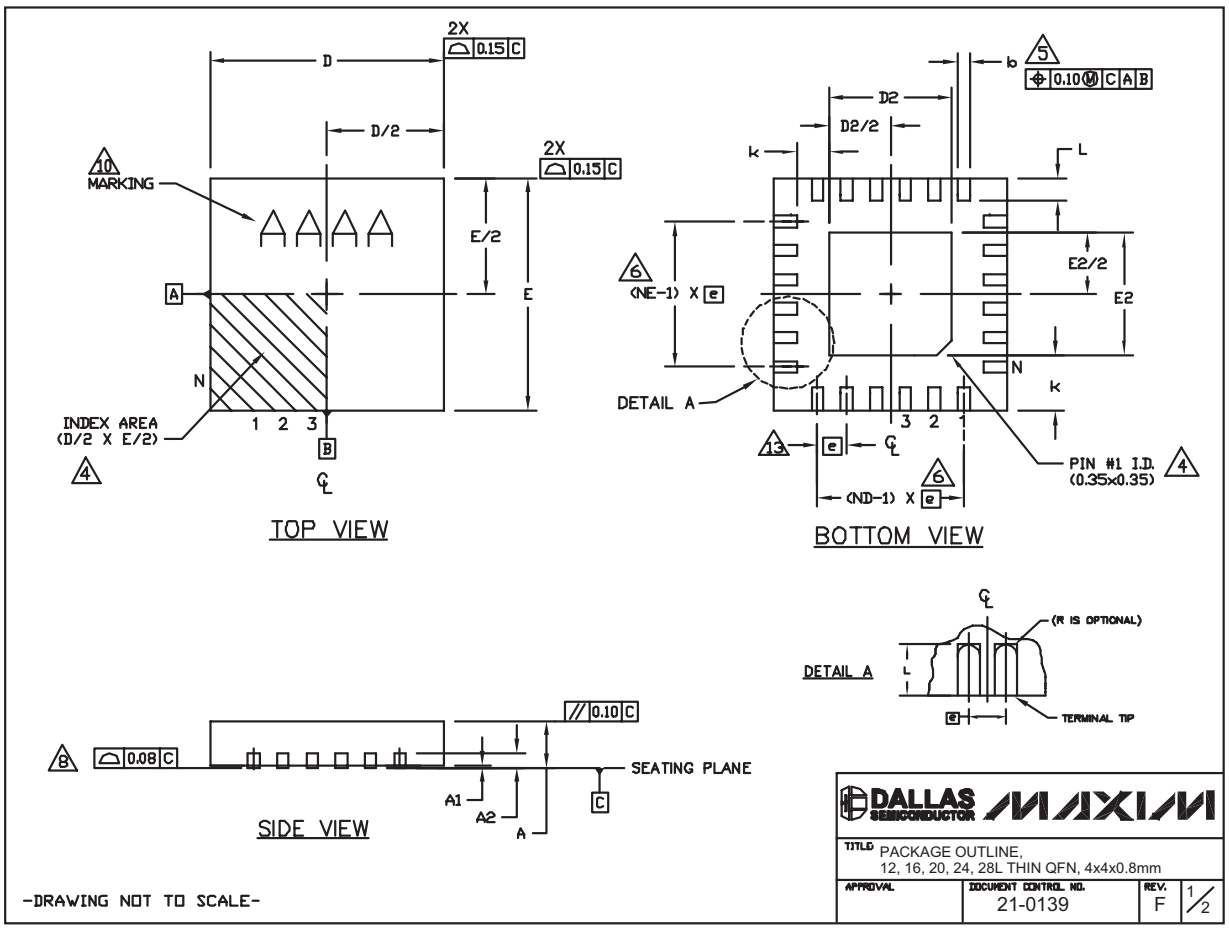
DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, QSOP .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0055	F	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



Low-Voltage, CMOS Analog Multiplexers/Switches

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS															
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	12			16			20			24			28		
ND	3			4			5			6			7		
NE	3			4			5			6			7		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm.
12. WARPAGE SHALL NOT EXCEED 0.10mm.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
15. ALL DIMENSIONS ARE THE SAME FOR LEADED & PbFREE PARTS.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE	PACKAGE OUTLINE, 12, 16, 20, 24, 28L THIN QFN, 4x4x0.8mm			
APPROVAL		DOCUMENT CONTROL NO. 21-0139	REV. F	2/2