NE5517/5517A
Dual Operational Transconductance Amplifier

Product Specification

DESCRIPTION

The NE5517 contains two current-controlled transconductance amplifiers, each with a differential input and push-pull output. The NE5517 offers significant design and performance advantages over similar devices for all types of programmable gain applications. Circuit performance is enhanced through the use of linearizing diodes at the inputs which enable a 10dB signal-to-noise improvement referenced to 0.5% THD. The NE5517 is suited for a wide variety of industrial and consumer applications and is recommended as the preferred circuit in the Dolby* HX (Headroom Extension) system.

Constant impedance buffers on the chip allow general use of the NE5517. These buffers are made of Darlington transistor and a biasing network which changes bias current in dependence of I_{ABC}.

Therefore, changes of output offset voltages are almost eliminated. This is an advantage of the NE5517 compared to LM13600. With the LM13600, a burst in the bias current I_{ABC} guides to an audible offset voltage change at the output. With the constant impedance buffers of the NE5517 this effect can be avoided and makes this circuit preferable for high quality audio applications.

FEATURES

- **Constant impedance buffers**
- **ΔV_{BE} of buffer is constant with amplifier I_{BIAS} change**
- **Pin compatible with LM13600**
- **Excellent matching between amplifiers**
- **Linearizing diodes**
- **High output signal-to-noise ratio**

APPLICATIONS

- **Multiplexers**
- **Timers**
- **Electronic music synthesizers**
- **Dolby™ HX Systems**
- **Current-controlled amplifiers, filters**
- **Current-controlled oscillators, impedances**

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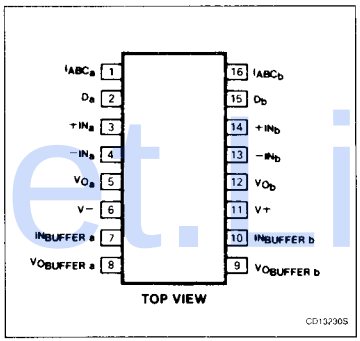
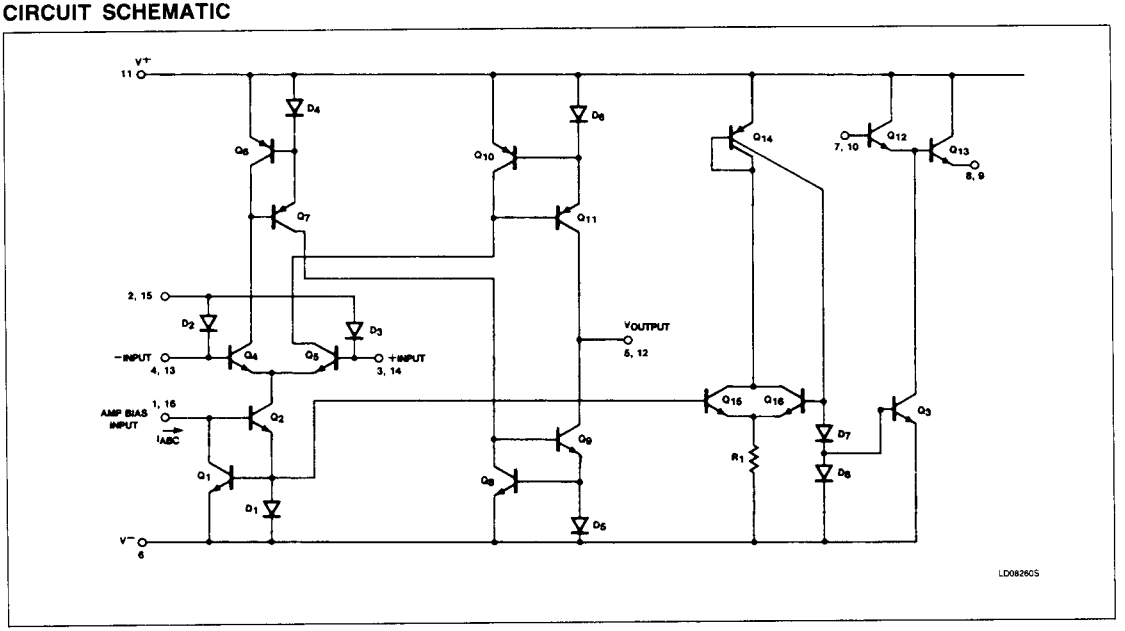
PIN CONFIGURATION



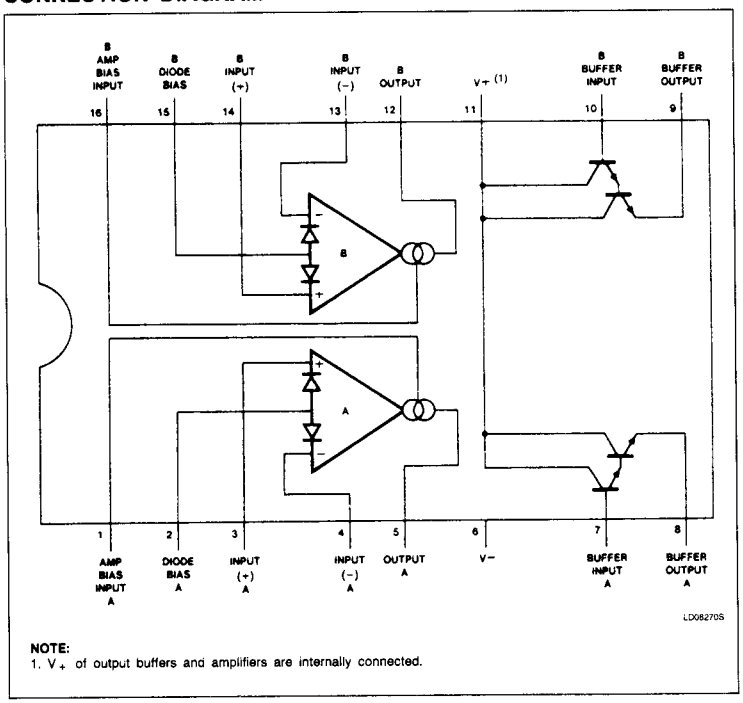
PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	I_{ABC}	Amplifier bias input A
2	D	Diode bias A
3	+IN	Non-inverting input A
4	−IN	Inverting input A
5	V_O	Output A
6	V−	Negative supply
7	IN_{BUFFER}	Buffer input A
8	VO_{BUFFER}	Buffer output A
9	VO_{BUFFER}	Buffer output B
10	IN_{BUFFER}	Buffer input B
11	V+	Positive supply
12	V_O	Output B
13	−IN	Inverting input B
14	+IN	Non-inverting input B
15	D	Diode bias B
16	I_{ABC}	Amplifier bias input B

CIRCUIT SCHEMATIC



CONNECTION DIAGRAM



NOTE:
1. V_+ of output buffers and amplifiers are internally connected.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	NE5517N
16-Pin Plastic DIP	0 to +70°C	NE5517AN
16-Pin SO DIP	0 to +70°C	NE5517D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage[1] NE5517 NE5517A	 36 V_{DC} or ±18 44 V_{DC} or ±22	 V V
P_D	Power dissipation, T_A = 25°C (still air)[2] NE5517N, NE5517AN NE5517D	 1500 1125	 mW mW
V_{IN}	Differential input voltage	±5	V
I_D	Diode bias current	2	mA
I_{ABC}	Amplifier bias current	2	mA
I_{SC}	Output short-circuit duration	Indefinite	
I_{OUT}	Buffer output current[3]	20	mA
T_A	Operating temperature range NE5517N, NE5517AN	 0°C to +70	 °C
V_{DC}	DC input voltage	$+V_S$ to $-V_S$	
T_{STG}	Storage temperature range	−65°C to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:
1. For selections to a supply voltage above ±22V, contact factory.
2. The following derating factors should be applied above 25°C:
   N package at 12.0mW/°C
   D package at 9.0mW/°C
3. Buffer output current should be limited so as to not exceed package dissipation.

DC ELECTRICAL CHARACTERISTICS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	NE5517			NE5517A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage			0.4	5		0.4	2	mV
		Over temperature range						5	mV
		I_{ABC} 5μA		0.3	5		0.3	2	mV
	$\Delta V_{OS}/\Delta T$	Avg. TC of input offset voltage		7			7		μV/°C
	V_{OS} including diodes	Diode bias current (I_D) = 500μA		0.5	5		0.5	2	mV
V_{OS}	Input offset change	5μA ≤ I_{ABC} ≤ 500μA		0.1			0.1	3	mV
I_{OS}	Input offset current			0.1	0.6		0.1	0.6	μA
	$\Delta I_{OS}/\Delta T$	Avg. TC of input offset current		0.001			0.001		μA/°C
I_{BIAS}	Input bias current			0.4	5		0.4	5	μA
		Over temperature range		1	8		1	7	μA
	$\Delta I_B/\Delta T$	Avg. TC of input current		0.01			0.01		μA/°C

DC ELECTRICAL CHARACTERISTICS[1] (Continued)

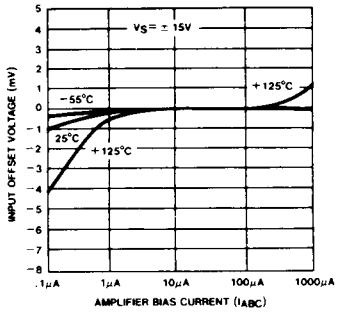
SYMBOL	PARAMETER	TEST CONDITIONS	NE5517			NE5517A			UNIT
			Min	Typ	Max	Min	Typ	Max	
g_M	Forward transconductance	Over temperature range	6700 5400	9600	13000	7700 4000	9600	12000	μmho μmho
	g_M tracking			0.3			0.3		dB
I_{OUT}	Peak output current	$R_L = 0$, $I_{ABC} = 5\mu A$ $R_L = 0$, $I_{ABC} = 500\mu A$ $R_L = 0$,	 350 300	5 500	 650	3 350 300	5 500	7 650	μA μA μA
V_{OUT}	Peak output voltage Positive Negative	 $R_L = \infty$, $5\mu A \leq I_{ABC} \leq 500\mu A$ $R_L = \infty$, $5\mu A \leq I_{ABC} \leq 500\mu A$	 +12 −12	 +14.2 −14.4		 +12 −12	 +14.2 −14.4		 V V
I_{CC}	Supply current	$I_{ABC} = 500\mu A$, both channels		2.6	4		2.6	4	mA
	V_{OS} sensitivity Positive Negative	 $\Delta V_{OS}/\Delta V+$ $\Delta V_{OS}/\Delta V-$		 20 20	 150 150		 20 20	 150 150	 μV/V μV/V
CMRR	Common-mode rejection ration		80	110		80	110		dB
	Common-mode range		±12	±13.5		±12	±13.5		V
	Crosstalk	Referred to input[2] 20Hz < f < 20kHz		100			100		dB
I_{IN}	Differential input current	$I_{ABC} = 0$, input = ±4V		0.02	100		0.02	10	nA
	Leakage current	$I_{ABC} = 0$ (Refer to test circuit)		0.2	100		0.2	5	nA
R_{IN}	Input resistance		10	26		10	26		kΩ
B_W	Open-loop bandwidth			2			2		MHz
SR	Slew rate	Unity gain compensated		50			50		V/μs
IN_{BUFFER}	Buff. input current	5		0.4	5		0.4	5	μA
VO_{BUFFER}	Peak buffer output voltage	5	10			10			V
	ΔV_{BE} of buffer	Refer to Buffer V_{BE} test[3] circuit		0.5	5		0.5	5	mV

NOTES:

1. These specifications apply for $V_S = \pm 15V$, $T_A = 25°C$, amplifier bias current (I_{ABC}) = 500μA, Pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.
2. These specifications apply for $V_S = \pm 15V$, $I_{ABC} = 500\mu A$, $R_{OUT} = 5k\Omega$ connected from the buffer output to $-V_S$ and the input of the buffer is connected to the transconductance amplifier output.
3. $V_S = \pm 15$, $R_{OUT} = 5k\Omega$ connected from Buffer output to $-V_S$ and $5\mu A \leq I_{ABC} \leq 500\mu A$.

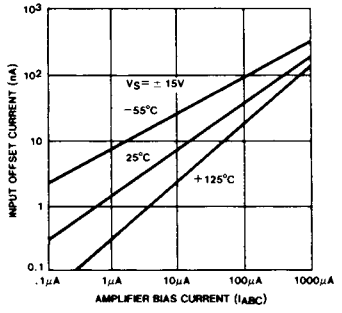
TYPICAL PERFORMANCE CHARACTERISTICS

Input Offset Voltage



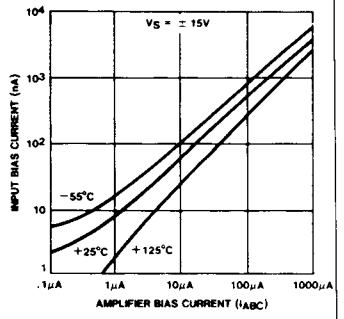
OP19330S

Input Offset Current



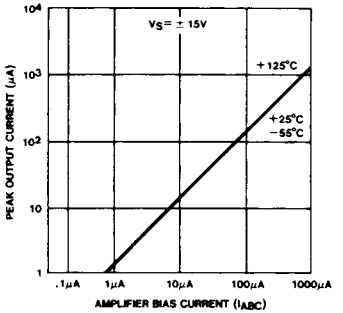
OP19340S

Input Bias Current



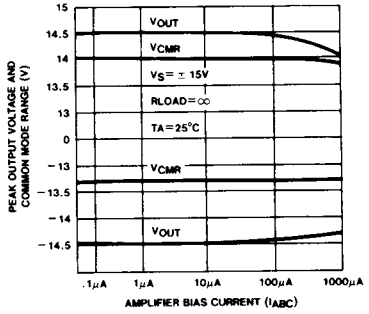
OP19350S

Peak Output Current



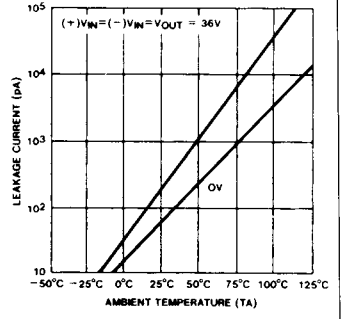
OP19360S

Peak Output Voltage and Common-Mode Range



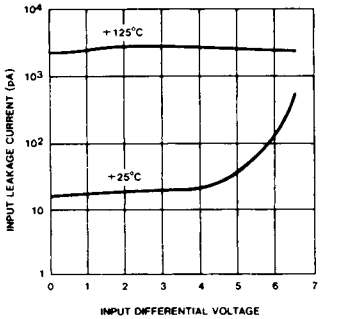
OP19370S

Leakage Current



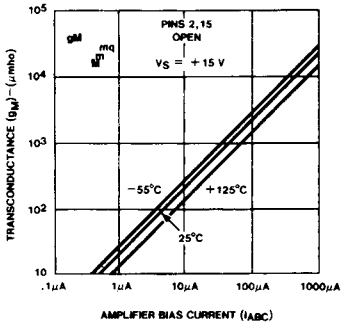
OP19380S

Input Leakage



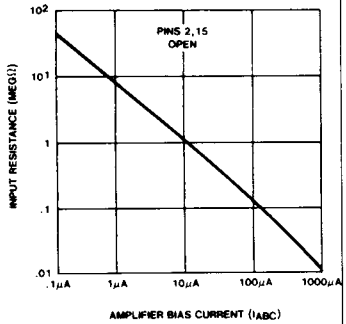
OP19390S

Transconductance



OP19401S

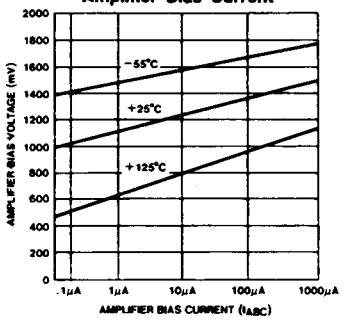
Input Resistance



OP19410S

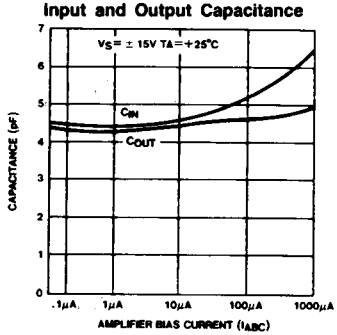
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Amplifier Bias Voltage vs Amplifier Bias Current



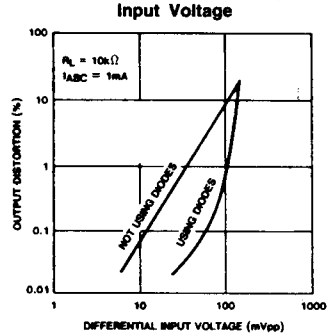
OP19420S

Input and Output Capacitance



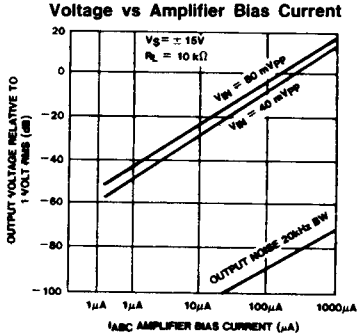
OP19430S

Distortion vs Differential Input Voltage



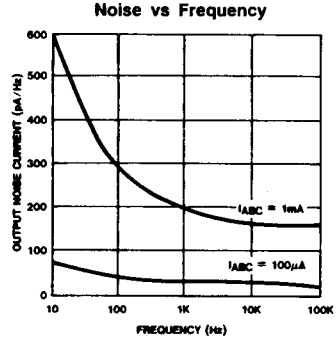
OP19440S

Voltage vs Amplifier Bias Current



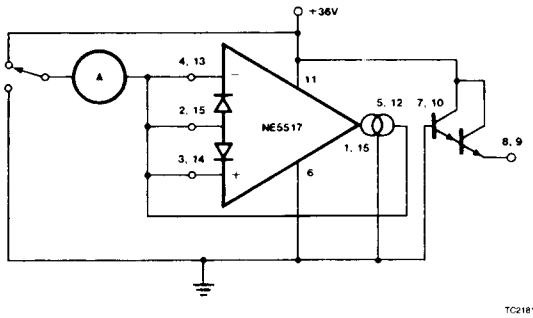
OP19460S

Noise vs Frequency

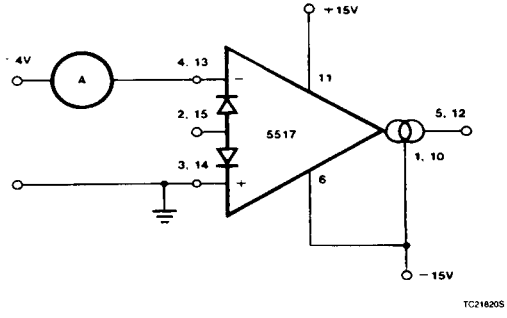


O19460S

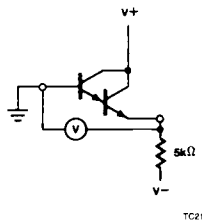
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



Leakage Current Test Circuit

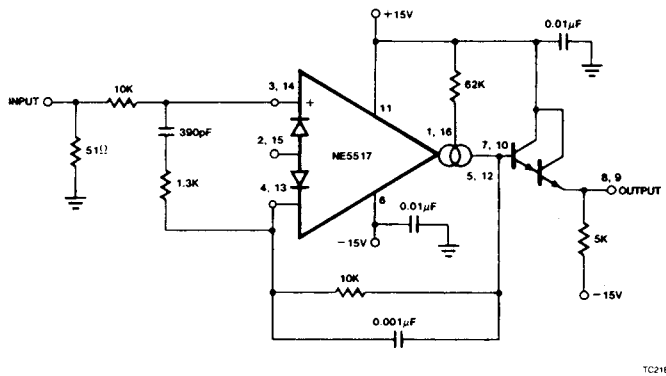


Differential Input Current Test Circuit



Buffer V_{BE} Test Circuit

APPLICATIONS



Unity Gain Follower

CIRCUIT DESCRIPTION

The circuit schematic diagram of one-half of the NE5517, a dual operational transconductance amplifier with linearizing diodes and impedance buffers, is shown in Figure 1.

1. Transconductance Amplifier

The transistor pair, Q_4 and Q_5, forms a transconductance stage. The ratio of their collector currents (I_4 and I_5, respectively) is defined by the differential input voltage, V_{IN}, which is shown in equation 1.

$$V_{IN} = \frac{KT}{q} \ln \frac{I_5}{I_4} \quad (1)$$

Where V_{IN} is the difference of the two input voltages

$KT \cong 26mV$ at room temperature (300°K).

Transistors Q_1, Q_2 and diode D_1 form a current mirror which focuses the sum of current I_4 and I_5 to be equal to amplifier bias current I_B:

$$I_4 + I_5 = I_B \quad (2)$$

If V_{IN} is small, the ratio of I_5 and I_4 will approach unity and the Taylor series of ln function can be approximated as

$$\frac{KT}{q} \ln \frac{I_5}{I_4} \approx \frac{KT}{q} \frac{I_5 - I_4}{I_4} \quad (3)$$

and $I_4 \approx I_5 \approx \frac{1}{2} I_B$

$$\frac{KT}{q} \ln \frac{I_5}{I_4} \approx \frac{KT}{q} \frac{I_5 - I_4}{\frac{1}{2} I_B} = \frac{2KT}{q} \frac{I_5 - I_4}{I_B} = V_{IN}$$

$$I_5 - I_4 = V_{IN} \frac{(I_B q)}{2KT} \quad (4)$$

The remaining transistors (Q_6 to Q_{11}) and diodes (D_4 to D_6) form three current mirrors that produce an output current equal to I_5 minus I_4. Thus:

$$V_{IN} \left\{ I_B \frac{q}{2KT} \right\} = I_0 \quad (5)$$

The term $\frac{(I_B q)}{2KT}$ is then the transconductance of the amplifier and is proportional to I_B.

2. Linearizing Diodes

For V_{IN} greater than a few millivolts, equation 3 becomes invalid and the transconductance increases nonlinearly. Figure 2 shows how the internal diodes can linearize the transfer function of the operational amplifier. Assume D_2 and D_3 are biased with current sources and the input signal current is I_S. Since

$I_4 + I_5 = I_B$ and $I_5 - I_4 = I_0$, that is:

$I_4 = \frac{1}{2}(I_B - I_0)$, $I_5 = \frac{1}{2}(I_B + I_0)$

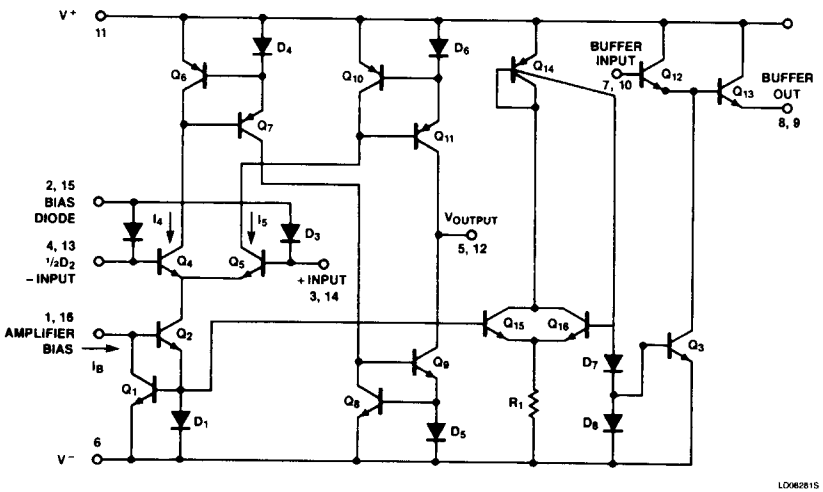


Figure 1. Circuit Diagram of NE5517

For the diodes and the input transistors that have identical geometries and are subject to similar voltages and temperatures, the following equation is true:

$$\frac{T}{q} \ln \frac{\frac{I_D}{2} + I_S}{\frac{I_D}{2} - I_S} = \frac{KT}{q} \ln \frac{\frac{1}{2}(I_B + I_0)}{\frac{1}{2}(I_B - I_0)}$$

$$I_0 = I_S \frac{(2^1B)}{I_D} \quad \text{for } |I_S| < \frac{I_D}{2} \qquad (6)$$

The only limitation is that the signal current should not exceed ½ I_D.

3. Impedance Buffer

The upper limit of transconductance is defined by the maximum value of I_B (2mA). The lowest value of I_B for which the amplifier will function therefore determines the overall dynamic range. At low values of I_B, a buffer with very low input bias current is desired. A Darlington amplifier with constant-current source (Q_{14}, Q_{15}, Q_{16}, D_7, D_8, and R_1) suits the need.

APPLICATIONS

Voltage-Controlled Amplifier

In Figure 3, the voltage divider R_2, R_3 divides the input-voltage into small values (mV range) so the amplifier operates in a linear manner.

It is:

$$I_{OUT} = -V_{IN} \times \frac{R_3}{R_2 + R_3} \times g_M;$$

$$V_{OUT} = I_{OUT} \times R_L;$$

$$A = \frac{V_{OUT}}{V_{IN}} = \frac{R_3}{R_2 + R_3} g_M R_L;$$

$$\boxed{A = \frac{R_3}{R_2 + R_3} \times g_M \times R_L}$$

(3) $g_M = 19.2\ I_{ABC}$

(g_M in μmhos for I_{ABC} in mA)

Since g_M is directly proportional to I_{ABC}, the amplification is controlled by the voltage V_C in a simple way.

When V_C is taken relative to $-V_{CC}$ the following formula is valid:

$$I_{ABC} = \frac{(V_C - 1.2V)}{R_1}$$

The 1.2V is the voltage across two base-emitter baths in the current mirrors. This

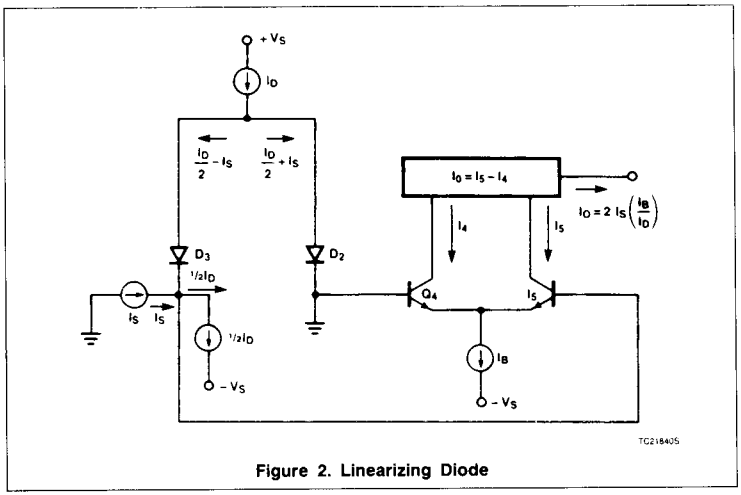


Figure 2. Linearizing Diode

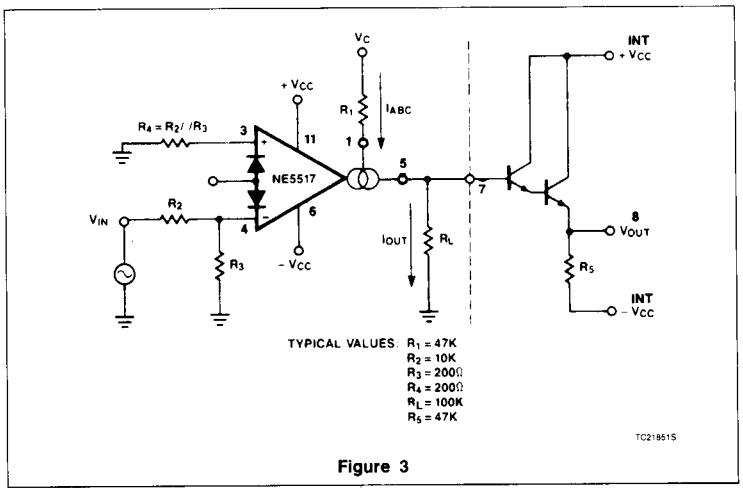


Figure 3

circuit is the base for many applications of the NE5517.

Stereo Amplifier With Gain Control

Figure 4 shows a stereo amplifier with variable gain via a control input. Excellent tracking of typical 0.3dB is easy to achieve. With the potentiometer, R_P, the offset can be adjusted. For AC-coupled amplifiers, the potentiometer may be replaced with two 510Ω resistors.

Modulators

Because the transconductance of an OTA (Operational Transconductance Amplifier) is directly proportional to I_{ABC}, the amplification of a signal can be controlled easily. The output current is the product from transconductance × input voltage. The circuit is effective up to approximately 200kHz. Modulation of 99% is easy to achieve.

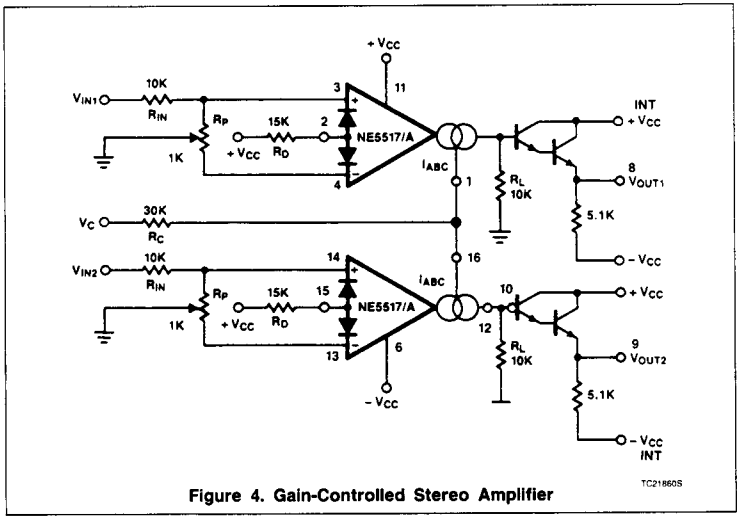


Figure 4. Gain-Controlled Stereo Amplifier

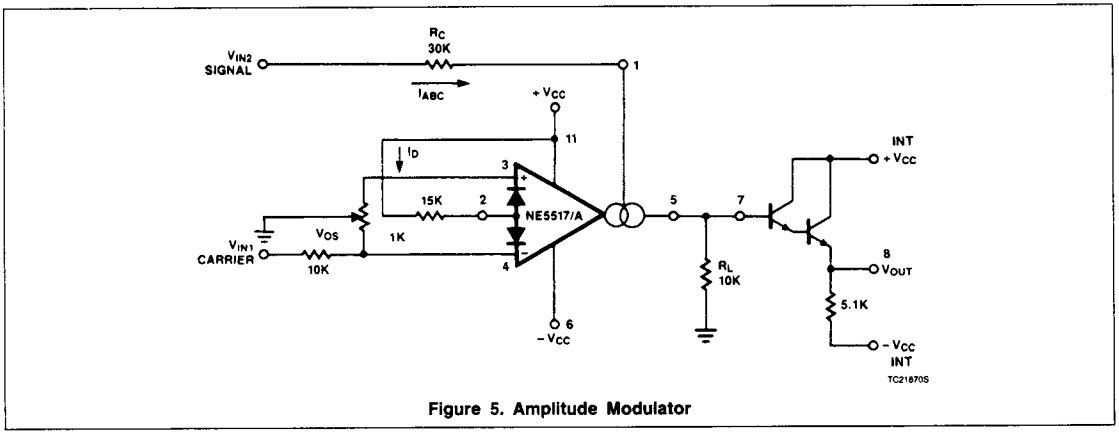


Figure 5. Amplitude Modulator

Voltage-Controlled Resistor (VCR)

Because an OTA is capable of producing an output current proportional to the input voltage, a voltage variable resistor can be made. Figure 6 shows how this is done. A voltage presented at the R_X terminals forces a voltage at the input. This voltage is multiplied by g_M and thereby forces a current through the R_X terminals:

$$R_X = \frac{R + R_A}{g_M \times R_A}$$

where g_M is approximately 19.21 μMHOs at room temperature. Figure 7 shows a Voltage Controlled Resistor using linearizing diodes. This improves the noise performance of the resistor.

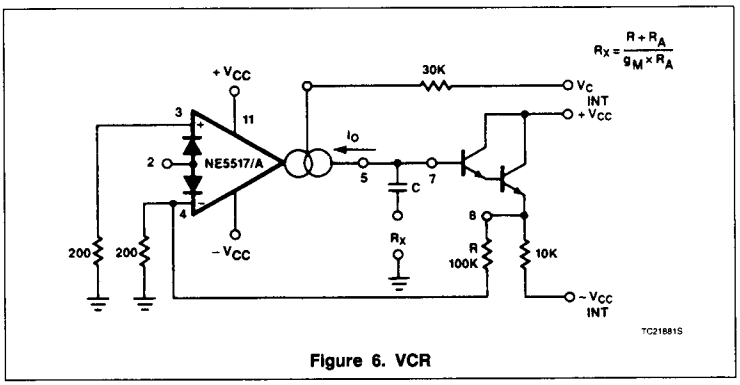


Figure 6. VCR

Voltage-Controlled Filters

Figure 8 shows a Voltage Controlled Low-Pass Filter. The circuit is a unity gain buffer until X_C/g_M is equal to R/R_A. Then, the frequency response rolls off at a 6dB per octave with the −3dB point being defined by the given equations. Operating in the same manner, a Voltage Controlled High-Pass Filter is shown in Figure 9. Higher order filters can be made using additional amplifiers as shown in Figures 10 and 11.

Voltage-Controlled Oscillators

Figure 12 shows a voltage-controlled triangle-square wave generator. With the indicated values a range from 2Hz to 200kHz is possible by varying I_{ABC} from 1mA to 10μA.

The output amplitude is determined by $I_{OUT} \times R_{OUT}$.

Please notice the differential input voltage is not allowed to be above 5V.

With a slight modification of this circuit you can get the sawtooth pulse generator, as shown in Figure 13.

APPLICATION HINTS

To hold the transconductance g_M within the linear range, I_{ABC} should be chosen not greater than 1mA. The current mirror ratio should be as accurate as possible over the entire current range. A current mirror with only two transistors is not recommended. A suitable current mirror can be built with a PNP transistor array which causes excellent matching and thermal coupling among the transistors. The output current range of the DAC normally reaches from 0 to −2mA. In this application, however, the current range is set through R_{REF} (10kΩ) to 0 to −1mA.

$$I_{DAC\ MAX} = 2 \times \frac{V_{REF}}{R_{REF}} = 2 \times \frac{5V}{10k} = 1mA$$

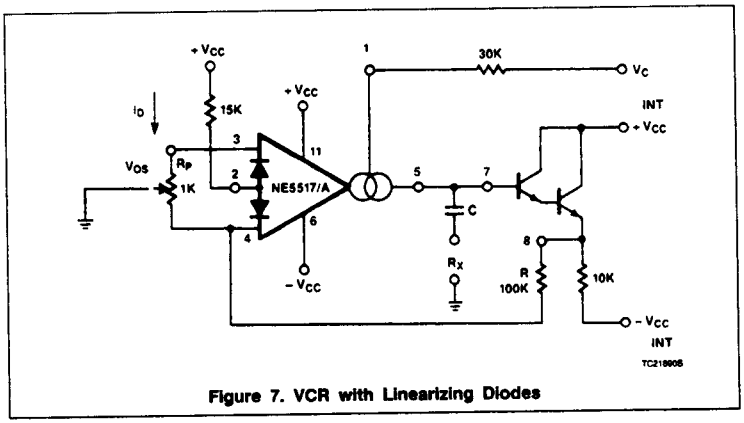
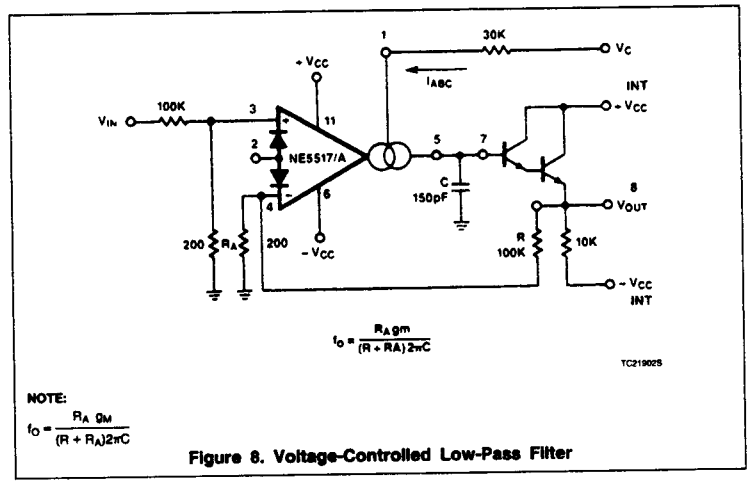


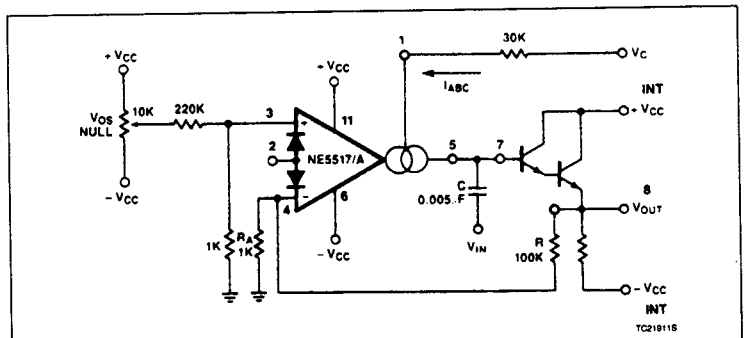
Figure 7. VCR with Linearizing Diodes



NOTE:

$f_o = \frac{R_A\ g_M}{(R + R_A)2\pi C}$

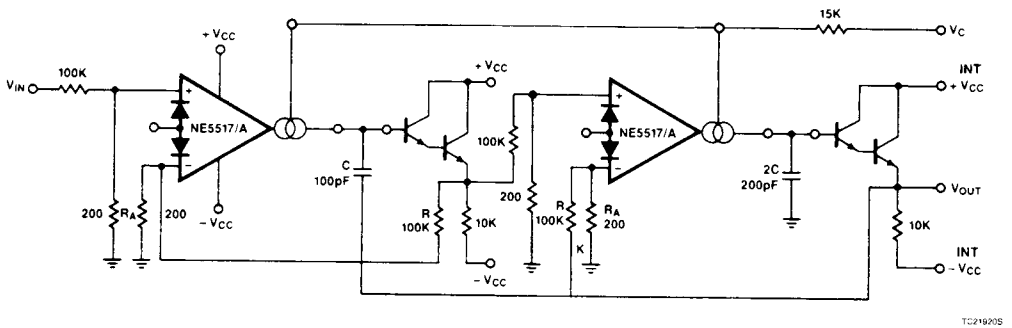
Figure 8. Voltage-Controlled Low-Pass Filter



NOTE:

$f_o = \frac{R_A\ g_M}{(R + R_A)2\pi C}$

Figure 9. Voltage-Controlled High-Pass Filter



NOTE:

$$f_O = \frac{R_A\, g_M}{(R + R_A)2\pi C}$$

Figure 10. Butterworth Filter — 2nd Order

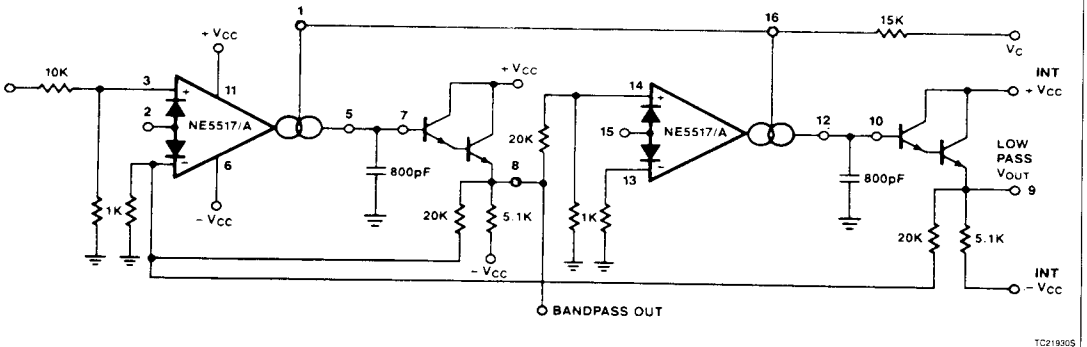


Figure 11. State Variable Filter

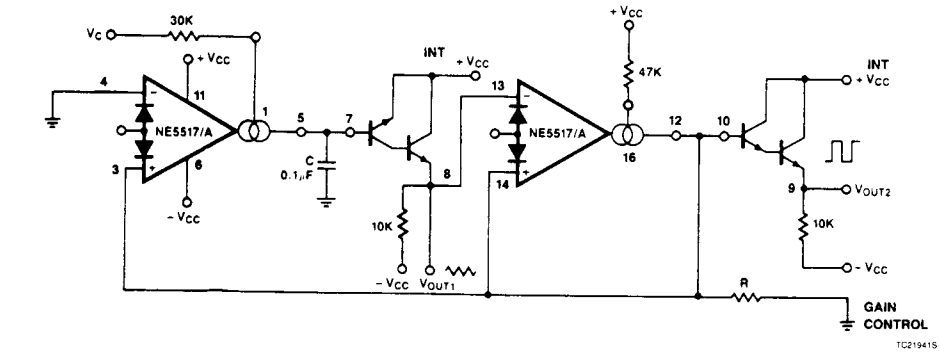
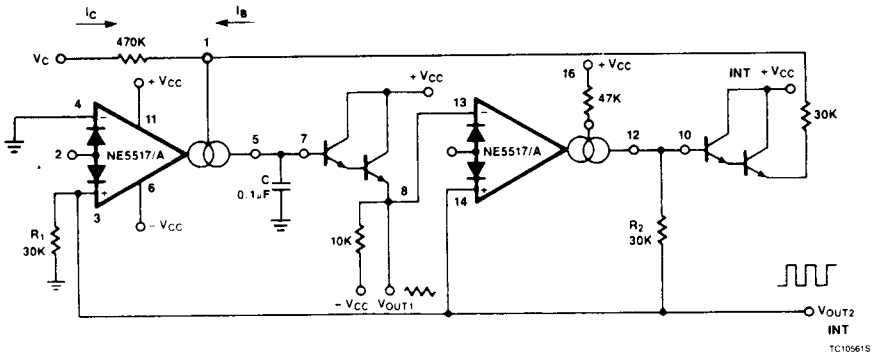


Figure 12. Triangle-Square Wave Generator (VCO)



NOTE:

$$V_{PK} = \frac{(V_C - 0.8)\,R_1}{R_1 + R_2} \quad T_H = \frac{2V_{PK} \times C}{I_B} \quad T_L = \frac{2V_{PK} \times C}{I_C} \quad f_{OSC} \frac{I_C}{2V_{PK} \times C} \quad I_C << I_B$$

Figure 13. Sawtooth Pulse VCO