Quad SPST CMOS Analog Switch

HI-201/883

The HI-201/883 is a monolithic device comprised of four independently selectable SPST switchers which feature fast switching speeds (185ns typical) combined with low power dissipation (15mW typical at +25°C).

Each switch provides low "ON" resistance operation for input signal voltages up to the supply rails and for signal currents up to 25mA continuous. Rugged DI construction eliminates latch-up and substrate SCR failure modes.

All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. The HI-201/883 is an ideal component for use in high frequency analog switching. Typical applications include signal path switching, sample and hold circuits, digital filters, and op amp gain switching networks.

HI-201/883 is available in a 16 Ld CerDIP package.

Features

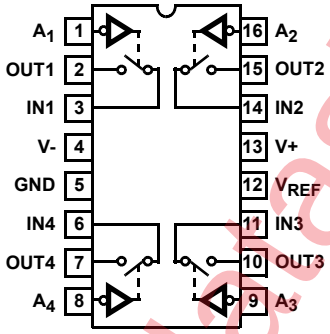
- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Low "On" Release . . . . . 100Ω Max
- Wide Analog Signal Range . . . . . ±15V
- TTL/CMOS Compatible . . . . . 2.4V (Logic "1")
- Turn-On Time. 500ns
- Analog Current Range (Continuous) 25mA
- No Latch-Up
- Replaces DG201

Applications

- High Frequency Analog Switching
- Sample and Hold Circuits
- Digital Filters
- Op Amp Gain Switching Networks

Pin Configuration

HI1-0201/883 (16 LD CERDIP)
TOP VIEW



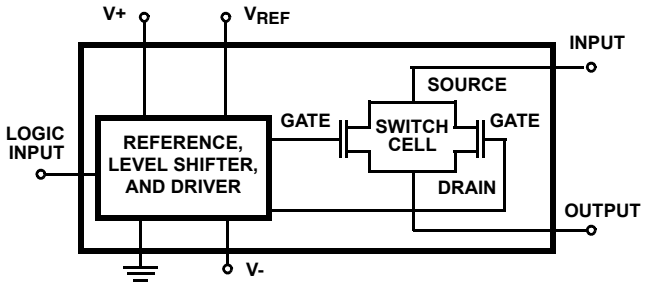


FIGURE 1. FUNCTIONAL DIAGRAM

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HI1-0201/883	HI1-201/883	-55 to +125	16 Ld CerDIP	F16.3

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
$\pm V_{SUPPLY}$ to Ground (V+, V-) . . . . . $\pm$20V
Analog Input Voltage, ($+V_S$) . . . . . $+V_{SUPPLY}$ +2V
($-V_S$) . . . . . $-V_{SUPPLY}$ -2V
Digital Input Voltage, ($+V_A$) . . . . . $+V_{SUPPLY}$ +4V
($-V_A$) . . . . . $-V_{SUPPLY}$ -4V
Peak Current (S or D)
(Pulse at 1ms, 10% Duty Cycle Max) 40mA
Continuous Current Any Terminal (Except S or D) 25mA

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CerDIP Package	86	22

Package Power Dissipation at +75°C
CerDIP Package 0.88W
Package Power Dissipation Derating Factor above +75°C
CerDIP Package . . . . . 11.76mW/°C
Junction Temperature . . . . . +175°C
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering 10s) . . . . . ≤275°C

Recommended Operating Conditions

Operating Temperature Range . . . . . -55°C to +125°C
Operating Supply Voltage Range ($\pm V_{SUPPLY}$) . . . . . $\pm$15V
Analog Input Voltage (V_S) . . . . . $\pm V_{SUPPLY}$
Logic Low Level (V_{AL}) . . . . . 0V to 0.8V
Logic High Level (V_{AH}) . . . . . 2.4V to $+V_{SUPPLY}$

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

TABLE 1. D.C. ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = −15V, V_{REF} = OPEN, GND = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE (°C)	MIN	MAX	UNITS
Switch "ON" Resistance	r_{DS}	V_A = 0.8V, V_S = 10V, I_D = -1mA, All Unused Channels V_A = 2.4V	1	+25	-	70	Ω
			2, 3	-55 to +125	-	100	Ω
		V_A = 0.8V, V_S = -10V, I_D = 1mA, All Unused Channels V_A = 2.4V	1	+25	-	70	Ω
			2, 3	-55 to +125	-	100	Ω
Source "OFF" Leakage Current	$I_{S(OFF)}$	V_S = +14V, V_D = -14V, V_A = 2.4V, All Unused Channels V_A = 2.4V, V_D = +14V, V_S = -14V	1	+25	-2	2	nA
			2, 3	-55 to +125	-100	100	nA
		V_S = -14V, V_D = +14V, V_A = 2.4V, All Unused Channels V_A = 2.4V, V_D = -14V, V_S = +14V	1	+25	-2	2	nA
			2, 3	-55 to +125	-100	100	nA
Drain "OFF" Leakage Current	$I_{D(OFF)}$	V_D = -14V, V_S = +14V, V_A = 2.4V, All Unused Channels V_A = 2.4V, V_D = +14V, V_S = -14V	1	+25	-2	2	nA
			2, 3	-55 to +125	-100	100	nA
		V_D = +14V, V_S = -14V, V_A = 2.4V, All Unused Channels V_A = 2.4V, V_D = -14V, V_S = +14V	1	+25	-2	2	nA
			2, 3	-55 to +125	-100	100	nA
Channel "ON" Leakage Current	$I_{D(ON)}$	V_D = V_S = +14V, V_A = 0.8V, All Unused Channels V_A = 0.8V, V_D = V_S = -14V	1	+25	-2	2	nA
			2, 3	-55 to +125	-100	100	nA
		V_D = V_S = -14V, V_A = 0.8V, All Unused Channels V_A = 0.8V, V_D = V_S = +14V	1	+25	-2	2	nA
			2, 3	-55 to +125	-200	200	nA
Low Level Input Current	I_{AL}	V_{AL} = 0.8V All Unused Channels V_A = 2.4V	1	+25	-0.5	0.5	µA
			2, 3	-55 to +125	-1.0	1.0	µA
High Level Input Current	I_{AH}	V_{AH} = 2.4V All Unused Channels V_{AH} = 4.0V	1	+25	-0.5	0.5	µA
			2, 3	-55 to +125	-1.0	1.0	µA
Supply Current	$+I_{CC}$	All Channels V_A = 0.8V	1, 2	+25, +125	-	1.5	mA
			3	-55	-	2.0	mA
		All Channels V_A = 2.4V	1, 2	+25, +125	-	1.5	mA
			3	-55	-	2.0	mA

TABLE 1. D.C. ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = −15V, V_{REF} = OPEN, GND = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE (°C)	MIN	MAX	UNITS
Supply Current	$-I_{CC}$	All Channels V_A = 0.8V	1, 2	+25, +125	-1.5	-	mA
			3	-55	-2.0	-	mA
		All Channels V_A = 2.4V	1, 2	+25, +125	-1.5	-	mA
			3	-55	-2.0	-	mA

TABLE 2. A.C. ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = −15V, V_{REF} = OPEN, GND = 0V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE (°C)	MIN	MAX	UNITS
Turn “ON” Time	t_{ON}	C_L = 100pF, R_L = 1kΩ	9	+25	-	600	ns
			10, 11	-55, +125	-	800	ns
Turn “OFF” Time	t_{OFF}	C_L = 100pF, R_L = 1kΩ	9	+25	-	500	ns
			10, 11	-55, +125	-	650	ns

TABLE 3. ELECTRICAL PERFORMANCE SPECIFICATIONS (NOTE 1)

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = −15V, V_{REF} = OPEN, GND = 0V

PARAMETERS	SYMBOL	CONDITIONS	NOTE	TEMPERATURE (°C)	MIN	MAX	UNITS
Address Capacitance	C_A	f = 1MHz, V_{AL} = 0V	1	+25	-	15	pF
Switches Input Capacitance	$C_{S\ (OFF)}$	f = 1MHz, V_{AH} = 5V, Measured Source to GND	1	+25	-	15	pF
Switch Output Capacitance	$C_{D\ (OFF)}$	f = 1MHz, V_{AH} = 5V, Measured Output to Ground	1	+25	-	20	pF
	$C_{D\ (ON)}$	f = 1MHz, V_{AL} = 0V, Measured Output to Ground	1	+25	-	30	pF
Drain to Source Capacitance	C_{DS}	f = 1MHz, V_{AH} = 5V	1	+25	-	2.0	pF
Off Isolation	V_{ISO}	f = 200kHz, V_A = 2.4, R_L = 1k, V_{GEN} = $1V_{P-P}$, C_L = 10pF	1	+25	55	-	dB
Cross Talk	V_{CT}	f = 200kHz, V_A = 2.4, R_L = 1k, V_{GEN} = $1V_{P-P}$, C_L = 10pF	1	+25	60	-	dB
Charge Transfer Error	V_{CTE}	f = 200kHz, V_A = 0 to 4V, C_L = 0.01µF	1	+25	-10	10	mV

NOTE:

1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (Tables 1 and 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1 (Note 2), 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

NOTE:

2. PDA applies to Subgroup 1 only.

Test Circuits

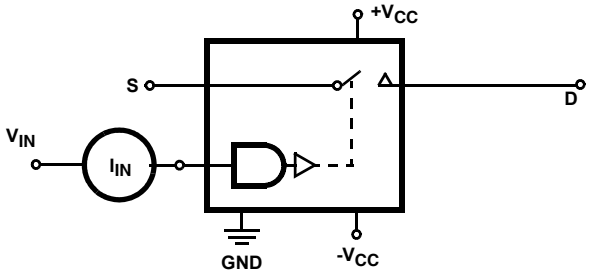


FIGURE 2. INPUT LEAKAGE CURRENT

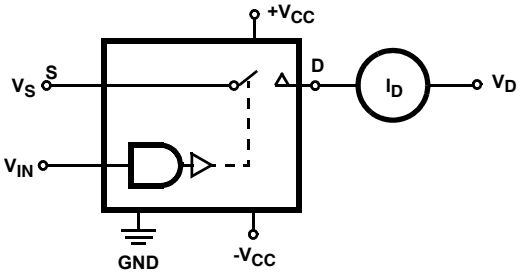


FIGURE 3. $I_{D\ (OFF)}$

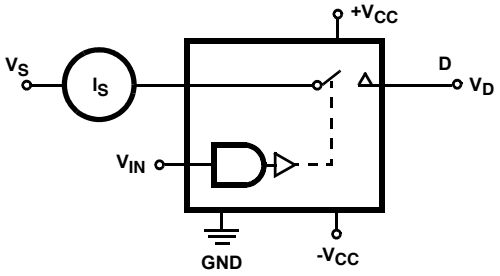


FIGURE 4. $I_{S\ (OFF)}$

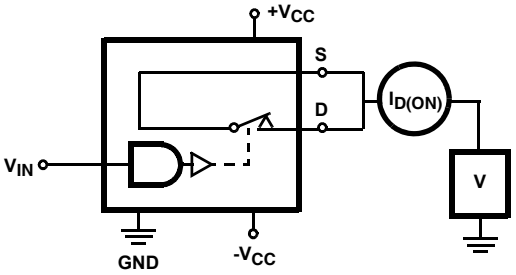


FIGURE 5. $I_{D\ (ON)}$

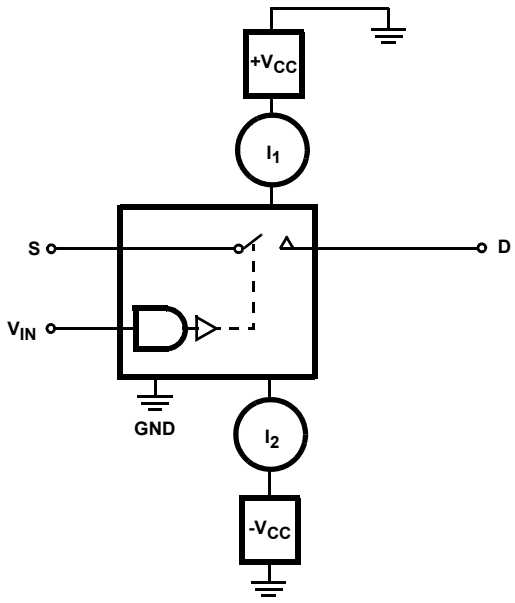


FIGURE 6. SUPPLY CURRENTS

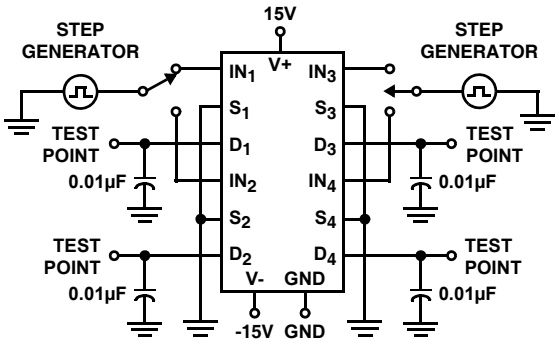


FIGURE 7. CHARGE TRANSFER ERROR

Test Circuits (Continued)

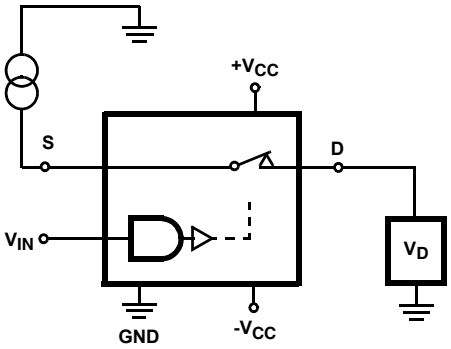


FIGURE 8. R_{DS}

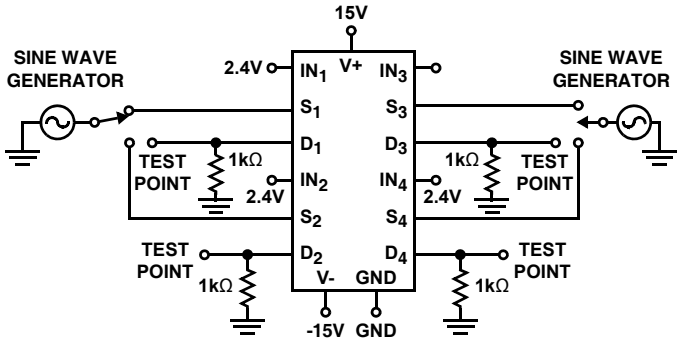


FIGURE 9. OFF CHANNEL ISOLATION

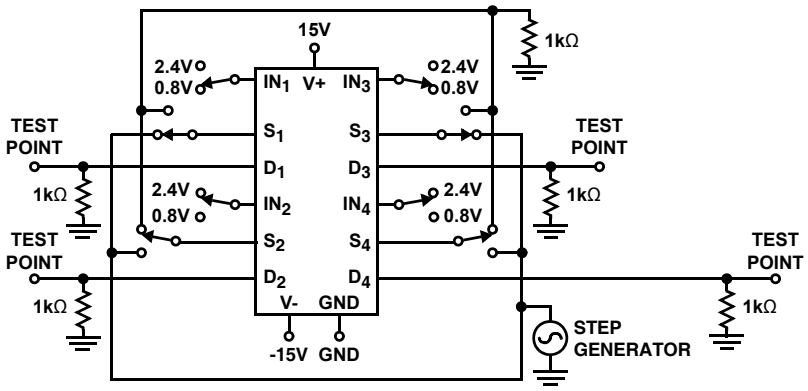


FIGURE 10. CROSSTALK BETWEEN CHANNELS

Switching Waveforms

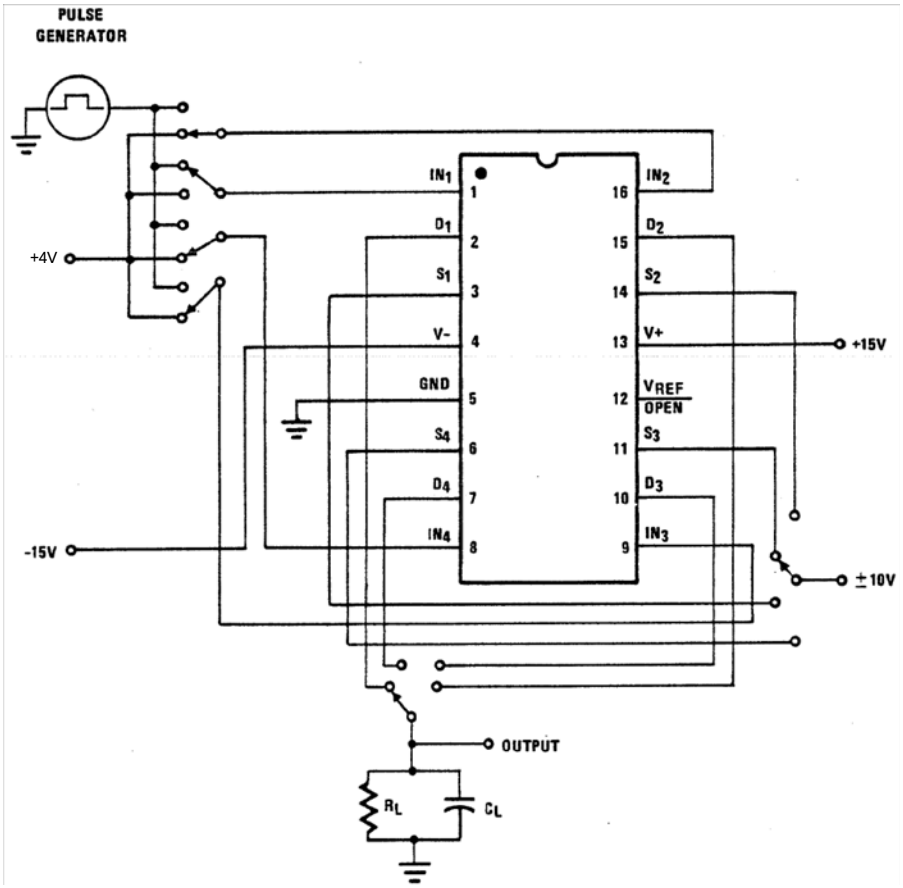


FIGURE 11.

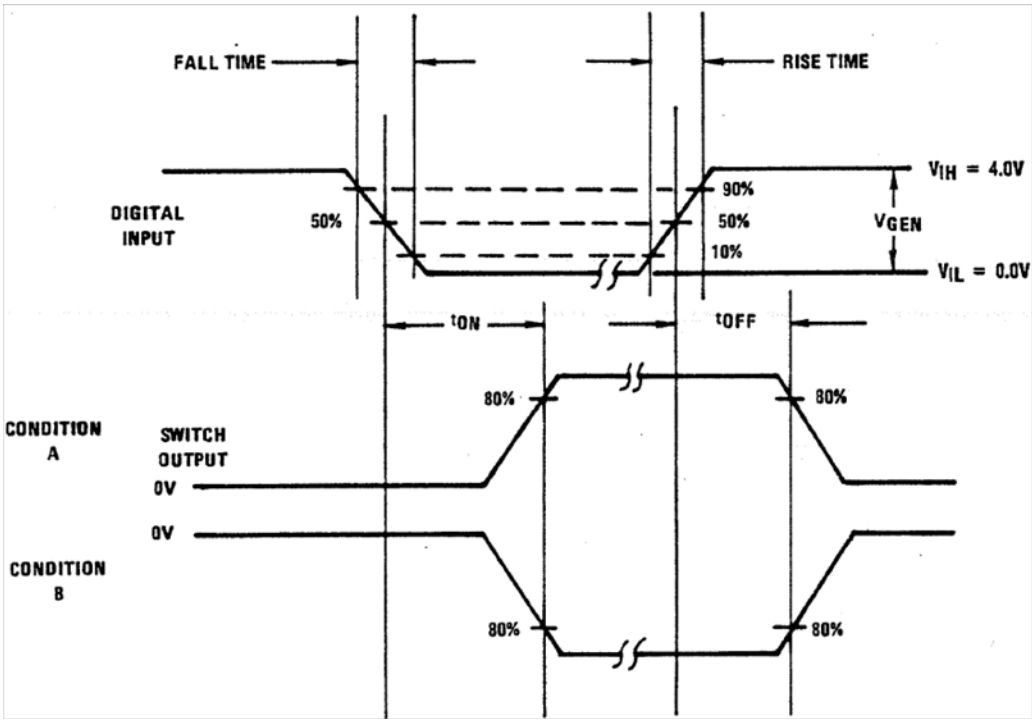


FIGURE 12.

Burn-In Circuit

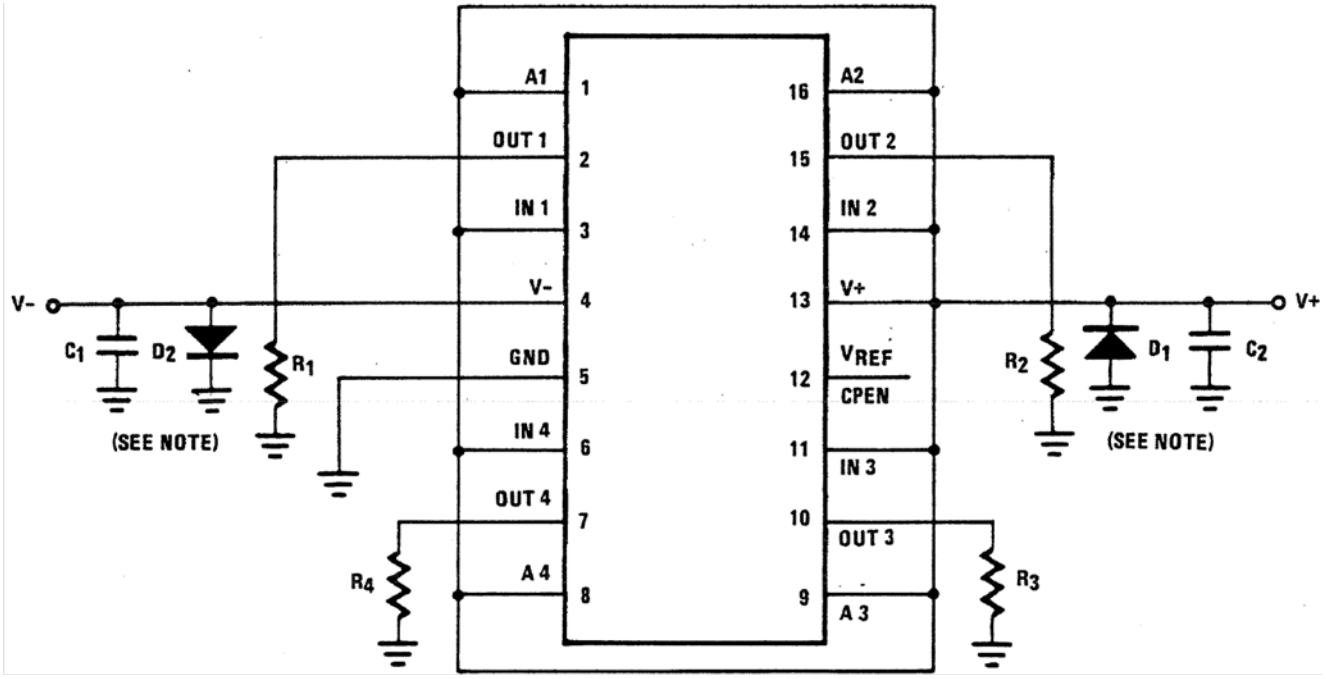


FIGURE 13. HI-201/883 CERDIP

NOTE:

$R_1 = R_2 = R_3 = R_4 = 10k\Omega$.

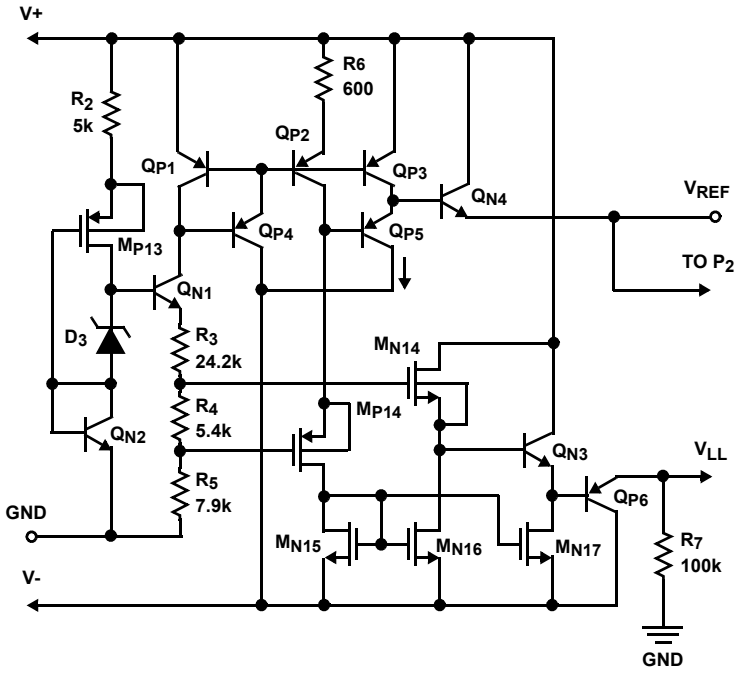
$C_1 = C_2 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row).

$D_1 = D_2$ = IN4002 or equivalent/board.

$|(V+) - (V-)| = 30V$.

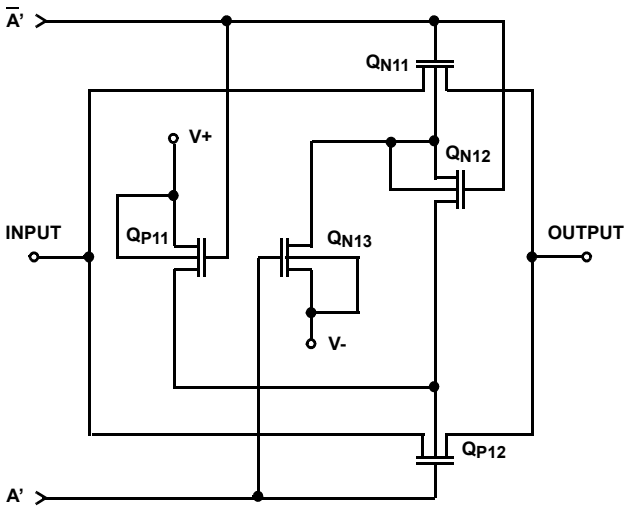
Schematic Diagrams

TTL/CMOS REFERENCE CIRCUIT V_{REF} CELL

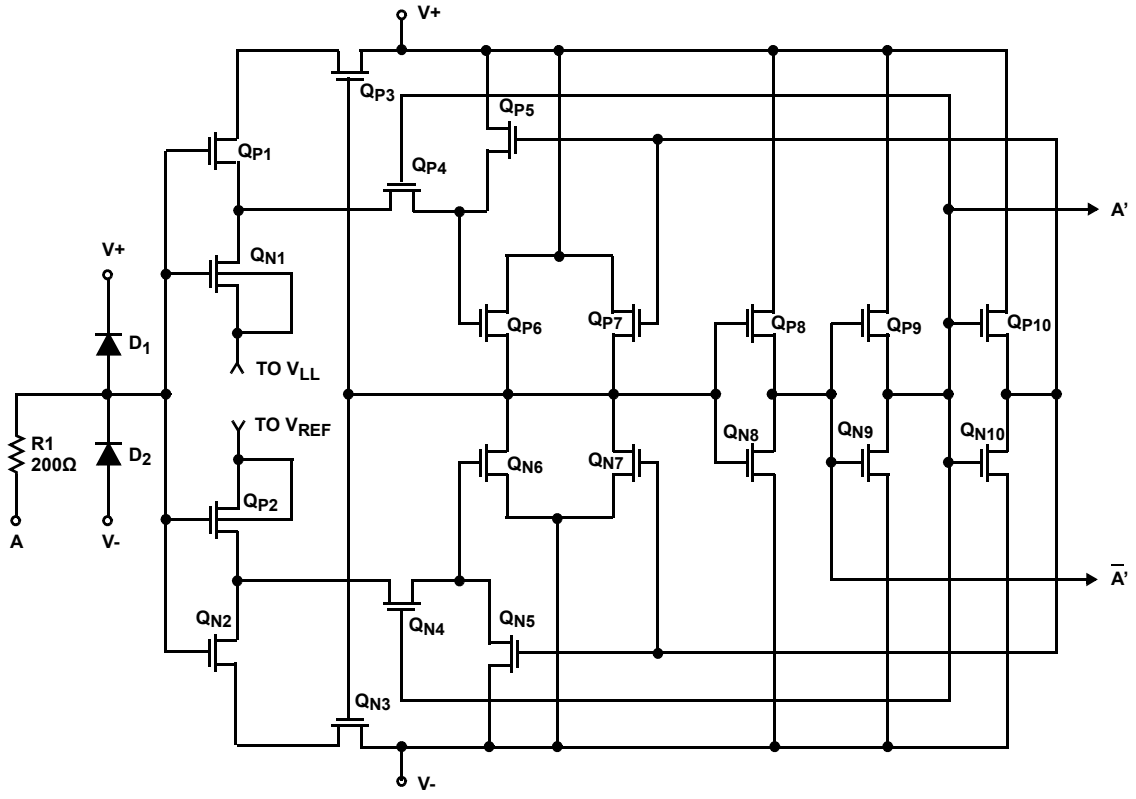


Schematic Diagrams (Continued)

SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



Typical Performance Curves $T_A = +25°C$, $V_{SUPPLY} = \pm15V$, $V_{AH} = 2.4V$, $V_{AL} = 0.8V$ and V_{REF} = Open

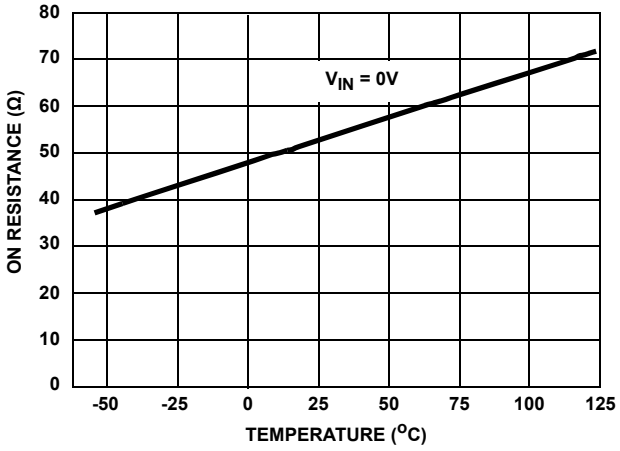


FIGURE 14. ON RESISTANCE vs TEMPERATURE

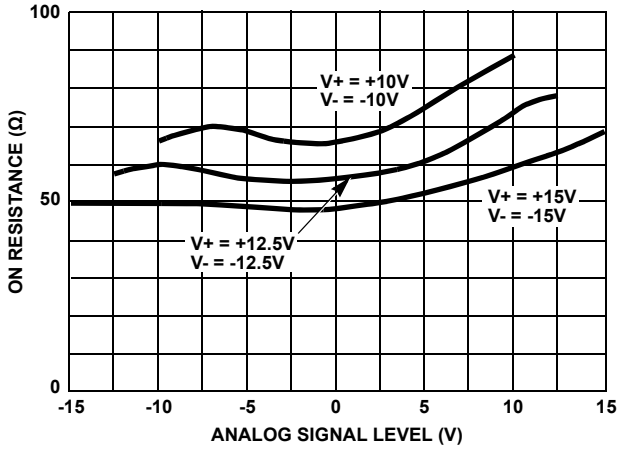


FIGURE 15. ON RESISTANCE vs ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE

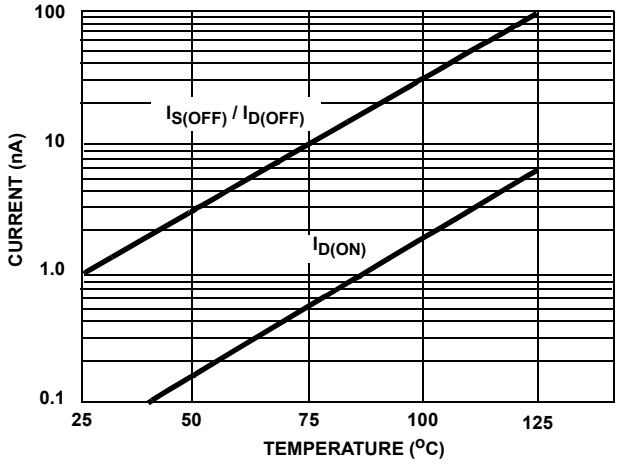


FIGURE 16. LEAKAGE CURRENT vs TEMPERATURE

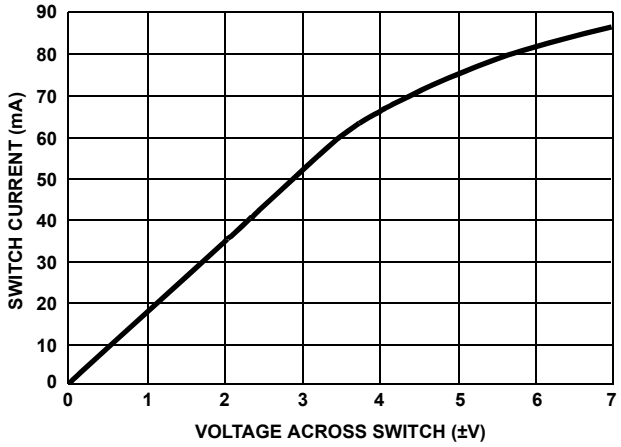


FIGURE 17A. SWITCH CURRENT vs VOLTAGE

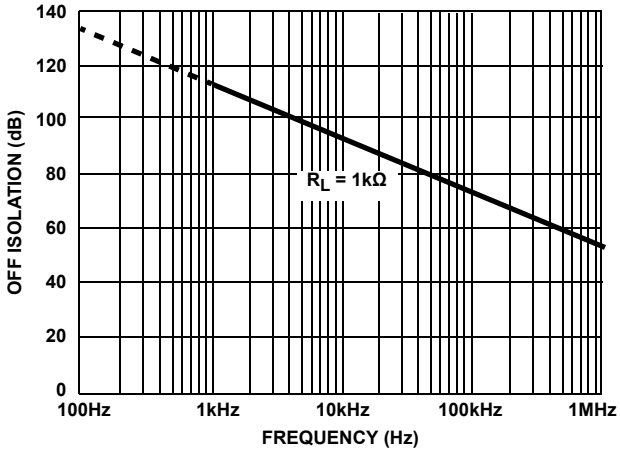


FIGURE 18. OFF ISOLATION vs FREQUENCY

Die Characteristics

DIE DIMENSIONS:

81 X 85 X 19 mils

METALLIZATION:

Type: Aluminum
Thickness: 16kÅ ±2kÅ

GLASSIVATION:

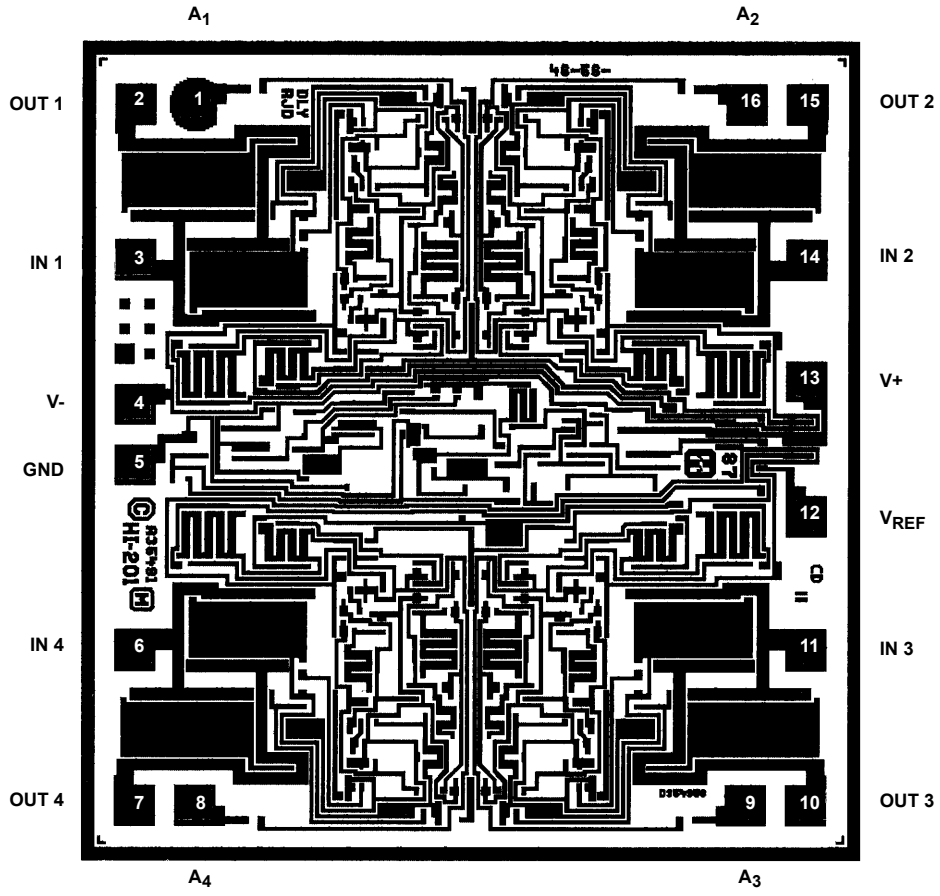
Type: Nitride over Silox
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

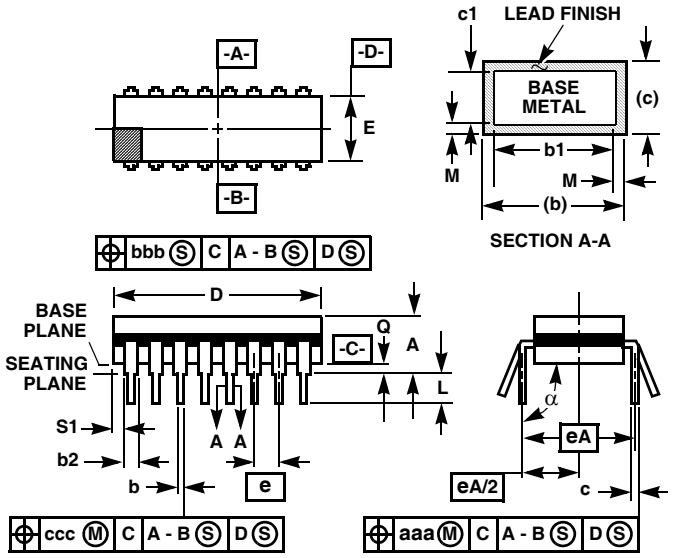
$2 \times 10^5 A/cm^2$ at 25mA

Metallization Mask Layout

HI-201/883



Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

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