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TECHNICAL DATA

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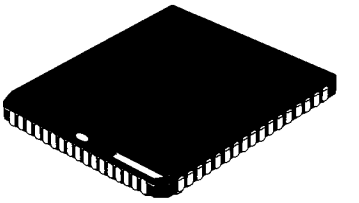
MCCS16C451

Product Preview

Multifunction I/O Controller for IBM PC/XT/AT™

The MCCS16C451 is a multifunction device designed for mother boards or add-in cards, and is compatible with IBM PC/XT/AT systems. The MCCS16C451 has an NS16450 compatible asynchronous communications element to provide a serial port, and a bidirectional parallel port interface that supports a Centronics type printer and allows the parallel port to receive data from external devices.

- Supports flexible PC/XT and AT port address decoding and interrupts and bus cycles
- 100% compatible with NS16450 and NS8250 UART
- One full-duplex asynchronous receiver/transmitter
- Programmable serial interface character length
- Programmable baud rate for receiver and transmitter
- Full modem control functions
- Double buffering in character mode
- False start-bit detection
- Centronics printer interface
- Parallel port extended mode supports bidirectional input and output
- Parallel port supports level sensitive interrupts
- Readable interrupt pending status
- Direct drive for parallel port interface
- 1.5 micron CMOS technology
- 68-lead PLCC package
- Operating temperature 0 to 70°C
- Single 5-volts supply
- Application Circuit in Section 5.1



FN PACKAGE
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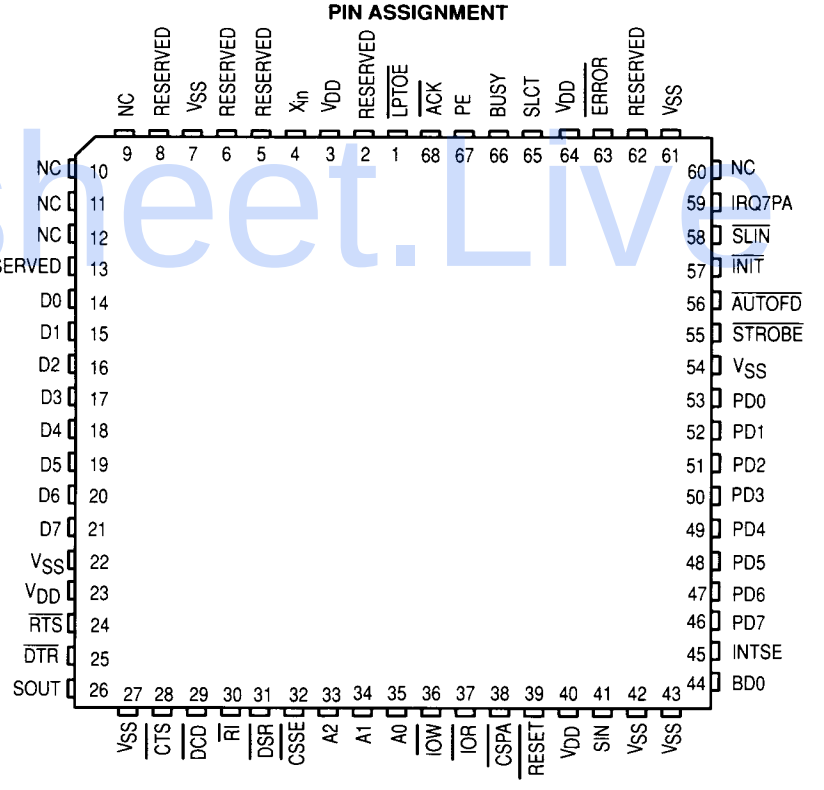
CASE 779

Ordering Information
MCCS16C451FN

PIN ASSIGNMENT



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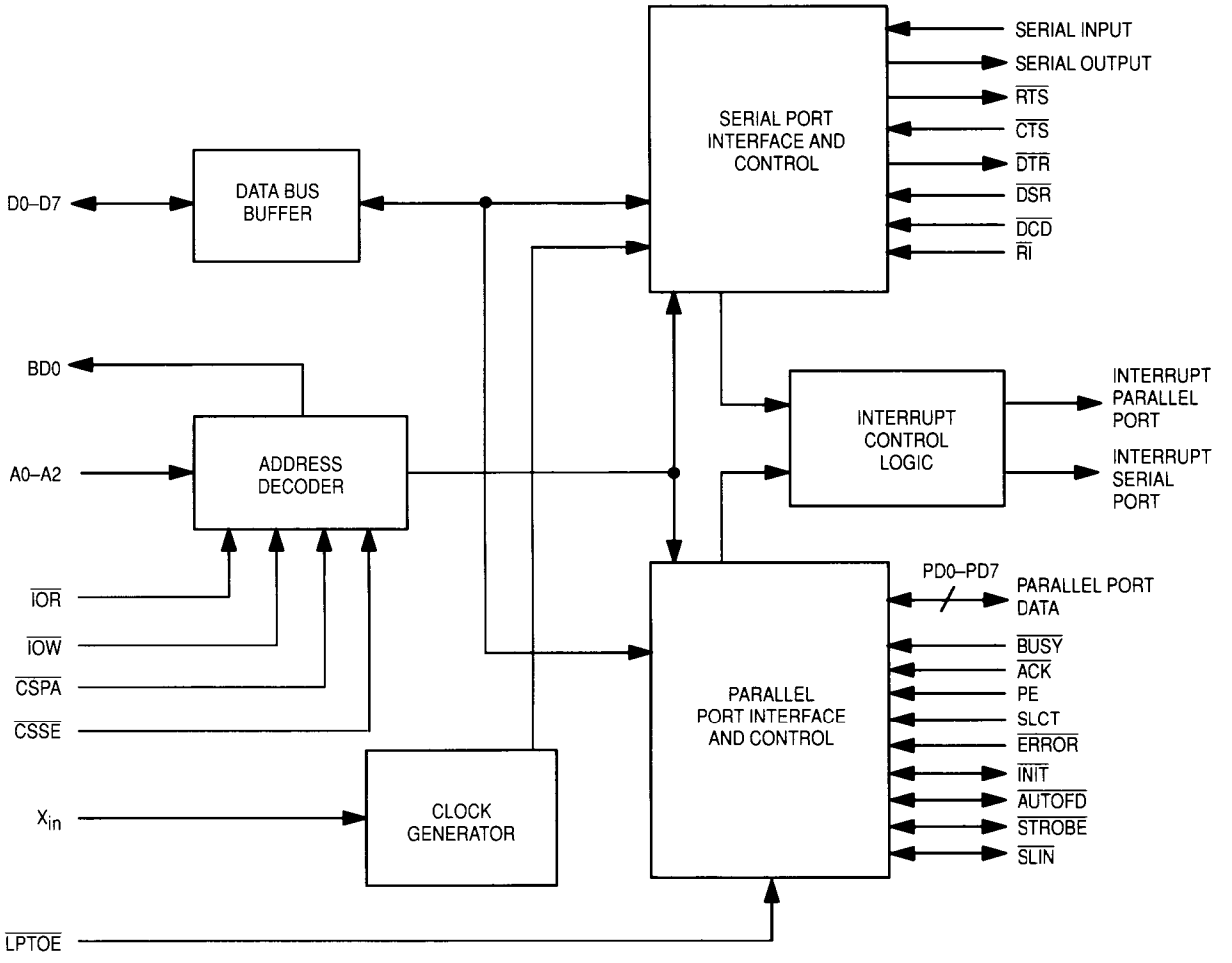
MOTOROLA

(Replaces MCS16C451/D)

CONTENTS

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

1.0 ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, All voltages with respect to V_{SS})

Parameter	Test Conditions	Symbol	Guaranteed Limits		Unit
			Min	Max	
Power Supply Voltage		V_{DD}	–0.5	7.0	V
All Input Voltages		V_{in}	–0.5	V_{DD} + 0.5	V
All Output Voltages		V_{out}	–0.5	V_{DD} + 0.5	V
DC Drain Current per Pin		I_D	—	25	mA
DC Drain Current V_{DD} and V_{SS}		I_{DD}	—	75	mA
Power Dissipation	V_{DD} = 5.25 V	W_D	—	1	W
Supply Current	V_{DD} = 5.25 V	I_{DD}	20	50	mA
Operating Temperature		T_{OP}	0	70	°C
Storage Temperature		T_{stg}	– 50	+ 150	°C
Lead Temperature (10 s Soldering)		T_{LED}	—	300	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$. Reliability or operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

2.0 DC CHARACTERISTICS (T_A = 0 to 70°C, V_{DD} = 4.75 to 5.25 Vdc)

Parameter	Test Conditions	Symbol	Guaranteed Limits		Unit
			Min	Max	
PINS 1, 4, 28–39, 41, 63, 65–68					
Input Low Voltage	V_{DD} = 4.75 to 5.25 V	V_{IL}	—	0.8	V
Input High Voltage	V_{DD} = 4.75 to 5.25 V	V_{IH}	2.0	—	V
Input Low Leakage Current	$V_{in} = V_{SS}$	I_{IL}	—	–10	µA
Input High Leakage Current	$V_{in} = V_{DD}$	I_{IH}	—	10	µA
PINS 14–21					
Input Low Voltage	V_{DD} = 4.75 to 5.25 V	V_{IL}	—	0.8	V
Input High Voltage	V_{DD} = 4.75 to 5.25 V	V_{IH}	2.0	—	V
Input Low Leakage Current	$V_{in} = V_{SS}$	I_{IL}	—	–10	µA
Input High Leakage Current	$V_{in} = V_{DD}$	I_{IH}	—	10	µA
Output Low Voltage	I_{OL} = 4 mA	V_{OL}	—	0.4	V
Output High Voltage	I_{OL} = –4 mA	V_{OH}	—	2.4	V
Leakage Current	$0 < V_{out} < V_{DD}$	I_{OZ}	–1	1	µA
PINS 46–53					
Input Low Voltage	V_{DD} = 4.75 to 5.25 V	V_{IL}	—	0.8	V
Input High Voltage	V_{DD} = 4.75 to 5.25 V	V_{IH}	2.0	—	V
Input Low Leakage Current	$V_{in} = V_{SS}$	I_{IL}	—	–10	µA
Input High Leakage Current	$V_{in} = V_{DD}$	I_{IH}	—	10	µA
Output Low Voltage	I_{OL} = 12 mA	V_{OL}	—	0.4	V
Output High Voltage	I_{OL} = –12 mA	V_{OH}	2.4	—	V
Leakage Current	$0 < V_{out} < V_{DD}$	I_{OZ}	–1	1	µA
PINS 55–58					
Input Low Voltage	V_{DD} = 4.75 to 5.25 V	V_{IL}	—	0.8	V
Input High Voltage	V_{DD} = 4.75 to 5.25 V	V_{IH}	2.0	—	V
Input Low Leakage Current	$V_{in} = V_{SS}$	I_{IL}	—	–10	µA
Input High Leakage Current	$V_{in} = V_{DD}$	I_{IH}	—	10	µA
Output Low Voltage	I_{OL} = 16 mA	V_{OL}	—	0.4	V
Leakage Current	$0 < V_{out} < V_{DD}$	I_{OZ}	–10	10	µA
PINS 24–26, 44					
Output Low Voltage	I_{OL} = 4 mA	V_{OL}	—	0.4	V
Output High Voltage	I_{OL} = –4 mA	V_{OH}	2.4	—	V
PINS 45, 59					
Output Low Voltage	I_{OL} = 8 mA	V_{OL}	—	0.4	V
Output High Voltage	I_{OL} = –8 mA	V_{OH}	2.4	—	V
Leakage Current	$0 < V_{out} < V_{DD}$	I_{OZ}	–1	1	µA
CAPACITANCE					
Input Capacitance	FC = 1 MHz (Unmeasured Pins to V_{SS})	C_I	—	10	pF
Output Capacitance	FC = 1 MHz (Unmeasured Pins to V_{SS})	C_O	—	10	pF

3.0 AC CHARACTERISTICS

Parameter	Test Conditions	Symbol	Guaranteed Limits		Unit
			Min	Max	
PROCESSOR WRITE CYCLE (Figure 1)					
Address Hold Time from $\overline{IOW}$ going High		t_1	5	—	ns
$\overline{CSSE}$ or $\overline{CSPA}$ Hold Time from $\overline{IOW}$ going High		t_2	5	—	ns
$\overline{IOW}$ Delay from $\overline{CSSE}$ or $\overline{CSPA}$		t_3	10	—	ns
$\overline{IOW}$ Delay from Address		t_4	25	—	ns
$\overline{IOW}$ Strobe Width		t_5	50	—	ns
Write Cycle		t_6	135	—	ns
Data Setup Time		t_7	15	—	ns
Data Hold Time		t_8	25	—	ns
PROCESSOR READ CYCLE (Figure 2)					
Address Hold Time from $\overline{IOR}$ going High		t_9	0	—	ns
$\overline{CSSE}$ or $\overline{CSPA}$ Hold Time from $\overline{IOR}$ going High		t_{10}	0	—	ns
$\overline{IOR}$ Delay from $\overline{CSSE}$ or $\overline{CSPA}$		t_{11}	10	—	ns
$\overline{IOR}$ Delay from Address		t_{12}	10	—	ns
$\overline{IOR}$ Strobe Width		t_{13}	75	—	ns
Read Cycle Time		t_{14}	135	—	ns
Serial Port Delay from $\overline{IOR}$ to Data	100 pF Loading	t_{15}	—	175	ns
Parallel Port Delay from $\overline{IOR}$ to Data	100 pF Loading		—	75	ns
Serial Port $\overline{IOR}$ to Floating Data Delay	100 pF Loading	t_{16}	0	100	ns
Parallel Port $\overline{IOR}$ to Floating Data Delay	100 pF Loading		0	35	ns
RECEIVER TIMING (Figure 3)					
Delay from Stop to Set Interrupt	(Receiver Clock Cycle)	t_{17}	—	1	ns
Delay from $\overline{IOR}$ to $\overline{RESET}$ Interrupt (RD RBR or RD LSR)	100 pF Loading	t_{18}	—	1	ns
TRANSMITTER TIMING (Figure 4)					
Delay from Initial INTR/RESET to Transmit Start (Baud Out Cycle)		t_{19}	8	16	*
Delay from Stop to Interrupt (THRE) (Baud Out Cycle)		t_{20}	1	2	*
Delay from $\overline{IOW}$ (WR THR) to $\overline{RESET}$ Interrupt	100 pF Loading	t_{21}	—	100	ns
Delay from Initial Write to Interrupt (Baud Out Cycle)		t_{22}	9	17	*
Delay from $\overline{IOR}$ (RD IIR) to $\overline{RESET}$ Interrupt (THRE)	100 pF Loading	t_{23}	—	250	ns
MODEM CONTROL TIMING (Figure 5)					
Delay from $\overline{IOW}$ (WR MCR) to Output	100 pF Loading	t_{24}	—	200	ns
Delay to Set Interrupt from Modem Input	100 pF Loading	t_{25}	—	250	ns
Delay to Reset Interrupt from $\overline{IOR}$ (RD MSR)	100 pF Loading	t_{26}	—	250	ns
PARALLEL PORT REGISTER AND CONTROL REGISTER TIMING (Figure 6)					
Parallel Port Delay of Valid Data from Parallel Port Data Register and Control Register to $\overline{IOW}$		t_{27}	—	45	ns
PARALLEL PORT INTERRUPT TIMING (Figure 7)					
Parallel Port Delay from Interrupt to $\overline{ACK}$		t_{28}	—	25	ns

*Baud Output Cycle

3.0 AC CHARACTERISTICS (Continued)

Parameter	Test Conditions	Symbol	Guaranteed Limits		Unit
			Min	Max	
PRINTER INTERFACE TIMING (Figure 8)					
Data Valid to Strobe		t_{29}	0.5	—	µs
Strobe Width		t_{30}	0.5	—	µs
Strobe Rising to Data Change		t_{31}	0.5	—	µs
Acknowledge Pulse Width		t_{32}	5	—	µs

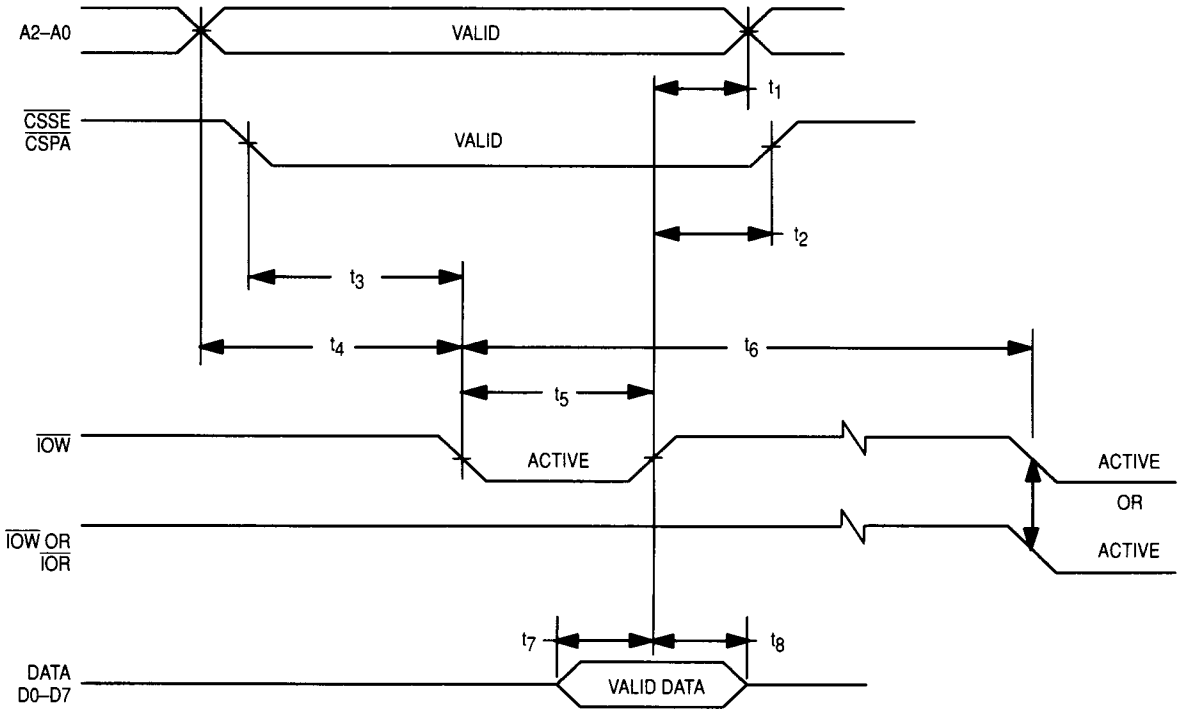


Figure 1. Write Cycle Timing

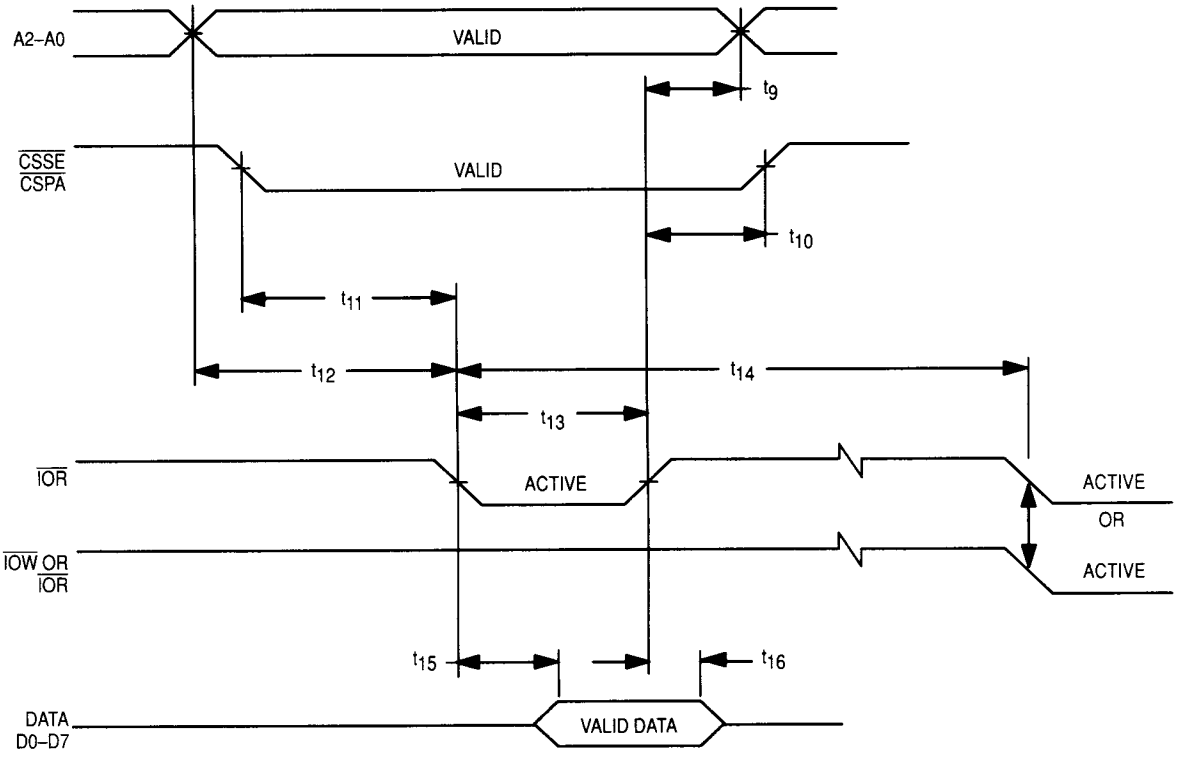


Figure 2. Read Cycle Timing

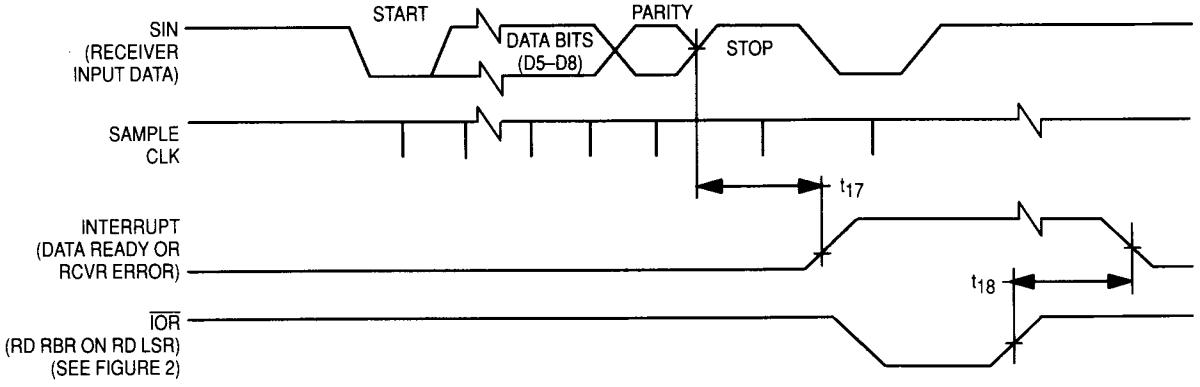


Figure 3. Receiver Timing

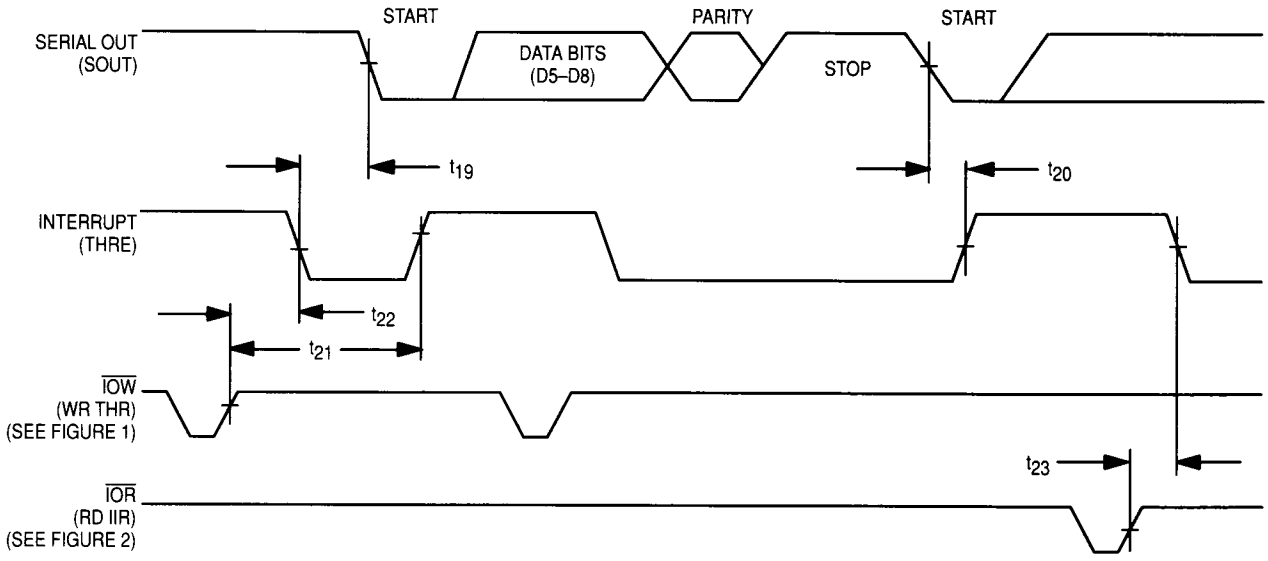


Figure 4. Transmitter Timing

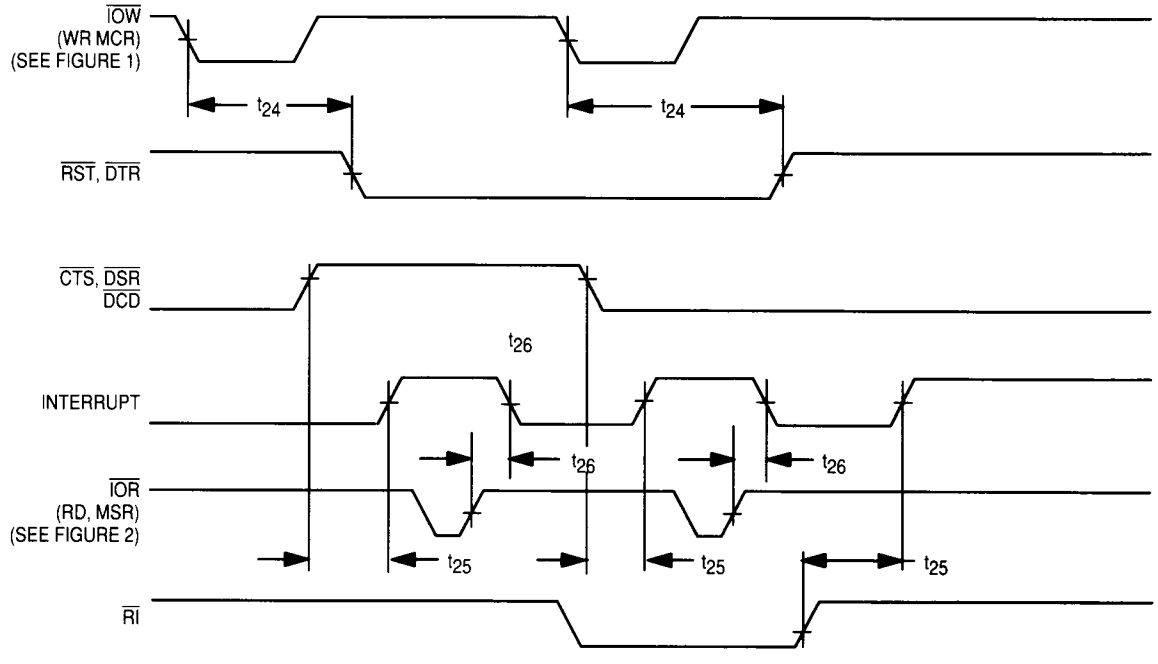


Figure 5. Modem Control Timing

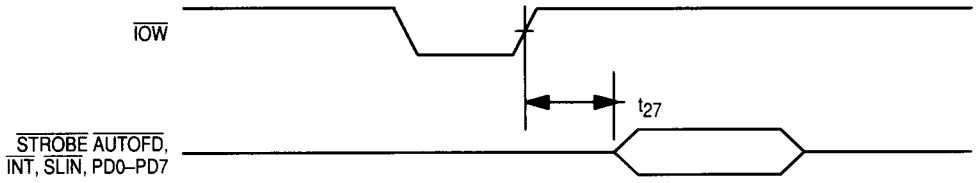


Figure 6. Parallel Port Data Register and Control Register Timing

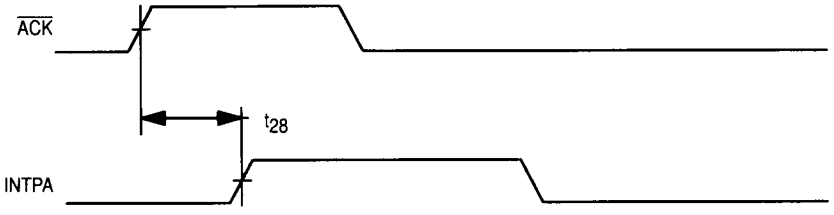


Figure 7. Parallel Port Interrupt Timing

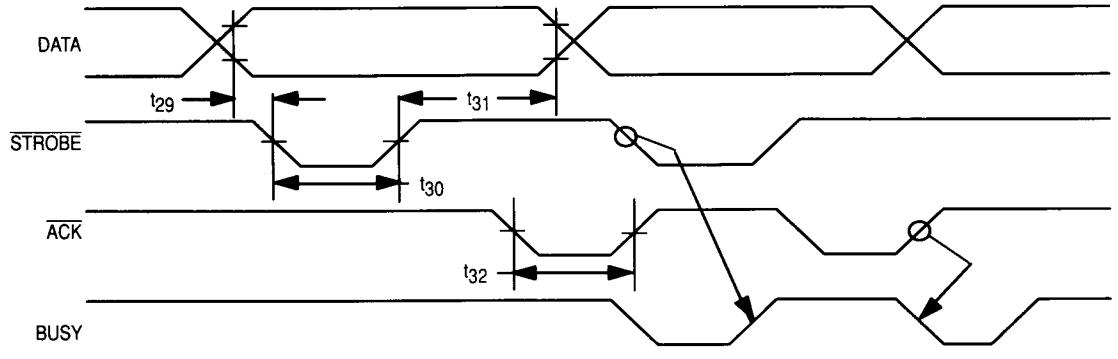


Figure 8. Printer Interface Timing

4.0 PIN DESCRIPTIONS

In this section of the data sheet the term receiving device or modem refers to the device connected to the MCCS16C451. The term sending device refers to the MCCS16C451. The term remote device refers to a device located at another location which is sending or receiving data from the location of the MCCS16C451.

$\overline{\text{LPTOE}}$ — LINE PRINTER OUTPUT ENABLE (Input, Pin 1)

When active low, the parallel data output enable signal enables the Write Data Registers to PD0–PD7. A logic high on this pin along with a logic high or 1 in bit 5 of the Write Control Register puts PD0–PD7 in a high impedance state where they can be used as inputs without the output latched data being looped back into the input port.

X_{in} — CLOCK IN (Input, Pin 4)

This pin is connected to an external clock source. This clock can be from any TTL source such as a oscillator or a system clock divided down. The frequency of the clock should be 1.8432, 2.4576, or 3.072 MHz. See Tables 13, 14, and 15.

DB0–DB7 — DATA BUS (Input/Output Pins 14–21)

These pins are the medium for transferring data to and from the MCCS16C451. These pins drive the data bus while $\overline{\text{CSSE}}$ or $\overline{\text{CSPA}}$ and $\overline{\text{IOR}}$ are active and they accept data while $\overline{\text{CSSE}}$ or $\overline{\text{CSPA}}$ and $\overline{\text{IOW}}$ are active. When $\overline{\text{CSSE}}$ or $\overline{\text{CSPA}}$ is not active, these pins are in a three-state mode where they neither drive nor accept data.

$\overline{\text{RTS}}$ — REQUEST TO SEND (Output, Pin 24)

When active low, this pin informs the modem or any receiving device that the MCCS16C451 is to send data. This signal is paired with a $\overline{\text{CTS}}$ (Clear To Send) signal coming from the modem or receiving device. See $\overline{\text{CTS}}$ for additional information.

$\overline{\text{DTR}}$ — DATA TERMINAL READY (Output, Pin 25)

When active low, this pin informs the modem or any receiving device that the MCCS16C451 is powered up and is ready to establish the communications link. This signal is paired with the $\overline{\text{DSR}}$ (Data Set Ready) signal. See $\overline{\text{DSR}}$ for additional information.

SOUT — SERIAL OUT (Output, Pin 26)

This pin delivers serial data to the receiving device or modem.

$\overline{\text{CTS}}$ — CLEAR TO SEND (Input, Pin 28)

This pin, when active low, indicates to the MCCS16C451 that the modem or receiving device is ready to receive data from the MCCS16C451. This signal is paired with $\overline{\text{RTS}}$ (Request To Send). See $\overline{\text{RTS}}$ for additional information.

$\overline{\text{DCD}}$ — DATA CARRIER DETECT (Input, Pin 29)

This pin, when active low, informs the MCCS16C451 that the receiving device or modem has detected a carrier wave or carrier signal. The carrier precedes the synchronization of data in the transmission bit stream. This signal indicates to the host that data will be transmitted from the remote site soon.

$\overline{\text{RI}}$ — RING INDICATOR (Input, Pin 30)

When active low, this pin indicates to the MCCS16C451 that the modem or data set has detected a ringing condition on the phone line. The modem or data set then is responsible for taking the phone line "OFF HOOK" to complete the call. However, the MCCS16C451 may be called upon to send an "OFF HOOK" command to the modem or data set.

$\overline{\text{DSR}}$ — DATA SET READY (Input, Pin 31)

This pin, when active low, indicates to the MCCS16C451 that the data set or modem is powered up and ready to establish the communications link. This signal is paired with the $\overline{\text{DTR}}$ (Data Terminal Ready) signal. See $\overline{\text{DTR}}$ for additional information.

$\overline{\text{CSSE}}$ — SERIAL PORT CHIP SELECT (Input, Pin 32)

When active low, this pin informs the MCCS16C451 that a data transfer is going to take place on the serial port. At this point, the address bus is sampled to determine the correct register or data location to select. The data bus is readied to receive data from the host if $\overline{\text{IOW}}$ also takes place or to drive the bus if $\overline{\text{IOR}}$ is also active. See $\overline{\text{IOW}}$ and $\overline{\text{IOR}}$ for more information.

A0–A2 — ADDRESS BUS (Input, Pins 33–35)

These pins along with bits in the control registers are used to select the proper register or data buffer (see Table 2). This address is used along with $\overline{\text{CSSE}}$, $\overline{\text{CSPA}}$, $\overline{\text{IOR}}$, and $\overline{\text{IOW}}$.

$\overline{\text{IOW}}$ — INPUT/OUTPUT WRITE (Input, Pin 36)

This active low input informs the MCCS16C451 that the system is preforming a write operation to the Input/Output bus. This pin is used in conjunction with the address pins and the $\overline{\text{CSSE}}$ or $\overline{\text{CSPA}}$ to perform a transfer of a byte of data from the system to the MCCS16C451.

$\overline{\text{IOR}}$ — INPUT/OUTPUT READ (Input, Pin 37)

This active low input informs the MCCS16C451 that the system is performing a read operation from the Input/Output bus. This pin is used in conjunction with the address pins and the $\overline{\text{CSSE}}$ or $\overline{\text{CSPA}}$ to perform a transfer of a byte of data from the system to the MCCS16C451.

$\overline{\text{CSPA}}$ — PARALLEL PORT CHIP SELECT (Input, Pin 38)

This pin, when active low, informs the MCCS16C451 that a data transfer is going to take place on the parallel port. At this point, the address bus is sampled to determine the correct register or data location to address. In addition, the data bus is readied to receive data from the host if $\overline{\text{IOW}}$ also takes place or, to drive the bus if $\overline{\text{IOR}}$ is active. See $\overline{\text{IOW}}$ and $\overline{\text{IOR}}$ for more information.

$\overline{\text{RESET}}$ — RESET (Input, Pin 39)

This pin, when active low, clears the parallel port control register and all serial port registers. The $\overline{\text{RESET}}$ signal must be valid for 500 ns for a valid reset to occur. See Table 16 for additional information.

SIN — SERIAL INPUT (Input, Pin 41)

This pin supplies the MCCS16C451 with serial data from a modem or data set.

BDO — BUS DATA OUTPUT (Output, Pin 44)

When high, BDO indicates that a serial or parallel port is being read from. When low, BDO indicates that a serial or parallel port is being written to. This pin can and should be used to enable a bus transceiver like the 74F245.

INTSE — SERIAL INTERRUPT (Output, Pin 45)

This three-stated active-high output is used to indicate to the system/host that the MCCS16C451 needs to be serviced. The interrupt is cleared by reading the interrupt register. The Interrupt Enable bit in the Interrupt Register also needs to be set to a 1 for the interrupt pin to occur.

PD0–PD7 — PARALLEL PORT DATA BUS (Input/Output Pin 46–53)

These pins supply data to and from the Parallel port. In normal operation these pins only output data to a parallel printer; however, they may also read data from devices connected to this port.

NOTE

The BIOS of a standard IBM PC/XT/AT does not support the flow of data from the printer to the system through these pins. This function works in conjunction with the $\overline{\text{LPTOE}}$ pin description. See $\overline{\text{LPTOE}}$, Figure 10, and Section 16 for more information.

$\overline{\text{STROBE}}$ — PRINTER STROBE (Input/Output, Pin 55)

This open-drain to ground signal, when active low, indicates to the printer that the data on the Printer Data Bus is stable and is ready to be read.

$\overline{\text{AUTOFD}}$ — AUTO-FORM FEED (Input/Output, Pin 56)

This signal, when active low, indicates to the printer that a line feed should be executed at the completion of every line printed. This is the hardware method of line feed. The software usually handles this operation.

$\overline{\text{INIT}}$ — PRINTER INITIALIZE (Input/Output, Pin 57)

This signal, when active low, indicates to the printer that its internal initialization routine should begin, and the internal print buffer should be cleared.

$\overline{\text{SLIN}}$ — PRINTER SELECT IN (Input/Output, Pin 58)

This signal, when active low, informs the printer that data will be coming soon. This signal must be active before the printer can receive data.

IRQPA — PARALLEL PORT INTERRUPT REQUEST (Output, Pin 59)

This three-stated active-high signal informs the system/host that the printer is ready for more data to be printed.

$\overline{\text{ERROR}}$ — PRINTER ERROR (Input, Pin 63)

This pin, when active low, indicates to the MCCS16C451 that the printer has developed an general error. The errors may include; 1) paper ended, 2) printer is off-line, or 3) printer in any other error state.

SLCT — PRINTER SELECTED (Input, Pin 65)

This pin, when active high, indicates to the MCCS16C451 that the printer is selected and ready to receive data to be printed.

BUSY — PRINTER BUSY (Input, Pin 66)

This pin, when active high, indicates to the MCCS16C451 that the printer is busy and is not ready to accept more data to be printed. This signal is active during; 1) data transfer, 2) print operation, 3) printer off-line, or 4) printer error state.

PE — PAPER EMPTY (Input, Pin 67)

This pin, when active high, indicates that the printer has run out of paper.

$\overline{\text{ACK}}$ — DATA ACKNOWLEDGMENT (Input, Pin 68)

This pin, when active high, indicates to the MCCS16C451 that the data that was just sent has been received by the printer and has been accepted.

V_{DD} — POWER (Input, Pins 3, 23, 40, 64)

+ 5 volts positive supply voltage. V_{DD} can range from + 4.75 to + 5.25 volts with respect to V_{SS}.

V_{SS} — POWER (Pins 7, 22, 27, 42, 43, 54, 61)

These pins supply the device with system ground.

RESERVED (Pins 2, 5, 6, 8, 13, 62)

These pins are reserved for other functions and should be connected to V_{SS}.

NC — NO CONNECT (Pins 9, 10, 11, 12, 60)

These pins have no internal connections.

5.0 FUNCTIONAL DESCRIPTION

The MCCS16C451 is a solution that provides one serial port and one bidirectional parallel port for an IBM PC/XT/AT compatible systems or any microprocessor system.

The serial port interface converts data from peripheral devices or modems from serial-in-data to parallel-out-data, which is supplied to the system data bus. Data provided by the CPU is converted from parallel-in-data to serial-out-data through the SOUT pin. The status of the parallel/asynchronous receiver transmitter can be read during any CPU operation. Status includes type and condition of the transfer operation in progress, and error conditions.

The MCCS16C451 provides a bidirectional parallel data port that supports a parallel Centronics type printer. The parallel port and serial port together, provide PC/AT compatible computers with a single device serving two systems ports.

The MCCS16C451 uses a TTL oscillator as the input clock source and can be connected, with the addition of buffers, to standard parallel and serial connectors on either an XT or AT compatible system. The external components required include: a high-power driver device, address decoding, clock source, and any interrupt request level devices. Refer to Figure 9 for applications circuitry.

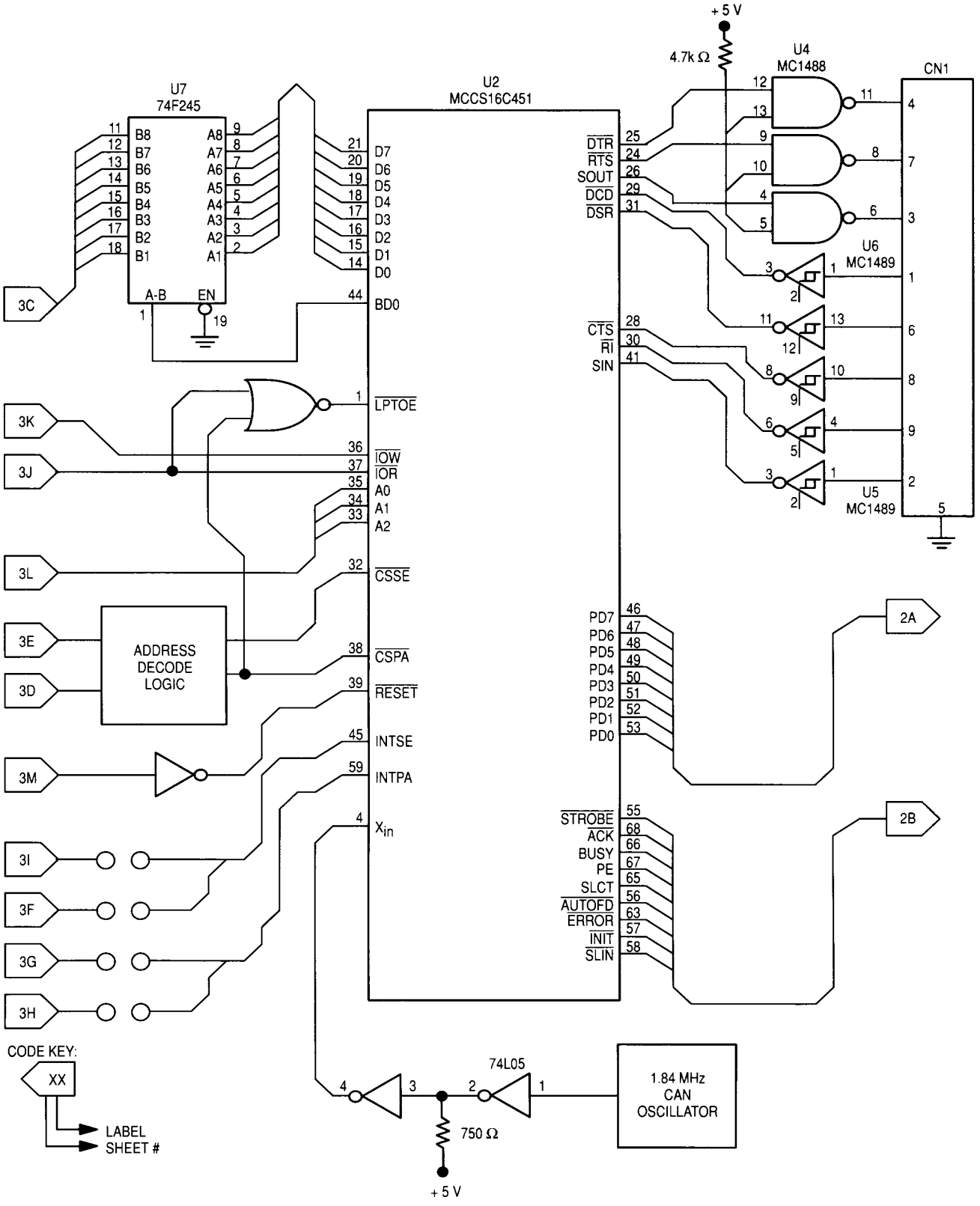


Figure 9. Application Circuit (Sheet 1 of 3)

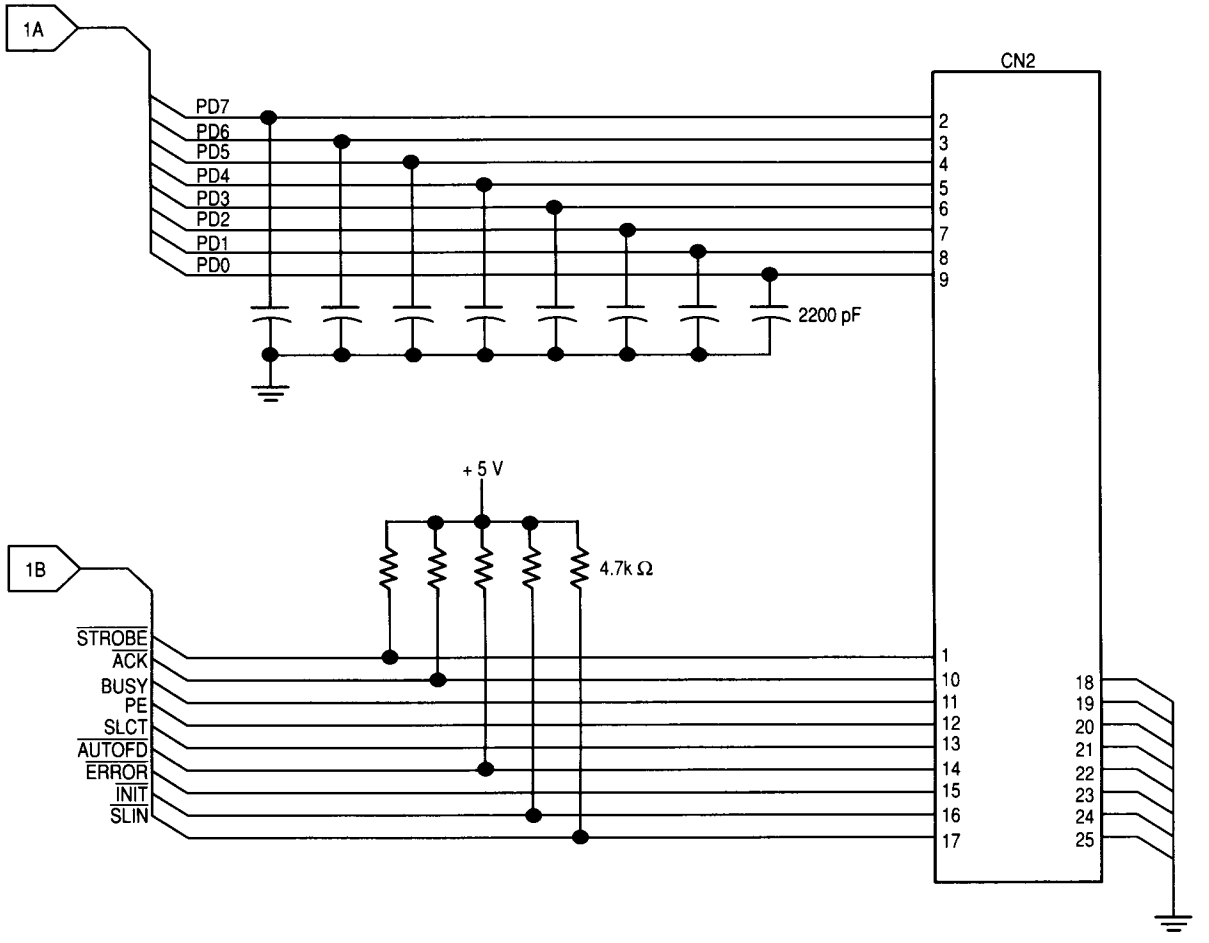


Figure 9. Application Circuit (Sheet 2 of 3)

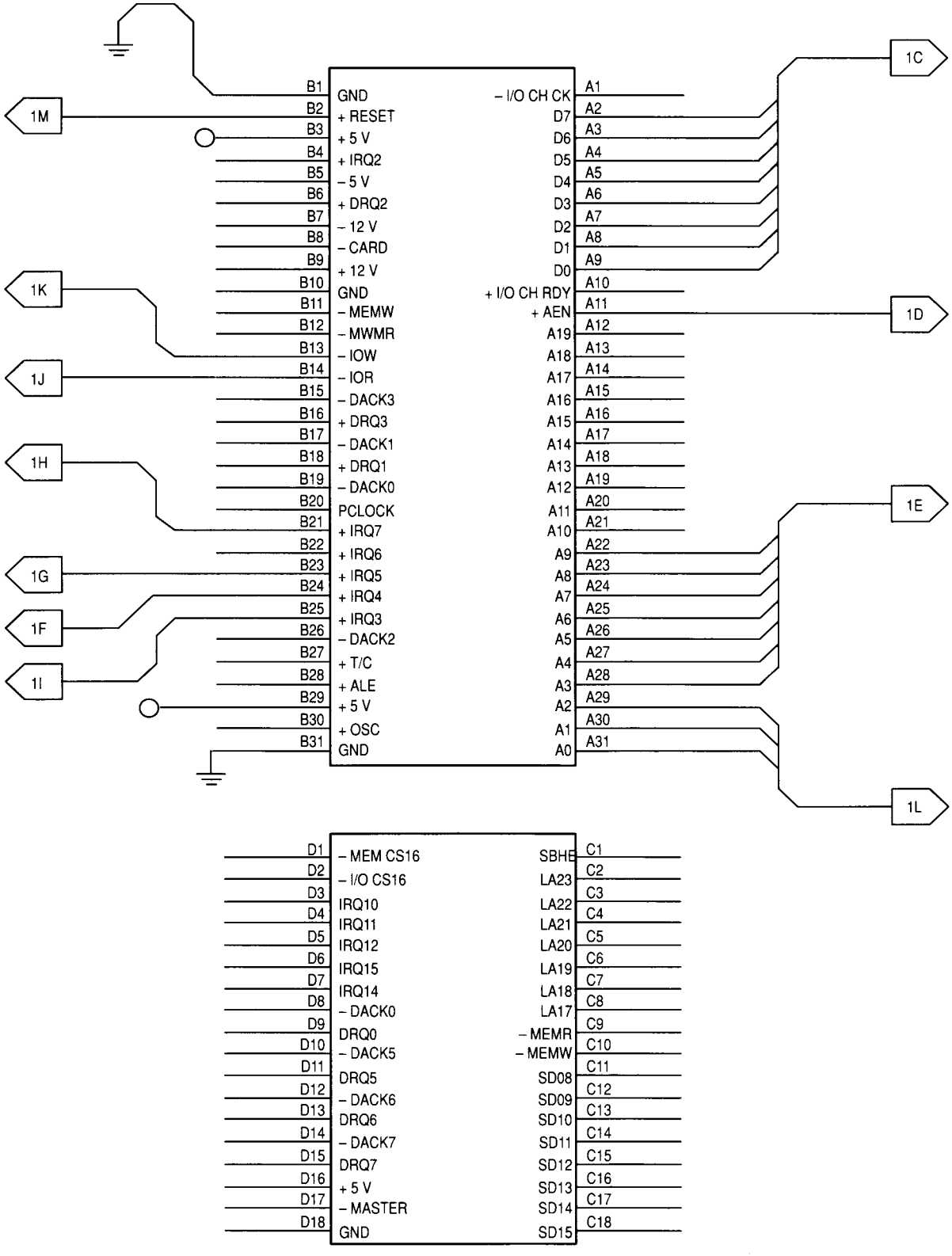


Figure 9. Application Circuit (Sheet 3 of 3)

6.0 SERIAL PORT INTERFACE

The serial port interface has three types of internal registers. A programmable baud rate generator divides the timing reference clock input by a divisor between 1 and $2^{16}-1$.

Control Registers

Bit Rate Select Register (DLL) (Division Latch LSB)
Bit Rate Select Register (DLM) (Division Latch MSB)
Line Control Register (LCR)
Interrupt Enable Register (IER)
Interrupt Identification Register (IIR)
Modem Control Register (MCR)

Status Registers

Line Status Registers (LSR)
Modem Status Registers (MSR)

Data Registers

Receiver Buffer Register (RBR)
Transmitter Holding Register (THR)
Scratch Register (SR)

Table 1. Serial Port Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Receiver Buffer Register (Read Only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1 (LSB)	Data Bit 0 (LSB)
Transmitter Holding Register (Write Only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Interrupt Enable Register	0	0	0	0	Enable Modem Status Interrupt	Enable Receiver Line Status Interrupt	Enable Transmitter Holding Register Interrupt	Enable Received Data Available Interrupt
Interrupt Identification Register	0	0	0	0	0	Interrupt ID Bit 1	Interrupt ID Bit 0	0 – If Interrupt Pending
Line Control Register	Division Latch Address Bit	Set Break	Stick Parity	Even Parity Select	Parity Enable	Number of Stop Bits	Word Length Select Bit 1	Word Length Select Bit 0
Modem Control Register	0	0	0	Loop Back	Out 2	Out 1	Request to Send	Data Terminal Ready
Line Status Register	0	Transmitter Empty	Transmitter Hold Register Empty	Break Interrupt	Framing Error	Parity Error	Overrun Error	Data Ready
Modem Status Register	Data Carrier Detect	Ring Indicator	Data Set Ready	Clear To Send	Delta Receiver Line Signal Detect	Trail Edge Ring Indicator	Delta Data Set Ready	Delta Clear To Send
Scratch Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

NOTE: Address, read, and write inputs are used with the Divisor Latch bit (DLAB) in the Line Control Register bit 7 to select the register to be read or written. Refer to Table 2 for register select states.

Table 2. Serial Port Internal Register Selection

DLAB (LCR Bit 7)	A2	A1	A0	Register
0	0	0	0	Receiver Buffer Register (Read Only)
0	0	0	0	Transmitter Holding Register (Write Only)
0	0	0	1	Interrupt Enable Register
X	0	1	0	Interrupt Identification Register (Read Only)
X	0	1	1	Line Control Register
X	1	0	0	Modem Control Register
X	1	0	1	Line Status Register
X	1	1	0	Modem Status Register
X	1	1	1	Scratch Register
1	0	0	0	Divisor Latch LSB
1	0	0	1	Divisor Latch MSB

NOTE: $\overline{\text{CSSE}}$ must also be low for any serial register to be accessed.
X = Don't Care
1 = Logic High
0 = Logic Low

6.1 TRANSMITTER HOLDING REGISTER AND RECEIVING BUFFER REGISTER

The Transmitter Holding Register (THR) and Receiving Buffer Register (RBR) are data registers that hold from five to eight bits of data. If fewer than eight data bits are transmitted or received, bit 0 is always the first serial data bit received or transmitted. Data registers are buffered twice to allow read and write operations to be executed at the same time the UART is converting parallel-to-serial or serial-to-parallel.

6.2 LINE CONTROL REGISTER

The Line Control Register (LCR) controls the data character format. The contents of the LCR can be read precluding the need to store line characteristics in system memory. Table 3 contains a bit definition summary of the Line Control Register.

Bit Function

0–1 The number of bits in each serial character is programmed according to the following states.

Bit 1	Bit 2	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

2 Specifies the number of stop bits in each character transmitted.
0 — One stop bit is generated in the transmitted data.
1 — If a 5-bit word is selected, 1.5 stop bits are generated. If 6-, 7-, or 8-bit word is selected two stop bits are generated. A programmed receiver checks for two stop bits.

3 Parity Enable Bit
1 — Generates and checks a parity bit between the last data word bit and stop bit.

Table 3. Line Control Register Bit Function Summary

Bit	Function	Logic High	Logic Low
0	Word Length Select Bit 0	*	*
1	Word Length Select Bit 1	*	*
2	Stop Bit Select	1.5 or 2 Stop Bits	1 Stop Bit
3	Parity Enable	Enabled	Disabled
4	Even Parity Select	Even Parity	Odd Parity
5	Stick Parity	Enabled	Disabled
6	Set Break	Enabled	Disabled
7	Divisor Latch Access Bit (DLAB)	Access Divisior Latches	Access Receiver, Transmitter, Interrupt Enable Registers

*See Text Section 6.2.

4 Parity type selection is sampled only if bit 3 above is a 1.
1 — Even parity selected
0 — Odd parity selected

5 Parity stick bit is active only if bit 3 is a 1.
1 — A parity bit is transmitted and received in the opposite state from the state indicated by bit 4 above. Parity can therefore be forced to a known state and the receiver can check the parity bit in a known state.

6 Set Break Bit
1 — Serial data is forced to the spacing, logic low, state. The break is disabled when this bit is set to 0. Bit 6 acts only on serial output and has no effect on the transmitting logic. Bit 6 enables the CPU to alert a terminal in a computer system. If the following sequence is used, erroneous or extraneous characters are not transmitted because of the break.
1) Load an all zero pad character in response to Line Status Register Bit 5.
2) Set break in response to the next Line Status Register Bit 5
3) Wait for the transmitter to become idle (Line Status Register Bit 6 is set), and clear break when normal transmission must be restored.

7 Divisor Latch Address Bit
1 — Enable access to the divisor latches DLL and DLM of the baud rate generator during a read or write operation. This bit must be input low to access the receiver buffer, the transmitter holding, or the interrupt enable registers.

6.3 LINE STATUS REGISTER

The Line Status Register is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of the serial port interface. Refer to Table 4 for a bit definition summary. Bits 1, 2, and 3 are three error flags that provide the status of an error condition detected in the receiver circuitry: Overrun error, Framing error, and Parity error. Error flags are set high by an error condition when stop bits are received. The absence of an error condition in the next character received does not reset the error flags. The flags reflect the last character only if no overrun occurred.

Table 4. Line Status Register Bit Definition Summary

Bit	Function	Logic High	Logic Low
0	Data Ready (DR)	Ready	Not Ready
1	Overrun Error (OE)	Error	No Error
2	Parity Error (PE)	Error	No Error
3	Framing Error (FR)	Error	No Error
4	Break Interrupt (BI)	Break	No Break
5	Transmitter Holding Register Empty (THRE)	Empty	Not Empty
6	Transmitter Empty (TEMT)	Empty	Not Empty
7	Not Used	—	Always Low

Bit Function

0 **Data Ready** — Indicates that the Receiver Buffer Register has been loaded with a received character (including Break) and that the CPU can access this Data. This bit is set high when an incoming character is received and transferred into the Receiver Buffer Register. When the CPU reads the data in the Receiver Buffer Register, this bit is reset low.

1 **Overrun Error** — This bit indicates an error condition that produced a Receiver Line Status Interrupt (priority 1 interrupt in the Interrupt Identification Register). See the Interrupt Enable Register bits 2 and 1 for information on enabling this interrupt. If logic 1, this bit indicates that an overrun error has occurred. Overrun error means that the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, overwriting the previous character. This bit is reset when the CPU reads the contents of the Line Status Register.

2 **Parity Error** — A parity error means that the last character received had a parity error based on the programmed and calculated parity of the received character (Line Control Register bit 4). This bit is set high when a parity error is detected and reset low when the CPU reads the contents of the Line Status Register. This bit indicates an error condition that produced a Receiver Line Status Interrupt (priority 1 interrupt in the Interrupt Identification Register). See the Interrupt Enable Register bits 2 and 1 for information on enabling this interrupt.

3 **Framing Error** — A framing error means that the last character received had an incorrect (low) stop bit, caused when the required stop bit is absent or by a stop bit too short to be detected. This bit is high when the stop bit following the last data bit or parity bit is detected as a zero (spacing level). This bit is reset low when the CPU reads the contents of the Line Status Register. This bit indicates an error condition that produced a Receiver Line Status Interrupt (priority 1 interrupt in the Interrupt Identification Register). See the Interrupt Enable Register bits 2 and 1 for information on enabling this interrupt.

4 **Break Interrupt** — This bit indicates that the last character received was a break character. A break character is defined as an invalid but complete data character, including parity and stop bits. This bit is set high when the received data input is held in the spacing (logic 0) state for a longer time than a full word transmission time (start bit + data bits + parity + stop bits). This bit will reset when the CPU reads the contents of the Line Status Register.

5 **Transmitter Holding Register Empty** — This bit indicates that the Transmitter Holding Register is empty and can receive another character. If the interrupt is enabled (Interrupt Enable Register bit 1), this bit (when active) causes an interrupt. The interrupt is cleared when the Interrupt Identification Register is read.

Bit 5 is set high when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. This bit is reset low when the CPU loads the Transmitter Holding Register with the next byte to be transferred. Bit 5 is not reset when the CPU reads the Line Status Register.

6 **Transmitter Empty** — This bit is set high when the Transmitter Holding Register and the Transmitter Shift Register are both empty. When a character is loaded into the Transmitter Holding Register, this bit is set low and remains low until the character is transferred out of SOUT (Serial output pin). Bit 6 is not reset when the CPU reads the Line Status Register.

7 **Not Used** — This bit is not used and is always 0.

6.4 MODEM CONTROL REGISTER

The Modem Control Register controls the interface with the modem or data set. This register can be read from or written to. The $\overline{RTS}$ and $\overline{DTR}$ outputs are the respective control bits in this register. A high input asserts a low at the output pins. Table 5 contains a bit definition summary for the Modem Control Register.

Table 5. Modem Control Register Bit Definition Summary

Bit	Function	Logic High	Logic Low
0	Data Terminal Ready	$\overline{DTR}$ Pin = 0	$\overline{DTR}$ Pin = 1
1	Request To Send	$\overline{RTS}$ Pin = 0	$\overline{RTS}$ Pin = 1
2	Programmable Out 1	See Text	
3	Programmable Out 2	See Text	
4	Loop	Internal Loop	External Loop
5	Not Used	—	Always Low
6	Not Used	—	Always Low
7	Not USed	—	Always Low

Bit Function

0 **Data Terminal Ready** — When set to a logic 1, the Data Terminal Ready output is forced to a logic 0. When this bit is reset to a logic 0, the Data Terminal Ready Output if forced to a logic 1.

1 **Request To Send** — When set to a logic 1, the Request To Send output is forced to a logic 0. When this bit is reset to a logic 0, the Request To Send output is forced to a logic 1.

2 **Programable Out 1** — This bit is tied to bit 6 of the Modem Status Register during internal loopback mode. This bit is changeable by the programmer and indicates RI in the MSR.

3 **Programable Out 2** — This bit is tied to bit 7 of the Modem Status Register during internal loopback mode. This bit is changeable by the programmer and indicates DCD in the MSR.

4 **Loop** — This bit provides a local loopback feature to perform diagnostic testing of the channel. When set to a logic 1, SOUT if set to the marking state, logic 1, and the receiver data input Serial Input (SIN) is disconnected. The output of the Transmitter Shift Register is looped back into the Receiver Shift Register input. The four modem control inputs are disconnected. Modem control outputs are disconnected and routed to the four modem control inputs internally. Modem control output pins are forced to the logic 1 state (inactive state). In the diagnostic mode, data transmitted is received immediately so the processor can verify the transmit and receive data paths of the selected serial port.

In loopback mode, MCR bits are tied to bits in MSR in the following format:

MCR	MSR	Function
Bit 0	Bit 5	Tests Data Terminal Ready to Data Set Ready circuit.
Bit 1	Bit 4	Tests Request to Send to Clear to Send circuit.
Bit 2	Bit 6	Tests Ring Indicator circuit.
Bit 3	Bit 7	Tests Data Carrier Detect circuit.

5 **Not Used** — This bit is not used and is always 0.

6 **Not Used** — This bit is not used and is always 0.

7 **Not Used** — This bit is not used and is always 0.

6.5 MODEM STATUS REGISTER

The Modem Status Register provides the CPU with the status of the modem input lines from the modem or peripheral device. The CPU can read the modem signal inputs by accessing the data bus interface of the MCCS16C451. Four bits in this register indicate if the modem inputs have changed since the last read of the Modem Status Register. These bits are set high when a control input from the modem changes state. When the CPU reads the Modem Status Register, these bits are reset low.

The $\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$, and $\overline{DCD}$ signals are the modem input lines for the channel. Bits 4 through 7 are status indications of these lines. If the modem status interrupt in the Interrupt Enable Register bit 3 is enabled, a change of state in a modem input signal is reflected by the modem status bits in the IIR Register and an interrupt is generated. The Modem Status Register is a priority 4 interrupt. Refer to Table 6 for bit definitions. Note that the state of the status bit is an inverted version of the actual input pin.

Table 6. Modem Status Register Bit Definition Summary

Bit	Function	Mnemonic
0	Delta Clear To Send	DCTS
1	Delta Data Set Ready	DDSR
2	Trailing Edge of Ring Indicator	TERI
3	Delta Data Carrier Detect	DDCD
4	Clear To Send	CTS
5	Data Set Ready	DSR
6	Ring Indicator	RI
7	Data Carrier Detect	DCD

Bit Function

0 **Delta Clear To Send** — Indicates that bit 4 and the corresponding input to the serial port interface has changed state since the last time it was read by the CPU.

1 **Delta Data Set Ready** — Indicates that bit 5 and the corresponding input to the serial port interface has changed state since the last time it was read by the CPU.

2 **Trailing Edge of Ring Indicator** — Indicates that bit 6 and the corresponding input to the serial port interface has changed state high-to-low since the last time it was read by the CPU. Low-to-high transition on bit 6 does not activate this bit.

3 **Delta Data Carrier Detect** — Indicates that bit 7 and the corresponding input to the serial port interface has changed state since the last time it was read by the CPU.

4 **Clear To Send** — This bit is the status of the Clear To Send input from the modem. This input tells the serial port that the modem is ready to receive data from the transmitter output of the serial port. If the serial port interface is in loop mode, Modem Control Register bit 4 = 1, this bit is equivalent to the Modem Control Register bit 1, Request To Send.

5 **Data Set Ready** — This bit is the status of the Data Set Ready input from the modem to the serial port. This input tells the CPU that the modem is ready to provide Received data to serial port receiver circuitry. If the serial port interface is in loop mode, Modem Control Register bit 4 = 1, this bit is equivalent to the Modem Control Register bit 0, Data Terminal Ready.

6 **Ring Indicator** — This bit indicates the status of the $\overline{RI}$ pin. If the serial port interface is in loop mode, Modem Control Register bit 4 = 1, this bit is the equivalent to Modem Control Register Bit 2.

7 **Data Carrier Detect** — Indicates the status of the receiver line carrier data detect signal input. If the serial port interface is in loop mode, Modem Control Register bit 4 = 1, this bit is the equivalent to Modem Control Register Bit 3.

Modem status inputs reflect the modem input lines with any change of status. Reading the Modem Status Register clears the delta modem status indications but does not affect the status bits. The status bits reflect the state of the input pins regardless of mask control signals. If bits 0–3 are true and a state change occurred during a read operation, the state changed is not reflected in the Modem Status Register. If bits 0–3 are false, the state change is indicated after the CPU read operation.

Setting status bits is inhibited for the Line Status Register and Modem Status Register during status read operations. If a status condition is generated during a CPU read, the status bit is not set until the trailing edge of the read operation.

If a status bit is set during a read operation and the same status condition occurs, that status bit is cleared at the trailing edge of the read instead of being set again.

6.6 DIVISOR LATCHES

The MCCS16C451 serial port interface contains a programmable baud rate generator that divides the clock from DC to frequency of the clock input. Any divisor from 1 to 2^{16}-1 can be used. The output frequency of the baud generator is 16X the baud rate [DIVISOR# = (FREQUENCY INPUT) / (BAUD RATE $\times$16)]. The divisor is stored in a 16-bit binary format by two 8-bit divisor latch registers (DLL, DLM). These divisor latch registers must be loaded during initialization. A 16-bit baud counter is immediately loaded after either of the divisor latches is loaded to prevent long counts on initial load.

6.7 RECEIVER BUFFER REGISTER

The MCCS16C451 serial port receiver circuitry is programmable for 5, 6, 7, or 8 data bits per character. Words with less than eight bits are right justified, LSB = Data bit 0, which is the first data bit received. Unused bits in a character less than eight bits are output as logic 0 to the parallel output by the serial port.

Data received at the SIN, Serial Input pin is shifted into the Receiver Shift Register by the 16X Clock provided by the Baud Rate Generator. Based on the position of the start bit, this clock is synchronized to the incoming data. When a complete character is shifted into the Receiver Shift Register, the assembled data bits are loaded in parallel into the Receiver Buffer Register. The Data Ready flag in the Line Status Register is set.

The data received is buffered twice to permit continuous data reception without loss of data. As the Receiver Shift Register is shifting a new character from the serial port, the Receiver Buffer Register is holding a previously received character for the CPU. If data in the Receiver Buffer Register in not read before complete reception of the next character, the data in the Receiver Register is lost, and the overrun error flag (bit 1 of the Line Status Register) is set to a 1. Table 7 contains a Receiver Buffer bit definition.

Table 7. Receiver Buffer Register Bit Definition

Bit	Function
0	Data Bit 0
1	Data Bit 1
2	Data Bit 2
3	Data Bit 3
4	Data Bit 4
5	Data Bit 5
6	Data Bit 6
7	Data Bit 7

6.8 TRANSMITTER HOLDING REGISTER

The Transmitter Holding Register holds parallel data from the data bus until the Transmitter Shift Register is empty and ready to accept a new character. The receiver and transmitter word length along with the number of stop bits are the same. If the character has less than eight bits, unused bits are ignored by the transmitter at the microprocessor data bus. Table 8 contains the bit definition of the Transmitter Holding Register.

Table 8. Transmitter Holding Register Bit Definition

Bit	Function
0	Data Bit 0
1	Data Bit 1
2	Data Bit 2
3	Data Bit 3
4	Data Bit 4
5	Data Bit 5
6	Data Bit 6
7	Data Bit 7

Bit 5 of the Line Status Register reflects the status of the Transmitter Holding Register. It shows if both the Transmitter Holding Register and Transmitter Shift Register are Empty.

6.9 SCRATCH REGISTER

The Scratch Register is an 8-bit read/write register. This register does not affect the port of the MCCS16C451. It is used by programmers to hold data temporarily. Table 9 contains bit definitions of the Scratch Register.

Table 9. Scratch Register Bit Definition

Bit	Function
0	Data Bit 0
1	Data Bit 1
2	Data Bit 2
3	Data Bit 3
4	Data Bit 4
5	Data Bit 5
6	Data Bit 6
7	Data Bit 7

6.10 INTERRUPT IDENTIFICATION REGISTER

The Interrupt Identification Register contains the interrupt status of the MCCS16C451. The serial port interface prioritizes interrupts into four levels to minimize software overhead during data character transfer. The four levels of interrupt condition include the following.

Priority Level	Function
1	Receiver Line Status
2	Receiver Data Ready
3	Transmitter Holding Register Empty
4	Modem Status

The Interrupt Identification register stores information on an interrupt that is pending and the type of that interrupt. When addressed during chip select time, this register indicates the highest priority interrupt pending. When no other interrupts are acknowledged by the unit the CPU services this interrupt. Table 10 contains Interrupt Identification Register bit definitions. Table 11 contains IIR Interrupt Identification set and reset information.

Table 10. Interrupt Identification Register Bit Definitions

Bit	Function	Logic High	Logic Low
0	Hard-wired priority or polled environment		Pending Interrupt
1–2	Identifies highest priority pending	*	*
3–7	Unused and are always 0		

*See Text Section 6.10.

Bit	Function
0	Used as either a hard-wired prioritized or polled environment. Indicates if an interrupt is pending. When this bit is 0 an interrupt is pending and the register contents can be used as a pointer to the appropriate interrupt service routine. When this bit is 1 no interrupt is pending.
1–2	Identifies the highest priority interrupt pending. See Table 11.
3–7	These bits are not used and are always set to 0.

Table 11. IIR Interrupt ID, SET, and $\overline{\text{RESET}}$

Interrupt Identification				Interrupt Set and $\overline{\text{RESET}}$ Functions		
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
X	X	1		None	None	
1	1	0	1	Receiver Line Status	OE, PE, FE, or BI	LSR Read
1	0	0	2	Received Data Available	Received Data Available	RBR Read
0	1	0	3	LSR(5)	LSR(5)	IIR read if THRE is source of interrupt else THR write
0	0	0	4	Modem Status	$\overline{\text{CTS}}$. $\overline{\text{DRS}}$, $\overline{\text{RI}}$, $\overline{\text{DCD}}$	MSR Read

X = Don't Care

6.11 INTERRUPT ENABLE REGISTER

The Interrupt Enable Register is a write-only register that enables the four serial port interrupts independently. The interrupts activate the interrupt output if they are enabled. All interrupts are disabled when bits 0–3 of this register are reset. Interrupts are enabled by setting the appropriate bits of this register to logic high. When interrupts are disabled, the Interrupt Identification Register and the active high INTR signal is inhibited. All other system functions operate normally, including the setting of the Line Status Register and the Modem Status Register. Table 12 contains Interrupt Enable Register bit definitions.

Table 12. Interrupt Enable Register Bit Definitions

Bit	Function	Logic High	Logic Low
0	Received Data Available Interrupt	Enabled	Disabled
1	Transmitter Holding Register Empty Interrupt	Enabled	Disabled
2	Receiver Line Status Interrupt	Enabled	Disabled
3	Modem Status Interrupt	Enabled	Disabled
4–7	Unused and are always 0	Enabled	Disabled

7.0 TRANSMITTING

The serial port interface transmitting function includes the Transmitter Holding Register, Transmitter Shift Register, and the associated control logic. Bits 5 and 6 in the Line Status Register indicate the status of the Transmitter Holding Register and the Transmitter Shift Register. To transmit a 5- to 8-bit word, the word is written to the Transmitter Holding Register through D0–D7. The microprocessor performs a write operation only if it is transmitting data.

When the transmitter is idle, bit 5 of the Line Status Register is high. This bit is set high when the word is automatically transferred from the Transmitter Holding Register to the Transmitter Shift Register and the start bit is transmitted.

When the transmitter is idle, bits 5 and 6 of the Line Status Register are high. The first word written causes bit 5 to be reset to zero. After the transfer, bit 5 returns high. Bit 6 remains low while the data word is transmitted. If a second character is transmitted to the Transmitter Holding Register, bit 5 of the Line Status Register is reset low. Because the data word cannot be transferred from the Transmitter Holding Register to the Transmitter Shift Register until it is empty, bit 5 of the Line Status register remains low until the word is completely transmitted. When the word is transmitted out of the Transmitter Shift Register, bit 6 of the Line Status Register is set high. Bit 5 of the Line Status Register is set high one transfer time later.

8.0 RECEIVING

Serial asynchronous data is input into SIN (Serial Input Pin). The idle state of the line providing the input into the SIN pin is logic high. The start bit detection circuitry continuously searches for a high-to-low transition. When a transition is detected, a counter is reset and counts by the 16X clock to 7.5, which is the center of the start bit. If the SIN signal is still low at the mid-bit sample of the start bit, the start bit is considered valid. By verifying the start bit, the receiver is prevented from assembling a false data character caused by a low going noise spike on the Serial Input Pin.

The Line Control Register determines the number of data bits in a character, the number of stop bits (if parity is used), and the type of parity. The Line Status Register provides status for the receiver to the Receiver Buffer Register. When the data is received, indicated by bit 0 of the Line Status Register being set high, the CPU reads the Receiver Buffer Register through D0–D7. This read resets bit 0 of the Line Status Register. If the RBR is not read before a new character transfer from the Receiver Shift Register to the Receiver Buffer Register, the overrun error status bit is set (Line Status Register bit 1). The parity check looks for even or odd parity on the parity bit which precedes the first stop bit. The parity error is set in Line Status Register bit 2 if an error is detected. If the stop bit is not high, a framing error is indicated by Line Status Register bit 3.

The center of the start bit is defined as clock count 7.5. If the data received by the Serial Input pin is a symmetrical square wave, the center of the data cells occur within ± 3.125% of the mid-point. This is a 46.875% error margin. The start bit can begin as much as one 16X clock cycle before it is detected.

9.0 BAUD RATE GENERATOR

The Baud Rate Generator generates clocking for the UART function and provides standard ANSI/CCITT bit rates. An external clock into X_{in} provides the oscillator driving the Baud Rate Generator.

The Divisor Latch Registers DLL and DLM, and the external frequency signal determine the data rate. The bit rate is selected by programming the two divisor latches. When DLL is set to 1 and DLM is set to 0 the divisor divides the X_{in} signal by 1 providing maximum baud rates for a given input frequency at the X_{in} input.

The Baud Rate Generator can use three different frequencies, 1.8432, 2.4576, or 3.072 MHz, to provide standard baud rates. With these frequencies, standard bit rates from 50 to 38.5 Kb/s are available. Refer to Tables 13, 14, and 15 for standard baud rates with these frequencies.

Table 13. Baud Rates fo 1.8432-MHz Clock Signal at X_{in}

Baud Rate	Divisor	Percent Error
50	2394	—
75	1536	—
110	1047	0.026
134.5	857	0.058
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.69
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
56000	2	2.86

Table 14. Baud Rates for 2.4576-MHz Clock Signal at X_{in}

Baud Rate	Divisor	Percent Error
50	3072	—
75	2048	—
110	1396	0.026
134.5	1142	0.0007
150	1024	—
300	512	—
600	256	—
1200	128	—
1800	85	0.392
2000	77	0.260
2400	64	—
3600	42	0.775
4800	32	—
7200	21	1.587
9600	16	—
19200	8	—
38400	4	—

Table 15. Baud Rates for 3.072-MHz Clock Signal at X_{in}

Baud Rate	Divisor	Percent Error
50	3840	—
75	2560	—
110	1745	0.026
134.5	1428	0.034
150	1280	—
300	640	—
600	320	—
1200	160	—
1800	107	0.312
2000	96	—
2400	80	—
3600	53	0.628
4800	40	—
7200	27	1.23
9600	20	—
19200	14	—
38400	5	—

10.0 RESETTING

The $\overline{\text{RESET}}$ input must be held low for 500 ns to reset MCCS16C451 circuits to an idle mode until initialization. A low state on the $\overline{\text{RESET}}$ signal causes the following events.

1) Initializes the transmitter and receiver internal clock counters.
2) Clears the Line Status Register except bits 5 and 6 which are set. Also clears the Modem Control Register. All discrete lines, memory elements and logic associated with these registers are also cleared or turned off. The Line Control Register, Divisor Latches, Receiver Buffer Register, and Transmitter Buffer Registers are not affected.

After the reset condition is removed, the MCCS16C451 remains idle until programmed. A hardware reset sets bit 5 and 6 of the Line Status Register. When interrupts are enabled bit 5 activates the interrupt. See Table 16 for more information.

Table 16. $\overline{\text{RESET}}$ Summary

Register/ Signal	$\overline{\text{RESET}}$ Control	$\overline{\text{RESET}}$
Interrupt Enable Register	Reset	All bits low (0–3 forced and 4–7 premanent)
Interrupt Identification Register	Reset	Bit 0 is high, bits 1–7 low
Line Control Register	Reset	All bits low
Modem Control Register	Reset	All bits low
Line Status Register	Reset	Bits 0–4 and 7 are low, bits 5–6 high
Modem Status Register	Reset	Bits 0–3 low, bits 4–7 input signal
Serial Output (SOUT)	Reset	All high
Interrupt RCVR Errors	Read LSR/ Reset	All low
Interrupt RCVR Data Ready	Read RBR/ Reset	All low
Interrupt LSR (5)	Read IIR/ Write THR/ Reset	All low
Interrupt Modem Change Status	Read MSR/ Reset	All low
$\overline{\text{RTS}}$	Reset	All high
$\overline{\text{DTR}}$	Reset	All high
$\overline{\text{SOUT}}$	Reset	All high

11.0 SOFTWARE RESETTING

A software reset returns the serial port to a completely known state without preforming a system reset. A software reset is accomplished by writing to the Line Control Registers, Divisor Latches, and Modem Control Register. The Line Status Registers and Receiver Buffer Register must be read before enabling interrupts to clear out residual data or status bits which can be invalid for subsequent operations.

12.0 PROGRAMMING

The serial port is programmed by the following control registers:

Bit Rate Select Register DLL (Divisor Latch LSB)
Bit Rate Select Register DLM (Divisor Latch MSB)
Line Control Register
Interrupt Enable Register
Modem Control Register

The control word defines the character length, number of stop bits, parity, baud rate, and modem interface. Then control registers can be written in any order, but the Interrupt Enable Register must be written last because it controls interrupt enables. After the serial port is programmed and operational, these registers can be updated whenever the serial port in not transmitting or receiving data.

13.0 PARALLEL PORT INTERFACE

The MCCS16C451 parallel port interface provides compatibility for the device and a Centronics type printer. When the $\overline{\text{CSPA}}$ signal is low, the parallel port is selected. Table 17 lists the registers associated with the parallel port interface.

See Table 22 for Address Map.

Table 17. Parallel Port Interface Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Read Status	BSY	$\overline{\text{ACK}}$	PE	SLCT	$\overline{\text{ERR}}$	1	1	1
Read Control	1	1	1	IRQEN	$\overline{\text{SLIN}}$	$\overline{\text{INIT}}$	$\overline{\text{AFD}}$	$\overline{\text{STROBE}}$
Write Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Write Control	1	1	DIR	IRQEN	$\overline{\text{SLIN}}$	$\overline{\text{INIT}}$	$\overline{\text{AFD}}$	$\overline{\text{STROBE}}$

The microprocessor reads information on the parallel bus through Read Data Register. The read and write functions of a register are controlled by the state of the read pin, $\overline{\text{IOR}}$, or the write pin, $\overline{\text{IOW}}$, and the parallel chip selects, $\overline{\text{CSPA}}$ and $\overline{\text{LPTOE}}$.

The $\overline{\text{LPTOE}}$ pin allows the printer bus (PD0–PD7) to be used as an input. In the typical application this pin is grounded so that the printer bus is only an output. When this pin is taken high the printer bus can be used to input data (e.g., from a scanner). See Figure 10 for the functional block diagram of $\overline{\text{LPTOE}}$. When $\overline{\text{LPTOE}}$ goes high and bit 5 of the Write Control Register (WCR) is 1 then the output data latch is put in a three-stated mode and the data buffer is used to input data from the PD0–PD7 bus to the D0–D7 bus on the microprocessor side of this device. When $\overline{\text{LPTOE}}$ and bit 5 of WCR is high or 1 will the output buffer be three-stated. In any other combination the output buffer will be looped back into the input buffer. Table 18 summaries this information. See also Figure 10 for more information.

Table 18. Printer Port Loopback Summary

WCR Bit 5	$\overline{\text{LPTOE}}$	Mode
0	0	Loopback
0	1	Loopback
1	0	Loopback
1	1	Data read from PD0–PD7

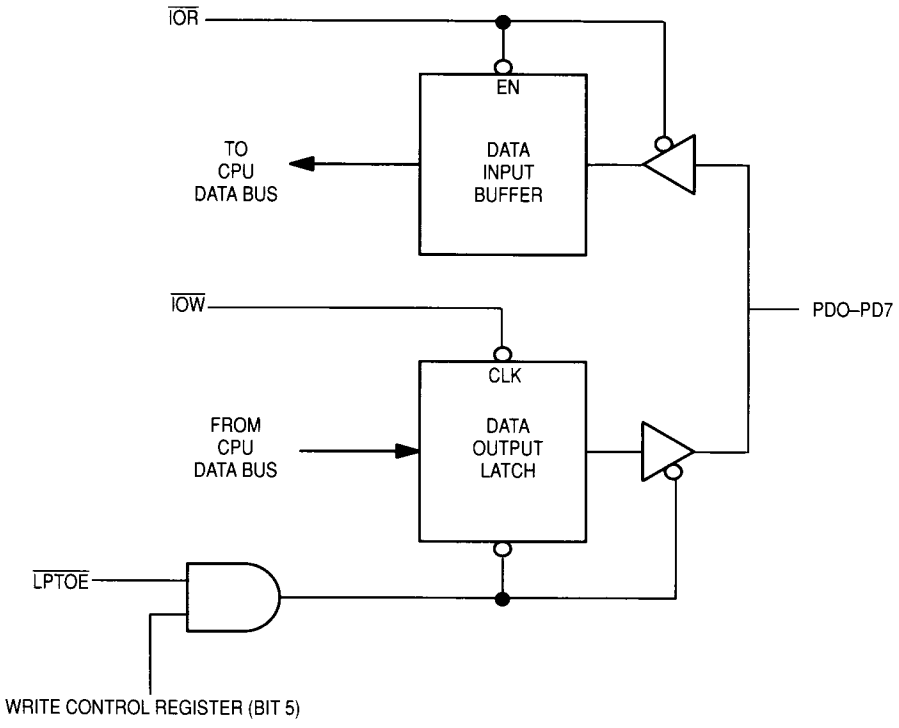


Figure 10. $\overline{\text{LPTOE}}$ Functional Block Diagram

14.0 READ STATUS REGISTER

The microprocessor reads the status of the printer in the five most significant bits of this Read Status Register. Table 19 contains the bit definitions for this register.

Table 19. Read Status Register Bit Definition Summary

Bit	Function	Logic High	Logic Low
0	Unused and always set to 1		
1	Unused and always set to 1		
2	Unused and always set to 1		
3	$\overline{\text{ERR}}$	Print Error	No error
4	SLCT	Printer is not selected	Printer is selected
5	PE	Paper ready	Paper is empty
6	$\overline{\text{ACK}}$	Printer accepted data	Data not accepted
7	BSY	Printer ready	Printer is busy

Bit Function

0–2 These bits are unused and are always set to 1.

3 Indicates that the printer is in an error condition. This occurs if: the printer has a mechanical failure, is off-line, runs out of paper, or can't understand the previous command.
1 — Printer Error
0 — Printer is nominal

4 Indicates to the system that the printer has been selected and is ready to receive data to be printed.
0 — Printer is not selected
1 — Printer is selected

5 Indicates that the printer has run out of paper.
0 — Printer has paper
1 — Printer is out of paper

6 Signal used by the printer to tell the sending system that the last data byte has been received and the next byte may now be placed on the bus. This signal pulses for every data byte transferred.

7 Status of the printer.
0 — Printer is ready to accept commands or data.
1 — Printer is busy processing the previous data or is off-line.

15.0 READ CONTROL REGISTER

The Read Control Register is for reading the state of the control lines. Table 20 contains the bit definitions for the Read Control Registers.

Table 20. Read Control Register Bit Definition Summary

Bit	Function	Logic Low	Logic High
0	$\overline{\text{STROBE}}$	Clock data to printer	—
1	$\overline{\text{AFD}}$	Autofeed paper	—
2	$\overline{\text{INIT}}$	Initialize printer	—
3	$\overline{\text{SLIN}}$	Printer selected	—
4	IRQEN	—	Interrupt enabled
5	Unused and must be set to 1		
6	Unused and must be set to 1		
7	Unused and must be set to 1		

Bit Function

0 Strobes to inform the printer of the presence of a valid byte on the parallel bus that is ready to be read by the printer.

1 Informs the printer that it should linefeed after every line printed.

2 Puts the printer into its initialization routine.

3 Indicates to the printer that data will soon be sent to the printer for printing.
0 — Printer is not selected
1 — Printer is selected

4 Enables the MCCS16C451 to interrupt the microprocessor when the printer is ready to accept more data.

5–7 These bits are unused and are always set to 1.

16.0 WRITE CONTROL REGISTER

The Write Control Register sets the state of the parallel port control lines. Table 21 contains the bit definitions for the Write Control Registers.

Table 21. Write Control Register Bit Definition Summary

Bit	Function	Logic Low	Logic High
0	$\overline{\text{STROBE}}$	Clock data to printer	—
1	$\overline{\text{AFD}}$	Autofeed paper	—
2	$\overline{\text{INIT}}$	Initialize printer	—
3	$\overline{\text{SLIN}}$	Printer selected	—
4	IRQEN	—	Interrupt enabled
5	DIR	Default	Input from PD0–PD7
6	Unused and must be set to 1		
7	Unused and must be set to 1		

Bit Function

0 Strobes to inform the printer of the presence of a valid byte on the parallel bus that is ready to be read by the printer.

1 Informs the printer that it should linefeed after every line printed.

2 Puts the printer into its initialization routine.

3 Indicates to the printer that data will soon be sent to the printer for printing.
0 — Printer is not selected
1 — Printer is selected

4 Enables the MCCS16C451 to interrupt the microprocessor when the printer is ready to accept more data.

5 Enables the printer port to be used as an input port. This bit defaults to 0, which in the configuration for output. See Figure 10 and Section 12.0 for more details.

6–7 These bits are unused and are always set to 1.

17.0 WRITE DATA REGISTER

The Write Data Register is used by the microprocessor to pass data one byte at a time to the printer's parallel bus.

18.0 ADDRESS DECODER

The parallel port address decoder selects register according to the states of the signals listed in Table 22.

19.0 INTERRUPT CONTROL LOGIC

The serial and parallel ports generate their own interrupts to the CPU. The $\overline{IRQ5}$ or $\overline{IRQ7}$ signals for the parallel port control the parallel port interrupt mechanism. These interrupts are found on the IBM PC/AT. The serial port generates the $\overline{IRQ3}$ or $\overline{IRQ4}$ signal for the interrupt service.

The MCCS16C451 supports PC/XT/AT systems with both parallel and serial port interrupts. For the parallel and serial ports interrupts are three-stated outputs.

Refer to Figure 11 for a logic diagram of the interrupt control logic.

Table 22. Address Decoder Register Selection

Control Signals					
$\overline{IOR}$	$\overline{IOW}$	$\overline{CSPA}$	A1	A0	Register Selected
0	1	0	0	0	Read Data Register
0	1	0	0	1	Read Status Register
0	1	0	1	0	Read Control Register
0	1	0	1	1	Invalid
1	0	0	0	0	Write Data Register
1	0	0	0	1	Invalid
1	0	0	1	0	Write Control Register
1	0	0	1	1	Invalid
0	0	X	X	X	Invalid
1	1	0	X	X	None
X	X	1	X	X	None

X = Don't Care

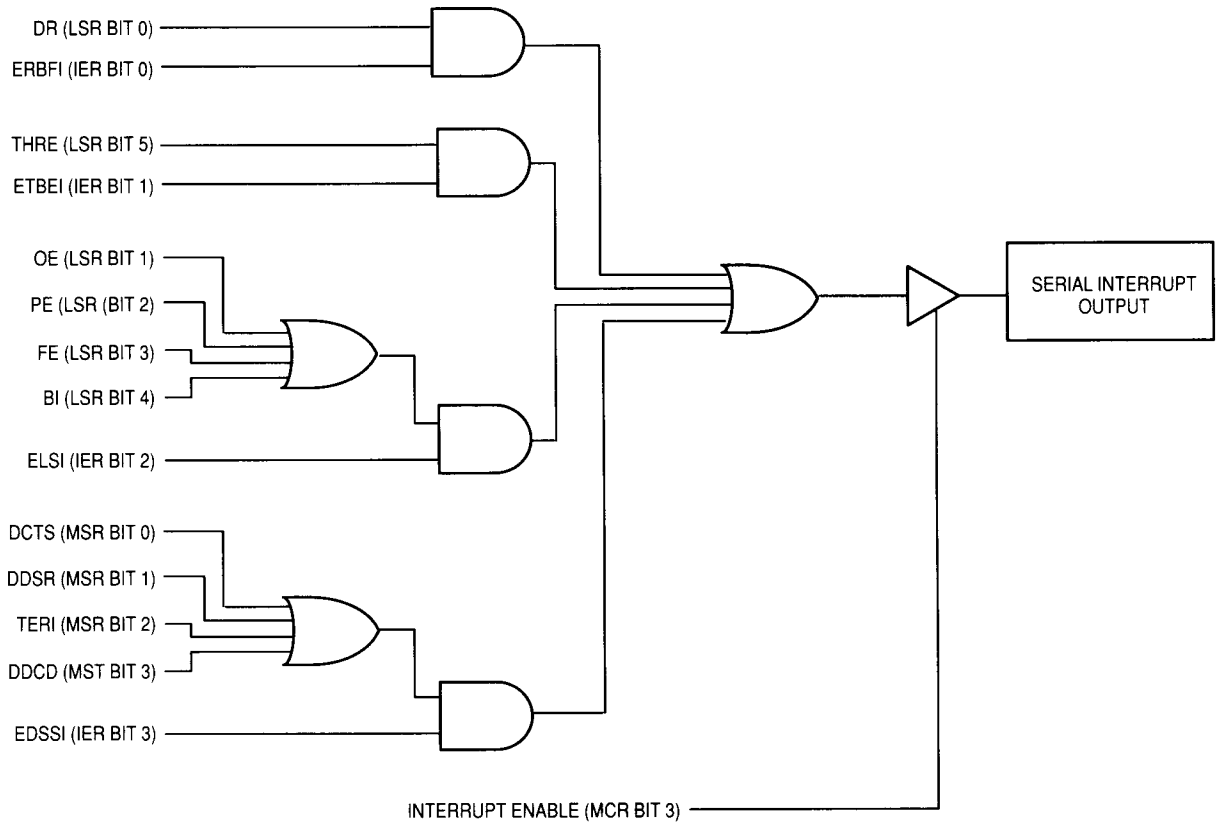
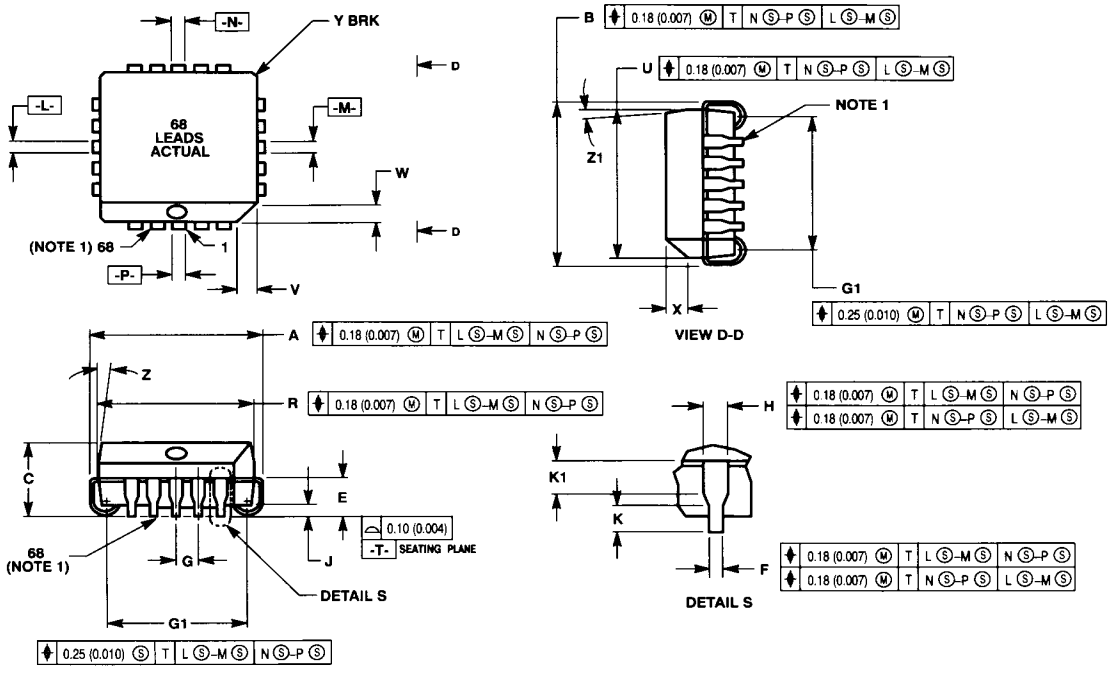


Figure 11. Serial Interrupt Control Logic Diagram

20.0 PACKAGE DIMENSIONS



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	25.02	25.27	0.985	0.995
B	25.02	25.27	0.985	0.995
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	24.13	24.28	0.950	0.956
U	24.13	24.28	0.950	0.956
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2	10	2	10
G1	23.12	23.62	0.910	0.930
K1	1.02	—	0.040	—
Z1	2	10	2	10

NOTES:
1. **DUE TO SPACE LIMITATION, CASE 779-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 68 LEADS.**
2. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.