MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N6543

Designers Data Sheet

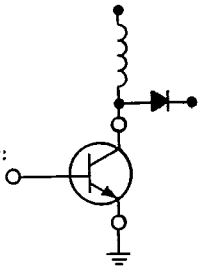
5 AMPERE
NPN SILICON
POWER TRANSISTOR
400 VOLTS
100 WATTS

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

This device is designed for high-voltage, high-speed, power switching inductive circuits where fall time is critical. It is particularly suited for 115 and 200 volt line operated SWITCHMODE applications such as:

- Switching Regulators
- PWM Inverters and Motor Controls
- Solenoid and Relay Drivers
- Deflection Circuits

Specification Features –
High Temperature Performance Specified for:
Reversed Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents



Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.

***MAXIMUM RATINGS**

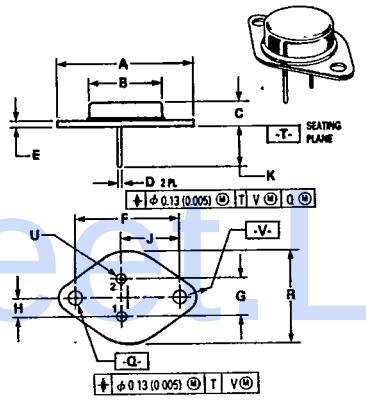
Rating	Symbol	2N6543	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	8.0	Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	5.0 10	Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	5.0 10	Adc
Emitter Current – Continuous – Peak (1)	I_E I_{EM}	10 20	Adc
Total Power Dissipation @ $T_C = 25^oC$ @ $T_C = 100^oC$ Derate above 25^oC	P_D	100 57.2 0.57	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.75	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



NOTES.
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

CASE 1-06
TO-204AA
(TO-3)

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***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS (1)				
Collector-Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	400	–	Vdc
Collector-Emitter Sustaining Voltage (Table 2, Figure 12) (I_C = 2.6 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C) (I_C = 5.0 Adc, V_{clamp} = Rated V_{CEO} -100 V, T_C = 100°C)	$V_{CEX(sus)}$	450 300	– –	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEV}	– –	0.5 3.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	–	3.0	mAdc
Emitter Cutoff Current (V_{EB} = 8.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased t = 1.0 s (non-repetitive) (V_{CE} = 100 Vdc)	$I_{S/b}$	0.2	– (See Figure 11)	Adc
Clamped Inductive SOA with base reverse biased	RBSOA	(See Figure 12)		
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 1.5 Adc, V_{CE} = 2.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	12 7.0	60 35	–
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.6 Adc) (I_C = 5.0 Adc, I_B = 1.0 Adc) (I_C = 3.0 Adc, I_B = 0.6 Adc, T_C = 100°C)	$V_{CE(sat)}$	– – –	1.0 5.0 2.0	Vdc
Base-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.6 Adc) (I_C = 3.0 Adc, I_B = 0.6 Adc, T_C = 100°C)	$V_{BE(sat)}$	– –	1.4 1.4	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain - Bandwidth Product (I_C = 200 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	f_T	6.0	28	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 MHz)	C_{ob}	50	200	pF
SWITCHING CHARACTERISTICS				
Resistive Load (Table 2)				
Delay Time	(V_{CC} · 250 Vdc, I_C 3.0 A, I_{B1} = I_{B2} = 0.6 A, t_p = 100 μs, Duty Cycle ≤ 2.0%)	t_d	–	0.05 μs
Rise Time		t_r	–	0.7 μs
Storage Time		t_s	–	4.0 μs
Fall Time		t_f	–	0.8 μs
Inductive Load, Clamped (Table 2)		Symbol	Typ	Max Unit
Storage Time	(I_C = 3.0 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 0.6 A, $V_{BE(off)}$ = 5.0 Vdc, T_C = 100°C)	t_{sv}	–	4.0 μs
Crossover Time		t_c	0.6	– μs
Fall Time		t_{fi}	–	0.8 μs
Storage Time	(I_C = 3.0 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 0.6 A, $V_{BE(off)}$ = 5.0 Vdc, T_C = 25°C)	t_{sv}	0.8	– μs
Crossover Time		t_c	0.3	– μs
Fall Time		t_{fi}	0.2	– μs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

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DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

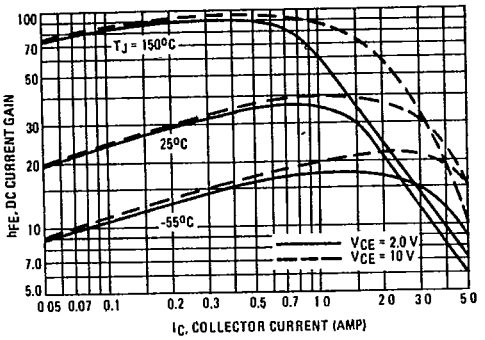

FIGURE 2 – COLLECTOR SATURATION REGION

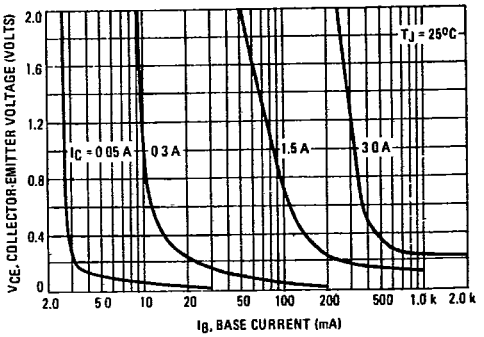

FIGURE 3 – "ON" VOLTAGE

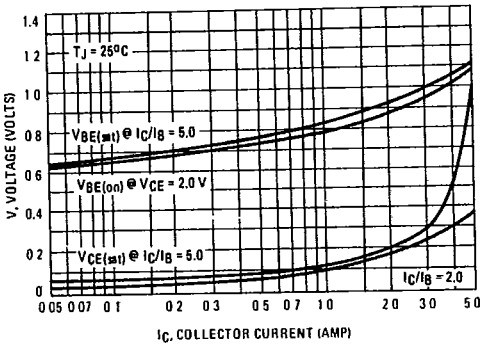

FIGURE 4 – TEMPERATURE COEFFICIENTS

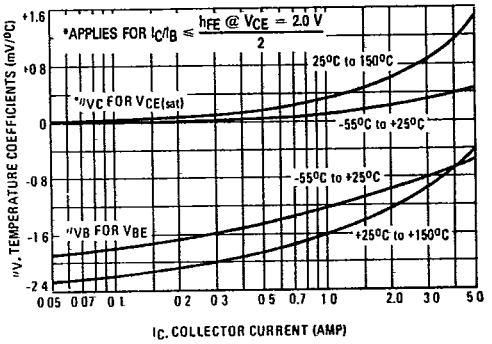

FIGURE 5 – COLLECTOR CUTOFF REGION

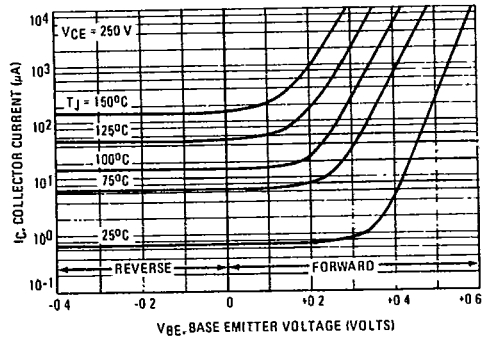

FIGURE 6 – CAPACITANCE

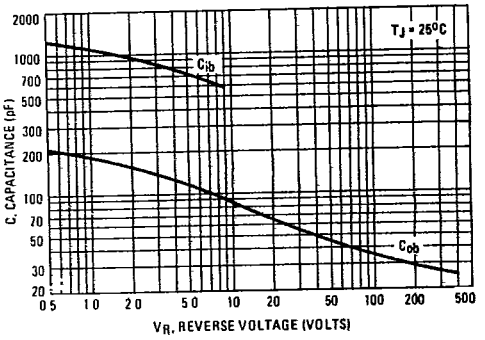

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FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS

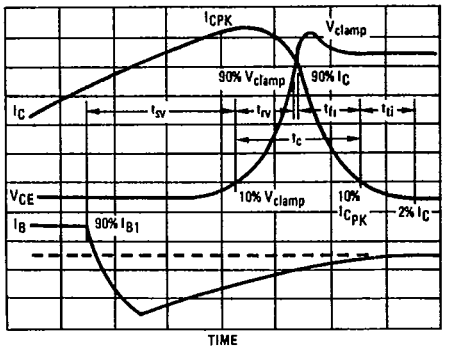

TABLE 1 – INDUCTIVE SWITCHING PERFORMANCE

I_C (A)	T_C °C	t_{sv} μs	t_{rv} μs	t_{fi} μs	t_{ti} μs	t_c μs
1.0	25	0.70	0.22	0.21	0.23	0.66
	100	1.20	0.37	0.19	0.39	0.95
3.0	25	1.10	0.09	0.12	0.08	0.29
	100	1.60	0.42	0.19	0.40	1.01
5.0	25	1.10	0.16	0.19	0.11	0.46
	100	1.70	0.45	0.37	0.26	1.08

Note: All Data Recorded in the Inductive Switching Circuit Shown in Table 2.

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SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 – TURN-ON TIME

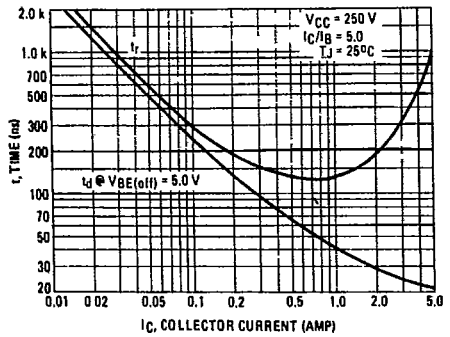

FIGURE 9 – TURN-OFF TIME

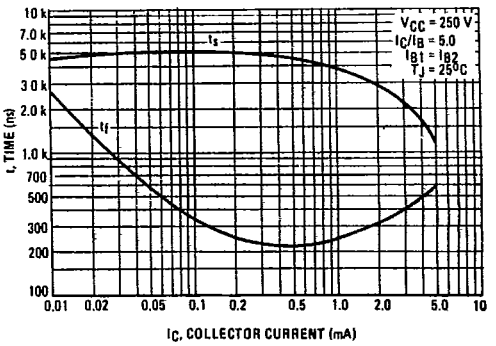

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TABLE 2 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CEO(sus)}$	$V_{CEX(sus)}$ AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	+10 V, 20 Ω, 0, 1, 2 PW Varied to Attain I_C = 100 mA	Drive Circuit: +4 V, PW, −4 V, 1 k, 0.01 µF, Q1, Q2, 20, 100, Q3, 0.1 µF, 1, 0.5 µF, Q4, +V_{in}, -5 V Set +V_{in} to Obtain a Forced h_{FE} = 5 and Adjust PW to Attain Specified Peak I_C. Duty Cycle ≤ 3% f = 1 kHz Q1 2N6406 Q3 2N5875 Q2 2N6406 Q4 2N5877 Diodes 1N4933	≈ +13 V, 0, ≈ −11 V, 1, 2 I_C = 3A PW ≈ 100 µs t_r ≤ 5 ns t_f ≤ 50 ns Duty Cycle ≤ 2%
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} (Unclamped)	L_{coil} = 180 µH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = Rated V_{CEX} Value	V_{CC} = 250 V R_L = 83 Ω D1 = 1N5820 or Equiv. R_B = 20 Ω
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT: TUT, 1 Input, 2, 1N4937 or Equivalent, See Above For Detailed Conditions, R_{coil}, L_{coil}, V_{clamp}, V_{CC}, R_S = 0.1 Ω OUTPUT WAVEFORMS: I_C, $I_{C(pk)}$, t_f Clamped, t_1, t_f, V_{CE}, V_{clamp}, Time, t_2 t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment: Scope-Tektronics 475 or Equivalent	RESISTIVE TEST CIRCUIT: 1, R_B, TUT, R_L, 2, D1, V_{CC}, -5 V

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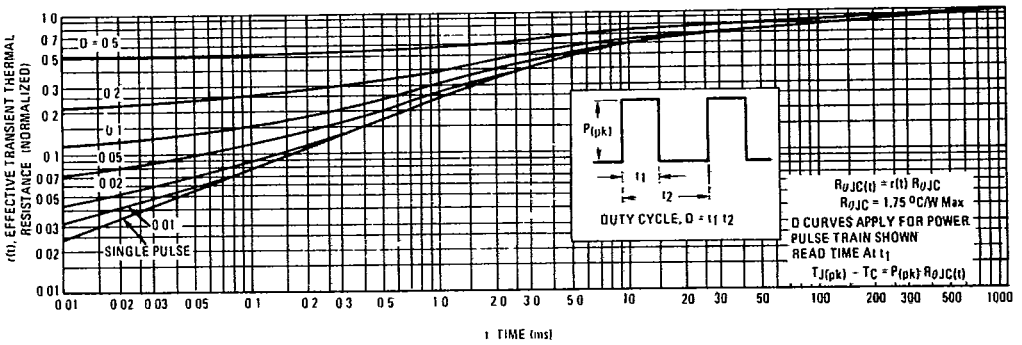
FIGURE 10 – THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 – FORWARD BIAS SAFE OPERATING AREA

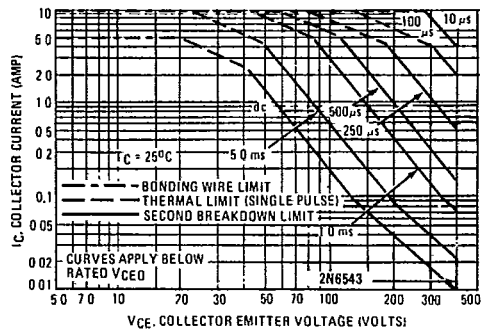


FIGURE 12 – REVERSE BIAS SAFE OPERATING AREA

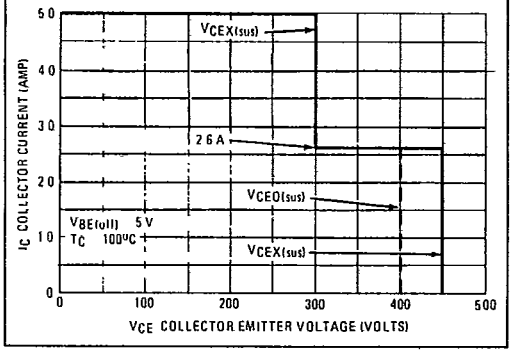
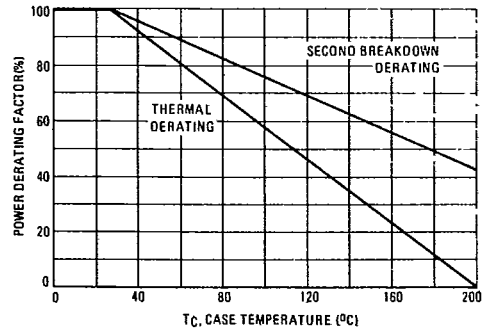


FIGURE 13 – POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete RBSOA characteristics.