Dual-Output or Two-Phase Synchronous Buck Controller with PMBus

Check for Samples: TPS40422

FEATURES

- **Single Supply Operation: 4.5 V to 20 V**
- **Output Voltage from 0.6 V to 5.6 V**
- **Dual or Two-Phase Synchronous Buck Controller**
- **PMBus Capability**
  - **Margining Up/Down with 2-mV Step**
  - **Programmable Fault Limit and Response**
  - **Output Voltage, Output Current Monitoring**
  - **External Temperature Monitoring with 2N3904**
  - **Programmable UVLO ON/OFF Thresholds**
  - **Programmable Soft Start Time and Turn On/Off Delay**
- **On-Chip Non-volatile Memory (NVM) to Store Custom Configurations**
- **180° Out-of-Phase to Reduce Input Ripple**
- **600-mV Reference Voltage with ±0.5% Accuracy from 0°C to 85°C**
- **Inductor DCR Current Sensing**
- **Programmable Switching Frequency from 200 kHz to 1 MHz**
- **Voltage Mode Control with Input Feed Forward**
- **Current Sharing for Multiphase Operation**
- **Supports Pre-biased Output**
- **Differential Remote Sensing**
- **External SYNC**
- **BPEXT Pin Boosts Efficiency by Supporting External Bias Power**
- **OC/OV/UV/OT Fault Protection**
- **40-Pin, 6 mm × 6 mm, QFN Package**

APPLICATIONS

- **Multiple Rail Systems**
- **Telecom Base Station**
- **Switcher/Router Networking**
- **Server and Storage System**

DESCRIPTION

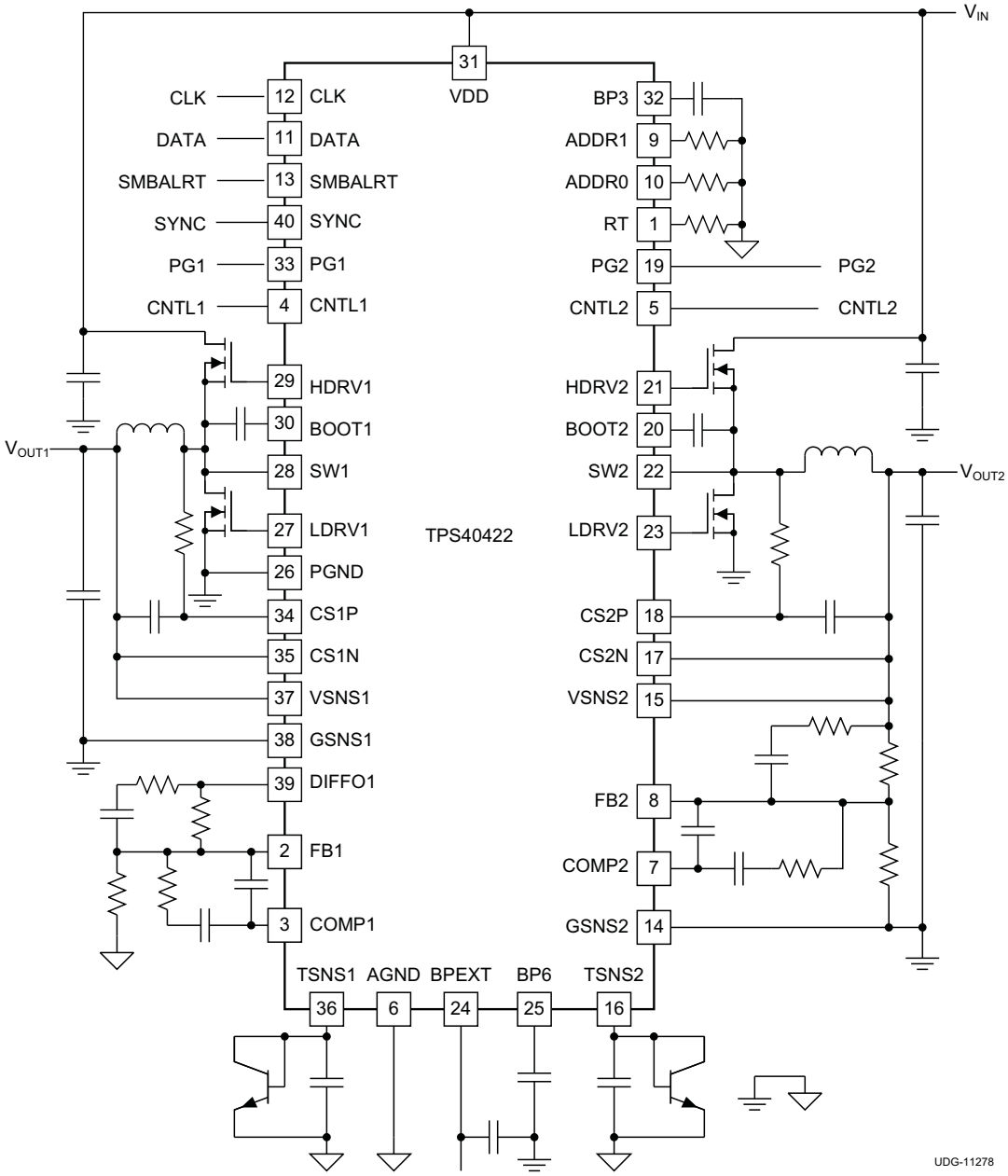
The TPS40422 is a dual-output PMBus synchronous buck controller. It can be configured also for a single, two-phase output.

Its wide input range can support 5-V and 12-V intermediate buses. The accurate reference voltage satisfies the need of precision voltage to the modern ASICs and potentially reduces the output capacitance. Voltage mode control is implemented to reduce noise sensitivity and also ensures low duty ratio conversion.

Using the PMBus protocol, the TPS40422 margining function, reference voltage, fault limit, UVLO threshold, soft start time and turn on/off delay can be programmed.

In addition, an accurate measurement system is implemented to monitor the output voltages, currents and temperatures for each channel.

SIMPLIFIED APPLICATION



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)(2)

TEMPERATUREE RANGE	PACKAGE	PINS	OUTPUT SUPPLY	MINIMUM QUANTITY	ORDERABLE DEVICE NUMBER
–40°C to 125°C	QFN	40	Tape and Reel	3000	TPS40422RHAR
			Tube	250	TPS40422RHAT

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNITS
Input voltage range(2)	VDD	–0.3	20	V
	BOOT1 , BOOT2, HDRV1, HDRV2	–0.3	30	
	BOOT1 - SW1, BOOT2 - SW2	–0.3	7	
	CLK, DATA, CNTL1, CNTL2, SYNC	–0.3	3.6	
	FB1, FB2, VSNS1, VSNS2, BPEXT	–0.3	7	
Output voltage range(3)	LDRV1, LDRV2, BP6	–0.3	7	V
	SW1, SW2	–1	30	
	COMP1, COMP2, DIFFO1, $\overline{\text{SMBALRT}}$, PG1, PG2, TSNS1, TSNS2	–0.3	7	
	ADDR0, ADDR1, BP3, RT	–0.3	3.6	
Electrostatic discharge	Human body model (HBM)	2		kV
	Charged device model (CDM)	1.5		
Storage junction temperature, T_J		–40	150	°C
Operating junction temperature, T_{stg}		–55	155	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.
(3) Voltage values are with respect to the SW terminal.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
VDD	Input operating voltage		4.5	20	V
T_J	Operating junction temperature		–40	125	°C
	Electrostatic discharge (ESD) ratings	Human Body Model (HBM)	2000		V
		Charge Device Model (CDM)	1500		

ELECTRICAL CHARACTERISTICS(1)

T_J = –40ºC to 125ºC, V_{IN} = V_{DD} = 12 V, RT set for 500 kHz, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{VDD}	Input supply voltage range		4.5		20	V
I_{VDD}	Input operating current	Switching, no driver load		18	25	mA
		Not switching		15	20	
UVLO						
$V_{IN(on)}$	Input turn on voltage(2)	Default settings		4.25		V
$V_{IN(off)}$	Input turn off voltage(2)	Default settings		4		V
$V_{INON(rng)}$	Programmable range for turn on voltage		4.25		16	V
$V_{INOFF(rng)}$	Programmable range for turn off voltage		4		15.75	V
$V_{INONOFF(acc)}$	Turn on and turn off voltage accuracy(1)	4.5 V ≤ V_{VDD} ≤ 20 V, all VIN_ON and VIN_OFF settings	–5%		5%	
ERROR AMPLIFIER						
V_{FB}	Feedback pin voltage	0°C ≤ T_J ≤ 85°C	597	600	603	mV
		–40°C ≤ T_J ≤ 125°C	594	600	606	
A_{OL}	Open-loop gain(3)		80			dB
G_{BWP}	Gain bandwidth product(3)			24		MHz
I_{FB}	FB pin bias current (out of pin)	V_{FB} = 0.6 V			50	nA
I_{COMP}	Sourcing	V_{FB} = 0 V	1	3		mA
	Sinking	V_{FB} = 1 V	3	9		
BP6 REGULATOR						
V_{BP6}	Output voltage	I_{BP6} = 10 mA	6.2	6.5	6.8	V
	Dropout voltage	V_{VIN} – V_{BP6}, V_{VDD} = 4.5 V, I_{BP6} = 25 mA		70	120	mV
I_{BP6}	Output current	V_{VDD} = 12 V	120			mA
V_{BP6UV}	Regulator UVLO voltage(3)		3.3	3.55	3.8	V
$V_{BP6UV(hyst)}$	Regulator UVLO voltage hysteresis(3)		230	255	270	mV
BPEXT						
$V_{BPEXT(swover)}$	BPEXT switch-over voltage		4.5	4.6		V
$V_{hys(swover)}$	BPEXT switch-over hysteresis		100		200	mV
$V_{BPEXT(do)}$	BPEXT dropout voltage	V_{BPEXT}–V_{BP6}, V_{BPEXT} = 4.8 V, I_{BP6} = 25 mA			100	mV
BOOTSTRAP						
$V_{BOOT(drop)}$	Bootstrap voltage drop	I_{BOOT} = 5 mA		0.7	1.0	V
BP3 REGULATOR						
V_{BP3}	Output voltage	V_{VDD} = 4.5 V, I_{BP3} ≤ 5 mA	3.1	3.3	3.5	V
OSCILLATOR						
f_{SW}	Adjustment range		100		1000	kHz
	Switching frequency	R_{RT} = 40 kΩ	450	500	550	kHz
V_{RMP}	Ramp peak-to-peak(3)			V_{VDD}/8.2		V
V_{VLY}	Valley voltage(3)		0.7	0.8	1.0	V

(1) Thresholds selected by entering high side parameters for PGOOD_ON and PGOOD_OFF. Cannot select same threshold for PGOOD_ON & PGOOD_OFF.
(2) By design, hysteresis of at least 150 mV is specified.
(3) Specified by design. Not production tested.

ELECTRICAL CHARACTERISTICS(1) (continued)

T_J = –40ºC to 125ºC, V_{IN} = V_{DD} = 12 V, RT set for 500 kHz, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYNCHRONIZATION						
V_{SYNCH}	SYNC high level threshold		2.0			V
V_{SYNCL}	SYNC low level threshold				0.8	V
t_{SYNC}	Minimum SYNC pulse width				100	ns
$f_{SYNC(max)}$	Maximum SYNC frequency(4)		2000			kHz
$f_{SYNC(min)}$	Minimum SYNC frequency(4)				200	
	SYNC frequency range (increase from nominal oscillator frequency)		–20%		20%	
PWM						
$t_{OFF(min)}$	Minimum off time		90	100		ns
$t_{ON(min)}$	Minimum pulse(5)			90	130	ns
t_{DEAD}	Output driver dead time	HDRV off to LDRV on	15	25	30	ns
		LDRV off to HDRV on	25	35	45	
SOFT START						
t_{SS}	Soft-start time	Factory default settings	2.4	2.7	3.0	ms
	Accuracy over range(5)	600 µs ≤ t_{SS} ≤ 9 ms	–15%		15%	
$t_{ON(delay)}$	Turn-on delay time(6)	Factory default settings		0		ms
$t_{OFF(delay)}$	Turn-off delay time	Factory default settings		0		ms
REMOTE SENSE AMPLIFIER						
$V_{DIFFO(err)}$	Error voltage from DIFFO1 to (V_{SNS1}– G_{SNS1})	(V_{SNS1}– G_{SNS1}) = 0.6 V	–5		5	mV
		(V_{SNS1}– G_{SNS1}) = 1.2 V	–8		8	
		(V_{SNS1}– G_{SNS1}) = 3.0 V	–17		17	
BW	Closed-loop bandwidth(5)		2			MHz
$V_{DIFFO(max)}$	Maximum DIFFOx output voltage		V_{BP6}-0.2			V
I_{DIFFO}	Sourcing		1			mA
	Sinking		1			
DRIVERS						
$R_{HS(up)}$	High-side driver pull-up resistance	(V_{BOOT}–V_{SW}) = 6.5 V, I_{HS} = -40 mA	0.8	1.5	2.5	Ω
$R_{HS(dn)}$	High-side driver pull-down resistance	(V_{BOOT}–V_{SW}) = 6.5 V, I_{HS} = 40 mA	0.5	1.0	1.5	
$R_{LS(up)}$	Low-side driver pull-up resistance	I_{LS} = -40 mA	0.8	1.5	2.5	
$R_{LS(dn)}$	Low-side driver pull-down resistance	I_{LS} = 40 mA	0.35	0.70	1.40	
$t_{HS(rise)}$	High-side driver rise time (5)	C_{LOAD} = 5 nF		15		ns
$t_{HS(fall)}$	High-side driver fall time (5)	C_{LOAD} = 5 nF		12		
$t_{LS(rise)}$	Low-side driver rise time (5)	C_{LOAD} = 5 nF		15		
$t_{LS(fall)}$	Low-side driver fall time (5)	C_{LOAD} = 5 nF		10		
CURRENT SENSING AMPLIFIER						
$V_{CS(rng)}$	Differential input voltage range	V_{CSxP}-V_{CSxN}	-60		60	mV
$V_{CS(cmr)}$	Input common-mode range		0		V_{BP6}–0.2	V
$V_{CS(os)}$	Input offset voltage	V_{CSxP} = V_{CSxN} = 0 V	-3		3	mV
A_{CS}	Current sensing gain			15.00		V/V
$V_{CS(out)}$	Amplfier output	(V_{CSxP}-V_{CSxN}) = 20 mV	270	300	330	mV
f_{C0}	Closed-loop bandwidth(5)		3	5		MHz
$V_{CS(chch)}$	Amplifier output difference between CH1, CH2	(V_{CS1P}– V_{CS1N}) = (V_{CS2P}–V_{CS2N}) = 20 mV, T_J = 25°C	-5.00%		5.00%	
		(V_{CS1P}– V_{CS1N}) = (V_{CS2P}–V_{CS2N}) = 20 mV, T_J = 85°C	-6.67%		6.67%	

(4) When using SYNC, the switching frequency is set to one-half the SYNC frequency.
(5) Specified by design. Not production tested.
(6) The minimum turn-on delay is 50 µs, when TON_DELAY is set to a factor of zero.

ELECTRICAL CHARACTERISTICS(1) (continued)

T_J = –40ºC to 125ºC, V_{IN} = V_{DD} = 12 V, RT set for 500 kHz, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT						
$t_{OFF(oc)}$	Off-time between restart attempts	Hiccup mode		7×t_{SS}		ms
DCR	Inductor DCR current sensing calibration value	Factory default settings		0.488		mΩ
		Programmable range	0.240		15.500	
$I_{OC(flt)}$	Output current overcurrent fault threshold	Factory default settings		30		A
		Programmable range	3		50	
$I_{OC(warn)}$	Output current overcurrent warning threshold	Factory default settings		27		A
		Programmable range	2		49	
$I_{OC(tc)}$	Output current fault/warning temperature coefficient(7)		3900	4000	4100	ppm/°C
$I_{OC(acc)}$	Output warning and fault accuracy	(V_{CSxP}-V_{CSxN}) = 30 mV	–15%		15%	
PGOOD (8)						
V_{FBPGH}	FB PGOOD high threshold	Factory default settings		675		mV
V_{FBPGL}	FB PGOOD low threshold	Factory default settings		525		mV
$V_{PG(acc)}$	PGOOD accuracy over range	4.5 V ≤ V_{VDD} ≤ 20 V, 468 mV ≤ V_{PGOOD} ≤ 675 mV	–4%		4%	
$V_{pg(hyst)}$	FB PGOOD hysteresis voltage			25	40	mV
R_{PGOOD}	PGOOD pulldown resistance	V_{FB} = 0, I_{PGOOD} = 5 mA		40	70	Ω
$I_{PGOOD(lk)}$	PGOOD pin leakage current	No fault, V_{PGOOD} = 5 V			20	µA
OUTPUT OVERVOLTAGE/UNDERVOLTAGE						
V_{FBOV}	FB pin over voltage threshold	Factory default settings		700		mV
V_{FBUV}	FB pin under voltage threshold	Factory default settings		500		mV
$V_{UVOV(acc)}$	FB UV/OV accuracy over range	4.5 V ≤ V_{VDD} ≤ 20 V	–4%		4%	
OUTPUT VOLTAGE TRIMMING AND MARGINING						
$V_{FBTM(step)}$	Resolution of FB steps with trim and margin			2		mV
$t_{FBTM(step)}$	Transition time per trim or margin step	After soft-start time		30		µs
$V_{FBTM(max)}$	Maximum FB voltage with trim and/or margin			660		mV
$V_{FBTM(min)}$	Minimum FB voltage with trim or margin only			480		mV
	Minimum FB voltage range with trim and margin combined			420		
V_{FBMH}	Margin high FB pin voltage	Factory default settings		660		mV
V_{FBML}	Margin low FB pin voltage	Factory default settings		540		mV
TEMPERATURE SENSE AND THERMAL SHUTDOWN						
T_{SD}	Junction shutdown temperature(7)		135	145	155	°C
T_{HYST}	Thermal shutdown hysteresis(7)		15	20	25	°C
$I_{TSNS(ratio)}$	Ratio of bias current flowing out of TSNS pin, state 2 to state 1		9.7	10.0	10.3	
I_{TSNS}(7)	State 1 current out of TSNSx pin			10		µA
I_{TSNS}(7)	State 2 current out of TSNSx pin			100		µA
V_{TSNS}	Voltage range on TSNSx pin(7)		0		1.00	V
$T_{SNS(acc)}$	External temperature sense accuracy(9)	0°C ≤ T_J ≤ 125°C	–5		5	°C
$T_{OT(flt)}$	Overtemperature fault limit(7)	Factory default settings		145		°C
	OT fault limit range(7)		120		165	°C
$T_{OT(warn)}$	Overtemperature warning limit(7)	Factory default settings		125		°C
	OT warning limit range(7)		100		140	°C
$T_{OT(step)}$	OT fault/warning step			5		°C
$T_{OT(hys)}$	OT fault/warning hysteresis(7)		15	20	25	°C

(7) Specified by design. Not production tested.
(8) Thresholds selected by entering high side parameters for PGOOD_ON and PGOOD_OFF. Cannot select same threshold for PGOOD_ON & PGOOD_OFF.
(9) Specified by design. Not production tested.

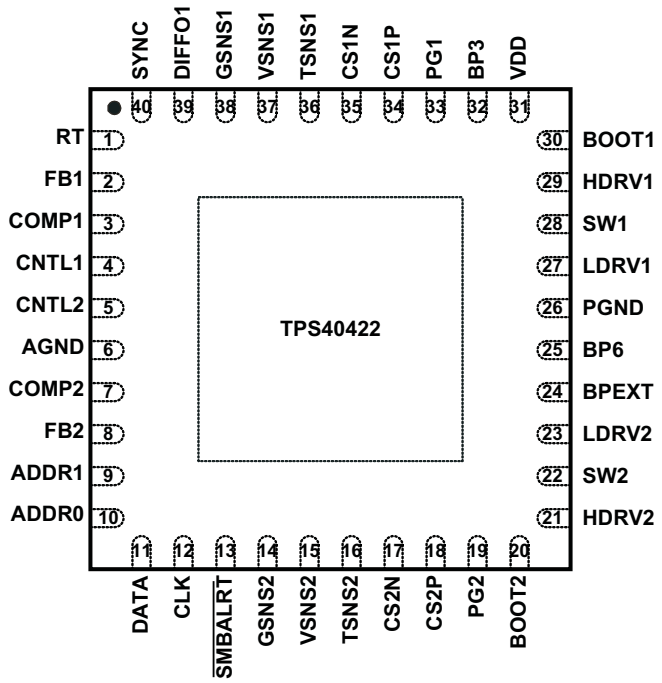
ELECTRICAL CHARACTERISTICS(1) (continued)

T_J = –40ºC to 125ºC, V_{IN} = V_{DD} = 12 V, RT set for 500 kHz, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MEASUREMENT SYSTEM						
$M_{VOUT(rng)}$	Output voltage measurement range(10)		0.5		5.8	V
$M_{VOUT(acc)}$	Output voltage measurement accuracy	V_{OUT} = 1.0 V	–2.0%		2.0%	
$M_{IOUT(rng)}$	Output current measurement signal range(10)	V_{CSxP}–V_{CSxN}, 0.2440 mΩ ≤ IOUT_CAL_GAIN ≤ 0.5795 mΩ	0		36	mV
		V_{CSxP}–V_{CSxN}, 0.5796 mΩ ≤ IOUT_CAL_GAIN ≤ 1.1285 mΩ	0		60	
		V_{CSxP}–V_{CSxN}, 1.1286 mΩ ≤ IOUT_CAL_GAIN ≤ 15.5 mΩ	0		90	
$M_{IOUT(acc)}$	Output current measurement accuracy	I_{OUT} ≥ 20 A, DCR = 0.5 mΩ	–1.0		1.0	A
PMBus ADDRESSING						
I_{ADD}	Address pin bias current		9.24	10.50	11.76	µA
PMBus INTERFACE						
V_{IH}	Input high voltage, CLK, DATA, CNTLx		2.1			V
V_{IL}	Input low voltage, CLK, DATA, CNTLx				0.8	V
I_{IH}	Input high level current, CLK, DATA		–10		10	µA
I_{IL}	Input low level current, CLK, DATA		–10		10	mA
I_{CTNL}	CNTL pin pull-up current			6		µA
V_{OL}	Output low level voltage, DATA, (10)	4.5 V ≤ V_{VDD} ≤ 20 V, I_{OUT} = 4 mA			0.8	V
I_{OH}	Output high level open drain leakage current, DATA, $\overline{SMBALRT}$	V_{OUT} = 5.5 V	0		10	µA
C_{OUT}	Pin capacitance, CLK, DATA(10)				1	pF
F_{PMB}	PMBus operating frequency range(10)	Slave mode	10		400	kHz
t_{BUF}	Bus free time between START and STOP(10)		4.7			µs
$t_{HD:STA}$	Hold time after repeated START(10)		4.0			µs
$t_{SU:STA}$	Repeated START setup time(10)		4.7			µs
$t_{SU:STO}$	STOP setup time(10)		4.0			µs
$t_{HD:DAT}$	Data hold time(10)	Receive mode	0			ns
		Transmit mode	300			
$t_{SU:DAT}$	Data setup time(10)		250			ns
$t_{TIMEOUT}$	Error signal/detect(10)		25		35	µs
$t_{LOW:MEXT}$	Cumulative clock low master extend time(10)				50	µs
$t_{LOW:SEXT}$	Cumulative clock low slave extend time(10)				25	µs
t_{LOW}	Clock low time(10)		4.7			µs
t_{HIGH}	Clock high time(10)		4.0			µs
t_{FALL}	CLK/DATA fall time(10)				300	µs
t_{RISE}	CLK/DATA rise time(10)				1000	µs

(10) Specified by design. Not production tested.

DEVICE INFORMATION



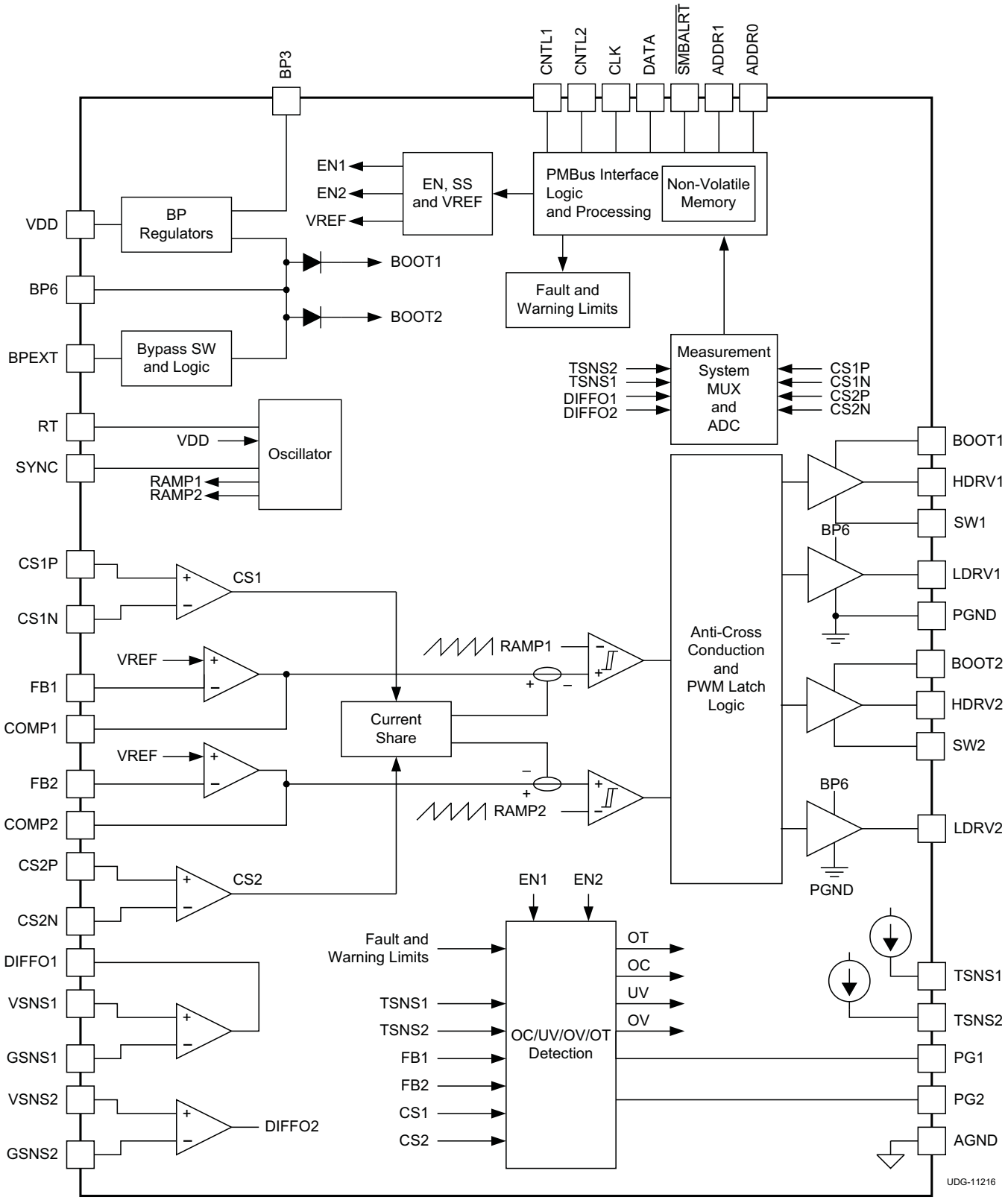
PIN DESCRIPTIONS

PIN	NO.	I/O	DESCRIPTION
ADDR0	10	I	Low-order address pin for PMBus address configuration. One of eight resistor values must be connected from this pin to AGND to select the low-order octal digit in the PMBus address.
ADDR1	9	I	High-order address pin for PMBus address configuration. One of eight resistor values must be connected from this pin to AGND to select the low-order octal digit in the PMBus address.
AGND	6	—	Low-noise ground connection to the controller. Connections should be arranged so that power level currents do not flow through the AGND path.
BOOT1	30	I	Bootstrapped supply for the high-side FET driver for channel 1 (CH1). Connect a capacitor (100 nF typical) from BOOT1 to SW1 pin.
BOOT2	20	I	Bootstrapped supply for the high-side FET driver for channel 2 (CH2). Connect a capacitor (100 nF typical) from BOOT2 to SW2 pin.
BP3	32	O	Output bypass for the internal 3.3-V regulator. Connect a 100 nF or larger capacitor from this pin to AGND.
BP6	25	O	Output bypass for the internal 6.5-V regulator. Connect a low ESR, 1 µF or larger ceramic capacitor from this pin to PGND.
BPEXT	24	I	External voltage input for BP6 switchover function. If the BPEXT function is not used, connect this pin directly to PGND. Otherwise connect a 100-nF or larger capacitor from this pin to PGND.
CLK	12	I	Clock input for the PMBus interface. Pull up to 3.3 V with a resistor.
CNTL1	4	I	Logic level input which controls startup and shutdown of CH1, determined by PMBus options.
CNTL2	5	I	Logic level input which controls startup and shutdown of CH2, determined by PMBus options.
COMP1	3	O	Output of the error amplifier for CH1 and connection node for loop feedback components.
COMP2	7	O	Output of the error amplifier for CH2 and connection node for loop feedback components. For two-phase operation, use COMP1 for loop feedback and connect COMP1 to COMP2.
CS1N	35	I	Negative terminal of current sense amplifier for CH1.
CS2N	17	I	Negative terminal of current sense amplifier for CH2.
CS1P	34	I	Positive terminal of current sense amplifier for CH1.
CS2P	18	I	Positive terminal of current sense amplifier for CH2.
DATA	11	I/O	Data input/output for the PMBus interface. Pull up to 3.3 V with a resistor.
DIFFO1	39	O	Output of the differential remote sense amplifier for CH1.

PIN DESCRIPTIONS (continued)

PIN	NO.	I/O	DESCRIPTION
FB1	2	I	Inverting input of the error amplifier for CH1. Connect a voltage divider to FB1 between DIFFO1 and AGND to program the output voltage for CH1.
FB2	8	I	Inverting input of the error amplifier for CH2. Connect a voltage divider to FB2 between VSNS2 and GSNS2 to program the output voltage for CH2. For two-phase operation, use FB1 to program the output voltage and connect FB2 to BP6 before applying voltage to VDD.
GSNS1	38	I	Negative terminal of the differential remote sense amplifier for CH1.
GSNS2	14	I	Negative terminal of the differential remote sense amplifier for CH2.
HDRV1	29	O	Bootstrapped gate drive output for the high-side N-channel MOSFET for CH1.
HDRV2	21	O	Bootstrapped gate drive output for the high-side N-channel MOSFET for CH2.
LDRV1	27	O	Gate drive output for the low side synchronous rectifier N-channel MOSFET for CH1.
LDRV2	23	O	Gate drive output for the low-side synchronous rectifier N-channel MOSFET for CH2.
PGND	26	—	Power GND.
PG1	33	O	Open drain power good indicator for CH1 output voltage.
PG2	19	O	Open drain power good indicator for CH2 output voltage.
RT	1	I	Frequency programming pin. Connect a resistor from this pin to AGND to set the oscillator frequency.
$\overline{\text{SMBALRT}}$	13	O	Alert output for the PMBus interface. Pull up to 3.3 V with a resistor.
SW1	28	I	Return of the high-side gate driver for CH1. Connect to the switched node for CH1.
SW2	22	I	Return of the high-side gate driver for CH2. Connect to the switched node for CH2.
SYNC	40	I	Logic level input for external clock synchronization. When an external clock is applied to this pin, the oscillator frequency sychronizes to one half of its frequency. When an external clock is not used, tie this pin to AGND.
TSNS1	36	I	External temperature sense input for CH1.
TSNS2	16	I	External temperature sense input for CH2.
VDD	31	I	Power input to the controller. Connect a low ESR, 100 nF or larger ceramic capacitor from this pin to AGND.
VSNS1	37	I	Positive terminal of the differential remote sense amplifier for CH1.
VSNS2	15	I	Positive terminal of the differential remote sense amplifier for CH2.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

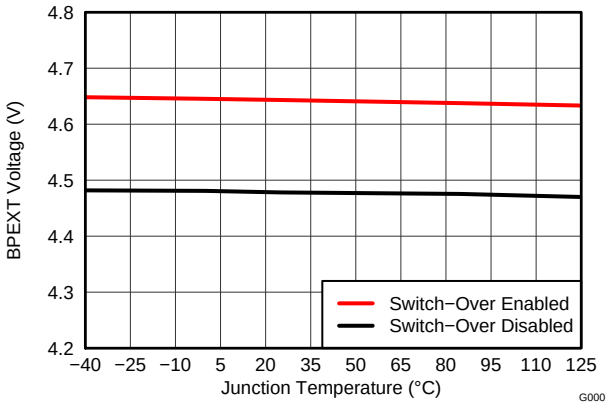


Figure 1. BPEXT Voltage vs. Junction Temperature

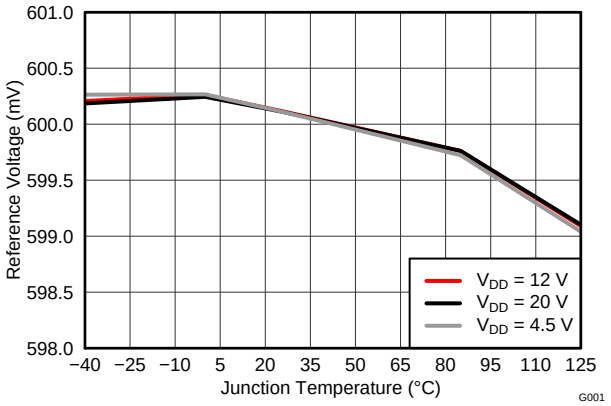


Figure 2. Reference Voltage vs. Junction Temperature

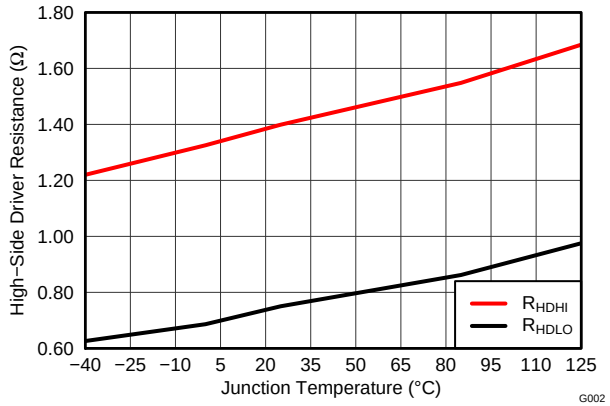


Figure 3. High-Side Driver Resistance vs. Junction Temperature

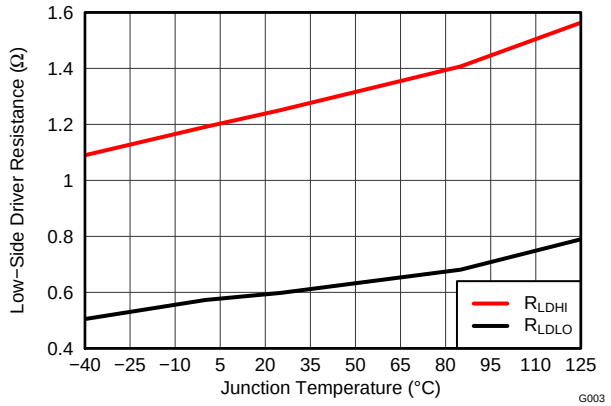


Figure 4. Low-Side Driver Resistance vs. Junction Temperature

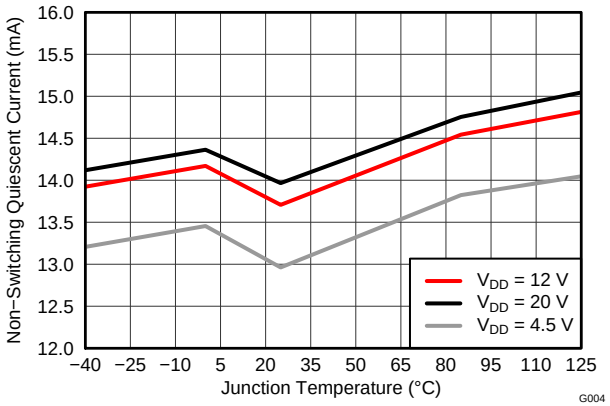


Figure 5. Non-Switching Quiescent Current vs. Junction Temperature

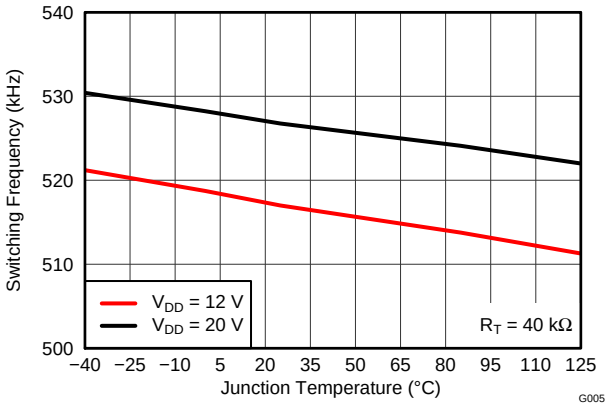


Figure 6. Switching Frequency vs. Junction Temperature

TYPICAL CHARACTERISTICS (continued)

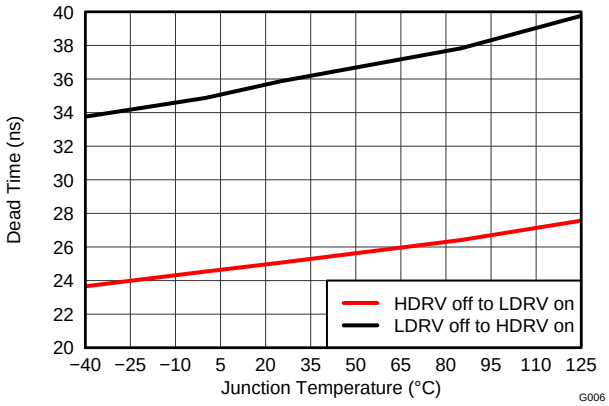


Figure 7. Dead Time vs. Junction Temperature

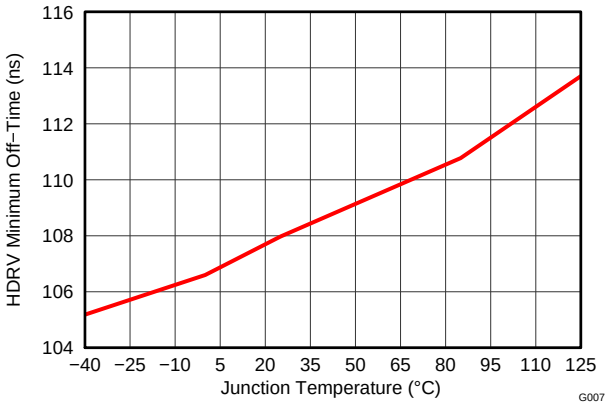


Figure 8. HDRV Minimum Off-Time vs. Junction Temperature

APPLICATION INFORMATION

General Description/Control Architecture

The TPS40422 is a flexible synchronous buck controller. It can be used as a dual-output controller, or as a two-phase single-output controller. It operates with a wide input range from 4.5 V to 20 V and generates accurate regulated output as low as 600 mV.

In dual output mode, voltage mode control with input feed-forward architecture is implemented. With this architecture, the benefits are less noise sensitivity, no control instability issues for small DCR applications, and a smaller minimum controllable on-time, often desired for high conversion ratio applications.

In two-phase single-output mode, a current-sharing loop is implemented to ensure a balance of current between phases. Because the induced error current signal to the loop is much smaller when compared to the PWM ramp amplitude, the control loop is modeled as voltage mode with input feed-forward.

DESIGN NOTE

To operate the device in two-phase mode, tie the FB2 pin to the BP6 pin and tie the COMP1 pin to the COMP2 pin. These connections must be made before applying voltage to the VDD pin.

PMBus General Description

Timing and electrical characteristics of the PMBus can be found in the PMB Power Management Protocol Specification, Part 1, revision 1.1 available at http://pmbus.org. The TPS40422 supports both the 100 kHz and 400 kHz bus timing requirements. The TPS40422 does not stretch pulses on the PMBus when communicating with the master device.

Communication over the TPS40422 device PMBus interface can either support the Packet Error Checking (PEC) scheme or not. If the master supplies CLK pulses for the PEC byte, it is used. If the CLK pulses are not present before a STOP, the PEC is not used.

The TPS40422 supports a subset of the commands in the PMBus 1.1 specification. Most all of the controller parameters can be programmed using the PMBus and stored as defaults for later use. All commands that require data input or output use the literal format. The exponent of the data words is fixed at a reasonable value for the command and altering the exponent is not supported. Direct format data input or output is not supported by the TPS40422. See the SUPPORTED COMMANDS section for specific details.

The TPS40422 also supports the SMBALERT response protocol. The SMBALERT response protocol is a mechanism by which a slave (the TPS40422) can alert the bus master that it wants to talk. The master processes this event and simultaneously accesses all slaves on the bus (that support the protocol) through the alert response address. Only the slave that caused the alert acknowledges this request. The host performs a modified receive byte operation to get the slave's address. At this point, the master can use the PMBus status commands to query the slave that caused the alert. For more information on the SMBus alert response protocol, see the System Management Bus (SMBus) specification.

The TPS40422 contains non-volatile memory that is used to store configuration settings and scale factors. The settings programmed into the device are not automatically saved into this non-volatile memory though. The STORE_USER_ALL command must be used to commit the current settings to non-volatile memory as device defaults. The settings that are capable of being stored in non-volatile memory are noted in their detailed descriptions.

Voltage Reference

The 600-mV bandgap cell is internally connected to the non-inverting input of the error amplifier. The reference voltage is trimmed with the error amplifier in a unity gain configuration to remove amplifier offset from the final regulation voltage. The 0.5-% tolerance on the reference voltage allows the user to design a very accurate power supply.

Output Voltage

The output voltage is set in a very similar to the way to a traditional analog controller using a voltage divider from the output to the feedback (FB) pin. The output voltage must be divided down to the nominal reference voltage of 600mV. Figure 9 shows the typical connections for the controller. The voltage at the load can be sensed using the unity gain differential voltage sense amplifier. This provides better load regulation for output voltages lower than 5V nominal (see electrical specifications for the maximum output voltage of the differential sense amplifier). For output voltages above this level, connect the output voltage directly to the junction of R1 and C1, leave DIFFO1 open and do not connect the VSNS1 pin to the output voltage. If desired the differential amplifier may also be used elsewhere in the overall system as a voltage buffer, provided the electrical specifications are not exceeded.

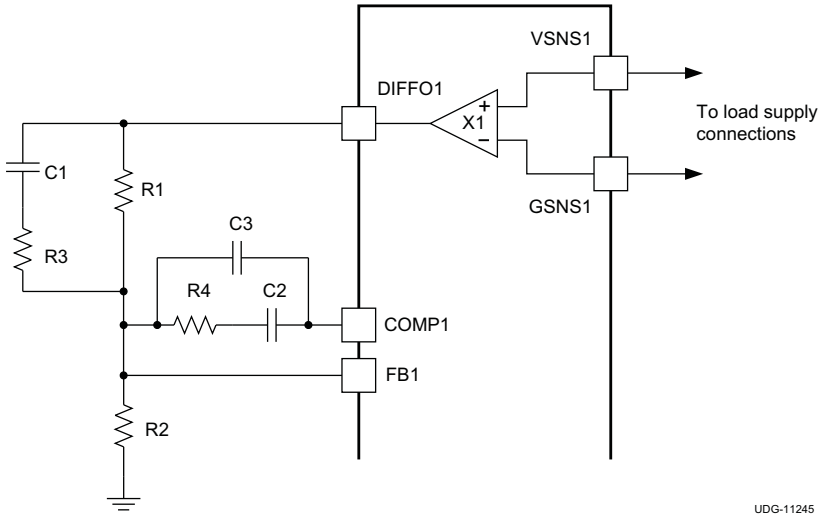


Figure 9. Setting the Output Voltage

The components in Figure 9 that determine the nominal output voltage are R1 and R2. R1 is normally chosen to make the feedback compensation values (R3, R4, C1, C2 andC3) come close to readily available standard values. R2 is then calculated in Equation 1.

$$R2 = V_{FB} \times \left(\frac{R1}{(V_{OUT} - V_{FB})} \right) \quad (1)$$

where

- V_{FB} is the feedback voltage
- V_{OUT} is the desired output voltage
- R1 and R2 are in the same units

DESIGN NOTE

There is no DIFFO2 pin. In dual-output mode, VSNS2 and GSNS2 are connected to the load for channel 2 and the DIFFO2 signal is used internally for voltage monitoring. Connect the output directly to the junction of R1 and C1 for channel 2 to set the output voltage and for feedback.

The feedback voltage can be changed –30% to +10% from the nominal 600 mV using PMBus commands. This allows the output voltage to vary by the same percentage. *See the PMBus Functionality section for further details.*

Voltage Feed Forward

The TPS40422 uses input voltage feed forward that maintains a constant power stage gain as input voltage varies and provides for very good response to input voltage transient disturbances. The simple constant power stage gain of the controller greatly simplifies feedback loop design because loop characteristics remains constant as the input voltage changes, unlike a buck converter without voltage feed forward. For modeling purposes, the gain from the COMP pin to the average voltage at the input of the L-C filter is 8.2 V/V.

Current Sensing

The TPS40422 uses a differential current sense scheme to sense the output current. The sense element can be either the series resistance of the power stage filter inductor or a separate current sense resistor. When using the inductor series resistance as in Figure 10, a filter must be used to remove the large AC component of voltage across the inductor and leave only the component of the voltage that appears across the resistance of the inductor. The values of R5 and C4 for the ideal case can be found by Equation 2. The time constant of the R-C filter should be equal to or greater than the time constant of the inductor itself. If the time constants are equal, the voltage appearing across C4 is be the current in the inductor multiplied the inductor resistance. The inductor ripple current is reflected in the voltage across C4 perfectly in this case and there is no reason to have a shorter R-C time constant.

The time constant of the R-C filter can be made longer than the inductor time constant because this is a voltage mode controller and the current sensing is done for overcurrent detection and output current reporting only. Extending the R-C filter time constant beyond the inductor time constant lowers the AC ripple component of voltage present at the current sense pins of the TPS40422 but allows the correct DC current information to remain intact. This also delays slightly the response to an overcurrent event, but reduces noise in the system leading to cleaner overcurrent performance and current reporting data over the PMBus

$$R5 \times C4 \geq \left(\frac{L}{R_{DCR}} \right) \quad (2)$$

where (from Figure 10)

- R5 and R_{ESR} are in Ω
- C4 is in F (suggest 100 nF, 10^{-7}F)
- L is in H

The maximum voltage that the TPS40422 is designed to accept across the curent sense pins is 60 mV. Because most all inductors have a copper conductor and because copper has a fairly large temperature coefficient of resistance, the resistance of the inductor and the current through the inductor should make a DC voltage less than 60 mV when the inductor is at the maximum temperature for the converter. This also applies for the external resistor in Figure 11. The full load output current multiplied by the sense resistor value, must be less that 110 mV at the maximum converter operating temperature.

In all cases, C4 should be placed as close to the current sense pins as possible to help avoid problems with noise.

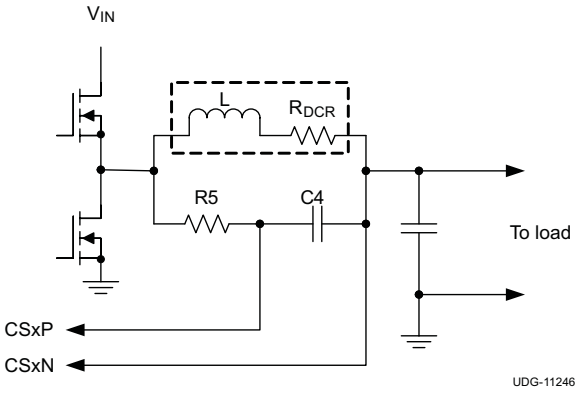


Figure 10. Current Sensing Using Inductor Resistance

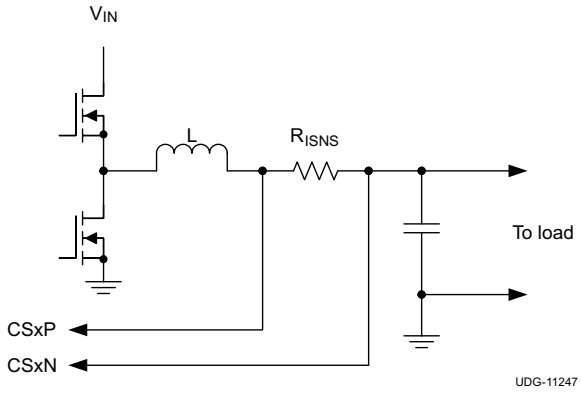


Figure 11. Current Sensing Using Sense Resistor

Once the current sensing method is chosen, the TPS40422 needs to be told what the resistance of the current sense element is. This allows the proper calculation of thresholds for the overcurrent fault and warning, as well as more accurate reporting of the actual output current. The IOUT_CAL_GAIN command is used to set the value of the sense element resistence of the device. IOUT_OC_WARN_LIMIT and IOUT_OC_FAULT_LIMIT set the levels for the overcurrent warning and fault levels respectively. (See the PMBus Functionality section for more details.)

Overcurrent Protection

The TPS40422 has overcurrent fault and warning thresholds for each channel which can be independently set, when operating in dual-output mode. When operating in two-phase mode, both channels share the same overcurrent fault and warning thresholds. The overcurrent thresholds are set over PMBus using the IOUT_OC_FAULT_LIMIT and IOUT_OC_WARN_LIMIT commands. (See the PMBus Functionality section for more details.)

The TPS40422 generates an internal voltage corresponding to the desired overcurrent threshold, using the IOUT_OC_FAULT_LIMIT threshold and the IOUT_CAL_GAIN setting, and adjusting for temperature using the measured external temperature value. The sensed current signal is amplified by the current sense amplifier with a fixed gain of 15 and then compared with this internal voltage threshold. A similar structure is used to activate an overcurrent warning based on the IOUT_OC_WARN_LIMIT threshold.

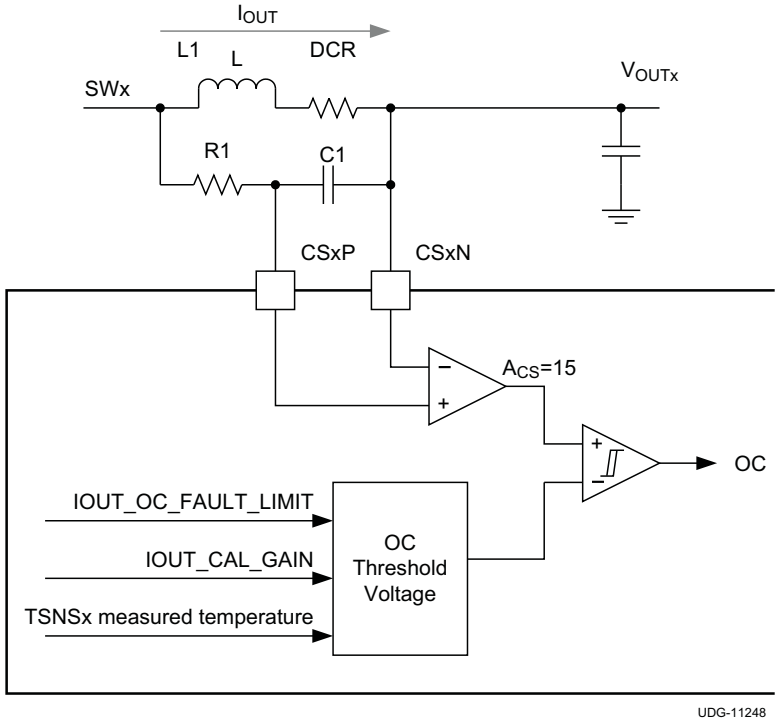


Figure 12. Overcurrent Protection

The TPS40422 implements cycle-by-cycle current limit when the peak sensed current exceeds the set threshold. In a time constant matched current sensor network, the signal across the CSxP and CSxN pins has both dc and ac inductor current information, so overcurrent trips when the dc current plus half of the ripple current exceeds the set threshold. When the time constant is not well-matched, the dc current which trips the overcurrent changes accordingly.

When the controller counts three consecutive clock cycles of an overcurrent condition, the high-side and low-side MOSFETs are turned off and the controller enters hiccup mode or latches the output off, depending on the IOUT_OC_FAULT_RESPONSE register. In continuous restart hiccup mode, after seven soft-start cycles, normal switching is attempted. If the overcurrent has cleared, normal operation resumes; otherwise, the sequence repeats.

Two-Phase Mode and Current Sharing Loop

The TPS40422 can be configured to operate in single-output two-phase mode for high-current applications. With proper selection of the external MOSFETs, this device can support up to 50-A of load current in a two-phase configuration. As shown in Figure 13, to configure TPS40422 as two-phase mode, FB2 is tied to BP6. In this mode, COMP1 must be connected to COMP2 to ensure current sharing between the two phases. For high-current applications, the remote sense amplifier is used to compensate for the parasitic offset to provide an accurate output voltage. DIFFO1, which is the output of the remote sensing amplifier, is connected to the resistor divider of the feedback network.

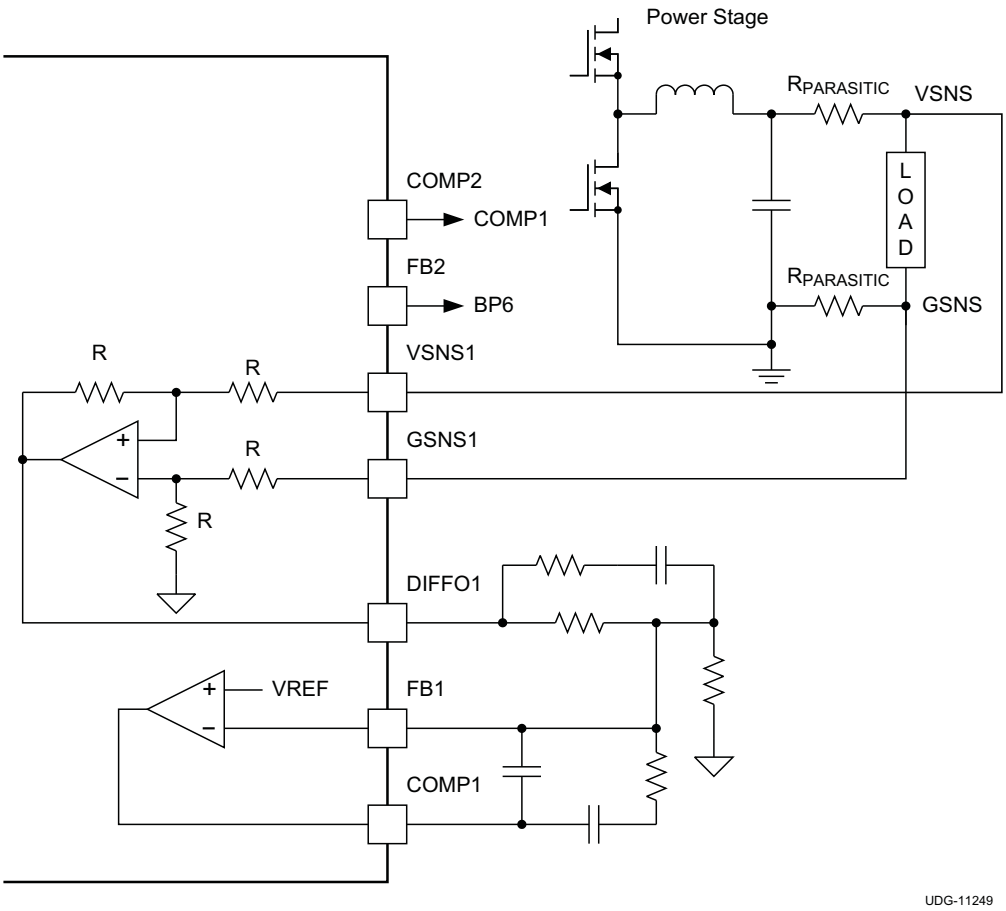


Figure 13. Two-Phase Mode Configuration

When the device operates in two-phase mode, a current sharing loop as shown in Figure 13 is designed to maintain the current balance between phases. Both phases share the same comparator voltage (COMP1). The sensed current in each phase is compared first in a current share block, then an error current and fed into COMP. The resulted error voltage is compared with the voltage ramp to generate the PWM pulse.

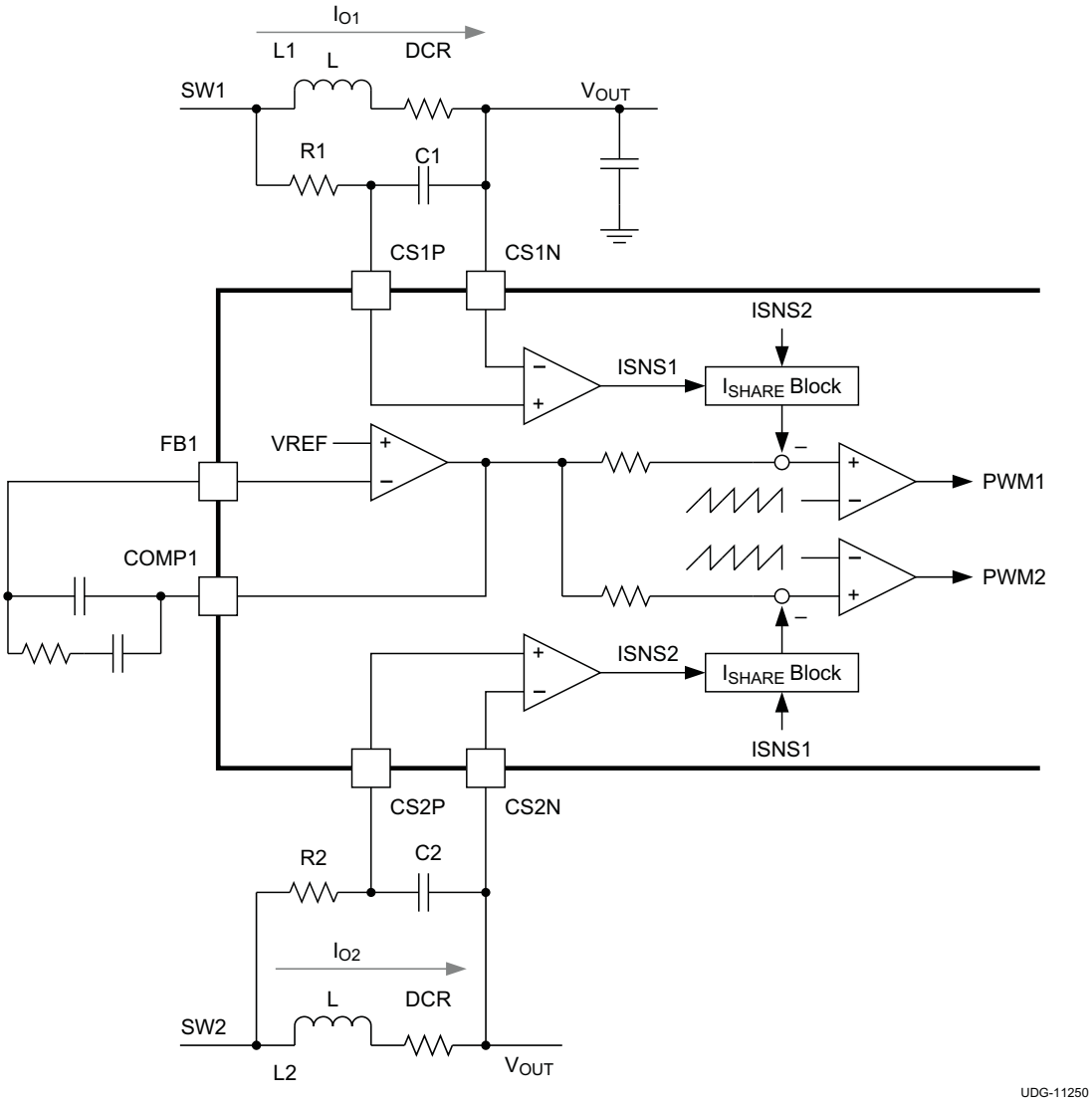


Figure 14. Two-Phase Mode Current Share Loop

Linear Regulators

The TPS40422 has two on-board linear regulators primarily intended to provide suitable power for the internal circuitry of the device. These pins, BP3 and BP6 must be properly bypassed to function properly. BP3 needs a minimum of 100 nF connected to AGND and BP6 should have approximately 1 µF of capacitance connected to PGND.

It is permissible to use the external regulator to power other circuits if desired, but care must be taken to ensure that the loads placed on the regulators do not adversely affect operation of the controller. The main consideration is to avoid loads with heavy transient currents that can affect the regulator outputs. Transient voltages on these outputs could result in noisy or erratic operation of the TPS40422.

Current limits must also be observed. Shorting the BP3 pin to GND damages the BP3 regulator. The BP3 regulator input comes from the BP6 regulator output. The BP6 regulator can supply 120 mA so the total current drawn from both regulators must be less than that. This total current includes the device operating current I_{VDD} plus the gate drive current required to drive the power FETs. The total available current from two regulators is described in Equation 3 and Equation 4:

$$I_{L(in)} = I_{BP6} - \left(I_{VDD} + I_{GATE}\right) \tag{3}$$

$$I_{GATE} = f_{SW} \times \left(Q_{gHIGH} + Q_{gLOW}\right) \tag{4}$$

where

- $I_{L(in)}$ is the total current that can be drawn from BP3 and BP6 in aggregate
- I_{BP6} is the current limit of the BP6 regulator (120-mA minimum)
- I_{VDD} is the quiescent current of the TPS40422 (15-mA maximum)
- I_{GATE} is the gate drive current required by the power FETs
- f_{SW} is the switching frequency
- Q_{gHIGH} is the total gate charge required by the high-side FETs
- Q_{gLOW} is the total gate charge required by the low-side FETs

BP Crossover

If the voltage on the BPEXT pin is lower than the switch-over voltage, $V_{BPEXT(swover)}$, then the internal BP6 regulator is used. If the voltage on the BPEXT pin exceeds this switch-over voltage, then the internal BP6 regulator is bypassed and the BP6 pin follows BPEXT, until the voltage on the BPEXT pin falls by the BPEXT switch-over hysteresis amount, $V_{HYS(swover)}$.

If the BPEXT function is not used, it is recommended to connect the BPEXT pin to GND. Depending on board layout, there may be noise injected into the BPEXT pin. If the voltage on the BPEXT pin changes dynamically in the application, crossing above and below the switch-over voltage, then an external 10 kΩ resistor can be connected from BPEXT to GND to increase noise immunity.

Switching Frequency Setting

The switching frequency is set by the value of the resistor connected from the RT pin to AGND. The RT resistor value is calculated in Equation 5.

$$R_{RT} = \frac{20 \times 10^9}{f_{SW}} \tag{5}$$

where

- R_{RT} is the the resistor from RT pin to AGND, in Ω
- f_{SW} is the desired switching frequency, in Hz

The TPS40422 device can also synchronize to an external clock that is ±20% of the master clock frequency which is two times the free running frequency.

PMBus Functionality

PMBus Address

The PMBus specification requires that each device connected to the PMBus have a unique address on the bus. The TPS40422 has 64 possible addresses (0 through 63 in decimal) that can be assigned by connecting resistors from the ADDR0 and ADDR1 pins to AGND. The address is set in the form of two octal (0-7) digits, one digit for each pin. ADDR1 is the high-order digit and ADDR0 is the low-order digit.

The E48 series resistors suggested for each digit value are shown in Table 1.

Table 1. E48 Series Resistors

DIGIT	RESISTANCE (kΩ)
0	11
1	18.7
2	27.4
3	38.3
4	53.6
5	82.5
6	127
7	187

The TPS40422 also detects values that are out of range on the ADDR0 and ADDR1 pins. If either pin is detected as having an out of range resistance connected to it, the device continues to respond to PMBus commands, but at address 127, which is outside of the possible programmed addresses. It is possible but not recommended to use the device in this condition, especially if other TPS40422 devices are present on the bus or if another device could possibly occupy the 127 address.

PMBus Connections

The TPS40422 supports both the 100-kHz and 400-kHz bus speeds. Connection for the PMBus interface should follow the *High Power DC* specifications given in section 3.1.3 on the System Management Bus (SMBus) Specification V2.0 for the 400-kHz bus speed or the *Low Power DC* specifications in section 3.1.2. The complete SMBus specification is available from the SMBus web site, smbus.org.

PMBus Data Format

There are three data formats supported in PMBus form commands that require representation of a literal number as their argument (commands that set thresholds, voltages or report such). A compatible device needs to only support one of these formats. The TPS40422 supports the *Linear* data format only for these commands. In this format, the data argument consists of two parts, a mantissa and an exponent. The number represented by this argument can be expressed as shown in Equation 6.

$$\text{Value} = \text{Mantissa} \times 2^{\text{exponent}} \tag{6}$$

PMBus Output Voltage Adjustment

The nominal output voltage of the converter can be adjusted using the VREF_TRIM command. See the VREF_TRIM command description for the format of this command as used in the TPS40422. The adjustment range is between -20% and +10% from the nominal output voltage. The VREF_TRIM command is typically used to trim the final output voltage of the converter without relying on high precision resistors being used in Figure 9. The resolution of the adjustment is 7 bits, with a resulting minimum step size of approximately 0.4%. Note that the output margining is accomplished using this same 7 bit structure so the total combined deviation from the nominal output for margining and VREF_TRIM is remains limited to between -20% and +10%. Exceeding this range is not supported.

The TPS40422 operates in three states that the are determine the actual output voltage:

- No output margin
- Margin high
- Margin low

These output states are set using the OPERATION command. The FB pin reference voltage is calculated as follows in each of these states.

No margin voltage:

$$V_{FB} = VREF\_TRIM + 0.6 \quad (7)$$

Margin high voltage state:

$$V_{FB} = STEP\_VREF\_MARGIN\_HIGH + VREF\_TRIM + 0.6 \quad (8)$$

Margin low state:

$$V_{FB} = STEP\_VREF\_MARGIN\_LOW + VREF\_TRIM + 0.6 \quad (9)$$

where

- V_{FB} is the FB pin voltage
- VREF_TRIM is the offset voltage in volts to be applied to the output voltage
- VREF_MARGIN_HIGH is the requested margin high voltage
- VREF_MARGIN_LOW is the requested margin low voltage

For these conditions, the output voltage is shown in Equation 10.

$$V_{OUT} = V_{FB} \times \left(\frac{(R2 + R1)}{R2} \right) \quad (10)$$

where

- V_{FB} is the pin voltage calculated in Equation 7, Equation 8 or Equation 9 depending on the output state
- R2 and R1 are in consistent units from Figure 9
- V_{OUT} is the output voltage

NOTE

The sum of the margin and trim voltages cannot be more tha between –20% and +10% of the nominal output voltage. The FB pin voltage can deviate no more that this from the nominal 600 mV.

Reading the Output Current

The average output current for the converter is readable using the READ_IOUT command. The results of this command support only positive or current sourced from the converter. If the converter is sinking current the result of this command is a reading of 0 A.

Soft-Start Time

The TPS40422 supports several soft-start times from 600 µs to 9 ms selected by the TON_RISE PMBus command. See the command description for full details on the levels and implementation. When selecting the soft-start time, care must be taken to ensure that the charging current for the output capacitors is considered. In some applications (e.g., those with large amounts of output capacitance) this current can lead to problems with nuisance tripping of the overcurrent protection circuitry. To ensure that this does not happen, the output capacitor charging current should be included when considering where to set the overcurrent threshold. The output capacitor charging current can be found using Equation 11:

$$I_{CAP} = \left(\frac{(V_{OUT} \times C_{OUT})}{t_{SS}} \right)$$

where

- I_{CAP} is the startup charging current of the output capacitance in A
- V_{OUT} is the output voltage of the converter in V
- C_{OUT} is the total output capacitance in F
- t_{SS} is the selected soft-start time in seconds (11)

With the charging current calculated, the overcurrent threshold can then be calibrated to the sum of the maximum load current and the output capacitor charging current plus some margin. The amount of margin required depends on the individual application, but 25% is a suggested starting point. More or less may be required.

Turn-On/Turn-Off Delay and Sequencing

The TPS40422 provides many sequencing options. Using the ON_OFF_CONFIG command, each rail can be configured to startup whenever the input is not in undervoltage lockout or to additionally require a signal on the CNTLx pin and/or receive an update to the OPERATION command over PMBus.

When the gating signal as specified by ON_OFF_CONFIG is reached for that rail, a programmable turn-on delay can be set with TON_DELAY. The rise time can be programmed with TON_RISE. When the specified signal(s) are set to turn the output off, a programmable turn-off delay set by TOFF_DELAY is used before switching is inhibited. More information can be found in the PMBus command descriptions.

When the output voltage is within the PGOOD window after the start-up period, the PGOOD pin is asserted. This can be connected to the CNTL pin of another rail in dual-output mode or on another device to control turn-on and turn-off sequencing.

Pre-Biased Output Start-Up

The TPS40422 contains a circuit that prevents current from being pulled from the output during the start-up sequence in a pre-biased output condition. There are no PWM pulses until the internal soft-start voltage rises above the error amplifier input (FBx pin), if the output is pre-biased. Once the soft-start voltage exceeds the error amplifier input, the device slowly initiates synchronous rectification by starting the synchronous rectifier with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This approach prevents the sinking of current from a pre-biased output, and ensures the output voltage start-up and ramp-to-regulation sequences are smooth and controlled.

DESIGN NOTE

During the soft-start sequence, when the PWM pulse width is shorter than the minimum controllable on-time, which is generally caused by the PWM comparator and gate driver delays, pulse skipping may occur and the output might show larger ripple voltage.

Undervoltage Lockout

The TPS40422 provides flexible user adjustment of the undervoltage lockout threshold and the hysteresis. Two PMBus commands VIN_ON and VIN_OFF allow the user to set these input voltage turn on and turn off thresholds independently, with a minimum of 4-V turn off to a maximum 16-V turn on. See the command descriptions for more details.

Overvoltage and Undervoltage Fault Protection

The TPS40422 has output overvoltage protection and undervoltage protection capability. The comparators that regulate the overvoltage and undervoltage conditions use the FBx pin as the output sensing point so the filtering effect of the compensation network connected from COMPx to FBx has an effect on the speed of detection. As the output voltage rises or falls below the nominal value, the error amplifier attempts to force FBx to match its reference voltage. When the error amplifier is no longer able to do this, the FB pin begins to drift and trip the overvoltage threshold (V_{OVP}) or the undervoltage threshold (V_{UVP}) .

When an undervoltage fault is detected, the device enters hiccup mode and resumes normal operation when the fault is cleared.

When an overvoltage fault is detected, the device turns off the high-side MOSFET and latches on the low-side MOSFET to discharge the output current to the regulation level (within the power good window)

When operating in dual-channel mode, both channels have identical but independent protection schemes which means one channel would not be affected when the other channel is in fault mode.

When operating in two-phase mode, only the FB1 pin is detected for overvoltage and undervoltage fault. Therefore both channels take action together during a fault.

Power Good

The TPS40422 has user selectable power good thresholds. These thresholds determine at what voltage the PGOOD pin is allowed to go high and the associated PMBus flags are cleared. There are three possible settings that can be had. See the POWER_GOOD_ON and POWER_GOOD_OFF command descriptions for complete details. Note that these commands establish symmetrical values above and below the nominal voltage. Values entered for each threshold should be the voltages corresponding to the threshold below the nominal output voltage. For instance, if the nominal output voltage is 3.3 V, and the desired power good on thresholds are ±5%, the POWER_GOOD_ON command is issued with 2.85 V as the desired threshold. The POWER_GOOD_OFF command must be set to a lower value (higher percentage) than the POWER_GOOD_ON command as well. The VOUT_SCALE_LOOP command must be set to approximately 0.1818 for these examples to work correctly.

The FB pin is used to sense the output voltage for the purposes of power good detection. Because of this there is the inherent filtering action provided by the compensation network connected from COMP to FB. As the output voltage rises or falls below the nominal value, the error amplifier attempts to force FB to match its reference voltage. When the error amplifier is no longer able to do this, the FB pin begins to drift and trip the power good threshold. For this reason the network from COMP to FB should have no purely resistive path.

Power good de-asserts during all startups, after any fault condition is detected or whenever the device is turned off or in a disabled state (OPERATION command or CNTLx pins put the device into a disabled or off state). The PGOOD pin acts like a diode to GND when the device has no power applied to the VDD pin.

Overtemperature Fault Protection

The TPS40422 provides programmable overtemperature fault and warning thresholds using measurements from the external temperature sensors connected on the TSNSx pins for each rail. More information can be found in the OT_FAULT_LIMIT (4Fh) and OT_WARN_LIMIT (51h) command descriptions.

Thermal Shutdown

If the junction temperature of the device reaches the thermal shutdown limit of 150°C, the PWMs and the oscillators are turned off and HDRVs and LDRVs are driven low. When the junction cools to the required level (130°C typical), the PWM initiates soft start as during a normal power-up cycle.

Programmable Fault Responses

The overcurrent and output undervoltage response can be programmed using the IOUT_OC_FAULT_RESPONSE command. More information can be found in the IOUT_OC_FAULT_RESPONSE (47h) command description.

User Data and Adjustable Anti-Cross Conduction Delay

The TPS40422 provides a command, MFR_SPECIFIC_00, which can be used as a scratchpad to store 14 bits of arbitrary data. These bits can represent anything that the user desires and can be stored in EEPROM for non-volatility. Bit 0 of this command is used to select between two dead time settings for the controller. The particular setting required for a given application depends upon several things, including total FET gate charge, FET gate resistance, PCB layout quality, temperature, etc. It is not possible to give a hard and fast rule as to when to use which setting, but generally, for FETs above 25 nC gate charge, the longer dead time setting should be looked at. The shorter dead time setting allows higher efficiency in applications where the FETs are generally small and switch very quickly, while may lead to minimum amounts of cross conduction in applications with larger, slower switching FETs. Conversely, using the longer dead time setting with smaller, faster switching FETs leads to excessive body diode conduction in the low-side FET, leading to a drop in converter efficiency.

CAUTION

Bit 1 of this command permanently locks certain parameters from being changed when set to 1. For more detail, see the MFR_SPECIFIC_00 command description.

SUPPORTED COMMANDS

The TPS40422 supports the following commands from the PMBus 1.1 specification.

PAGE (00h)

The PAGE command provides the ability to configure, control, and monitor through only one physical address both channels (outputs) of the TPS40422.

Command	PAGE							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w	r	r	r	r	r	r	r/w
Function	PA	X	X	X	X	X	X	P0
Default Value	0	X	X	X	X	X	X	0

Table 2. PAGE Command Truth Table

PA	P0	LOGIC RESULTS
0	0	All commands address the first channel
0	1	All commands address the second channel
1	0	Illegal input. Ignore this write, take no action
1	1	All commands address both channels

If PAGE=11, then any read commands affect the first channel. Any value written to read-only registers is ignored.

OPERATION (01h)

OPERATION is a paged register. The OPERATION command is used to turn the device output on or off in conjunction with input from the CNTLx pins. It is also used to set the output voltage to the upper or lower MARGIN voltages. The unit stays in the commanded operating mode until a subsequent OPERATION command or a change in the state of the CNTLx pins instructs the device to change to another mode.

Command	OPERATION							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w	r	r/w	r/w	r/w	r/w	r	r
Function	ON	X	Margin				X	X
Default Value	0	0	0	0	0	0	X	X

On

This bit is an enable command to the converter.

- 0: output switching is disabled. Both drivers placed in an off or low state.
- 1: output switching is enabled. The device is allowed to begin power conversion assuming no fault conditions exist.

Margin

If Margin Low is enabled, load the value from the VOUT_MARGIN_LOW command. If Margin High is enabled, load the value from the VOUT_MARGIN_HIGH command. (See PMBus specification for more information)

- 00XX: Margin Off
- 0101: Margin Low (Act on Fault)
- 0110: Margin Low (Act on Fault)
- 1001: Margin High (Act on Fault)
- 1010: Margin High (Act on Fault)

ON_OFF_CONFIG (02h)

ON_OFF_CONFIG is a paged register. The ON_OFF_CONFIG command configures the combination of CNTLx pins input and serial bus commands needed to turn the unit on and off. The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

Command	ON_OFF_CONFIG							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r/w	r/w	r/w	r/w	r
Function	X	X	X	pu	cmd	cpr	pol	cpa
Default Value	X	X	X	1	0	1	1	0

pu

The pu bit sets the default to either operate any time power is present or for the on/off to be controlled by CNTLx pins and PMBus OPERATION command. This bit is used in conjunction with the 'cp', 'cmd', and 'on' bits to determine start up.

Bit Value	ACTION
0	Channel powers up any time power is present regardless of state of the CNTLx pins.
1	Channel does not power up until commanded by the CNTLx pins and OPERATION command as programmed in bits [2:0] of the ON_OFF_CONFIG register.

cmd

The cmd bit controls how the device responds to the OPERATION command.

Bit Value	ACTION
0	Channel ignores the “on” bit in the OPERATION command.
1	Channel responds to the “on” bit in the OPERATION command.

cpr

The cpr bit sets the CNTLx pins response. This bit is used in conjunction with the 'cmd', 'pu', and 'on' bits to determine start up.

Bit Value	ACTION
0	Channel ignores the CNTLx pins. On/off is controlled only by the OPERATION command.
1	Channel requires the CNTLx pins to be asserted to start the unit.

pol

The pol bit controls the polarity of the CNTLx pins. For a change to become effective, the contents of the ON_OFF_CONFIG register must be stored to non-volatile memory using the STORE_USER_ALL command and the device power cycled. Simply writing a new value to this bit does not change the polarity of the CNTLx pins.

Bit Value	ACTION
0	CNTLx pins is active low.
1	CNTLx pins is active high.

cpa

The cpa bit sets the CNTLx pins action when turning the controller off. This bit is read internally and cannot be modified by the user.

Bit Value	ACTION
0	Turn off the output using the programmed delay.

CLEAR_FAULTS (03h)

The CLEAR_FAULTS command is used to clear any fault bits that have been set. This command clears all bits in all status registers in the selected page simultaneously. At the same time, the device negates (clears, releases) its SMBALERT signal output if the device is asserting the SMBALERT signal. The CLEAR_FAULTS command does not cause a unit that has latched off for a fault condition to restart. If the fault is still present when the bit is cleared, the fault bit is immediately reset and the host notified by the usual means.

WRITE_PROTECT (10h)

The WRITE_PROTECT command is used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes. This command is not intended to provide protection against deliberate or malicious changes to the device configuration or operation. All supported command parameters may have their parameters read, regardless of the WRITE_PROTECT settings. The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

Command	WRITE_PROTECT							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	X	X	X	X	X
Function	bit7	bit6	bit5	X	X	X	X	X
Default Value	0	0	0	X	X	X	X	X

bit5

Bit Value	ACTION
0	Enable all writes as permitted in bit6 or bit7
1	Disable all writes except the WRITE_PROTECT, PAGE, OPERATION and ON_OFF_CONFIG. (bit6 and bit7 must be 0 to be valid data)

bit6

Bit Value	ACTION
0	Enable all writes as permitted in bit5 or bit7
1	Disable all writes except for the WRITE_PROTECT, PAGE and OPERATION commands. (bit5 and bit7 must be 0 to be valid data)

bit7

Bit Value	ACTION
0	Enable all writes as permitted in bit5 or bit6
1	Disable all writes except for the WRITE_PROTECT command. (bit5 and bit6 must be 0 to be valid data)

In any case, only one of the three bits may be set at any one time. Attempting to set more than one bit results in an alert being generated and the cml bit is STATUS_WORD being set.

STORE_USER_ALL (15h)

The STORE_USER_ALL command stores all of the current storable register settings in the EEPROM memory as the new defaults on power up.

It is permissible to use this command while the device is switching. Note however that the device continues to switch but ignores all fault conditions until the internal store process has completed.

EEPROM programming faults cause the device to NACK and set the 'cml' bit in the STATUS_BYTE and the 'oth' bit in the STATUS_CML registers.

RESTORE_USER_ALL (16h)

The RESTORE_USER_ALL command restores all of the storable register settings from EEPROM memory.

This command should not be used while the device is actively switching. If this is done, the device stops switching the output drivers and the output voltage drops. Depending on loading conditions, the output voltage could reach an undervoltage level and trigger an undervoltage fault response if programmed to do so. The command can be used while the device is switching, but it is not recommended as it results in a restart that could disrupt power sequencing requirements in more complex systems. It is strongly recommended that the device be stopped before issuing this command.

CAPABILITY (19h)

The CAPABILTY command provides a way for a host system to determine some key capabilities of this PMBus device.

Command	CAPABILITY							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	PEC	SPD		ALRT	Reserved			
Default Value	1	0	1	1	0	0	0	0

The default values indicate that the TPS40422 supports Packet Error Checking (PEC), a maximum bus speed of 400 kHz (SPD) and the SMBus Alert Response Protocol using a SMBALERT pin (ALRT).

VOUT_MODE (20h)

The PMBus specification dictates that the data word for the VOUT_MODE command is one byte that consists of a 3-bit mode and 5-bit exponent parameter, as shown below. The 3-bit mode sets whether the device uses the Linear or Direct modes for output voltage related commands. The 5-bit parameter sets the exponent value for the linear data mode. The mode and exponent parameters are set and do not permit the user to change the values.

Command	VOUT_MODE							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	Mode			Exponent				
Default Value	0	0	0	1	1	1	1	1

Mode:

Value fixed at 000, linear mode.

Exponent

Value fixed at 10111, Exponent for Linear mode values is –9.

VIN_ON (35h)

The VIN_ON command sets the value of the input voltage at which the unit should start operation assuming all other required startup conditions are met. Values are mapped to the nearest supported increment. Values outside the supported range are treated as invalid data and cause the device set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers. The value of VIN_ON remains unchanged on an out-of-range write attempt. The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

The supported VIN_ON values are:

4.25 (default)	4.5	4.75	5	5.25
5.5	5.75	6	6.25	6.5
6.75	7	7.25	7.5	8
8.25	8.5	8.75	9	9.25
9.5	10	10.5	11	11.5
12	12.5	13	14	15
16				

VIN_ON must be set higher than VIN_OFF. Attempting to write either VIN_ON lower than VIN_OFF or VIN_OFF higher than VIN_ON results in the new value being rejected, SMBALERT being asserted along with the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

The data word that accompanies this command is divided into a fixed 5-bit exponent and an 11-bit mantissa. The four most significant bits of the mantissa are fixed, while the lower 7 bits may be altered.

Command	**VIN_ON**															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	1	1	1	1	0	0	0	0	0	0	0	1	0	0	0	1

Exponent

–2 (dec), fixed.

Mantissa

The upper four bits are fixed at 0.
The lower seven bits are programmable with a default value of 9 (dec). This corresponds to a default of 4.25 V.

VIN_OFF (36h)

The VIN_OFF command sets the value of the input voltage at which the unit should stop operation. Values are mapped to the nearest supported increment. Values outside the supported range is treated as invalid data and causes the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers. The value of VIN_OFF remains unchanged during an out-of-range write attempt. The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

The supported VIN_OFF values are:

4 (default)	4.25	4.5	4.75	5
5.25	5.5	5.75	6	6.25
6.5	6.75	7	7.25	7.5
8	8.25	8.5	8.75	9
9.25	9.75	10.25	10.75	11.25
11.75	12	13.75	14.75	15.75

VIN_ON must be set higher than VIN_OFF. Attempting to write either VIN_ON lower than VIN_OFF or VIN_OFF higher than VIN_ON resultx in the new value being rejected, SMBALERT being asserted along with the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

The data word that accompanies this command is divided into a fixed 5 bit exponent and an 11 bit mantissa. The 4 most significant bits of the mantissa are fixed, while the lower 7 bits may be altered.

Command	**VIN_OFF**															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	1	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0

Exponent

–2 (dec), fixed.

Mantissa

The upper four bits are fixed at 0.
The lower seven bits are programmable with a default value of 8 (dec). This corresponds to a default value of 4.0 V.

IOUT_CAL_GAIN (38h)

IOUT_CAL_GAIN is a paged register. The IOUT_CAL_GAIN is the ratio of the voltage at the current sense element to the sensed current. The units are Ohms (Ω). The effective current sense element can be the DC resistance of the inductor or a separate current sense resistor. The default setting is 0.488 mΩ, and the resolution is 30.5 µΩ. The range is 0.244 mΩ to 15.5 mΩ. The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL or STORE_DEFAULT_CODE commands.

Command	**IOUT_CAL_GAIN**															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	1	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0

Exponent

–15 (dec), fixed.

Mantissa

The upper two bits are fixed at 0.
The lower nine bits are programmable with a default value of 16 (dec).

Depending on the value of IOUT_CAL_GAIN, the current sense amplifier used for current monitoring (but not overcurrent or current sharing) changes, as shown in Table 3.

Table 3. Current Sense Amplifier Settings

IOUT_CAL_GAIN (mΩ) RANGE		CSA GAIN (V/V)
MIN	MAX	
0.244	0.5795	25
0.5796	1.1285	15
1.1286	15.5	10

IOUT_CAL_OFFSET (39h)

IOUT_CAL_OFFSET is a paged register. The IOUT_CAL_OFFSET is used to compensate for offset errors in the READ_IOUT results and the IOUT_OC_FAULT_LIMIT and IOUT_OC_WARN_LIMIT thresholds. The units are amperes. The default setting is 0 A. The resolution of the argument for this command is 62.5 mA and the range is +3937.5 mA to -4000 mA. Values written outside of this range alias into the supported range. For example, 1110 0100 0000 0001 has an expected value of –63.9375 A, but results in 1110 0111 1111 0001 which is –3.9375 A. This occurs because the read-only bits are fixed. The exponent is always –4 and the 5 msb bits of the Mantissa are always equal to the sign bit. The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

Command	IOUT_CAL_OFFSET															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r/w	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Exponent

–4 (dec), fixed.

Mantissa

MSB is programmable with sign, next 4 bits are sign extend only.
Lower six bits are programmable with a default value of 0 (dec).

IOUT_OC_FAULT_LIMIT (46h)

IOUT_OC_FAULT_LIMIT is a paged register. The IOUT_OC_FAULT_LIMIT command sets the value of the output current, in amperes, that causes the overcurrent detector to indicate an overcurrent fault condition. The IOUT_OC_FAULT_LIMIT should be set equal to or greater than the IOUT_OC_WARN_LIMIT. Writing a value to IOUT_OC_FAULT_LIMIT less than IOUT_OC_WARN_LIMIT causes the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers as well as assert the SMBALRT signal. The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

The IOUT_OC_FAULT_LIMIT takes a two-byte data word formatted as shown below:

Command	IOUT_OC_FAULT_LIMIT															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0

Exponent

–1 (dec), fixed.

Mantissa

The upper four bits are fixed at 0.
The lower seven bits are programmable with a default value of 60 (dec).

The actual output current for a given mantissa and exponent is shown in Equation 12.

$$I_{OUT(oc)} = \text{Mantissa} \times 2^{\text{Exponent}} = \frac{\text{Mantissa}}{2} \quad (12)$$

The default output fault current setting is 30 A. Values of $I_{OUT(oc)}$ can range between 3 A and 50 A in 500-mA increments.

IOUT_OC_FAULT_RESPONSE (47h)

IOUT_OC_FAULT_RESPONSE is a paged register. The IOUT_OC_FAULT_RESPONSE command instructs the device on what action to take in response to an IOUT_OC_FAULT_LIMIT or a VOUT undervoltage (UV) fault. The device also:

- Sets the IOUT_OC bit in the STATUS_BYTE
- Sets the IOUT/POUT bit in the STATUS_WORD
- Sets the IOUT OC Fault bit in the STATUS_IOUT register
- Notifies the host by asserting SMBALERT

The contents of this register can be stored to non-volatile memory using the STORE_USER command.

Command	IOUT_OC_FAULT_RESPONSE							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r/w	r/w	r/w	r	r	r
Function	X	X	RS[2]	RS[1]	RS[0]	X	X	X
Default Value	0	0	1	1	1	1	0	0

RS[2:0]

000: A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared (See section 10.7 of the PMBus spec.)

111: A one value for the Retry Setting means that the unit goes through a normal startup (Soft start) continuously, without limitation, until it is commanded off or bias power is removed or another fault condition causes the unit to shutdown.

Any value other than 000 or 111 is not accepted. Attempting to write any other value is rejected, causing the TPS404022 to assert $\overline{\text{SMBALERT}}$ along with the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

IOUT_OC_WARN_LIMIT (4Ah)

IOUT_OC_WARN_LIMIT is a paged register. The IOUT_OC_WARN_LIMIT command sets the value of the output current, in amperes, that causes the over-current detector to indicate an over-current warning. When this current level is exceeded the device:

- Sets the OTHER bit in the STATUS_BYTE
- Sets the IOUT/POUT bit in the STATUS_WORD
- Sets the IOUT overcurrent Warning (OCW) bit in the STATUS_IOUT register, and
- Notifies the host by asserting $\overline{\text{SMBALRT}}$

The IOUT_OC_WARN_LIMIT threshold should always be set to less than or equal to the IOUT_OC_FAULT_LIMIT. Writing a value to IOUT_OC_WARN_LIMIT greater than IOUT_OC_FAULT_LIMIT causes the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers as well as assert the $\overline{\text{SMBALRT}}$ signal. The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

The IOUT_OC_WARN_LIMIT takes a two byte data word formatted as shown below:

Command	IOUT_OC_WARN_LIMIT															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	1	1	1	1	1	0	0	0	0	0	1	1	0	1	1	0

Exponent

–1 (dec), fixed.

Mantissa

The upper four bits are fixed at 0.
Lower seven bits are programmable with a default value of 54 (dec).

The actual output warning current level for a given mantissa and exponent is:

$$I_{OUT(OCW)} = \text{Mantissa} \times 2^{\text{Exponent}} - \frac{\text{Mantissa}}{2} \quad (13)$$

The default output warning current setting is 27 A. Values of $I_{OUT(OCW)}$ can range from 2 A to 49 A in 500-mA increments.

OT_FAULT_LIMIT (4Fh)

OT_FAULT_LIMIT is a paged register. The OT_FAULT_LIMIT command sets the value of the temperature, in degrees Celsius, that causes an over-temperature fault condition, when the sensed temperature from the external sensor exceeds this limit. Upon triggering the over-temperature fault, the following actions are taken:

- Sets the TEMPERATURE bit in the STATUS_BYTE
- Sets the OT Fault bit in the STATUS_TEMPERATURE
- Notifies the host by asserting $\overline{\text{SMBALERT}}$

Once the over-temperature fault is tripped, the output is latched off until the external sensed temperature falls 20°C from the OT_FAULT_LIMIT, at which point the output goes through a normal startup (soft-start).

The OT_FAULT_LIMIT must always be greater than the OT_WARN_LIMIT. Writing a value to OT_FAULT_LIMIT less than or equal to OT_WARN_LIMIT causes the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers as well as asserts the $\overline{\text{SMBALERT}}$ signal. The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

The OT_FAULT_LIMIT takes a two byte data word formatted as shown below.

Command	OT_FAULT_LIMIT															
Format	Unsigned binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0

Exponent

0 (dec), fixed.

Mantissa

The upper three bits are fixed at 0.
Lower eight bits are programmable with a default value of 145 (dec).

The default over-temperature fault setting is 145°C. Values can range from 120°C to 165°C in 1°C increments.

OT_WARN_LIMIT (51h)

OT_WARN_LIMIT is a paged register. The OT_ WARN _LIMIT command sets the value of the temperature, in degrees Celsius, that causes an over-temperature warning condition, when the sensed temperature from the external sensor exceeds this limit. Upon triggering the over-temperature warning, the following actions are taken:

- Sets the TEMPERATURE bit in the STATUS_BYTE
- Sets the OT Warning bit in the STATUS_TEMPERATURE
- Notifies the host by asserting $\overline{\text{SMBALERT}}$

Once the over-temperature warning is tripped, warning is latched until the external sensed temperature falls 20°C from the OT_WARN_LIMIT.

The OT_WARN_LIMIT must always be less than the OT_FAULT_LIMIT. Writing a value to OT_WARN_LIMIT greater than or equal to OT_FAULT_LIMIT causes the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers as well as assert the $\overline{\text{SMBALERT}}$ signal. The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

The OT_WARN_LIMIT takes a two byte data word formatted as shown below:

Command	OT_WARN_LIMIT															
Format	Unsigned binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1

Exponent

0 (dec), fixed.

Mantissa

The upper three bits are fixed at 0.
Lower eight bits are programmable with a default value of 125 (dec).

The default over-temperature fault setting is 125°C. Values can range from 100°C to 140°C in 1°C increments.

TON_RISE (61h)

TON_RISE is a paged register. The TON_RISE command sets the time in ms, from when the output starts to rise until the voltage has entered the regulation band. It also determines the rate of the transition of the reference voltage (either due to VREF_TRIM or STEP_VREF_MARGIN_x commands) when this transition is executed during the soft-start period. There are several discrete settings that this command supports. Commanding a value other than one of these values results in the nearest supported value being selected.

The supported TON_RISE times over PMBus are:

- 600 µs
- 900 µs
- 1.2 ms
- 1.8 ms
- **2.7 ms (default value)**
- 4.2 ms
- 6.0 ms
- 9.0 ms

A value of 0 ms instructs the unit to bring its output voltage to the programmed regulation value as quickly as possible. The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

The TON_RISE command is formatted as a linear mode two's complement binary integer.

Command	TON_RISE															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	1	1	1	0	0	0	0	0	0	0	1	0	1	0	1	1

Exponent

–4 (dec), fixed.

Mantissa

The upper two bits are fixed at 0.
The lower eight bits are programmable with a default value of 43 (dec).

STATUS_BYTE (78h)

STATUS_BYTE is a paged register. The STATUS_BYTE command returns one byte of information with a summary of the most critical device faults. Three fault bits are flagged in this particular command: output overvoltage, output overcurrent, and over-temperature. The STATUS_BYTE reports communication faults in the CML bit. Other communication faults set the NONE OF THE ABOVE bit.

Command	STATUS_BYTE							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	X	OFF	VOUT_OV	IOUT_OC	VIN_UV	TEMPERATURE	CML	NONE OF THE ABOVE
Default Value	0	0	0	0	0	0	0	0

A "1" in any of these bit positions indicates that:

OFF:

The device is not providing power to the output, regardless of the reason. In TPS40422, this flag means that the converter is not enabled.

VOUT_OV:

An output overvoltage fault has occurred.

IOUT_OC:

An output over current fault has occurred.

VIN_UV:

An input undervoltage fault has occurred.

TEMPERATURE:

A temperature fault or warning has occurred.

CML:

A **C**ommunications, **M**emory or **L**ogic fault has occurred.

NONE OF THE ABOVE:

A fault or warning not listed in bit1 through bits 1-7 has occurred, for example an undervoltage condition or an over current warning condition

STATUS_WORD (79h)

STATUS_WORD is a paged register. The STATUS_WORD command returns two bytes of information with a summary of the device's fault/warning conditions. The low byte is identical to the STATUS_BYTE above. The additional byte reports the warning conditions for output overvoltage and overcurrent, as well as the power good status of the converter.

Command	STATUS_WORD (low byte)							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	X	OFF	VOUT_OV	IOUT_OC	VIN_UV	TEMPERATURE	CML	NONE OF THE ABOVE
Default Value	0	x	0	0	0	0	0	0

A "1" in any of the low byte (STATUS_BYTE) bit positions indicates that:

OFF:

The device is not providing power to the output, regardless of the reason. In TPS40422, this flag means that the converter is not enabled.

VOUT_OV:

An output overvoltage fault has occurred.

IOUT_OC:

An output over current fault has occurred.

VIN_UV:

An input undervoltage fault has occurred.

TEMPERATURE:

A temperature fault or warning has occurred.

CML:

A **C**ommunications, **M**emory or **L**ogic fault has occurred.

NONE OF THE ABOVE:

A fault or warning not listed in bits 1-7 has occurred

Command	STATUS_WORD (high byte)							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	VOUT	IOUT/POUT	X	MFR	$\overline{\text{POWER\_GOOD}}$	X	X	X
Default Value	0	0	0	0	0	0	0	0

A "1" in any of the high byte bit positions indicates that:

VOUT:

An output voltage fault or warning has occurred

IOUT/POUT:

An output current warning or fault has occurred. The PMBus specification states that this also applies to output power. TPS40422 does not support output power warnings or faults.

MFR:

An internal thermal shutdown (TSD) fault has occurred in the device.

$\overline{\text{POWER\_GOOD}}$:

The power good signal has not transitioned from high-to-low. This is not implemented in 2-phase operation.

STATUS_VOUT (7Ah)

STATUS_VOUT is a paged register. The STATUS_VOUT command returns one byte of information relating to the status of the converter's output voltage related faults. The only bits of this register supported are:

- VOUT_OV Fault
- VOUT_UV Fault

Command	STATUS_VOUT							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	VOUT OV Fault	X	X	VOUT UV Fault	X	X	X	X
Default Value	0	0	0	0	0	0	0	0

A "1" in any of these bit positions indicates that:

VOUT OV Fault:

The device has seen the output voltage rise above the output overvoltage threshold.

VOUT UV Fault:

The device has seen the output voltage fall below the output undervoltage threshold.

STATUS_IOUT (7Bh)

STATUS_IOUT is a paged register. The STATUS_IOUT command returns one byte of information relating to the status of the converter's output current related faults. The only bits of this register supported are .

- IOUT_OC Fault
- IOUT_OC Warning

Command	STATUS_IOUT							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	IOUT_OV Fault	X	IOUT OC Warning	X	X	X	X	X
Default Value	0	0	0	0	0	0	0	0

A "1" in any of these bit positions indicates that:

IOUT_OV Fault:

The device has seen the output current rise above the level set by IOUT_OC_FAULT_LIMIT.

VOUT_UV Fault:

The device has seen the output current rise relating to the level set by IOUT_OC_WARN_LIMIT.

STATUS_TEMPERATURE (7Dh)

STATUS_TEMPERATURE is a paged register. The STATUS_TEMPERATURE command returns one byte of information relating to the status of the external temperature related faults. The only bits of this register supported are:

- OT Fault
- OT Warning

Command	STATUS_TEMPERATURE							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	OT Fault	OT Warning	X	X	X	X	X	X
Default Value	0	0	0	0	0	0	0	0

A "1" in any of these bit positions indicates that:

OT Fault:

The measured external temperature has exceeded the level set by OT_FAULT_LIMIT.

OT Warning:

The measured external temperature has exceeded the level set by OT_WARN_LIMIT.

STATUS_CML (7Eh)

The STATUS_CML command returns one byte of information relating to the status of the converter's communication related faults. The bits of this register supported by the TPS40422 are:

- nvalid/Unsuppported Command
- Invalid/Unsupported Data
- Packet Error Check Failed
- Memory Fault Detected
- Other Communication Fault.

I

Command	STATUS_CML							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	Invalid/ Unsuppported Command	Invalid/ Unsupported Data	Packet Error Check Failed	Memory Fault Detected	X	X	Other Communication Fault	X
Default Value	0	0	0	0	0	0	0	0

A "1" in any of these bit positions indicates that:

Invalid/Unsupported Command:

An invalid or unsupported command has been received.

Invalild/Unsupported Data

Invalid or unsupported data has been received

Packet Error Check Failed

A packet has failed the CRC error check.

Memory Fault Detected

A fault has been detected with the internal memory.

Other Communication Fault

Some other communication fault or error has occurred

STATUS_MFR_SPECIFIC (80h)

The STATUS_MFR_SPECIFIC command returns one byte of information relating to the status of manufacturer-specific faults or warnings.

Command	STATUS_MFR_SPECIFIC							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	OTFI	X	X	IVADDR	X	X	X	TWOPH_EN
Default Value	0	0	0	0	0	0	0	0

A "1" in any of these bit positions indicates that:

OTFI:

The internal temperature is above the thermal shutdown (TSD) fault threshold

IVADDR:

The PMBus address detection circuit is not resolving to a valid address. In this event, the device responds to the address 127 (dec).

TWOPH_EN:

The part has detected that it is in two-phase mode (by pulling FB2 high). This bit does not trigger $\overline{\text{SMBALERT}}$.

READ_VOUT (8Bh)

READ_VOUT is a paged register. The READ_VOUT commands returns two bytes of data in the linear data format that represent the output voltage of the controller. The output voltage is sensed at the remote sense amplifier output pin so voltage drop to the load is not accounted for. The data format is as shown below:

Command	READ_VOUT															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Mantissa															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The setting of the VOUT_MODE affects the results of this command as well. In the TPS40422, VOUT_MODE is set to linear mode with an exponent of –9 and cannot be altered. The output voltage calculation is shown in Equation 14.

$$V_{OUT} = \text{Mantissa} \times 2^{\text{Exponent}} \quad (14)$$

READ_IOUT (8Ch)

READ_IOUT is a paged register. The READ_IOUT commands returns two bytes of data in the linear data format that represent the output current of the controller. The output current is sensed across the CSxP and CSxN pins. The data format is as shown below:

Command	READ_IOUT															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Exponent					Mantissa										
Default Value	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

The output current is scaled before it reaches the internal analog to digital converter so that resolution of the output current read is 62.5 mA, though resolution may be less depending on the setting of IOUT_CAL_GAIN. The maximum value that can be reported is 64 A. It is mandatory that the IOUT_CAL_GAIN and IOUT_CAL_OFFSET parameters are set correctly in order to obtain accurate results. The output current can be found by using Equation 15.

$$I_{OUT} = \text{Mantissa} \times 2^{\text{Exponent}} \tag{15}$$

Exponent

Fixed at -4..

Mantissa

The lower 10 bits are the result of the ADC conversion of the input voltage. The 11th bit is fixed at 0 because only positive numbers are considered valid. Any computed negative current is reported as 0 A..

READ_TEMPERATURE_2 (8Eh)

READ_TEMPERATURE_2 is a paged register. The READ_TEMPERATURE_2 command returns the external temperature in degrees Celsius of the current channel.

Command	READ_TEMPERATURE_2															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Exponent					Mantissa										
Default Value	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1

Exponent

0 (dec), fixed.

Mantissa

The lower 11 bits are the result of the ADC conversion of the external temperature. The default reading is 25 (dec) corresponding to a temperature of 25°C.

PMBUS_REVISION (98h)

The PMBUS_REVISION command returns a single, unsigned binary byte that indicates that the TPS40422 is compatible with the 1.1 revision of the PMBus specification.

Command	PMBUS_REVISION							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Default Value	0	0	0	1	0	0	0	1

MFR_SPECIFIC_00 (D0h)

The MFR_SPECIFIC_00 register is dedicated as a user scratch pad.

Command	MFR_SPECIFIC_00															
Format	Unsigned binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	User scratch pad															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

VREF_TRIM (MFR_SPECIFIC_04) (D4h)

VREF_TRIM is a paged register. The VREF_TRIM command is used to apply a fixed offset voltage to the reference voltage. It is most typically used by the end user to trim the output voltage at the time the PMBus device is assembled into the end user system. The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

The effect of this command is determined by the settings of the VOUT_MODE command. In this device, the VOUT_MODE is fixed to Linear with an exponent of –9 (decimal).

$$V_{REF(offset)} = VREF\_TRIM \times 2^{-9} \tag{16}$$

The maximum trim range is -20% to +10% of the nominal reference voltage (600 mV) in 2 mV steps. Permissible values range from -120 mV to +60 mV. If a value outside this range is given with this command, the TPS40422 sets the reference voltage to the upper or lower limit depending on the direction of the setting, asserts SMBALERT and sets the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

Including settings from both VREF_TRIM and STEP_VREF_MARGIN_x commands, the net permissible reference voltage adjustment range is -180 mV to +60 mV (-30% to +10%). If a value outside this range is given with this command, the TPS40422 sets the reference voltage to the upper or lower limit depending on the direction of the setting, asserts SMBALERT and sets the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

The reference voltage transition occurs at the rate determined by the TON_RISE command if the transition is executed during soft-start. Any transition in the reference voltage after soft-start is complete occurs at the rate determined by the highest programmable TON_RISE.

Command	VREF_TRIM															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r/w	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w
Function	High Byte								Low Byte							
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

STEP_VREF_MARGIN_HIGH (MFR_SPECIFIC_05) (D5h)

STEP_VREF_MARGIN_HIGH is a paged register. The STEP_VREF_MARGIN_HIGH command sets the target voltage which the reference voltage changes to when the OPERATION command is set to "Margin High". The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

The effect of this command is determined by the settings of the VOUT_MODE command. In this device, the VOUT_MODE is fixed to Linear with an exponent of –9 (decimal). The actual reference voltage commanded by a margin high command can be found by:

$$V_{REF(MH)} = (STEP\_VREF\_MARGIN\_HIGH + VREF\_TRIM) \times 2^{-9} \quad (17)$$

The margin high range is 0% to 10% of the nominal reference voltage (600 mV) in 2-mV steps. Permissible values range from 0 mV to 60 mV. If a value outside this range is given with this command, the TPS40422 sets the reference voltage to the upper or lower limit depending on the direction of the setting, asserts SMBALERT and sets the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

Including settings from both VREF_TRIM and STEP_VREF_MARGIN_x commands, the net permissible reference voltage adjustment range is -180 mV to 60 mV (-30% to 10%). If a value outside this range is given with this command, the TPS40422 sets the reference voltage to the upper or lower limit depending on the direction of the setting, asserts SMBALERT and sets the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

The reference voltage transition occurs at the rate determined by the TON_RISE command if the transition is executed during soft-start. Any transition in the reference voltage after soft-start is complete occurs at the rate determined by the highest programmable TON_RISE.

Command	STEP_VREF_MARGIN_HIGH															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w
Function	High Byte								Low Byte							
Default Value	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0

The default value of STEP_VREF_MARGIN_HIGH is 30 (dec). This corresponds to a default margin high voltage of 60 mV (±10%) .

STEP_VREF_MARGIN_LOW (MFR_SPECIFIC_06) (D6h)

STEP_VREF_MARGIN_LOW is a paged register. The STEP_VREF_MARGIN_LOW command sets the target voltage which the reference voltage changes to when the OPERATION command is set to "Margin Low". The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

The effect of this command is determined by the settings of the VOUT_MODE command. In this device, the VOUT_MODE is fixed to Linear with an exponent of –9 (decimal). The actual output voltage commanded by a margin high command is shown in Equation 18.

$$V_{REF(ML)} = (STEP\_VREF\_MARGIN\_LOW + VREF\_TRIM) \times 2^{-9} \quad (18)$$

The margin low range is -20% to 0% of the nominal reference voltage (600 mV) in 2-mV steps. Permissible values range from -120 mV to 0 mV. If a value outside this range is given with this command, the TPS40422 sets the reference voltage to the upper or lower limit depending on the direction of the setting, asserts SMBALERT and sets the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

Including settings from both VREF_TRIM and STEP_VREF_MARGIN_x commands, the net permissible reference voltage adjustment range is -180 mV to 60 mV (-30% to +10%). If a value outside this range is given with this command, the TPS40422 sets the reference voltage to the upper or lower limit depending on the direction of the setting, asserts SMBALERT and sets the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

The reference voltage transition occurs at the rate determined by the TON_RISE command if the transition is executed during soft-start. Any transition in the reference voltage after soft-start is complete occurs at the rate determined by the highest programmable TON_RISE.

Command	**STEP_VREF_MARGIN_LOW**															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r/w	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w
Function	High Byte								Low Byte							
Default Value	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1	0

The default value of STEP_VREF_MARGIN_LOW is -30 (dec). This corresponds to a default margin low voltage of -60 mV (±10%).

PCT_VOUT_FAULT_PG_LIMIT (MFR_SPECIFIC_07) (D7h)

PCT_VOUT_FAULT_PG_LIMIT is a paged register. The PCT_VOUT_FAULT_PG_LIMIT command is used to set the PGOOD, VOUT_UNDER_VOLTAGE (UV) and VOUT_OVER_VOLTAGE (OV) limits as a percentage of nominal.

In two-phase mode, the user can write to PAGE 0 (channel 1) only. Any writes to PAGE 1 are not acknowledged.

The PCT_VOUT_FAULT_PG_LIMIT takes a one byte data word formatted as shown below:

Command	PCT_VOUT_FAULT_PG_LIMIT							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w
Function	X	X	X	X	X	X	PCT_MSB	PCT_LSB
Default Value	0	0	0	0	0	0	0	0

The PGOOD, VOUT_UNDER_VOLTAGE (UV) and VOUT_OVER_VOLTAGE (OV) settings are shown in Table 4, as a percentage of nominal reference voltage on the FBx pins.

Table 4. Protection Settings

PCT_MSB	PCT_LSB	UV	PGL LOW	PGL HIGH	PGH HIGH	PGH LOW	OV
0	0	-16.67%	-12.5%	-8.33%	12.50%	8.33%	16.67%
0	1	-12.50%	-8.33%	-4.17%	8.33%	4.17%	12.50%
1	0	-29.17%	-20.83%	-16.67%	8.33%	4.17%	12.50%
1	1	-41.67%	-37.50%	-33.33%	8.33%	4.17%	12.50%

The PGOOD pin can be tripped if the output voltage is too high (using PGH high) or too low (using PGL low). Additionally, the PGOOD pin has hysteresis. When the output trips PGOOD going low (at PGL low), the output must rise past PGL high before PGOOD is reset. Likewise, when the output trips PGOOD going high (at PGH high), the output must lower past PGH low before PGOOD is reset.

Additionally, when output overvoltage (OV) is tripped, the output must lower below the PGH low threshold, before PGOOD and OV are reset. Likewise, when output undervoltage (UV) is tripped, the output must rise above the PGOOD high threshold, before PGOOD and UV are reset.

SEQUENCE_TON_TOFF_DELAY (MFR_SPECIFIC_08) (D8h)

SEQUENCE_TON_TOFF_DELAY is a paged register. The SEQUENCE_TON_TOFF_DELAY command is used to set the delay for turning on the device and turning off the device as a ratio of TON_RISE.

In two-phase mode, the user can only write to PAGE 0 (channel 1). Any writes to PAGE 1 is not acknowledged.

The SEQUENCE_TON_TOFF_DELAY takes a one byte data word formatted as shown below:

Command	SEQUENCE_TON_TOFF_DELAY							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r	r/w	r/w	r/w	r
Function	TON_DELAY			X	TOFF_DELAY			X
Default Value	0	0	0	0	0	0	0	0

TON_DELAY:

This parameter selects the delay from when the output is enabled until soft-start beings, as a multiple of the TON_RISE time. The default value is 0. Values can range from 0 to 7 in increments of 1.

TOFF_DELAY:

This parameter selects the delay from when the output is disabled until the output stops switching, as a multiple of the TON_RISE time. The default value is 0. Values can range from 0 to 7 in increments of 1.

OPTIONS (MFR_SPECIFIC_21) (E5h)

The OPTIONS register can be used for setting user selectable options, as shown below.

Command	OPTIONS															
Format	Unsigned binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X	X	X	X	X	EN_ADC_CNTL	CH2_DTC	CH1_DTC
Default Value	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	0

The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

A “1” in any of these bit positions indicates that:

EN_ADC_CNTL:

Enables ADC operation used for voltage, current and temperature monitoring.

CH2_DTC:

Increases the non-overlap dead time for gate drivers on channel 2.

CH1_DTC:

Increases the non-overlap dead time for gate drivers on channel 1.

DEVICE_CODE (MFR_SPECIFIC_44) (FCh)

The DEVICE_CODE command returns a two byte unsigned binary 12-bit device identifier code and 4-bit revision code in the following format.

Command	MFR_SPECIFIC_44															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Identifier Code												Revision Code			
Default Value	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	0

This command is oriented toward providing similar information to the DEVICE_ID command but for devices that do not support block read and write functions.

Identifier Code

Fixed at 7 (dec).

Revision Code

Fixed at 4 (dec).

REVISION HISTORY

Changes from Original (OCTOBER) to Revision A	Page
• Added Application Information section	13

Changes from Revision A (DECEMBER 2011) to Revision B	Page
• Added updated SYNC pin description in PIN DESCRIPTIONS table	9
• Added clarity to BP Crossover section	19

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS40422RHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TPS40422RHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

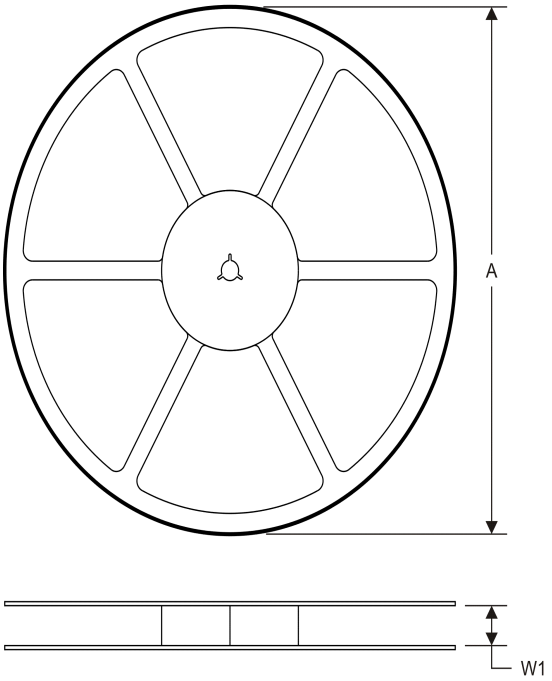
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

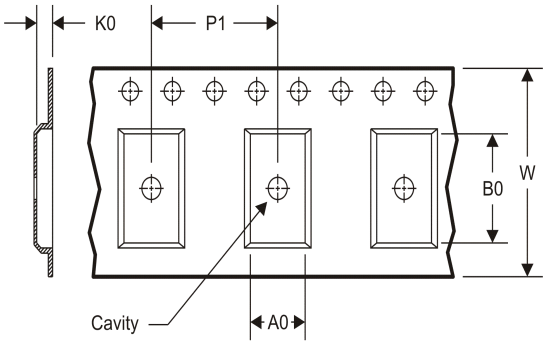
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



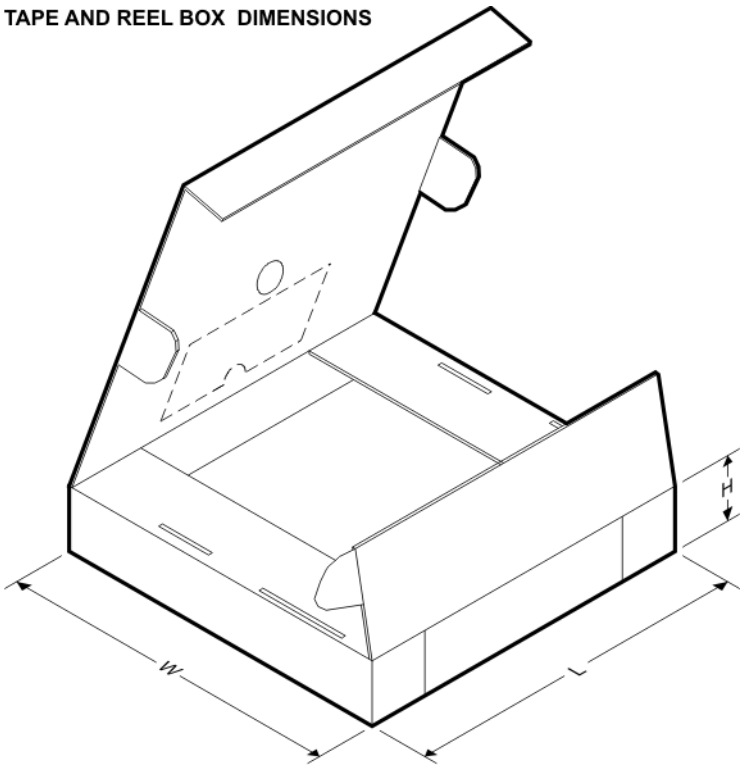
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS40422RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2
TPS40422RHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2

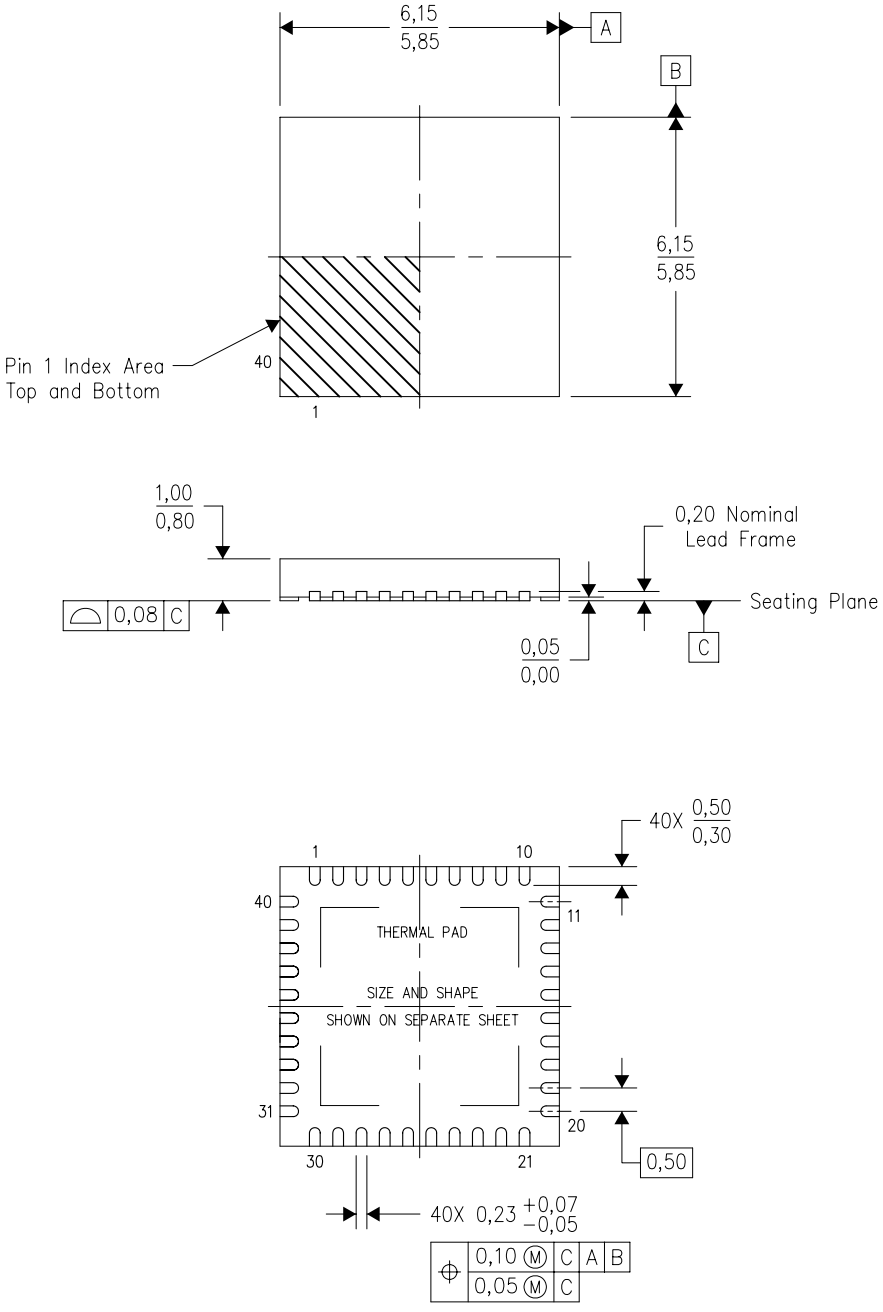
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS40422RHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
TPS40422RHAT	VQFN	RHA	40	250	210.0	185.0	35.0

RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



Bottom View

4204276/E 06/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Package complies to JEDEC MO–220 variation VJJD–2.

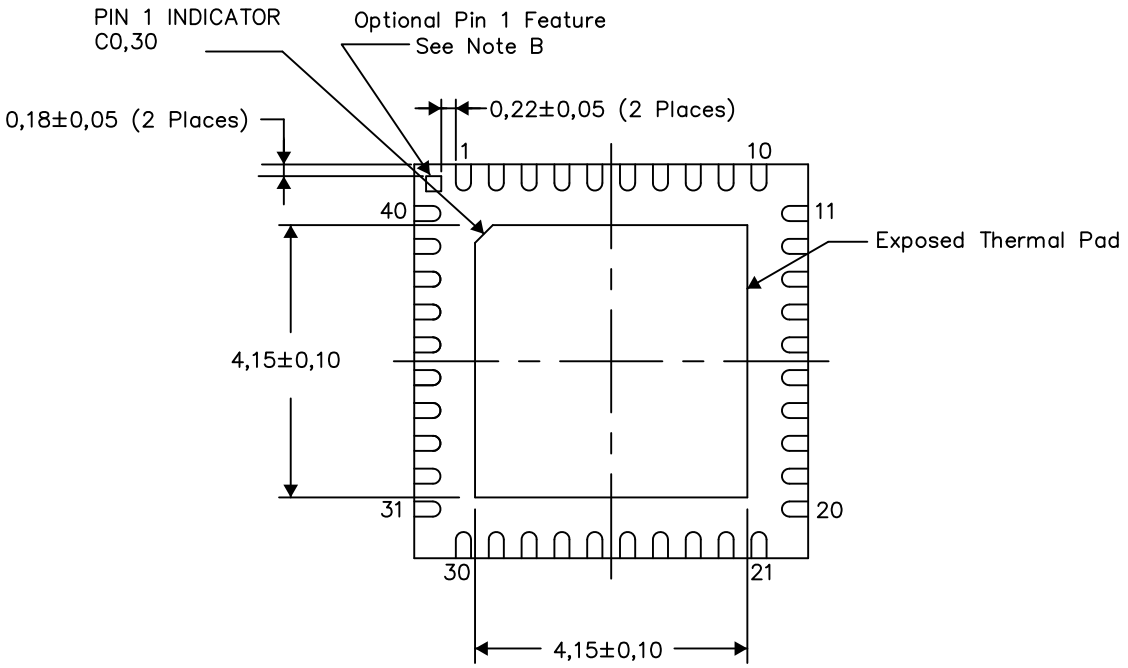
RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

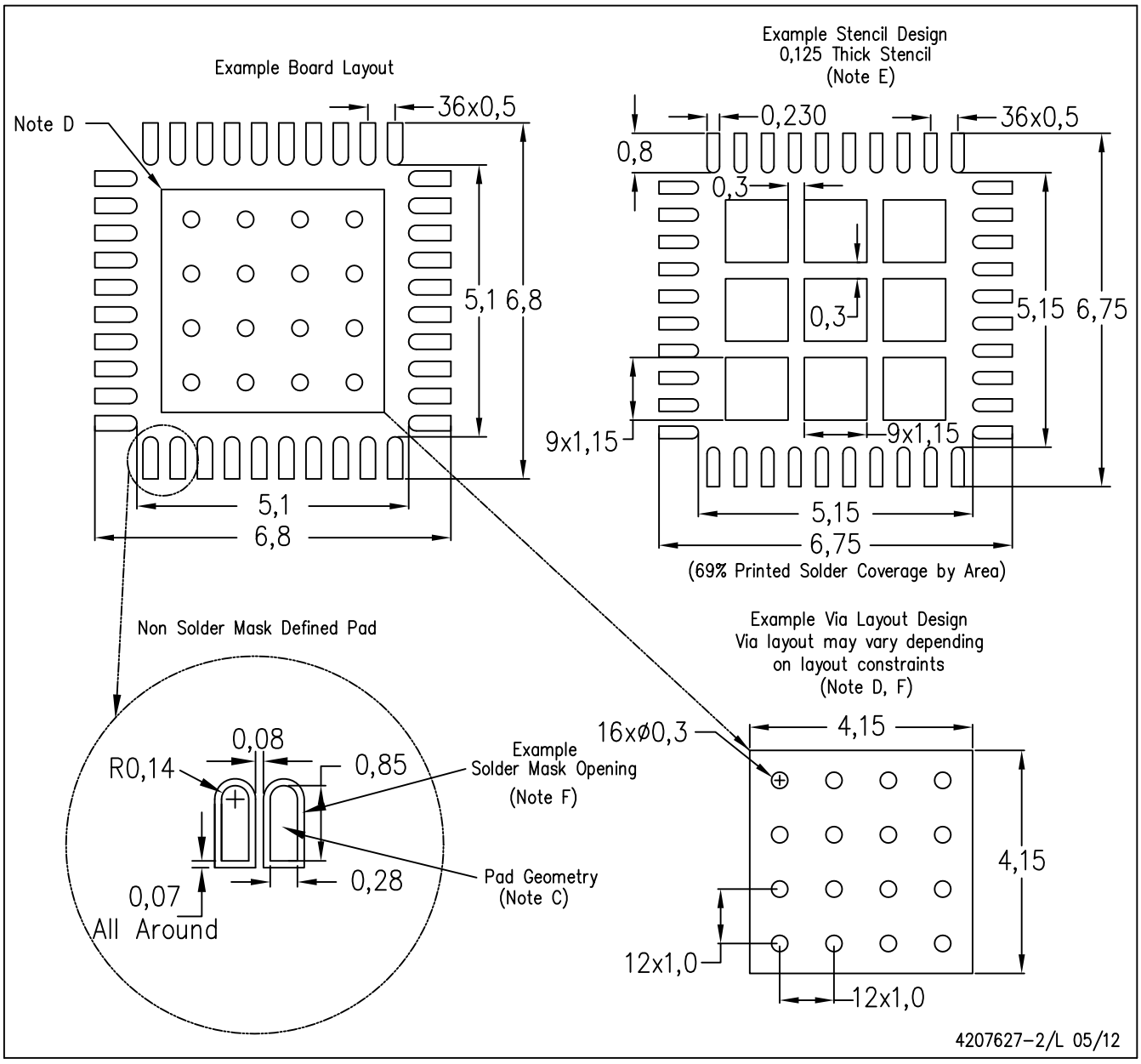
Exposed Thermal Pad Dimensions

4206355–2/Q 05/12

NOTES: A. All linear dimensions are in millimeters

B. The Pin 1 Identification mark is an optional feature that may be present on some devices In addition, this Pin 1 feature if present is electrically connected to the center thermal pad and therefore should be considered when routing the board layout.

RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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