

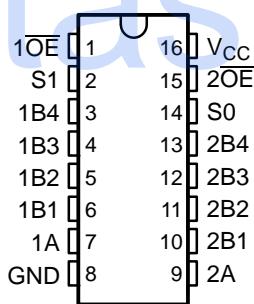
FEATURES

- High-Bandwidth Data Path (up to 500 MHz⁽¹⁾)
- 5-V Tolerant I/Os With Device Powered Up or Powered Down
- Low and Flat ON-State Resistance (r_{on}) Characteristics Over Operating Range ($r_{on} = 4 \Omega$ Typ)
- Rail-to-Rail Switching on Data I/O Ports
 - 0- to 5-V Switching With 3.3-V V_{CC}
 - 0- to 3.3-V Switching With 2.5-V V_{CC}
- Bidirectional Data Flow With Near-Zero Propagation Delay
- Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)} = 3.5 \text{ pF}$ Typ)
- Fast Switching Frequency ($f_{OE} = 20 \text{ MHz}$ Max)

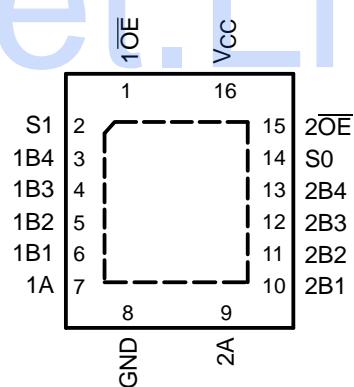
(1) For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report *CBT-C, CB3T, and CB3Q Signal-Switch Families*, literature number SCDA008.

- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption ($I_{CC} = 0.6 \text{ mA}$ Typ)
- V_{CC} Operating Range From 2.3 V to 3.6 V
- Data I/Os Support 0- to 5-V Signal Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)
- Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- Supports Both Digital and Analog Applications: USB Interface, Differential Signal Interface Bus Isolation, Low-Distortion Signal Gating

DBQ, DGV, OR PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The SN74CB3Q3253 is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3253 provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.



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DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The SN74CB3Q3253 is organized as two 1-of-4 multiplexers/demultiplexers with separate output-enable(\overline{OE} , OE) inputs. The select (S_0 , S_1) inputs control the data path of each multiplexer/demultiplexer. When \overline{OE} is low, the associated multiplexer/demultiplexer is enabled, and the A port is connected to the B port, allowing bidirectional data flow between ports. When \overline{OE} is high, the associated multiplexer/demultiplexer is disabled, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

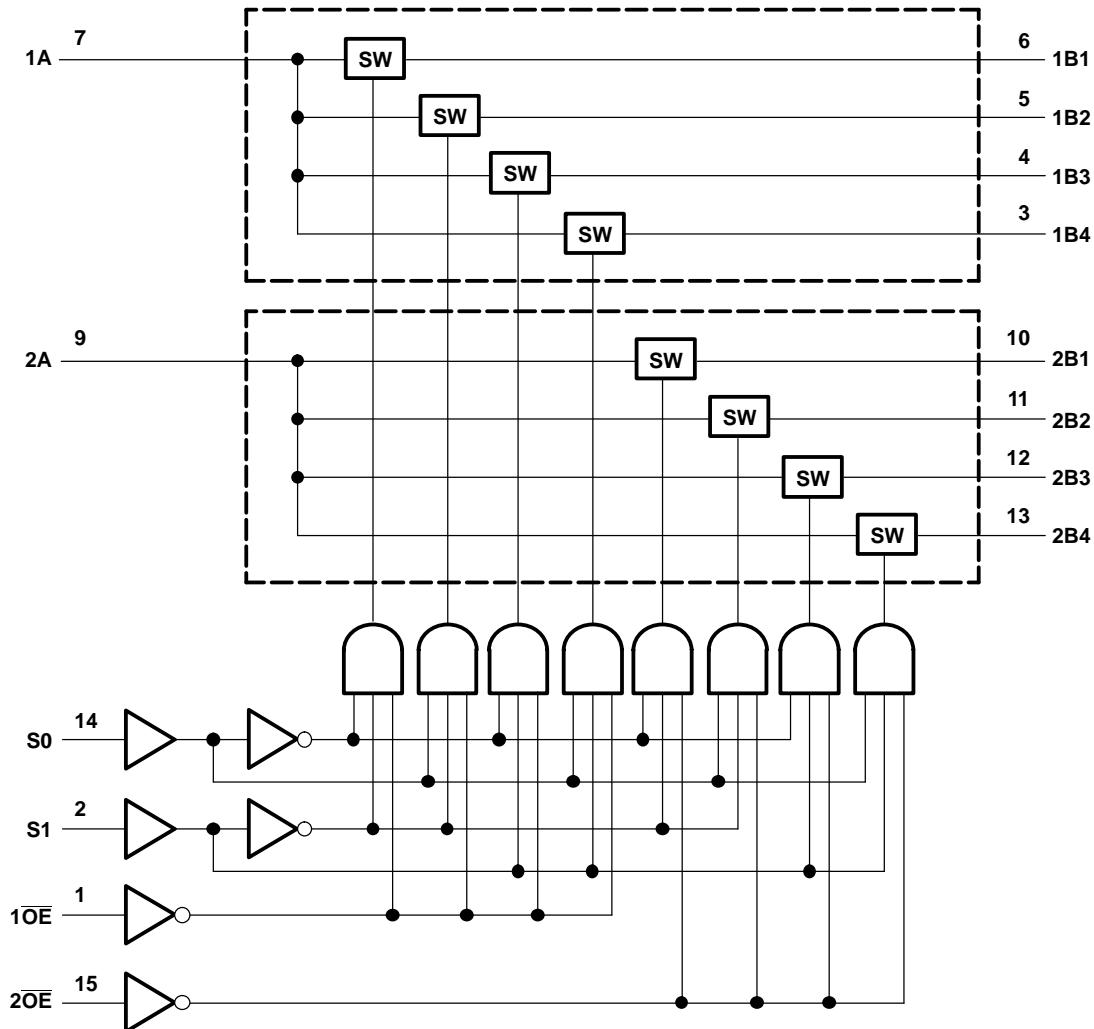
T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN – RGY	Tape and reel	SN74CB3Q3253RGYR	BU253
	SSOP (QSOP) – DBQ	Tape and reel	SN74CB3Q3253DBQR	BU253
	TSSOP – PW	Tube	SN74CB3Q3253PW	BU253
		Tape and reel	SN74CB3Q3253PWR	
	TVSOP – DGV	Tape and reel	SN74CB3Q3253DGVR	BU253

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

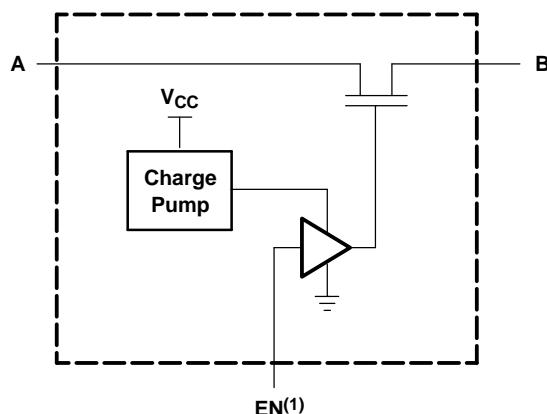
FUNCTION TABLE (EACH MULTIPLEXER/DEMULTIPLEXER)

\overline{OE}	INPUTS			INPUT/OUTPUT A	FUNCTION
	S_1	S_0			
L	L	L		B1	A port = B1 port
L	L	H		B2	A port = B2 port
L	H	L		B3	A port = B3 port
L	H	H		B4	A port = B4 port
H	X	X		Z	Disconnect

LOGIC DIAGRAM (POSITIVE LOGIC)



SIMPLIFIED SCHEMATIC, EACH FET SWITCH (SW)



(1) EN is the internal enable signal applied to the switch.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	4.6	V
V _{IN}	Control input voltage range ⁽²⁾⁽³⁾		-0.5	7	V
V _{I/O}	Switch I/O voltage range ⁽²⁾⁽³⁾⁽⁴⁾		-0.5	7	V
I _{IK}	Control input clamp current	V _{IN} < 0		-50	mA
I _{I/OK}	I/O port clamp current	V _{I/O} < 0		-50	mA
I _{I/O}	ON-state switch current ⁽⁵⁾			±64	mA
	Continuous current through V _{CC} or GND			±100	mA
θ _{JA}	Package thermal impedance	DBQ package ⁽⁶⁾		90	°C/W
		DGV package ⁽⁶⁾		120	
		PW package ⁽⁶⁾		108	
		RGY package ⁽⁷⁾		39	
T _{stg}	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) V_I and V_O are used to denote specific conditions for V_{I/O}.
- (5) I_I and I_O are used to denote specific conditions for I_{I/O}.
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.
- (7) The package thermal impedance is calculated in accordance with JESD 51-5.

Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2.3	3.6	V
V _{IH}	High-level control input voltage	V _{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V _{CC} = 2.7 V to 3.6 V	2	5.5	
V _{IL}	Low-level control input voltage	V _{CC} = 2.3 V to 2.7 V	0	0.7	V
		V _{CC} = 2.7 V to 3.6 V	0	0.8	
V _{I/O}	Data input/output voltage		0	5.5	V
T _A	Operating free-air temperature		-40	85	°C

- (1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics⁽¹⁾

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP ⁽²⁾	MAX	UNIT
V _{IK}		V _{CC} = 3.6 V, I _I = -18 mA				-1.8		V
I _{IN}	Control inputs	V _{CC} = 3.6 V, V _{IN} = 0 to 5.5 V				±1		µA
I _{OZ} ⁽³⁾		V _{CC} = 3.6 V, V _O = 0 to 5.5 V, V _I = 0, V _{IN} = V _{CC} or GND				±1		µA
I _{off}		V _{CC} = 0, V _O = 0 to 5.5 V, V _I = 0				1		µA
I _{CC}		V _{CC} = 3.6 V, I _{I/O} = 0, Switch ON or OFF, V _{IN} = V _{CC} or GND			0.6	2		mA
ΔI _{CC} ⁽⁴⁾	Control inputs	V _{CC} = 3.6 V, One input at 3 V, Other inputs at V _{CC} or GND				30		µA
I _{CCD} ⁽⁵⁾	Per control input	V _{CC} = 3.6 V, A and B ports open, Control input switching at 50% duty cycle			0.15	0.16		mA/ MHz
		S input			0.04	0.05		
C _{in}	Control inputs	V _{CC} = 3.3 V, V _{IN} = 5.5 V, 3.3 V, or 0			2.5	3.5		pF
C _{io(OFF)}	A port	V _{CC} = 3.3 V, Switch OFF, V _{IN} = V _{CC} or GND, V _{I/O} = 5.5 V, 3.3 V, or 0			8	11		pF
	B port	V _{CC} = 3.3 V, Switch OFF, V _{IN} = V _{CC} or GND, V _{I/O} = 5.5 V, 3.3 V, or 0			3.5	4.5		pF
C _{io(ON)}		V _{CC} = 3.3 V, Switch ON, V _{IN} = V _{CC} or GND, V _{I/O} = 5.5 V, 3.3 V, or 0			13	17		pF
r _{on} ⁽⁶⁾	V _{CC} = 2.3 V, TYP at V _{CC} = 2.5 V	V _I = 0,	I _O = 30 mA			4	10	Ω
		V _I = 1.7 V,	I _O = -15 mA			4.5	11	
	V _{CC} = 3 V	V _I = 0,	I _O = 30 mA			3.5	8	
		V _I = 2.4 V,	I _O = -15 mA			4	10	

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

(2) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

(5) This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 2).

(6) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

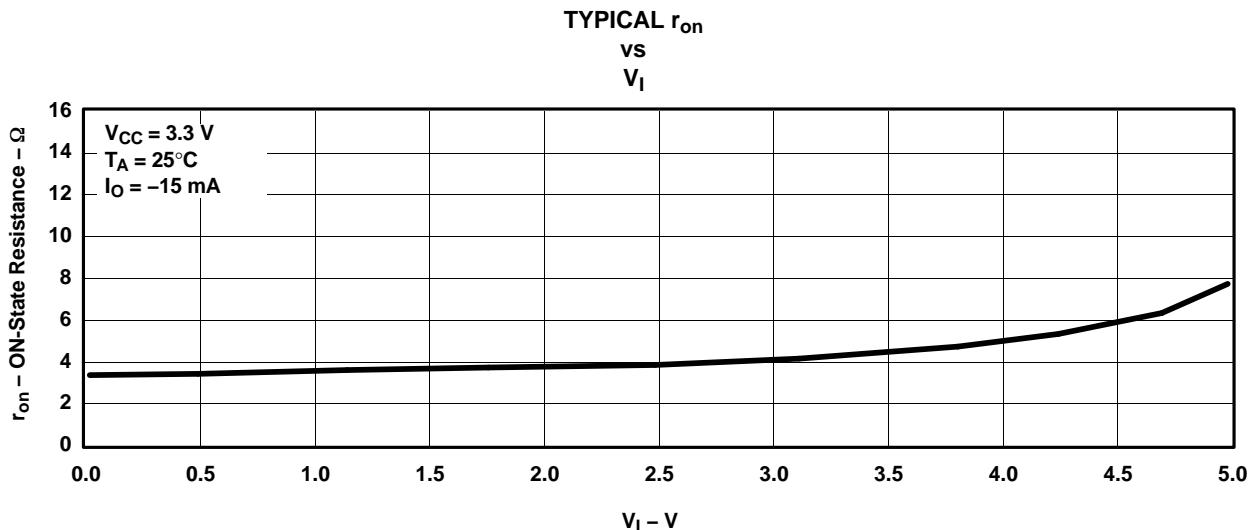
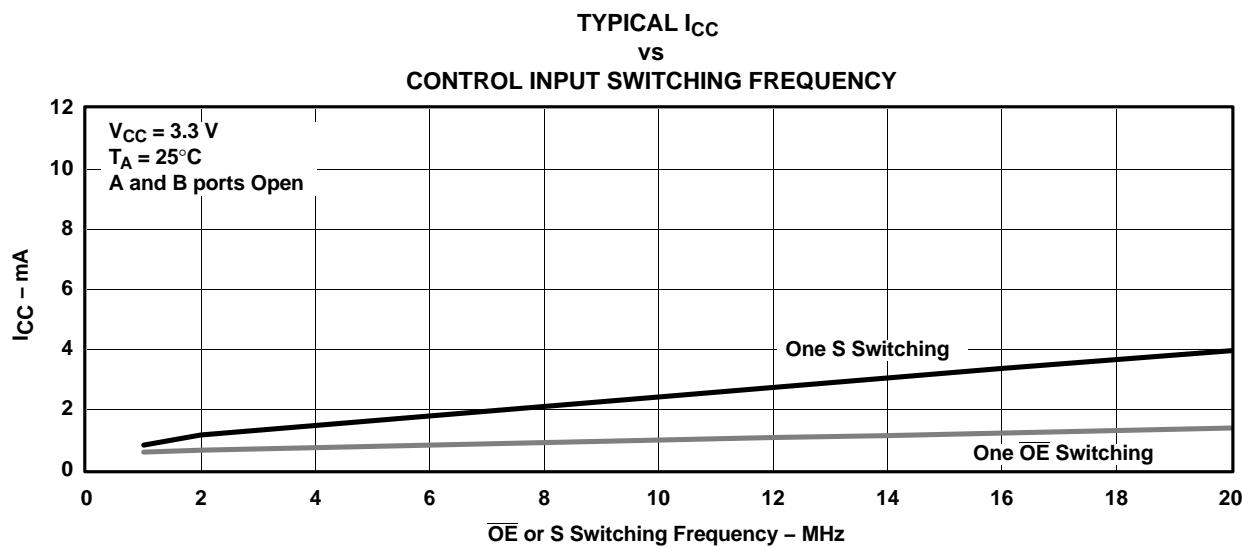
Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

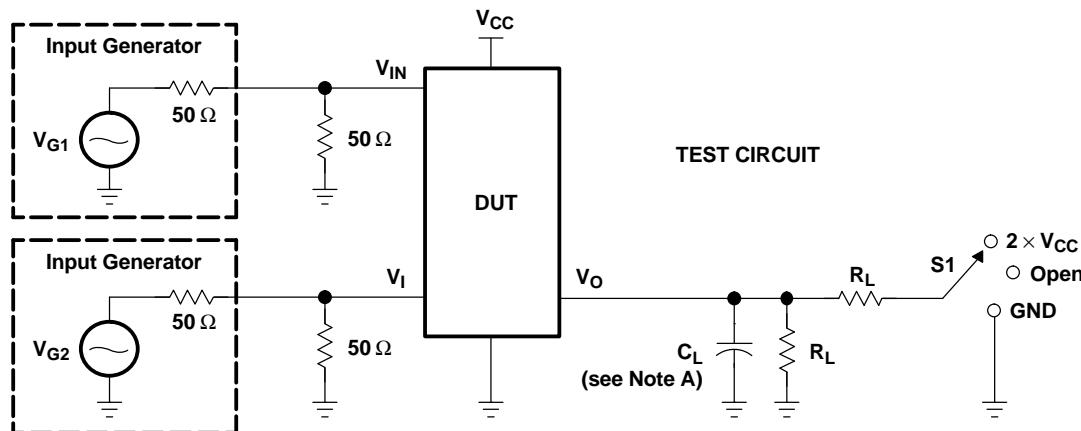
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
f _{OE} or f _S ⁽¹⁾	OE or S	A or B	10		20		MHz
t _{pd} ⁽²⁾	A or B	B or A	0.12		0.18		ns
t _{pd(s)}	S	A	1.5	6.7	1.5	5.9	ns
t _{en}	S	B	1.5	6.7	1.5	5.9	ns
	OE	A or B	1.5	6.7	1.5	5.9	
t _{dis}	S	B	1	6.1	1	6.1	ns
	OE	A or B	1	6.1	1	6.1	

(1) Maximum switching frequency for control input (V_O > V_{CC}, V_I = 5 V, R_L ≥ 1 MΩ, C_L = 0).

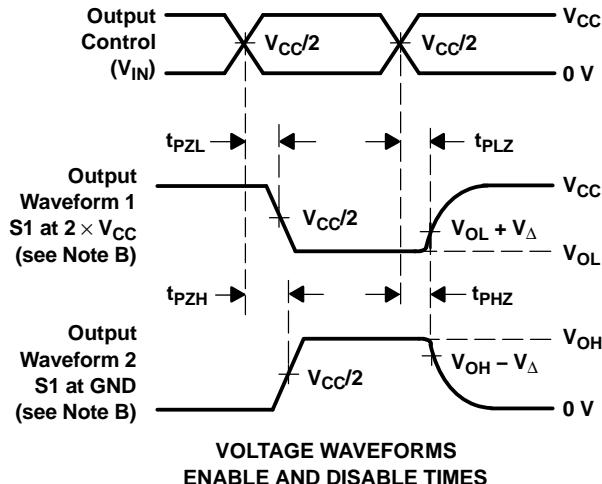
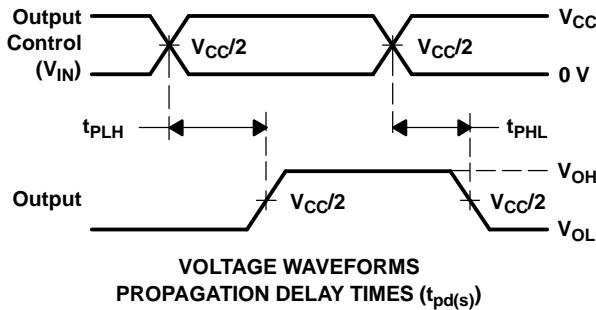
(2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

Figure 1. Typical r_{on} vs V_I , $V_{CC} = 3.3$ V and $I_O = -15$ mAFigure 2. Typical I_{CC} vs \overline{OE} or S Switching Frequency, $V_{CC} = 3.3$ V

PARAMETER MEASUREMENT INFORMATION



TEST	V _{CC}	S1	R _L	V _I	C _L	V _Δ
t _{pd(s)}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	V _{CC} or GND V _{CC} or GND	30 pF 50 pF	
t _{PZL} /t _{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V _{CC} 2 × V _{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t _{PHZ} /t _{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	GND GND	500 Ω 500 Ω	V _{CC} V _{CC}	30 pF 50 pF	0.15 V 0.3 V



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
 - F. t_{PZL} and t_{PZH} are the same as t_{en}.
 - G. t_{PLH} and t_{PHL} are the same as t_{pd(s)}. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
 - H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74CB3Q3253DBQRE4	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
74CB3Q3253DBQRG4	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CB3Q3253DGVR4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3Q3253DBQR	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74CB3Q3253DGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3Q3253PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3Q3253PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3Q3253PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3Q3253PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3Q3253PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3Q3253RGYR	ACTIVE	QFN	RGY	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

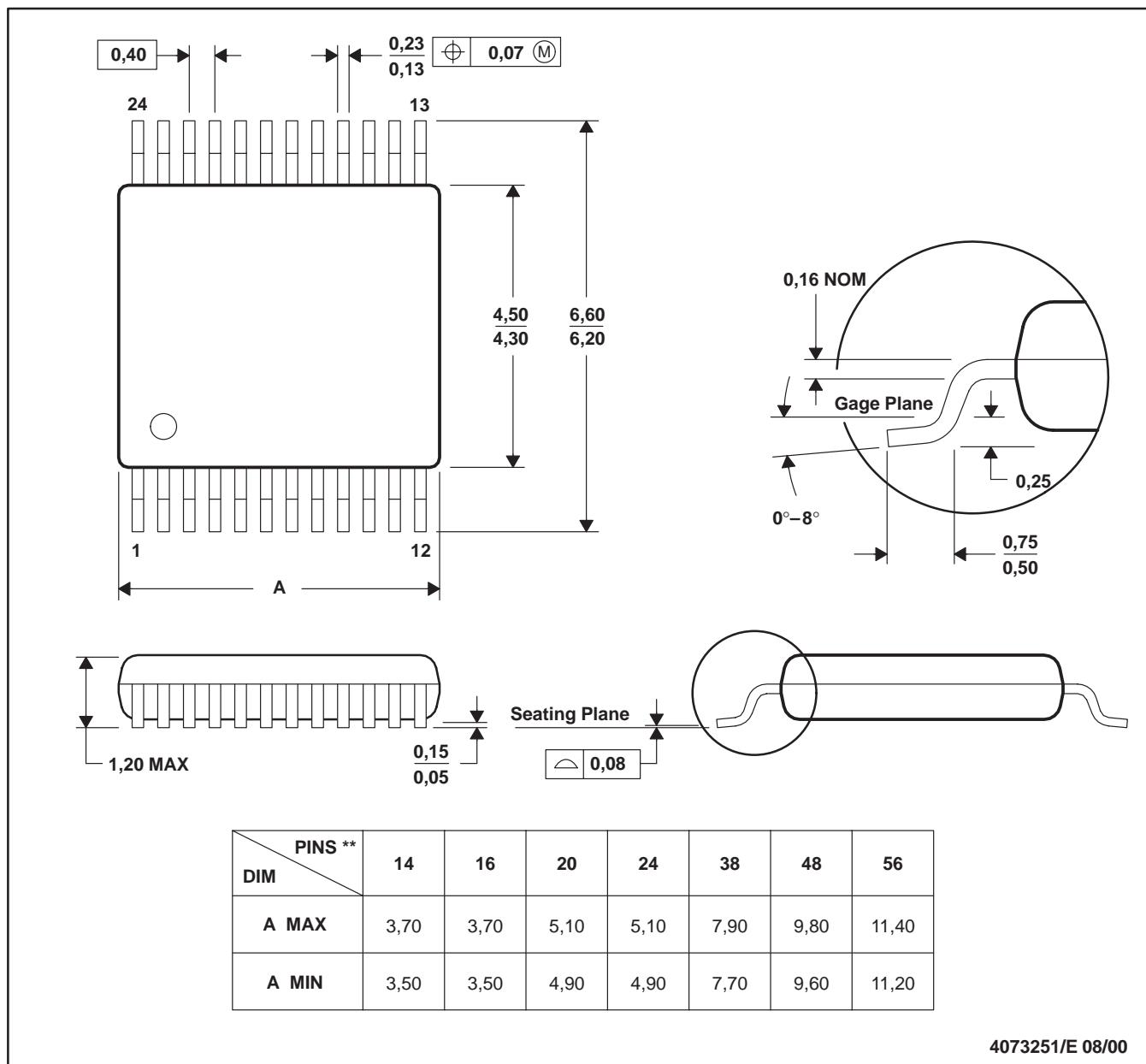
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DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

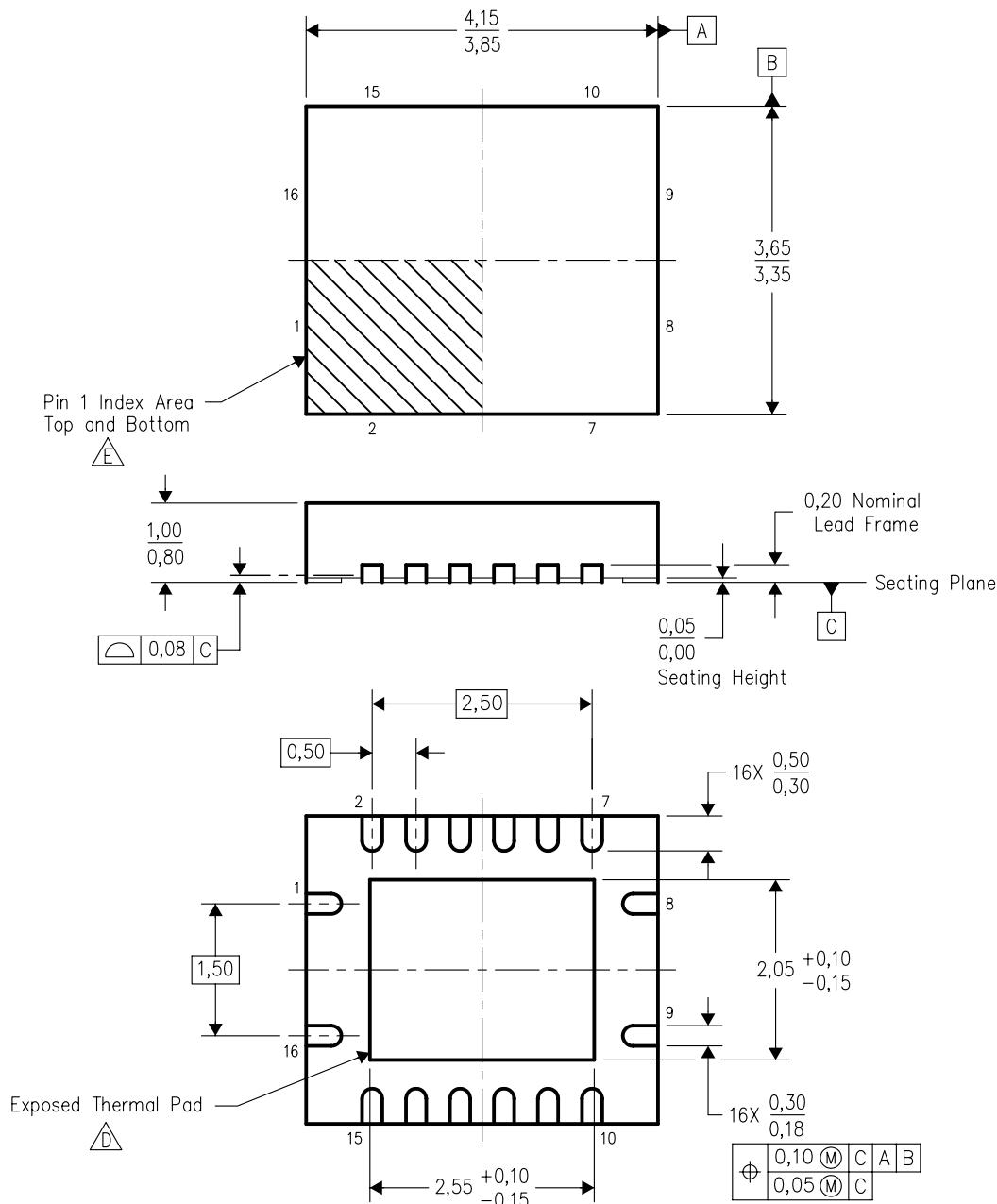


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 - D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

MECHANICAL DATA

RGY (R-PQFP-N16)

PLASTIC QUAD FLATPACK



Bottom View

4203539-3/G 04/2005

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. QFN (Quad Flatpack No-Lead) package configuration.

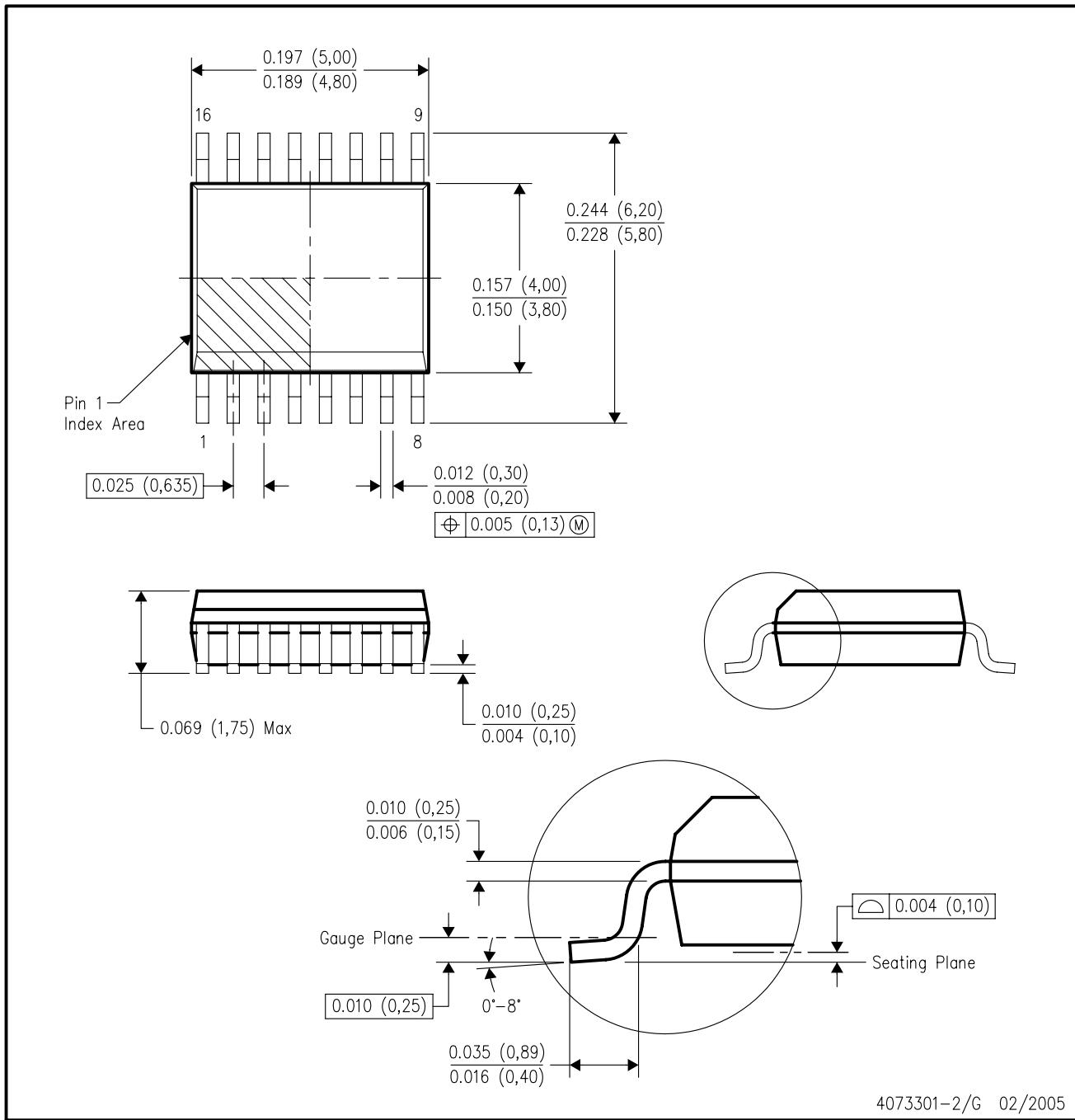
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.

E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

F. Package complies to JEDEC MO-241 variation BB.

DBQ (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE

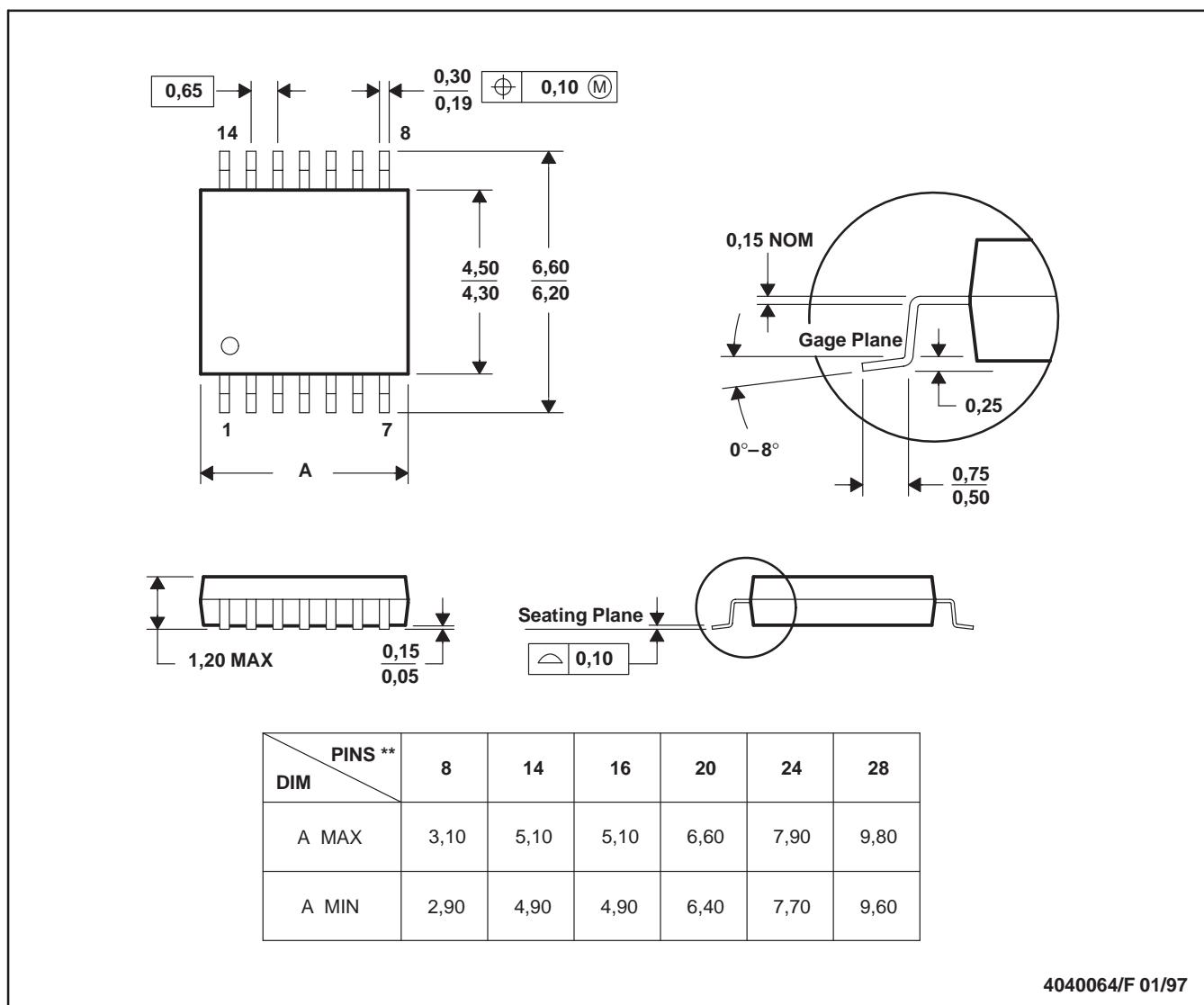


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
 - Falls within JEDEC MO-137 variation AB.

PW (R-PDSO-G^{**})

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - Falls within JEDEC MO-153

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

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SN74CB3Q3253, Status: ACTIVE

Dual 1-of-4 FET Multiplexer/Demultiplexer 2.5-V/3.3-V Low-Voltage High-Bandwidth Bus Switch

 View ROHS Compliant Devices

View RoHS Compliant Devices

 clear gif Features Quality & Pb-Free Data Related Products Tools & Software Samples Pricing/Packaging Inventory Symbols/Footprints Technical Documents Applications Notes Simulation Models Reference Designs

Refine Your Selection

- Logic: Digital Bus Exchange/Multiplexing

Support

- KnowledgeBase
- Contact Technical Support
- TI Cross Reference
- Training
- Part Marking Lookup
- Part Number Nomenclature

Datasheet

 Download Datasheet

SN74CB3Q3253 (Rev. A) (sn74cb3q3253.pdf, 309 KB)

20 Nov 2003 [Download](#)

SN74CB3Q3253

Voltage Nodes(V)	2.5, 3.3
Vcc range(V)	2.3 to 3.6
r_{on(max)}(ohms)	11
t_{pd max(ns)}	0.18
	Samples
	Inventory

Product Information

 Features Save this to your personal libraryHigh-Bandwidth Data Path (Up To 500 MHz[†])

5-V Tolerant I/Os with Device Powered-Up or Powered-Down

Low and Flat ON-State Resistance (r_{on}) Characteristics Over Operating Range ($r_{on} = 4$ Typical)

Rail-to-Rail Switching on Data I/O Ports

- 0- to 5-V Switching With 3.3-V V_{CC}
- 0- to 3.3-V Switching With 2.5-V V_{CC}

Bidirectional Data Flow, With Near-Zero Propagation Delay

Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)} = 3.5 \text{ pF}$ Typical)Fast Switching Frequency ($f_{OE} = 20 \text{ MHz}$ Max)

Data and Control Inputs Provide Undershoot Clamp Diodes

Low Power Consumption ($I_{CC} = 0.6 \text{ mA}$ Typical) V_{CC} Operating Range From 2.3 V to 3.6 V

Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)

Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs

 I_{off} Supports Partial-Power-Down Mode Operation

Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

ESD Performance Tested Per JESD 22

- 2000-V Human-Body Model (A114-B, Class II)
- 1000-V Charged-Device Model (C101)

Supports Both Digital and Analog Applications: USB Interface, Differential Signal Interface Bus

Isolation, Low-Distortion Signal Gating



For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, CBT-C, CB3T, and CB3Q Signal-Switch Families, literature number SCDA008.

Description

The SN74CB3Q3253 is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading

and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3253 provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

The SN74CB3Q3253 is organized as two 1-of-4 multiplexers/demultiplexers with separate output-enable ($OE\backslash$, $2OE\backslash$) inputs. The select (S_0 , S_1) inputs control the data path of each multiplexer/demultiplexer. When $OE\backslash$ is low, the associated multiplexer/demultiplexer is enabled, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $OE\backslash$ is high, the associated multiplexer/demultiplexer is disabled, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $OE\backslash$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Pricing/Packaging/CAD Design Tools/Samples

			Price	Packaging				CAD Design Tools		Samples
Device	Status	Temp (°C)	Budget Price (\$US) QTY	Industry Standard (TI Pkg) Pins	Top Side Marking	Standard Pack Quantity	Symbols	Footprints	Samples	
74CB3Q3253DBQRE4	ACTIVE	-40 to 85	0.62 1KU	SSOP/QSOP (DBQ) 16	View	2500	<input type="checkbox"/>	<input type="checkbox"/>	Request Free Samples	
74CB3Q3253DBQRG4	ACTIVE	-40 to 85	0.68 1KU	SSOP/QSOP (DBQ) 16	View	2500	<input type="checkbox"/>	<input type="checkbox"/>	Purchase Samples	
74CB3Q3253DGVRE4	ACTIVE	-40 to 85	0.84 1KU	TVSOP (DGV) 16		2000	<input type="checkbox"/>	<input type="checkbox"/>	Request Free Samples	
SN74CB3Q3253DBQR	ACTIVE	-40 to 85	0.62 1KU	SSOP/QSOP (DBQ) 16	View	2500	<input type="checkbox"/>	<input type="checkbox"/>	Request Free Samples	
SN74CB3Q3253DGVR	ACTIVE	-40 to 85	0.84 1KU	TVSOP (DGV) 16		2000	<input type="checkbox"/>	<input type="checkbox"/>	Request Free Samples	
SN74CB3Q3253PW	ACTIVE	-40 to 85	0.62 1KU	TSSOP (PW) 16	View	90	<input type="checkbox"/>	<input type="checkbox"/>	Purchase Samples	
SN74CB3Q3253PWE4	ACTIVE	-40 to 85	0.62 1KU	TSSOP (PW) 16	View	90	<input type="checkbox"/>	<input type="checkbox"/>	Purchase Samples	
SN74CB3Q3253PWR	ACTIVE	-40 to 85	0.62 1KU	TSSOP (PW) 16	View	2000	<input type="checkbox"/>	<input type="checkbox"/>	Request Free Samples	
SN74CB3Q3253PWRE4	ACTIVE	-40 to 85	0.62 1KU	TSSOP (PW) 16	View	2000	<input type="checkbox"/>	<input type="checkbox"/>	Request Free Samples	
SN74CB3Q3253PWRG4	ACTIVE	-40 to 85	0.68 1KU	TSSOP (PW) 16	View	2000	<input type="checkbox"/>	<input type="checkbox"/>	Purchase Samples	
SN74CB3Q3253RGYR	ACTIVE	-40 to 85	0.84 1KU	QFN (RGY) 16		1000	<input type="checkbox"/>	<input type="checkbox"/>	Request Free Samples	

Inventory

			TI Inventory Status		Reported Distributor Inventory							
			As of 9:09 AM GMT, 25 Nov 2005		As of 9:09 AM GMT, 25 Nov 2005				View all Distributors			
			In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase	Choose a Region		
74CB3Q3253DBQRE4			0*	>10k 27 Feb	14 Weeks	None Reported	View Distributors					
74CB3Q3253DBQRG4			As of 9:09 AM GMT, 25 Nov 2005		As of 9:09 AM GMT, 25 Nov 2005							
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase					
	0*	>10k 3 Feb	10 Weeks	None Reported	View Distributors							
74CB3Q3253DGVRE4			As of 9:09 AM GMT, 25 Nov 2005		As of 9:09 AM GMT, 25 Nov 2005							
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase					
	0*	>10k 27 Feb	14 Weeks	None Reported	View Distributors							

	0*	2944 30 Nov	8 Weeks	None Reported View Distributors			
		775 21 Dec					
		787 28 Dec					
		687 1 Feb					
		49 8 Feb					
SN74CB3Q3253DBQR	As of 9:09 AM GMT, 25 Nov 2005			As of 9:09 AM GMT, 25 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 27 Feb	14 Weeks	Americas	DigiKey	>1k	
SN74CB3Q3253DGVR	As of 9:09 AM GMT, 25 Nov 2005			As of 9:09 AM GMT, 25 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	2944 30 Nov	8 Weeks	Americas	DigiKey	>1k	
		775 21 Dec					
		787 28 Dec					
		687 1 Feb					
		49 8 Feb					
SN74CB3Q3253PW	As of 9:09 AM GMT, 25 Nov 2005			As of 9:09 AM GMT, 25 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	1*	>10k 31 Mar	16 Weeks	None Reported View Distributors			
SN74CB3Q3253PWE4	As of 9:09 AM GMT, 25 Nov 2005			As of 9:09 AM GMT, 25 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	1*	>10k 31 Mar	16 Weeks	None Reported View Distributors			
SN74CB3Q3253PWR	As of 9:09 AM GMT, 25 Nov 2005			As of 9:09 AM GMT, 25 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*		16 Weeks	Americas	DigiKey	585	
SN74CB3Q3253PWRE4	As of 9:09 AM GMT, 25 Nov 2005			As of 9:09 AM GMT, 25 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*		16 Weeks	None Reported View Distributors			
SN74CB3Q3253PWRG4	As of 9:09 AM GMT, 25 Nov 2005			As of 9:09 AM GMT, 25 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*		16 Weeks	None Reported View Distributors			
SN74CB3Q3253RGYR	As of 9:09 AM GMT, 25 Nov 2005			As of 9:09 AM GMT, 25 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	8000*	>10k 9 Jan	8 Weeks	Americas	DigiKey	451	

* Our information is updated daily, so please check back with us soon if this does not meet your needs. You may also contact your [TI Authorized Distributor](#), including those [listed above](#), for real time stock information.

** Lead time information is not available at this time. However, our information is updated daily so please check back with us soon. Please contact your preferred [TI Authorized Distributor](#) for additional information.

Quality & Lead (Pb)-Free Data

	Product Content					MTBF/FIT Rate
Device	Eco Plant*	Lead/Ball Finish	MSL Rating/Peak Reflow	Details	Details	
74CB3Q3253DBQRE4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR	View	View	
74CB3Q3253DBQRG4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
74CB3Q3253DGVRE4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74CB3Q3253DBQR	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR	View	View	
SN74CB3Q3253DGVR	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74CB3Q3253PW	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74CB3Q3253PWE4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74CB3Q3253PWR	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74CB3Q3253PWRE4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74CB3Q3253PWRG4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74CB3Q3253RGYR	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR	View	View	

* The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please click on the Product Content Details "View" link in the table above for the latest availability information and additional product content details.

If the information you are requesting is not available online at this time, contact one of our [Product Information Centers](#) regarding the availability of this information.

Technical Documents

Datasheets

[Keep track of what's new](#)

SN74CB3Q3253 (Rev. A) (sn74cb3q3253.pdf, 309 KB)

20 Nov 2003 [Download](#)

Application Notes

Semiconductor Packing Material Electrostatic Discharge (ESD) Protection (szza047.htm, 9 KB)

08 Jul 2004 [Abstract](#)

Shelf-Life Evaluation of Lead-Free Component Finishes (szza046.htm, 9 KB)

24 May 2004 [Abstract](#)

Understanding and Interpreting Standard-Logic Data Sheets (Rev. B) (szza036b.htm, 8 KB)

28 May 2003 [Abstract](#)

Bus FET Switch Solutions for Live Insertion Applications (scda009.htm, 9 KB)

07 Feb 2003 [Abstract](#)

CBT-C, CB3T, and CB3Q Signal-Switch Families (scda008.htm, 9 KB)

04 Feb 2003 [Abstract](#)

[View Application Notes for DIGITAL BUS EXCHANGE/MULTIPLEXING SWITCHES](#)

User Guides

Signal Switch Data Book (Rev. A) (scdd003a.pdf, 19732 KB)

14 Nov 2003 [Download](#)

LOGIC Pocket Data Book (scyd013.pdf, 4835 KB)

05 Dec 2002 [Download](#)

Simulation Models

IBIS Model

IBIS Model of SN74CB3Q3253 (scdm060.ibs, 129 KB)

02 Sep 2003 [ibis / zip](#)

More Literature

Logic Selection Guide 2005 (Rev. X) (sdyu001x.pdf, 6909 KB)

15 Mar 2005 [Download](#)

Digital Bus Switch Selection Guide (Rev. A) (scdb006a.pdf, 719 KB)

10 Nov 2004 [Download](#)

Logic Cross-Reference (Rev. A) (scyb017a.pdf, 2938 KB)

07 Oct 2003 [Download](#)

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15445 Innovation Drive
San Diego, CA 92128

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