Microelectronics
Product Note
June 1996

Lucent Technologies
Bell Labs Innovations

AV6220A MPEG-2 System-Layer Demultiplexer

Features

- Compliant with ISO/IEC 13818-1 MPEG-2 System and DVB requirements (transport stream format)
- Identifies and extracts up to 32 user-definable packet IDs (PIDs) from a transport stream (TS)
- Filters up to eight service information (SI) or program specific information (PSI) tables
- Accepts transport data from a TS interface or over the host data bus for CD-ROM applications
- Recovers a 27 MHz system clock using the program clock reference or original program clock reference from the transport stream and an external VCXO
- Generates audio bit clock rates of 512, 384, 256, 192, 128, and 64 kbits/s using an external VCXO
- Supports bit-serial or byte-parallel transport stream input and elementary stream outputs
- Operates at a maximum TS input rate of 12 Mbytes/s parallel or 54 Mbits/s serial
- Operates at a maximum video stream output rate of 27 Mbytes/s parallel or 27 Mbits/s serial
- Six selectable video and audio data output modes with separate or combined streams
- Processes dedicated transport stream header, adaptation field, and packetized elementary stream header information fields
- Provides a flexible TS frame synchronization routine
- Provides error code insertion capability
- Performs video and audio presentation time stamp and decoding time stamp processing required for video and audio synchronization
- Provides a DRAM controller for up to 1 Mbyte of external DRAM which allows host access to information contained in selected TS packets
- Maintains up to 34 separate DRAM queues: 1 audio delay, 1 video buffer, and 32 PID/SI table associated buffers
- Contains a scrambling interface for encryption/decryption and conditional access
- Supports interfacing to a variety of audio, video, and combined audio/video decoders
- Supports interfacing to a variety of microprocessor devices

Applications

The Lucent Technologies' AV6220A design offers an open and interoperable solution for the design of systems for MPEG-2 applications such as:

- Integrated receiver decoders (IRD)
  - — Cable TV
  - — Direct broadcast satellite (DBS)
  - — Video-on-demand
  - — Interactive TV
- Headend uplink facilities
- CD-ROM video entertainment solutions
- PC multimedia solutions

Description

Lucent Technologies' AV6220A MPEG-2 System-Layer Demultiplexer (MSLD) provides users with efficient, cost-effective MPEG-2 transport layer demultiplexing. This device complies with the MPEG-2 and DVB specifications and provides a comprehensive feature set. It demultiplexes TS packets into packetized elementary streams (PES), elementary streams (ES), PSI, SI, systems, and private data.

The AV6220A works seamlessly with multiple MPEG-2 video, audio, and combined video/audio decoders, as well as a variety of processors. It accepts either serial or byte wide TS inputs and may also receive TS data through the host interface for CD-ROM applications. The MSLD provides clock recovery for the system 27 MHz clock and assists in the synchronization of video and audio streams.

The AV6220A is available in a low-cost, 160-pin plastic metric quad flat pack (MQFP) and uses advanced 0.55 µm, 5.0 V, CMOS technology that provides low power consumption of less than 1 W.

Description (continued)

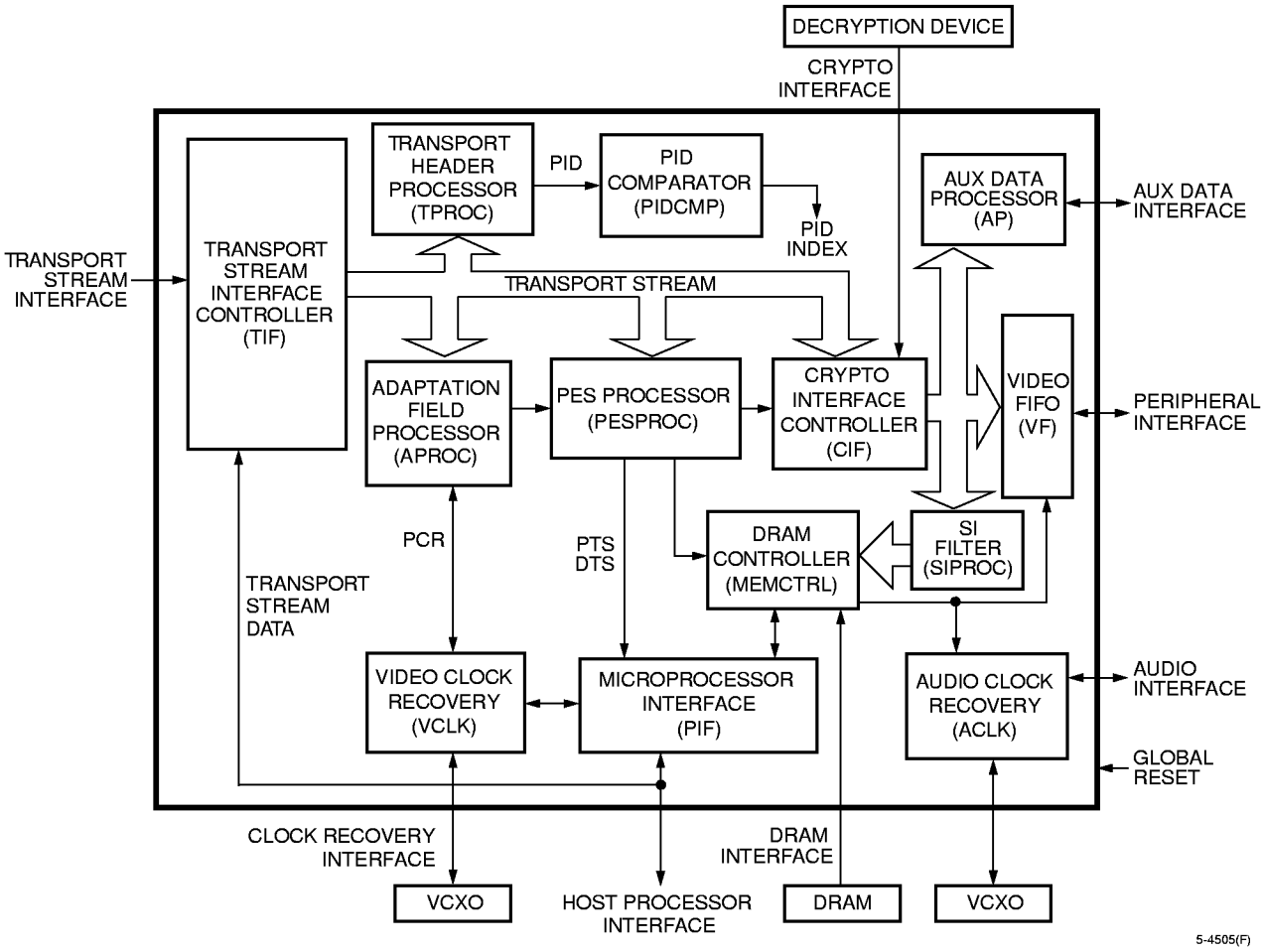

Figure 1. AV6220A MSLD Block Diagram

Description (continued)

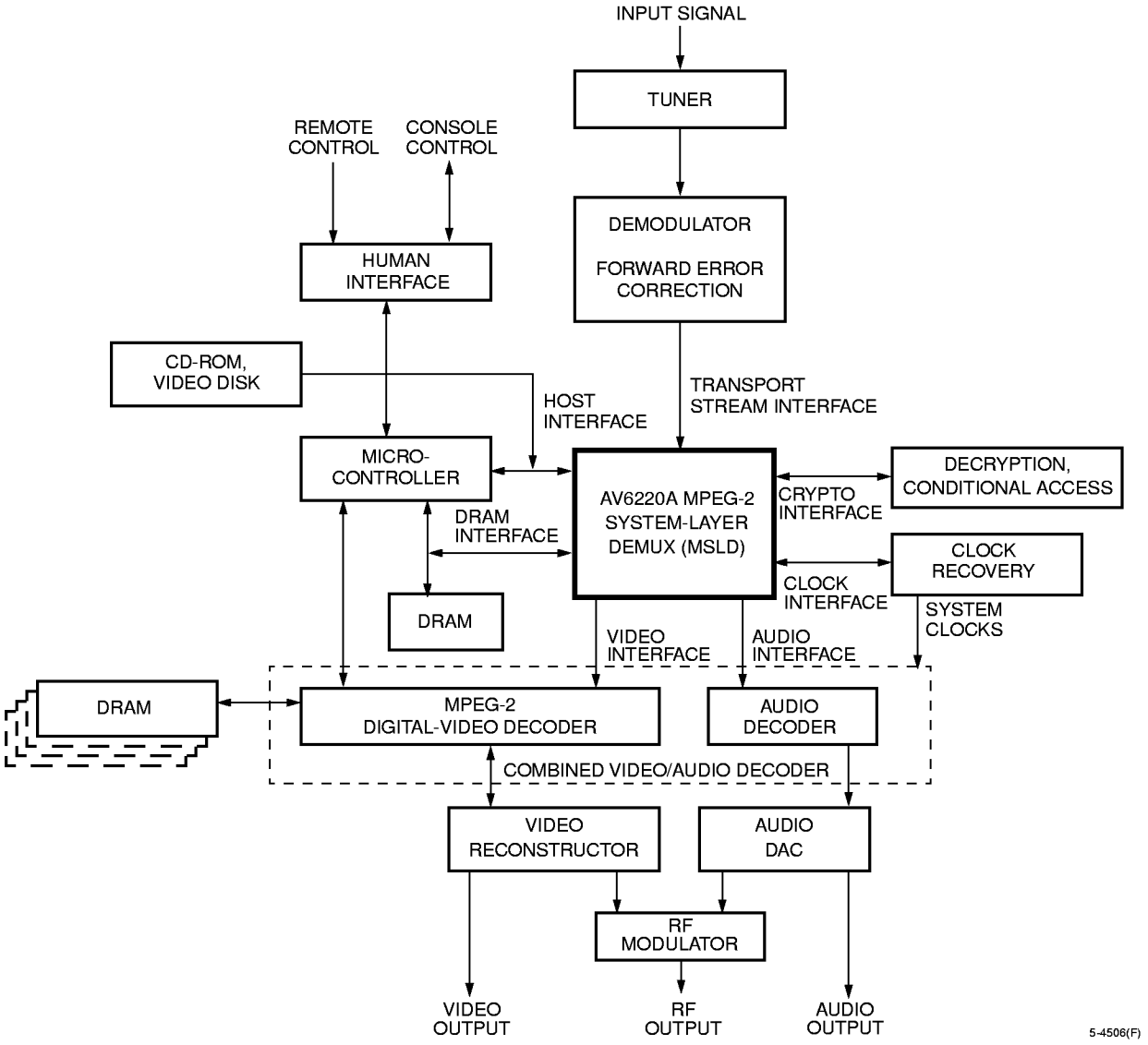

Figure 2. AV6220A MSLD Typical Set-Top Box Application Diagram

Interface Information

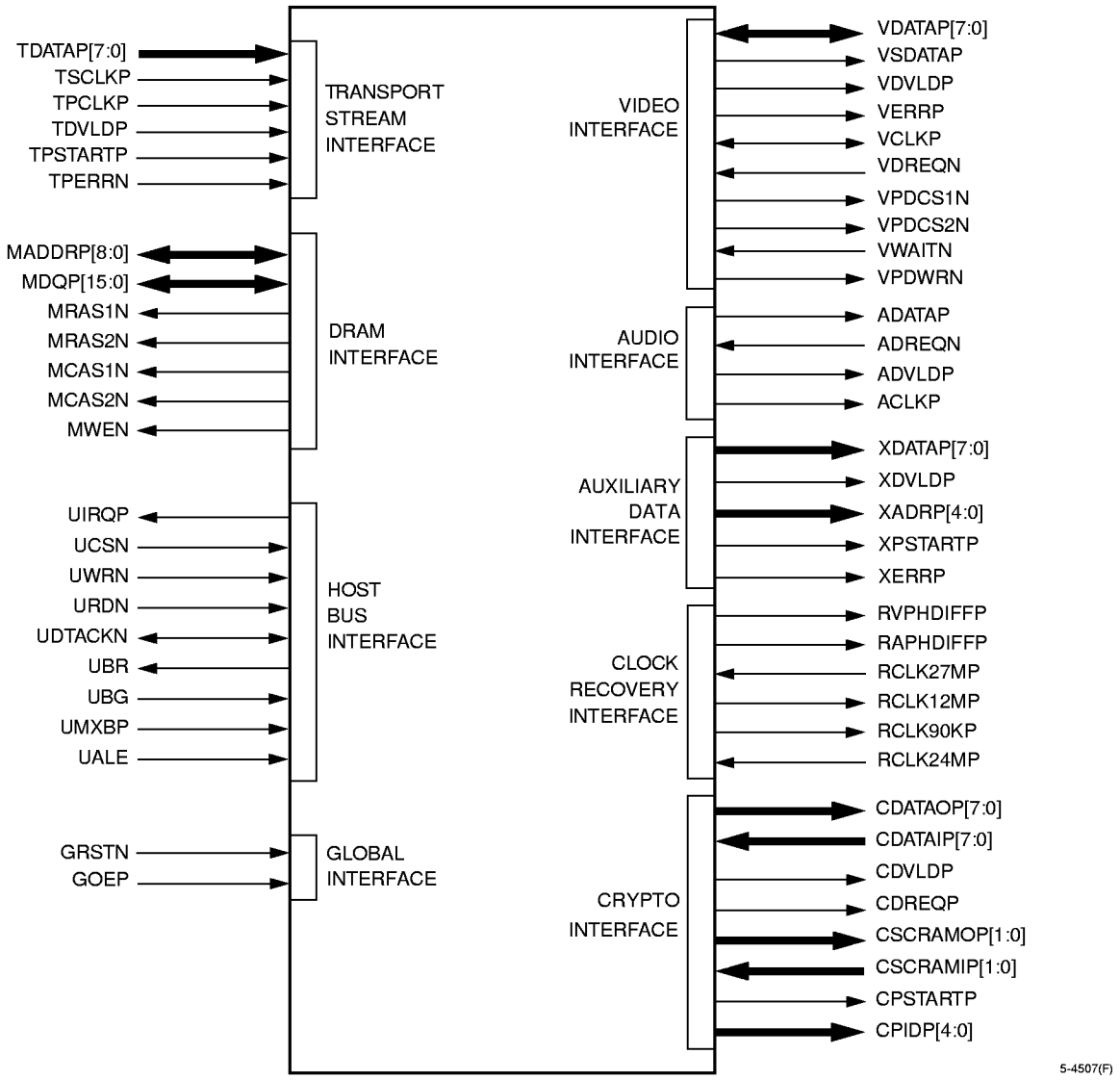

Figure 3. AV6220A MSLD Interface Diagram

Pin Information

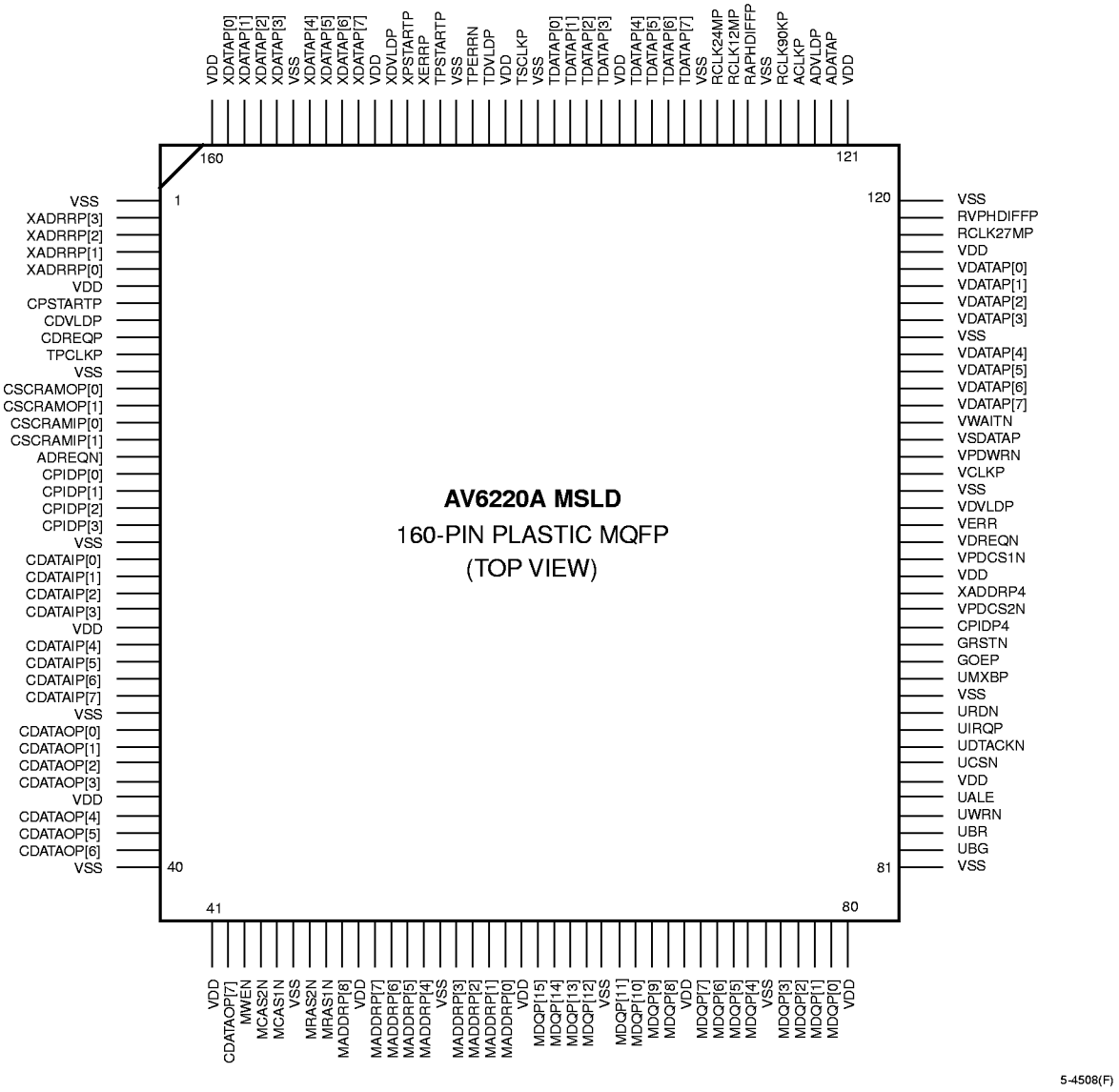

Figure 4. AV6220A MSLD Pin Diagram

Pin Information (continued)

Table 1. AV6220A Pin Descriptions

Pin	Name	I/O	Description	Pin	Name	I/O	Description
1	VSS	—	GND.	41	VDD	—	Power Supply. +5 V.
2	XADDRP[3]	O	Auxiliary Address.	42	CDATAOP[7]	O	Crypto Data Out.
3	XADDRP[2]	O	Auxiliary Address.	43	MWEN	O	DRAM Write Enable.
4	XADDRP[1]	O	Auxiliary Address.	44	MCAS2N	O	DRAM Col. Addr. Strobe 2.
5	XADDRP[0]	O	Auxiliary Address.	45	MCAS1N	O	DRAM Col. Addr. Strobe 1.
6	VDD	—	Power Supply. +5 V.	46	VSS	—	GND.
7	CPSTARTP	O	Crypto Packet Start.	47	MCAS2N	O	DRAM Col. Addr. Strobe 2.
8	CDVLDP	O	Crypto Data Valid.	48	MCAS1N	O	DRAM Col. Addr. Strobe 1.
9	CDREQP	O	Crypto Data Request.	49	MADDRP[8]	I/O	DRAM Memory Address.
10	TPCLKP	I/O	Transport Stream Parallel Clock.	50	VDD	—	Power Supply. +5 V.
11	VSS	—	GND.	51	MADDRP[7]	I/O	DRAM Memory Address.
12	CSCRAMOP[0]	O	Crypto Scrambling Bits Out.	52	MADDRP[6]	I/O	DRAM Memory Address.
13	CSCRAMOP[1]	O	Crypto Scrambling Bits Out.	53	MADDRP[5]	I/O	DRAM Memory Address.
14	CSCRAMIP[0]	I	Crypto Scrambling Bits In.	54	MADDRP[4]	I/O	DRAM Memory Address.
15	CSCRAMIP[1]	I	Crypto Scrambling Bits In.	55	VSS	—	GND.
16	ADREQN	I	Audio Data Request.	56	MADDRP[3]	I/O	DRAM Memory Address.
17	CPIDP[0]	O	Crypto PID.	57	MADDRP[2]	I/O	DRAM Memory Address.
18	CPIDP[1]	O	Crypto PID.	58	MADDRP[1]	I/O	DRAM Memory Address.
19	CPIDP[2]	O	Crypto PID.	59	MADDRP[0]	I/O	DRAM Memory Address.
20	CPIDP[3]	O	Crypto PID.	60	VDD	—	Power Supply. +5 V.
21	VSS	—	GND.	61	MDQP[15]	I/O	DRAM Data.
22	CDATAIP[0]	I	Crypto Data In.	62	MDQP[14]	I/O	DRAM Data.
23	CDATAIP[1]	I	Crypto Data In.	63	MDQP[13]	I/O	DRAM Data.
24	CDATAIP[2]	I	Crypto Data In.	64	MDQP[12]	I/O	DRAM Data.
25	CDATAIP[3]	I	Crypto Data In.	65	VSS	—	GND.
26	VDD	—	Power Supply. +5 V.	66	MDQP[11]	I/O	DRAM Data.
27	CDATAIP[4]	I	Crypto Data In.	67	MDQP[10]	I/O	DRAM Data.
28	CDATAIP[5]	I	Crypto Data In.	68	MDQP[9]	I/O	DRAM Data.
29	CDATAIP[6]	I	Crypto Data In.	69	MDQP[8]	I/O	DRAM Data.
30	CDATAIP[7]	I	Crypto Data In.	70	VDD	—	Power Supply. +5 V.
31	VSS	—	GND.	71	MDQP[7]	I/O	DRAM Data.
32	CDATAOP[0]	O	Crypto Data Out.	72	MDQP[6]	I/O	DRAM Data.
33	CDATAOP[1]	O	Crypto Data Out.	73	MDQP[5]	I/O	DRAM Data.
34	CDATAOP[2]	O	Crypto Data Out.	74	MDQP[4]	I/O	DRAM Data.
35	CDATAOP[3]	O	Crypto Data Out.	75	VSS	—	GND.
36	VDD	—	Power Supply. +5 V.	76	MDQP[3]	I/O	DRAM Data.
37	CDATAOP[4]	O	Crypto Data Out.	77	MDQP[2]	I/O	DRAM Data.
38	CDATAOP[5]	O	Crypto Data Out.	78	MDQP[1]	I/O	DRAM Data.
39	CDATAOP[6]	O	Crypto Data Out.	79	MDQP[0]	I/O	DRAM Data.
40	VSS	—	GND.	80	VDD	—	Power Supply. +5 V.

Pin Information (continued)

Table 1. AV6220A Pin Descriptions (continued)

Pin	Name	I/O	Description	Pin	Name	I/O	Description
81	VSS	—	GND.	121	VDD	—	Power Supply. +5 V.
82	UBG	I	µP Bus Grant.	122	ADATAP	O	Audio Data.
83	UBR	O	µP Bus Request.	123	ADVLDP	O	Audio Data Valid.
84	UWRN	I	µP Write Enable.	124	ACLKP	O	Audio Clock.
85	UALE	I	µP Address Latch Enable.	125	RCLK90KP	O	90 kHz Clock.
86	VDD	—	Power Supply. +5 V.	126	VSS	—	GND.
87	UCSN	I	µP Chip Select.	127	RAPHDIFFP	O	Audio Clock Phase Diff.
88	UDTACKN	O	µP Data Acknowledge.	128	RCLK12MP	O	12.288 MHz Clock.
89	UIRQP	O	µP Interrupt.	129	RCLK24MP	I	24.576 MHz Clock.
90	URDN	I	µP Read Enable.	130	VSS	—	GND.
91	VSS	—	GND.	131	TDATAP[7]	I	Transport Stream Data.
92	UMXBP	I	µP Multiplex Enable.	132	TDATAP[6]	I	Transport Stream Data.
93	GOEP	I	Global Output Enable.	133	TDATAP[5]	I	Transport Stream Data.
94	GRSTN	I	Global Reset.	134	TDATAP[4]	I	Transport Stream Data.
95	CPIDP4	O	Crypto PID Bit 4.	135	VDD	—	Power Supply. +5 V.
96	VPDCS2N	O	Peripheral Device Chip Select 2.	136	TDATAP[3]	I	Transport Stream Data.
97	XADDRP4	O	Auxiliary Address Bit 4.	137	TDATAP[2]	I	Transport Stream Data.
98	VDD	—	Power Supply. +5 V.	138	TDATAP[1]	I	Transport Stream Data.
99	VPDCS1N	O	Peripheral Device Chip Select 1.	139	TDATAP[0]	I	Transport Stream Data.
100	VDREQN	I	Video Data Request.	140	VSS	—	GND.
101	VERR	O	Video Data Error.	141	TSCLKP	I	Transport Stream Serial Clock.
102	VDVLDP	O	Video Data Valid.	142	VDD	—	Power Supply. +5 V.
103	VSS	—	GND.	143	TDVLDP	I	Transport Stream Data Valid.
104	VCLKP	I/O	Video Clock.	144	TPERRN	I	Transport Stream Packet Error.
105	VPDWRN	O	Video Proc. Data Write.	145	VSS	—	GND.
106	VSDATAP	O	Serial Video Data.	146	TPSTARTP	I	Transport Stream Packet Start.
107	VWAITN	I	Video Decoder Wait.	147	XERRP	O	Auxiliary Error.
108	VDATAP[7]	I/O	Video Data.	148	XPSTARTP	O	Auxiliary Packet Start.
109	VDATAP[6]	I/O	Video Data.	149	XDVLDP	O	Auxiliary Data Valid.
110	VDATAP[5]	I/O	Video Data.	150	VDD	—	Power Supply. +5 V.
111	VDATAP[4]	I/O	Video Data.	151	XDATAP[7]	O	Auxiliary Data.
112	VSS	—	GND.	152	XDATAP[6]	O	Auxiliary Data.
113	VDATAP[3]	I/O	Video Data.	153	XDATAP[5]	O	Auxiliary Data.
114	VDATAP[2]	I/O	Video Data.	154	XDATAP[4]	O	Auxiliary Data.
115	VDATAP[1]	I/O	Video Data.	155	VSS	—	GND.
116	VDATAP[0]	I/O	Video Data.	156	XDATAP[3]	O	Auxiliary Data.
117	VDD	—	Power Supply. +5 V.	157	XDATAP[2]	O	Auxiliary Data.
118	RCLK27MP	I	27 MHz Video Sys.Clock.	158	XDATAP[1]	O	Auxiliary Data.
119	RVPHDIFFP	O	Video Clock Phase Diff.	159	XDATAP[0]	O	Auxiliary Data.
120	VSS	—	GND.	160	VDD	—	Power Supply. +5 V.

Ordering Information

Description	Package	Device Code	Comcode
MPEG-2 System-Layer Demultiplexer	160-pin, plastic MQFP	AV6220A27J-DB	107530289

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June 1996
PN96-042VES (Replaces PN95-076VES)

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