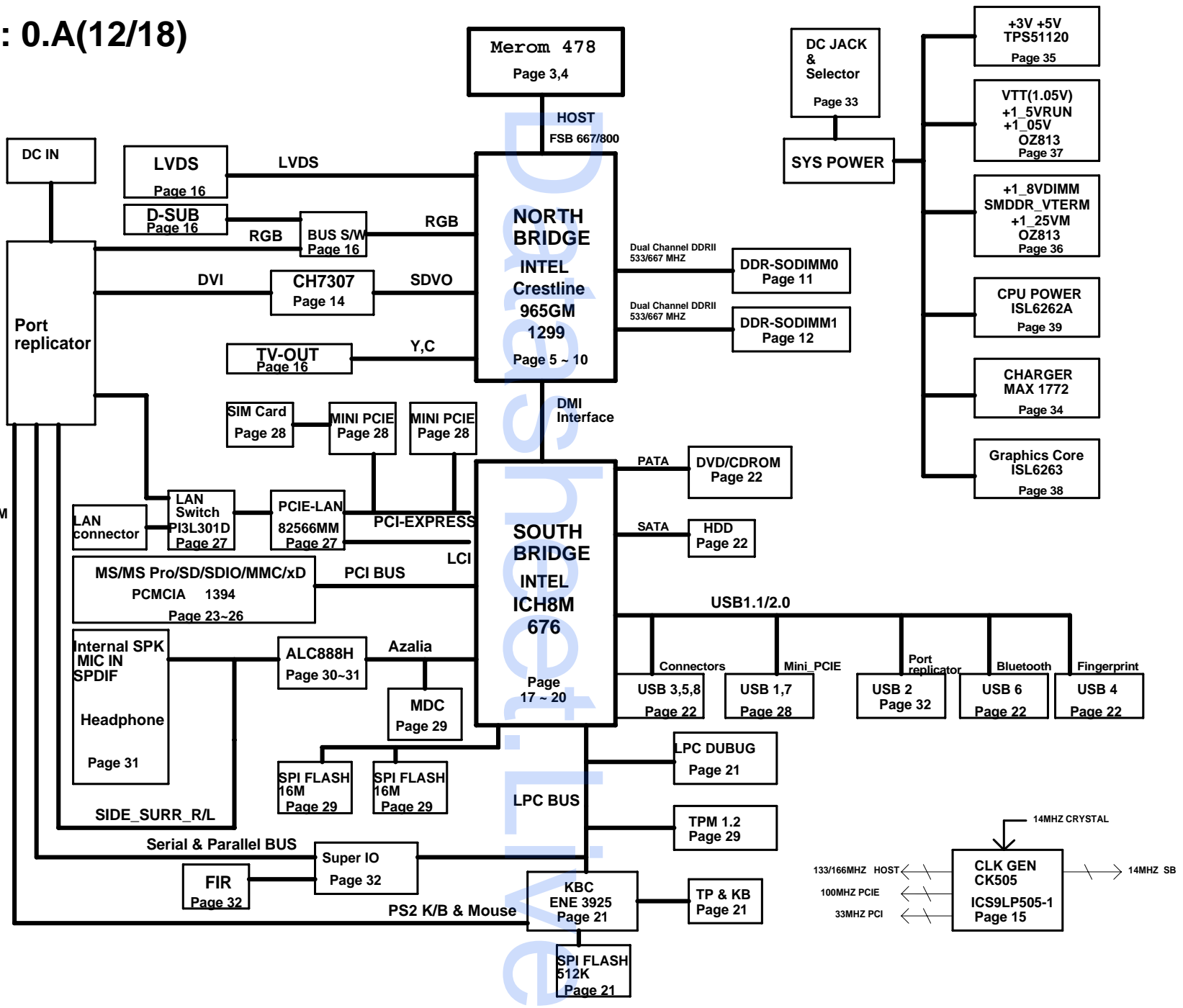


MS-1421 VER : 0.A(12/18)

- 01 : BLOCK DIAGRAM
- 02 : PLATFORM
- 03 : Merom-1 CPU (HOST BUS)
- 04 : Merom-2 CPU (POWER/GND)
- 05 : 965GM-1 (HOST)
- 06 : 965GM-2 (DMI / VGA)
- 07 : 965GM-3 (DDR)
- 08 : 965GM-4 (Power-1)
- 09 : 965GM-5 (Power-2)
- 10 : 965GM-6 (GND)
- 11 : DDR2_SODIMMO
- 12 : DDR2_SODIMM1
- 13 : DDR2_Termination
- 14 : SDVO- CH7307
- 15 : CLOCK GEN (SLG8SP512)
- 16 : VGA, LVDS, .BL,TV,BUS SW
- 17 : ICH8M-1 (CPU/IDE/Azalia)
- 18 : ICH8M-2 (PCI/USB/PCIE/DMI)
- 19 : ICH8M-3 (SM BUS/GPIO)
- 20 : ICH8M-4 (POWER/GND)
- 21 : KBC/EC/uP (ENE3925)
- 22 : HDD,CDROM,BT,USB CONN.
- 23 : R5C847_PCI
- 24 : R5C847_Cardbus & Media Card
- 25 : R5C847_1394
- 26 : R5C847_Media Card CONN
- 27 : PCIE LAN (INTEL82566MM)
- 28 : MINI_PCIE, LED, SW
- 29 : MDC, TPM, FAN,SPI FLASH ROM
- 30 : AZALIA CODEC(ALC888)
- 31 : Audio Amp. & Jacks
- 32 : Super I/O&Port Replicator
- 33 : M_Battery select
- 34 : M_Battery Charger
- 35 : M_System Power
- 36 : DDR2 RAM POWER, +1.25V
- 37 : M_VTT, +1.5V
- 38 : M_Graphics Core
- 39 : M_CPU power
- 40 : Screw/EMI
- 41 : Non_Footprint for BOM
- 42 : Power Sequency-1
- 43 : Power Sequency-2
- 44 : Power_Diagram(DC & Battery)
- 45 : Power_Diagram(Only Battery)
- 46 : AMT BLOCK DIAGRAM
- 47 : Change History



| | | | |
|---------------------------|---------------------------|-------|---------|
| MSI CORPORATION | | | |
| File BLOCK DIAGRAM | | | |
| Size | Document Number | Rev | |
| C | MS-14211 | 0A | |
| Date | Monday, December 25, 2006 | Sheet | 1 of 49 |

Voltage Rails

| Voltage | Description | Control Signal |
|----------------|------------------------------------------|-----------------|
| PWR_SRC | AC ADAPTER OR BATTERY IN OR DOCK IN | |
| +3VALW | 3.3V always on power rail | PWR_SRC |
| +5VALW | 5.0V always on power rail | PWR_SRC |
| +3VSUS | 3.3V power rail | SUS_ON |
| +5VSUS | 5.0V power rail | SUS_ON |
| +1_8VDIMM | 1.8V power rail DDR | PM_SLP_S4 |
| SMDDDR_VTERM | 0.9V DDR Termination voltage | PM_SLP_S4 |
| +1_25VM | 1.25V power rail AMT | PM_SLP_M |
| +1_05VM | 1.05V power rail AMT | PM_SLP_M |
| +3VMCLK | 3V power rail for AMT Clock Generator | PM_SLP_M |
| +3VRUN | 3.3V switched power rail | PM_SLP_S3(RUND) |
| +5VRUN | 5.0V switched power rail | PM_SLP_S3(RUND) |
| +1_25VRUN | 1.25V switched power rail | PM_SLP_S3(RUND) |
| +1_5VRUN | 1.5V power rail | PM_SLP_S3 |
| +1_05VRUN(VTT) | 1.05 rail for Processor & 965GM I/O | PM_SLP_S3 |
| VHCORE | Core Voltage for Processor | VR_ON |
| +VGFX_CORE | Graphic core of GMCH switched power rail | GFX_VR_EN |
| ADD5V | 5.0V Power rail Audio codec | +5VSUS(RUND) |
| +2.5VRUN | 2.5V power rail CH7307(DVI) | +3VRUN |

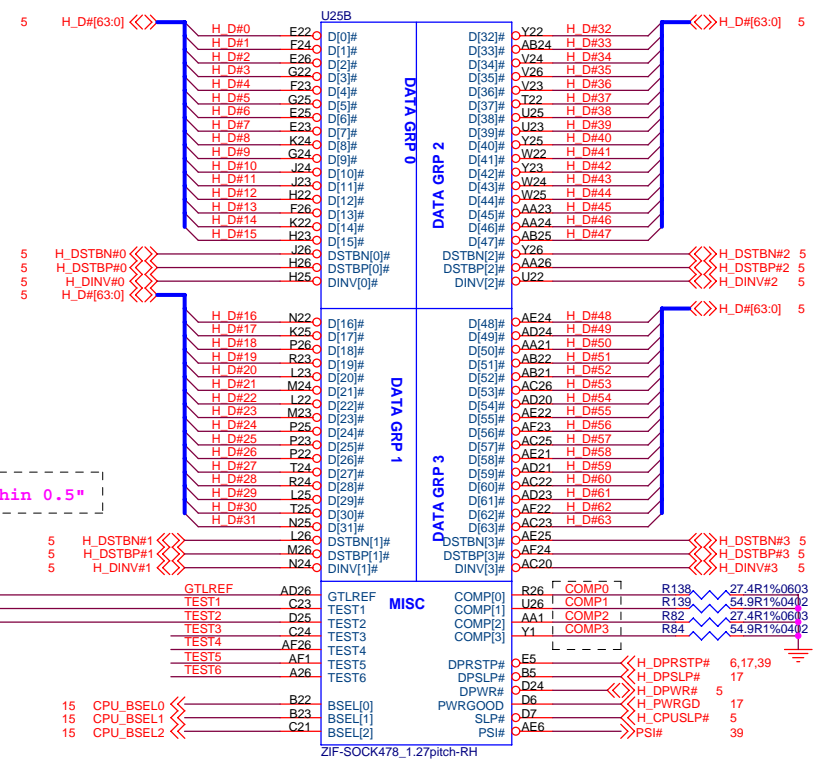
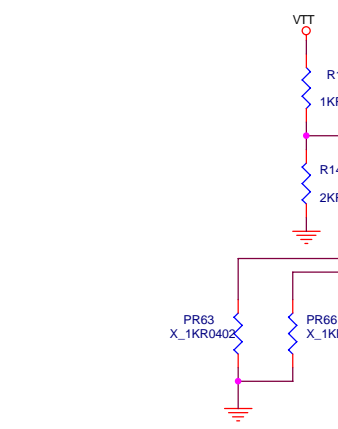
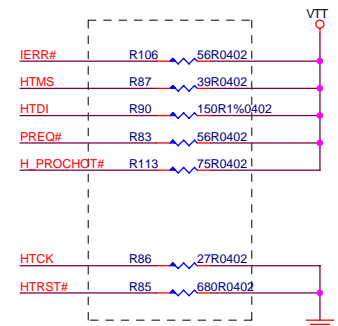
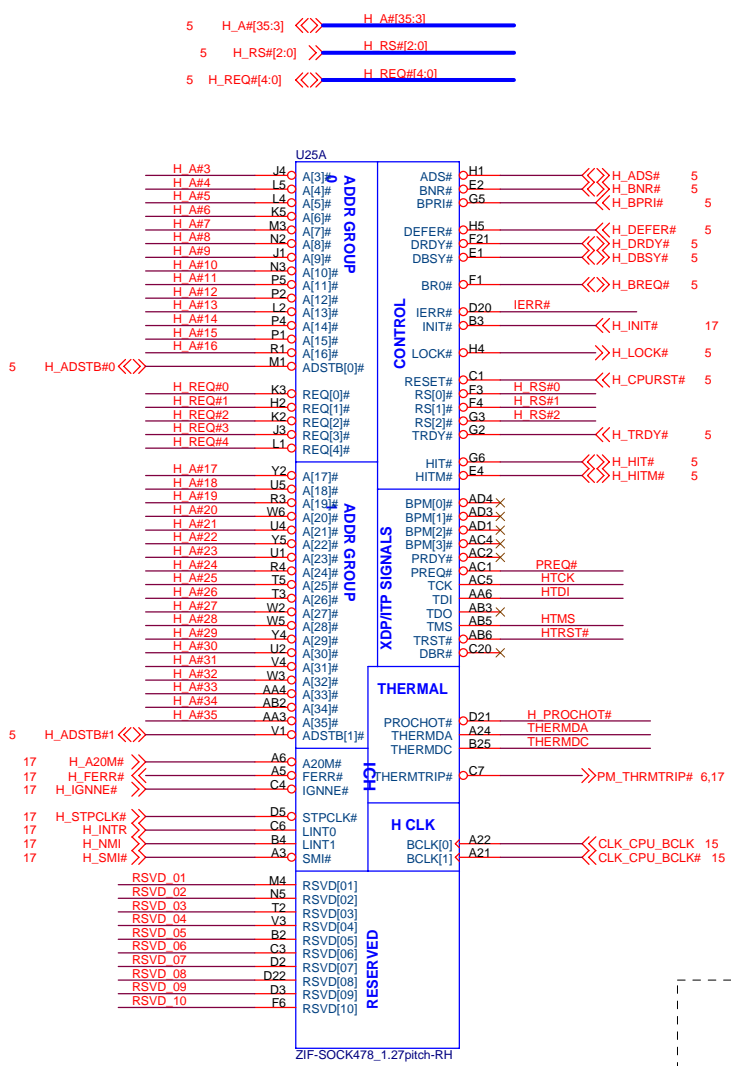
POWER STATES

| STATE \ SIGNAL | SLP_S3# | SLP_S4# | SLP_S5# | S4_STATE# | SLP_M# | +V*ALWAYS | +V*SUS | +V*M | +V*RUN | Clocks |
|---------------------------|---------|---------|---------|-----------|--------|-----------|--------|------|--------|--------|
| S0(Full ON) / M0 | HIGH | HIGH | HIGH | HIGH | HIGH | ON | ON | ON | ON | ON |
| S3(Suspend to RAM) / M1 | LOW | HIGH | HIGH | HIGH | HIGH | ON | ON | ON | OFF | ON |
| S4(Suspend to Disk) /M1 | LOW | HIGH | HIGH | LOW | HIGH | ON | ON | ON | OFF | ON |
| S5 / Soft OFF / M1 | LOW | HIGH | LOW | LOW | HIGH | ON | ON | ON | OFF | ON |
| S3(Suspend to RAM)/MOFF | LOW | HIGH | HIGH | HIGH | LOW | ON | ON | OFF | OFF | OFF |
| S4(Suspend to Disk)/MOFF | LOW | LOW | HIGH | LOW | LOW | ON | OFF | OFF | OFF | OFF |
| S5 / Soft OFF / MOFF | LOW | LOW | LOW | LOW | LOW | ON | OFF | OFF | OFF | OFF |

Note : WHEN AC MODE , System turn on then +V*SUS will always keep high

MSI CORPORATION

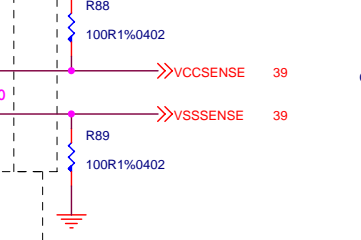
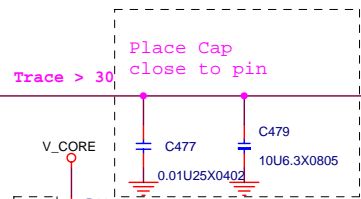
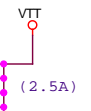
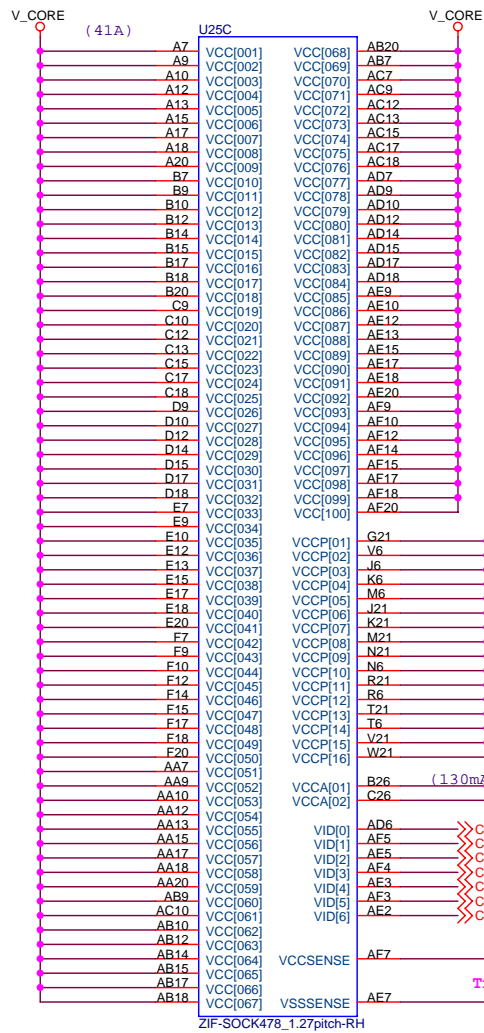
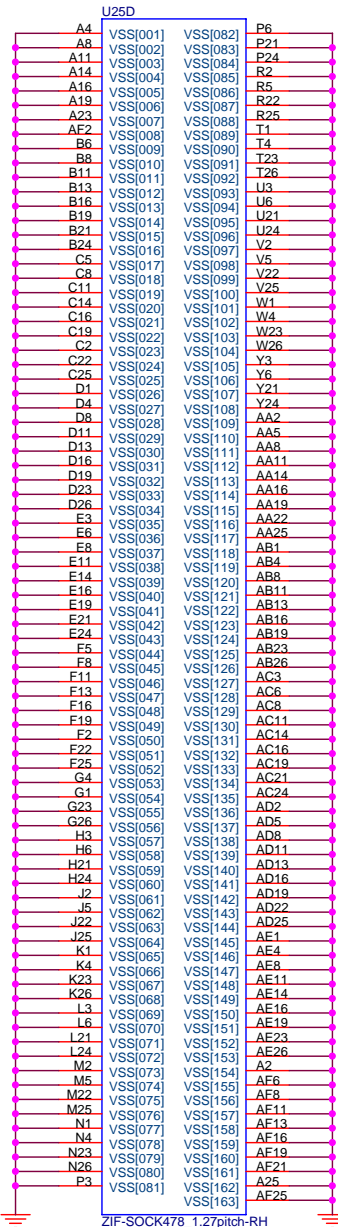
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|-------|---------------------------|-----------------|-----------------|-----|----|
| Title | | PLATFORM | | Rev | 0A |
| Size | Custom | Document Number | MS-14211 | | |
| Date: | Monday, December 25, 2006 | Sheet | 2 | of | 49 |



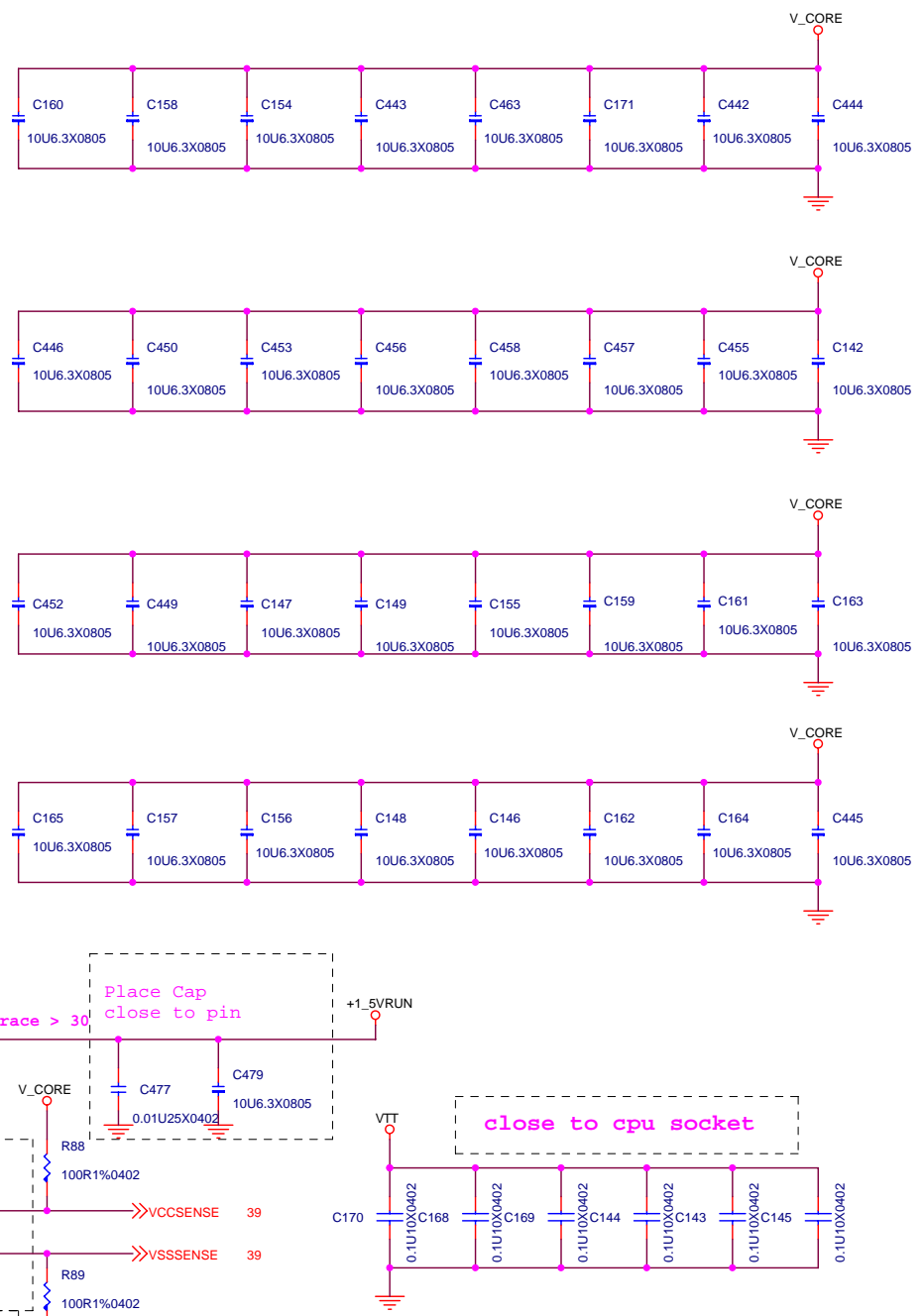
Within 0.5"

Within 0.5"
25mils Spacing
COMP0,2 --- 18mils
COMP1,3 --- 5mils

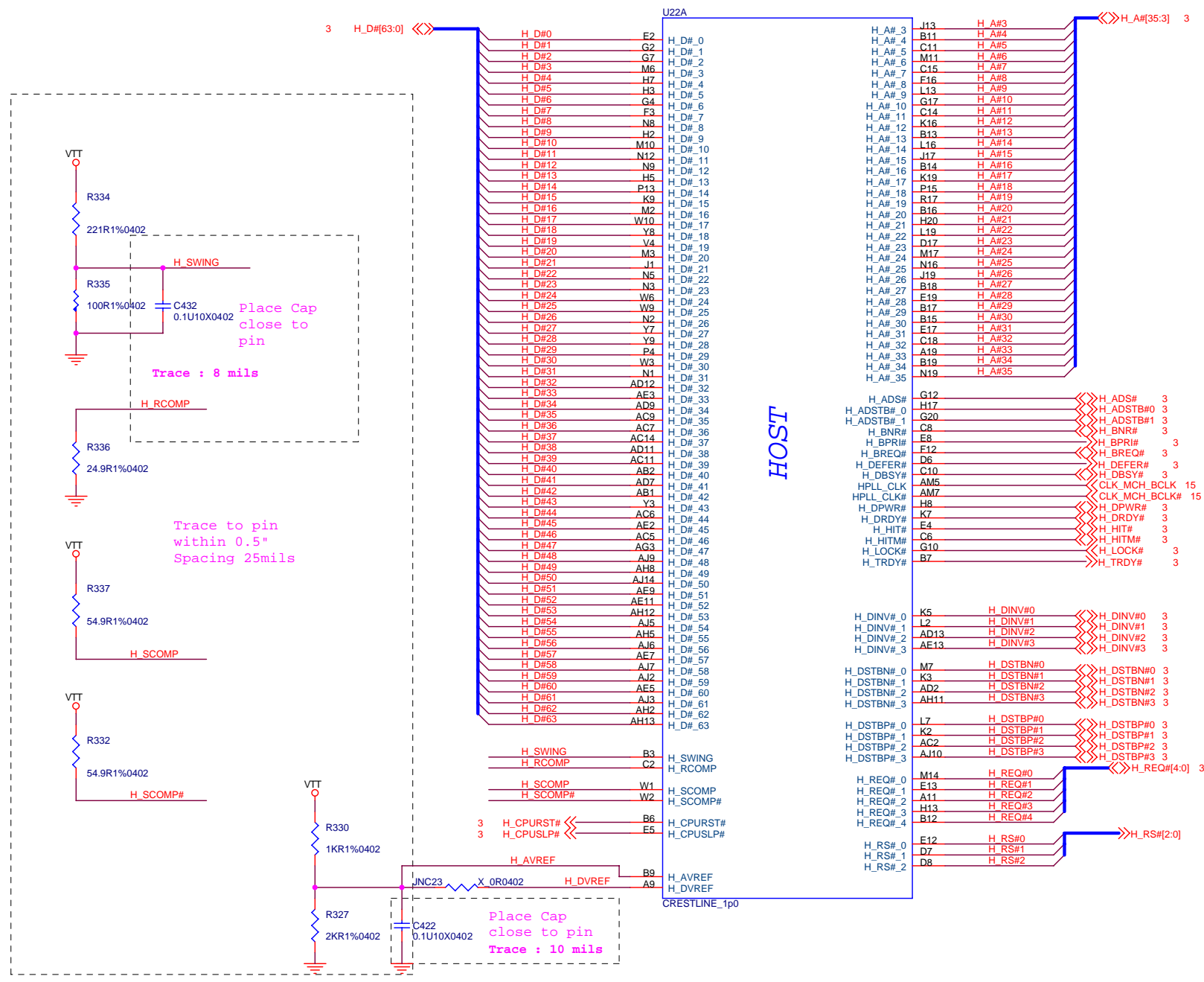
| MSI CORPORATION | | |
|----------------------------------|----------------------------------|---------|
| Title: Merom-1 (HOST BUS) | | |
| Size: Custom | Document Number: MS-14211 | Rev: 0A |
| Date: Monday, December 25, 2006 | Sheet: 3 of 49 | |



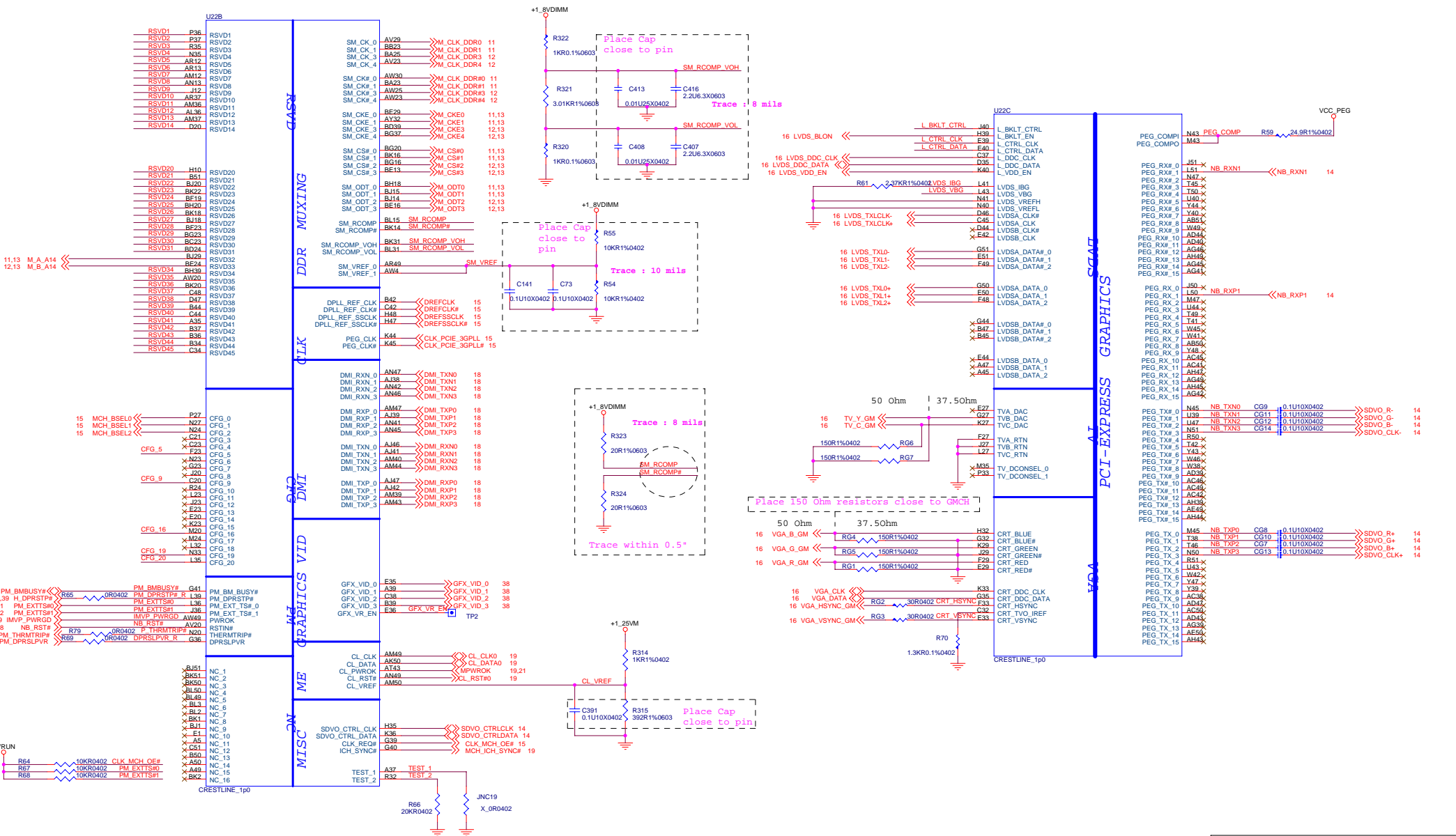
Trace width = 18mils
Trace spacing = 7mils
other spacing = 50mils
length matched within 25mils
Place R close to CPU within 1"



| | | |
|----------------------------|---------------------------|---------------|
| MSI CORPORATION | | |
| Merom-2 (POWER/GND) | | |
| Title | Document Number | Rev |
| Size | Custom | OA |
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| Date: | Monday, December 25, 2006 | Sheet 4 of 49 |



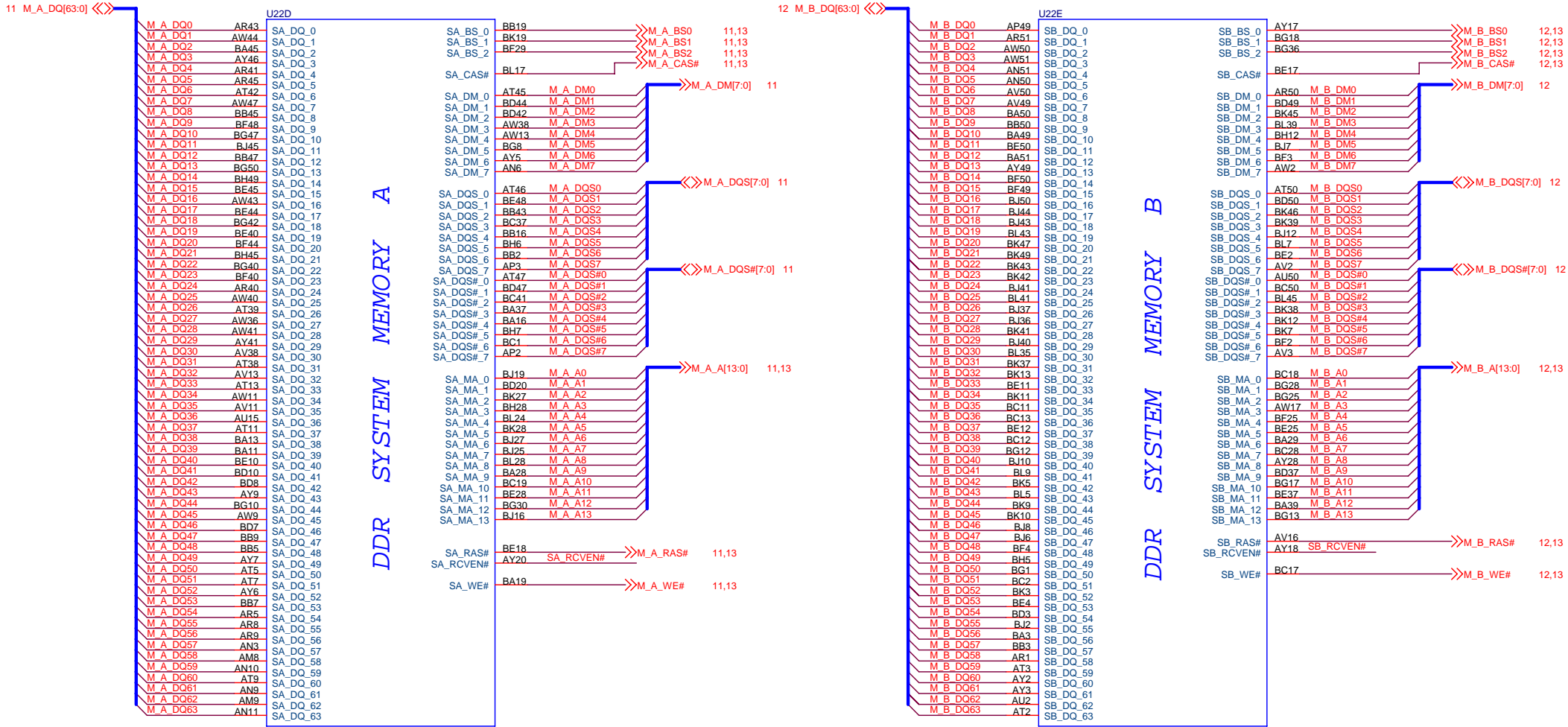
| | | |
|-------------------------------|---------------------------|---------------|
| MSI CORPORATION | | |
| CRESTLINE-1 (HOST BUS) | | |
| Title | | |
| Size | Document Number | Rev |
| B | MS-14211 | 0A |
| Date: | Monday, December 25, 2006 | Sheet 5 of 49 |



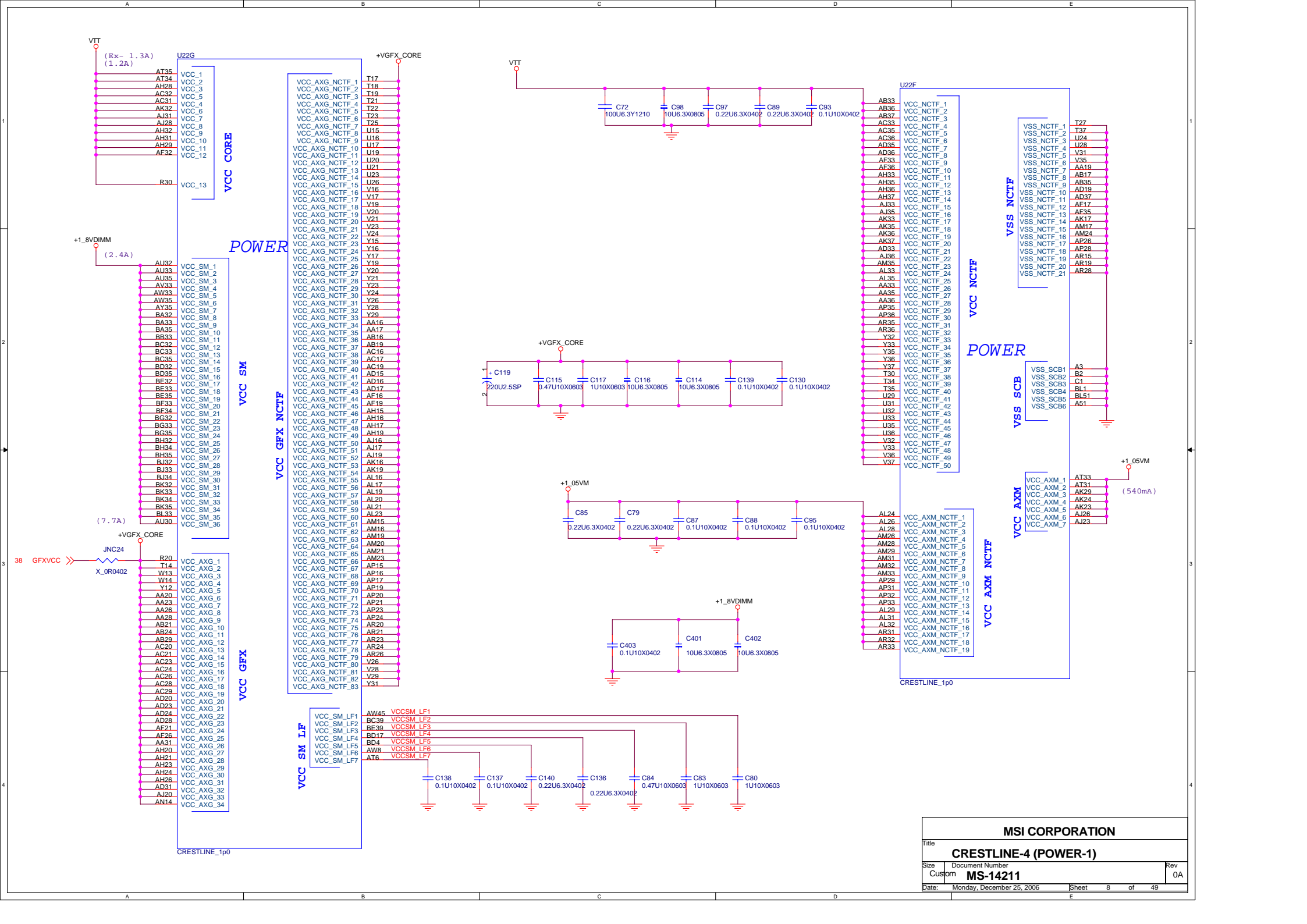
Strapping Configuration

| CFG5 (Default=High) | CFG9 (Default=High) | CFG16 (Default=High) | CFG19 (Default=Low) | CFG20 (Default=Low) | SDVO_CTRLDATA |
|------------------------|-----------------------------------------|-------------------------------------------------|------------------------------------|------------------------------------------------------------------------------------------------------------|-------------------------------------------------|
| 0= DMI x2 1= DMI x4 | 0= Reverse Lanes 1= Normal Operation | 0=Dynamic ODT Disabled 1=Dynamic ODT Enabled | 0= Normal 1= DMI Lanes Reversed | 0 = Only SDVO or PCIe is operational 1 = SDVO and PCIe are operating simultaneously via the PEG port | 1: SDVO card present 0: No SDVO card present |

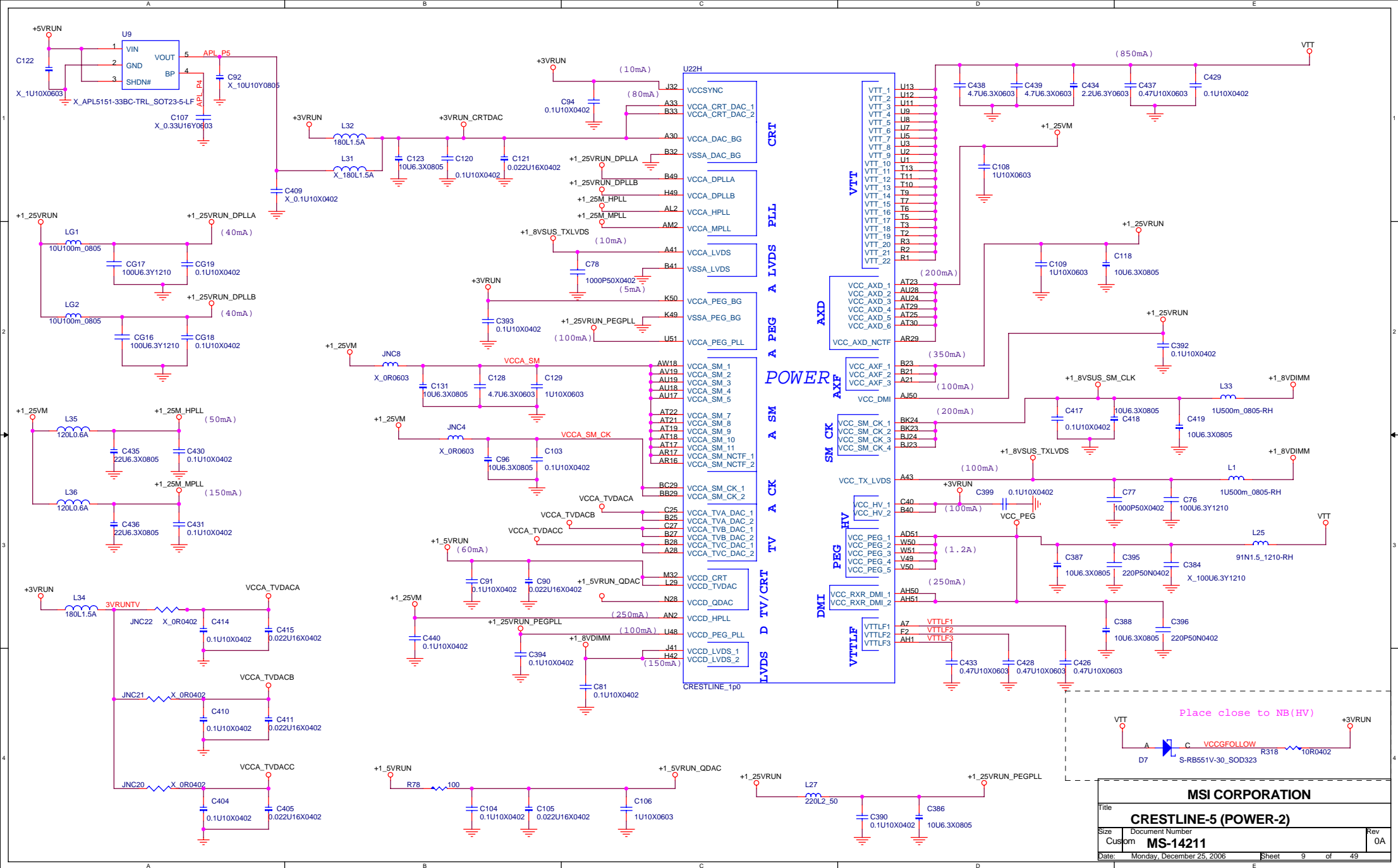
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|---------------------------------|-----------------|---------|
| MSI CORPORATION | | |
| CRESTLINE-2 (DMI/VGA) | | |
| Part No. | Document Number | Rev |
| Customer | MS-14211 | GA |
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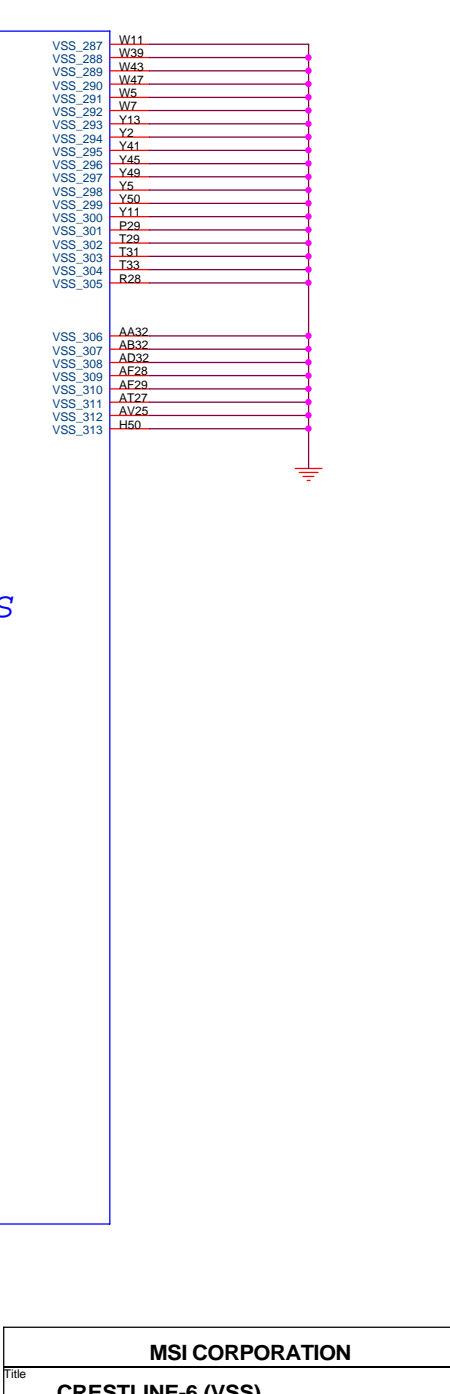
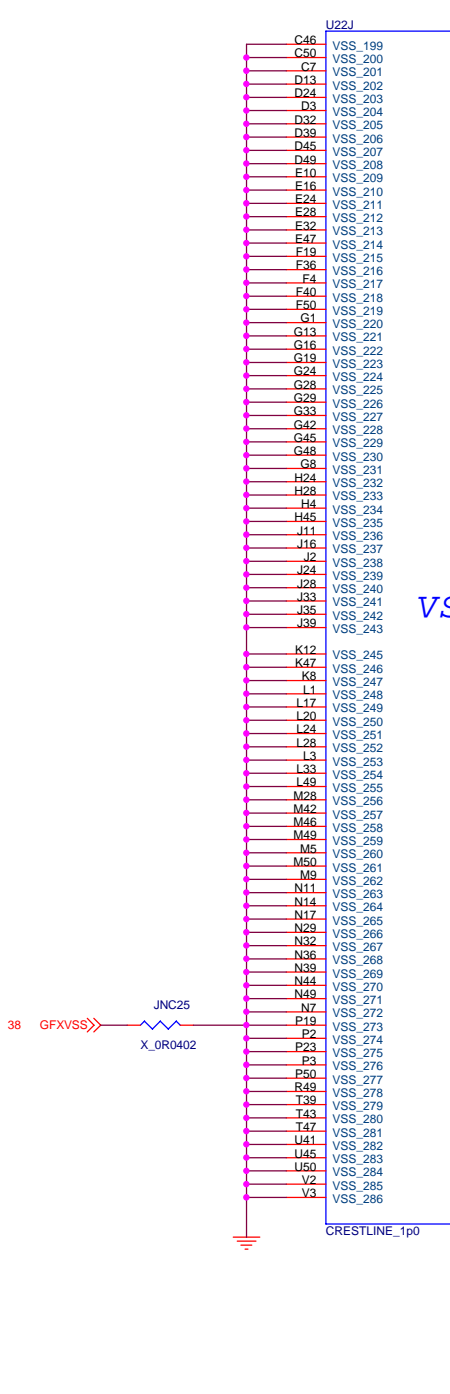
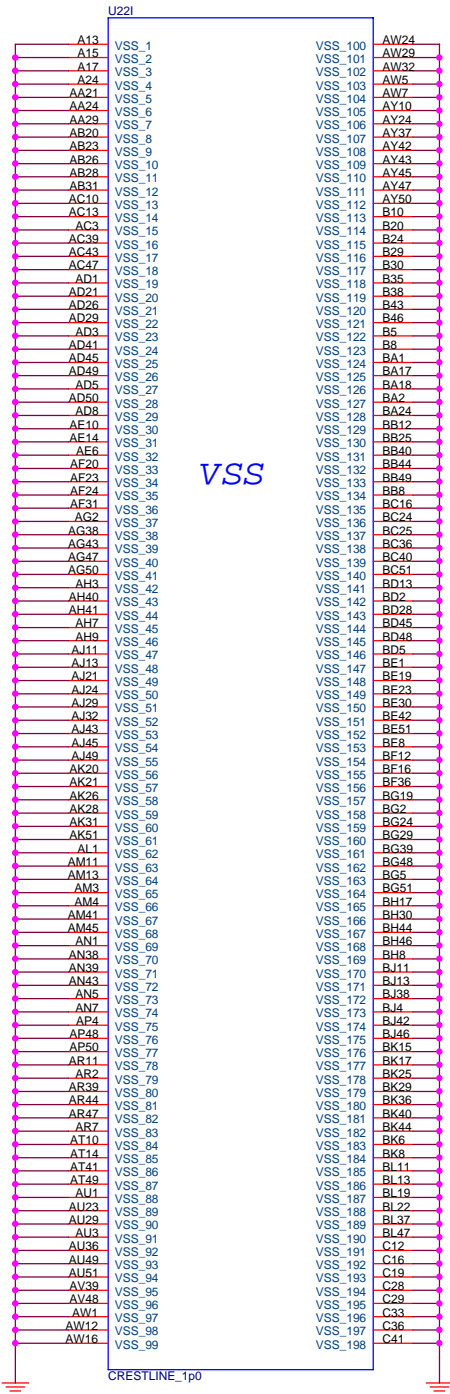


| | | |
|--------------------------|---------------------------|---------------|
| MSI CORPORATION | | |
| Title | | |
| CRESTLINE-3 (DDR) | | |
| Size | Document Number | Rev |
| Custom | MS-14211 | 0A |
| Date: | Monday, December 25, 2006 | Sheet 7 of 49 |

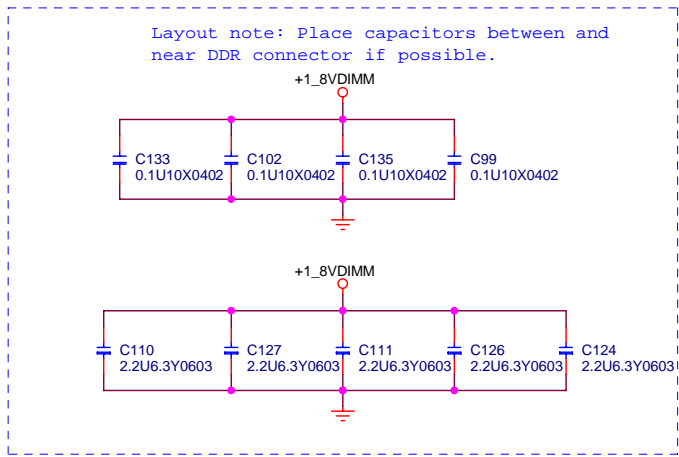
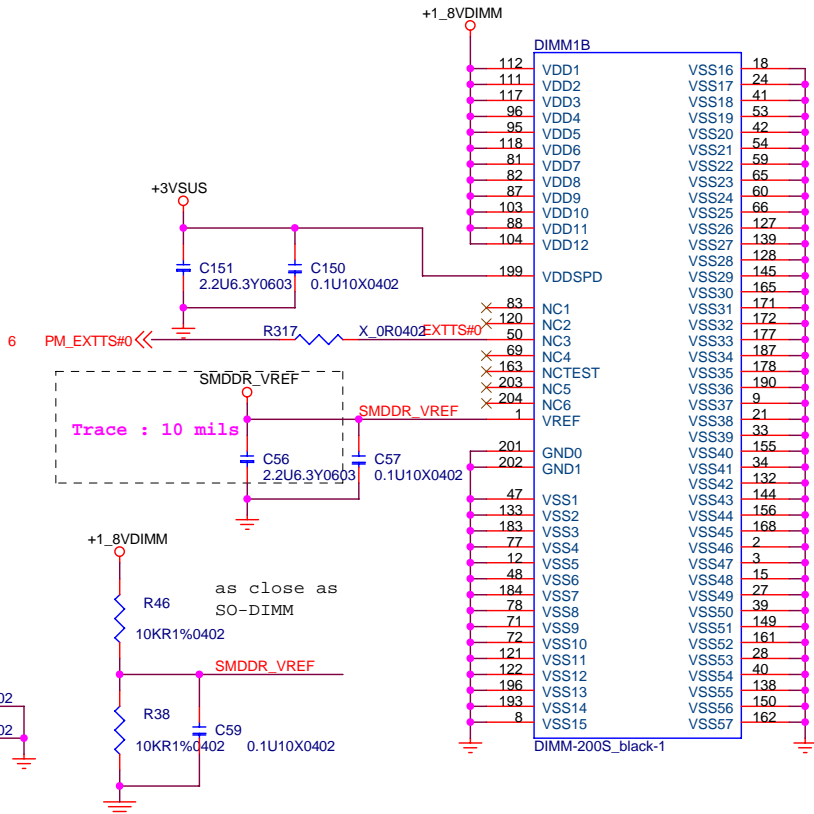
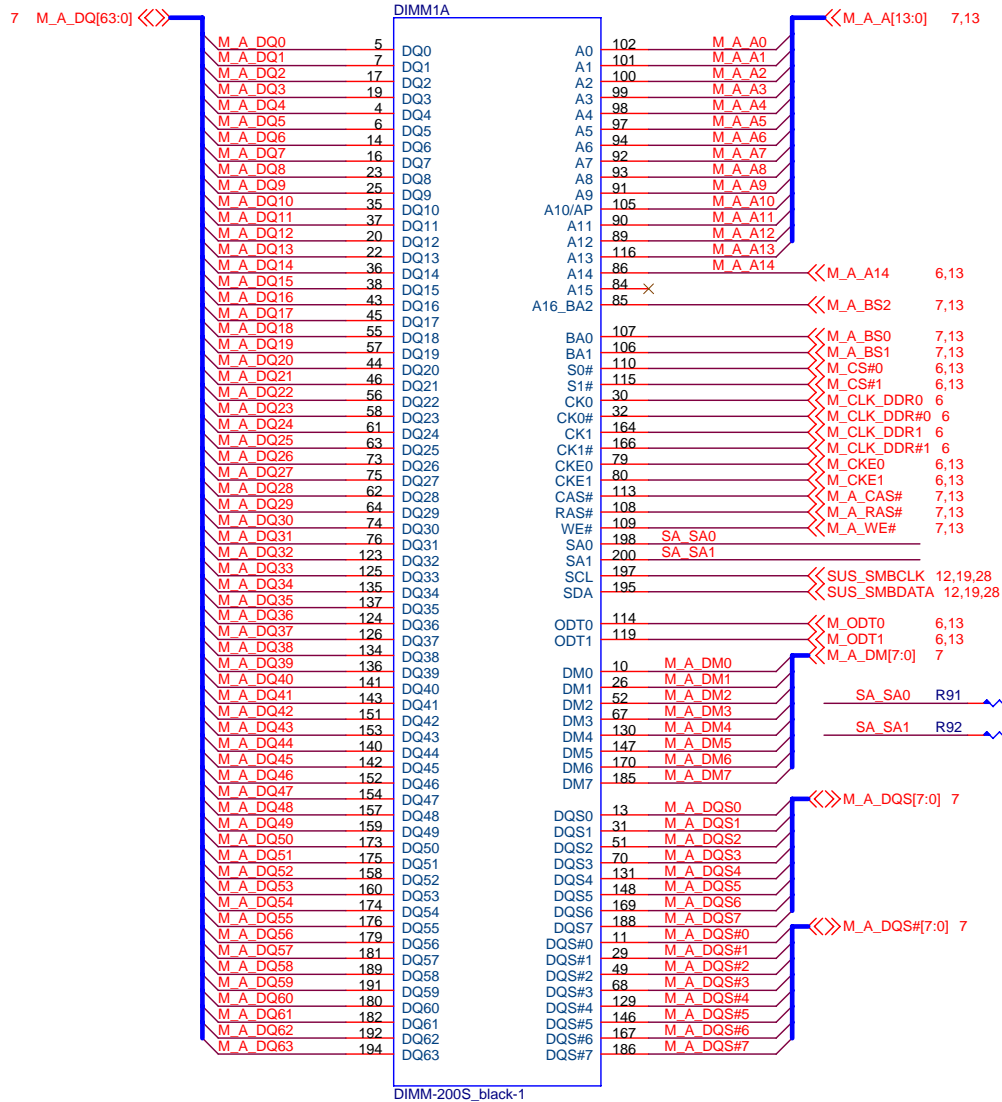


| | | |
|------------------------------|---------------------------|---------------|
| MSI CORPORATION | | |
| Title | | |
| CRESTLINE-4 (POWER-1) | | |
| Size | Document Number | Rev |
| Custom | MS-14211 | 0A |
| Date: | Monday, December 25, 2006 | Sheet 8 of 49 |

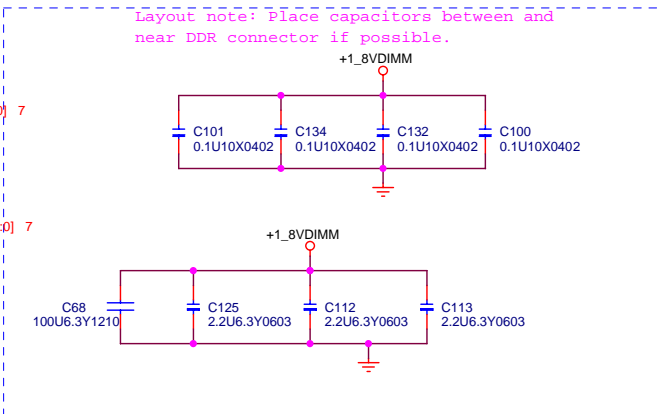
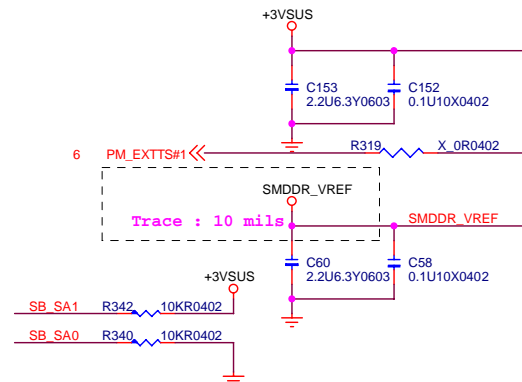
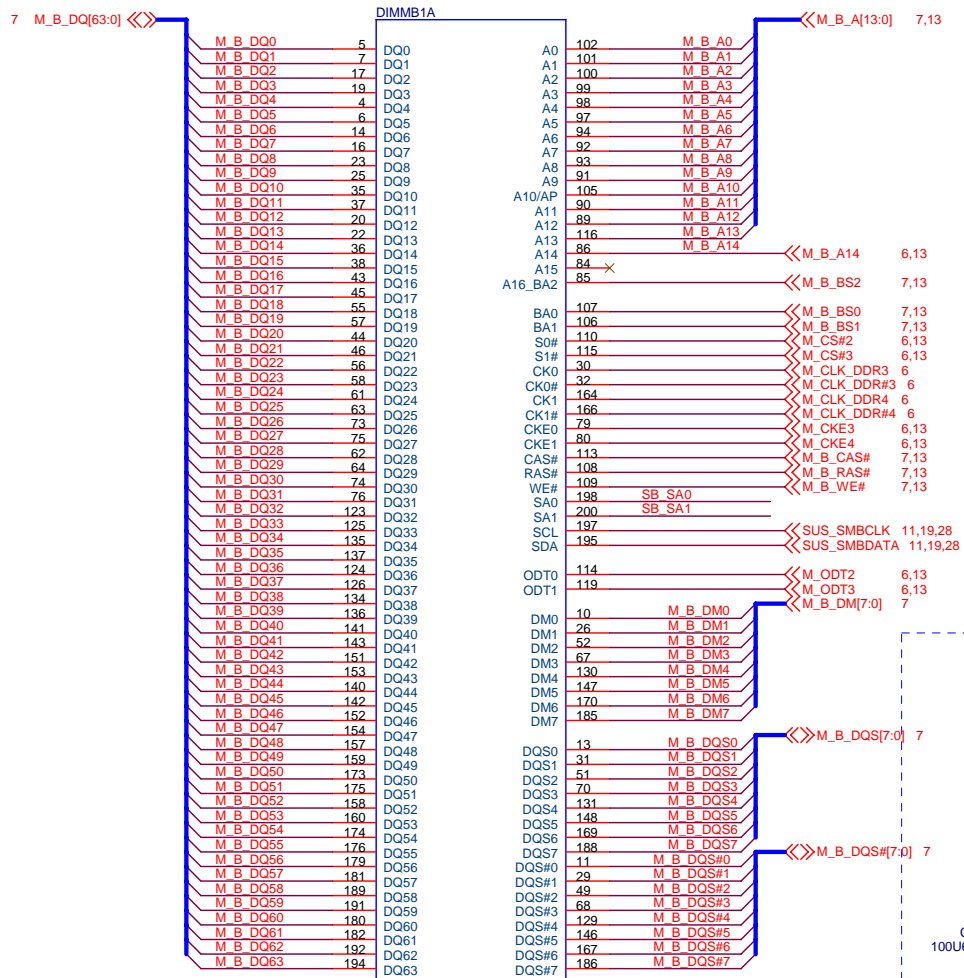




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|--------------------------|---------------------------|----------------|
| MSI CORPORATION | | |
| Title | | |
| CRESTLINE-6 (VSS) | | |
| Size | Document Number | Rev |
| Custom | MS-14211 | 0A |
| Date: | Monday, December 25, 2006 | Sheet 10 of 49 |

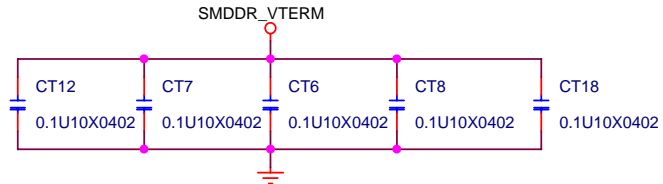
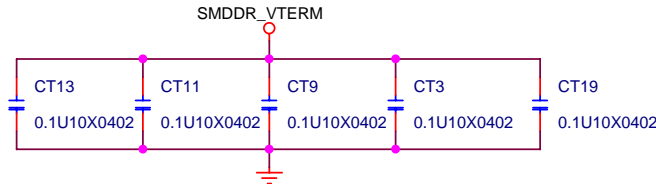
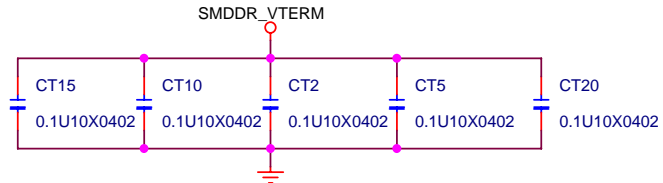
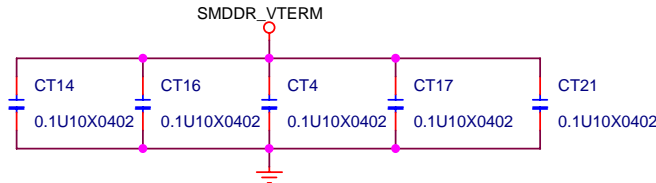
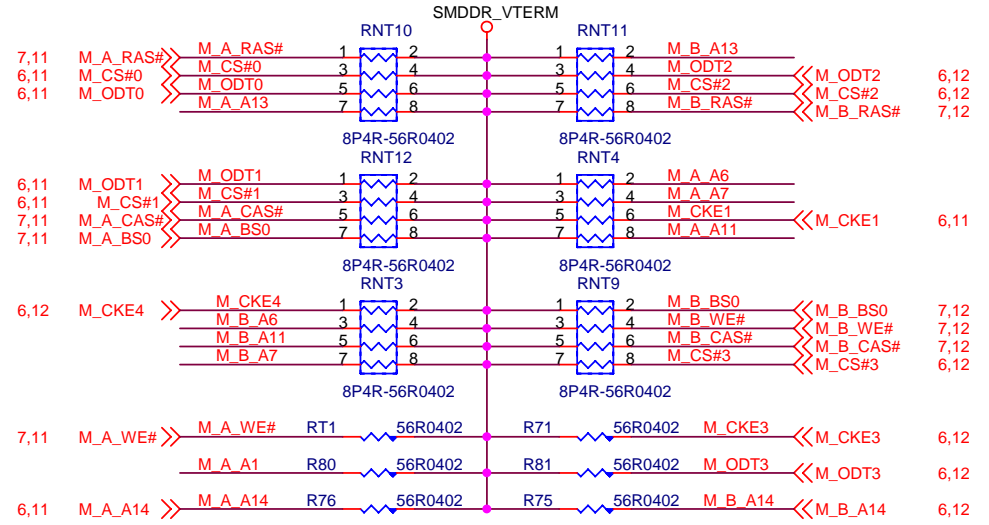
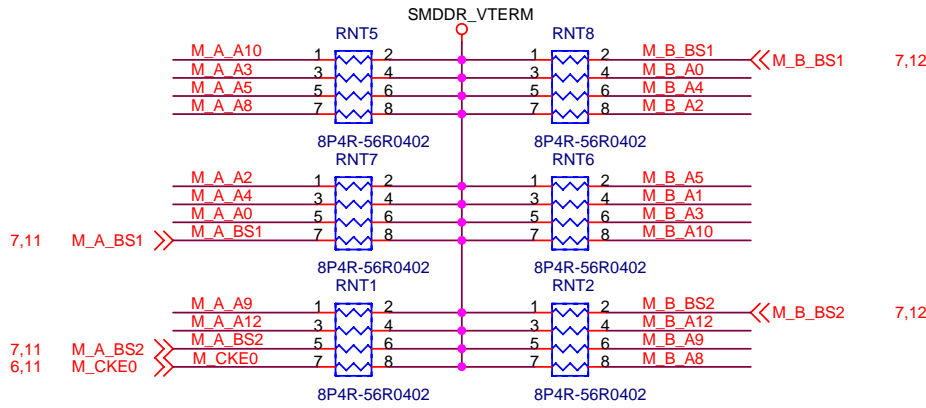


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| MSI CORPORATION | | |
| Title | | |
| DDR2 SODIMM 0 | | |
| Size | Document Number | Rev |
| Custom | MS-14211 | 0A |
| Date: | Monday, December 25, 2006 | Sheet 11 of 49 |



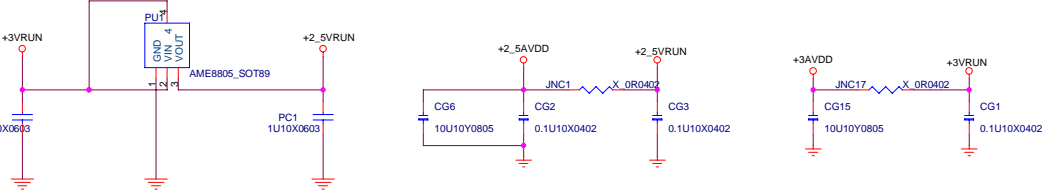
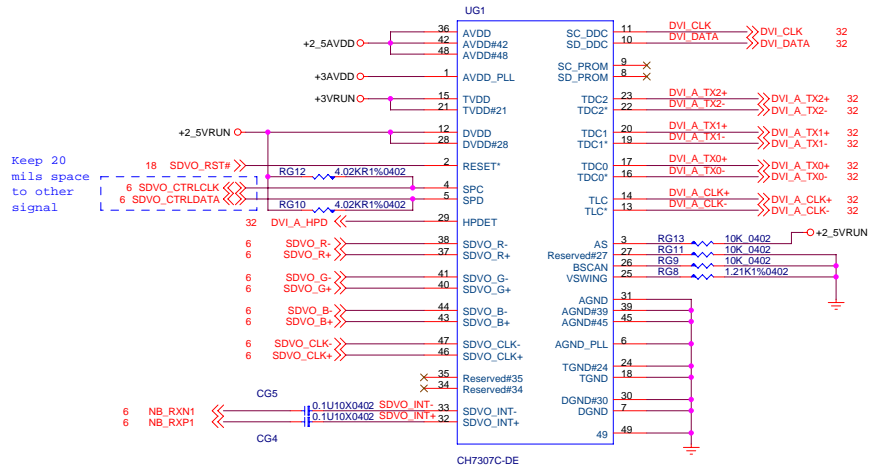
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| MSI CORPORATION | | |
| Title | | |
| DDR2 SODIMM 1 | | |
| Size | Document Number | Rev |
| Custom | MS-14211 | 0A |
| Date: | Monday, December 25, 2006 | Sheet 12 of 49 |

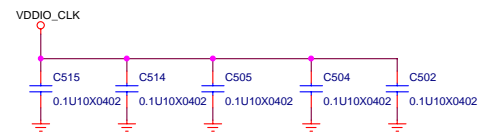
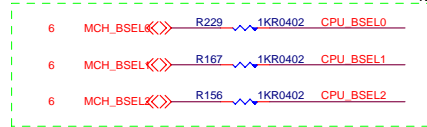
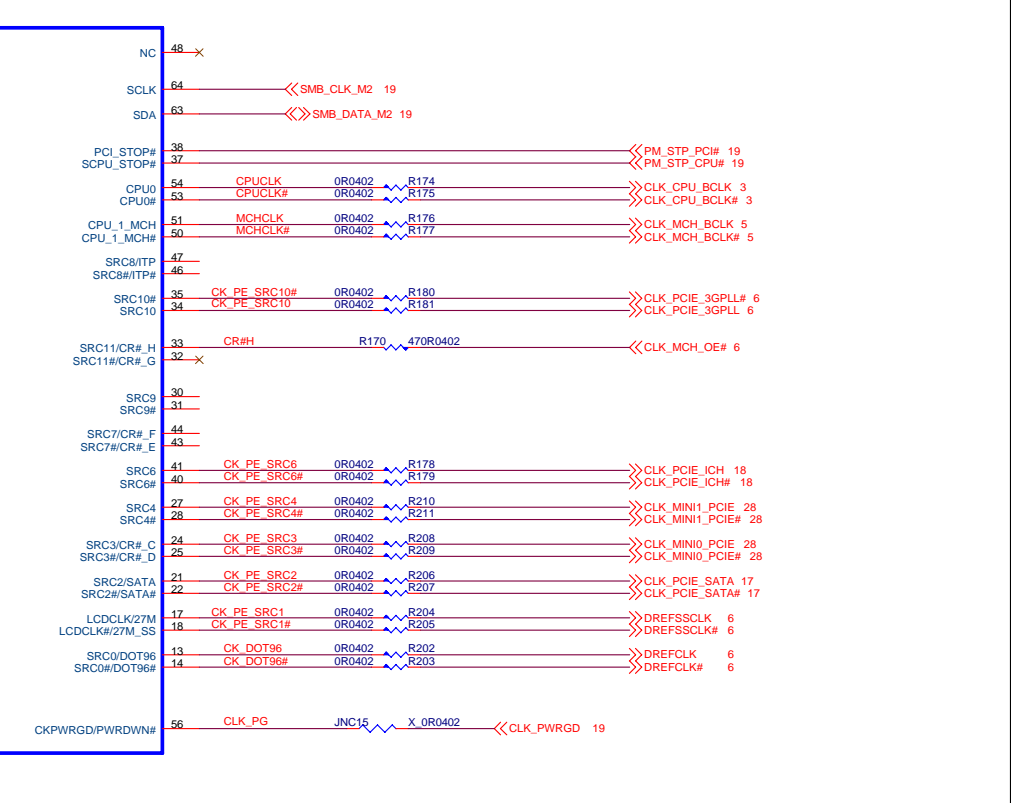
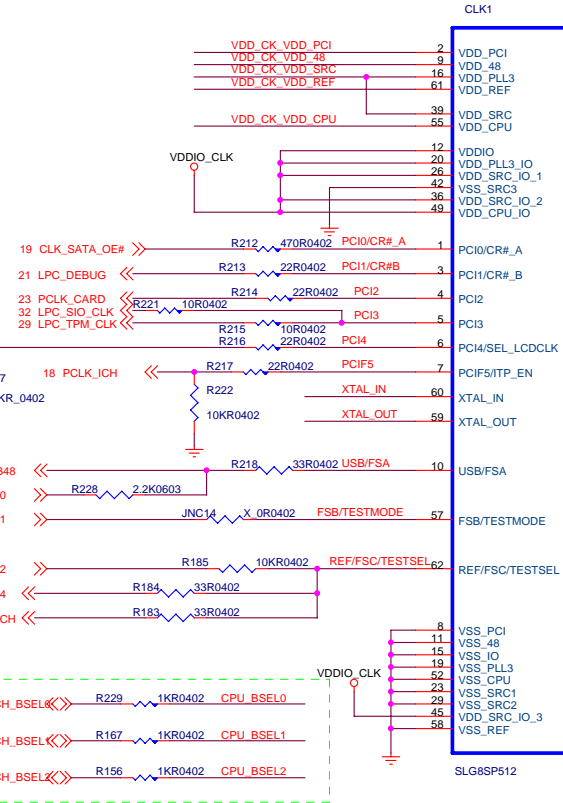
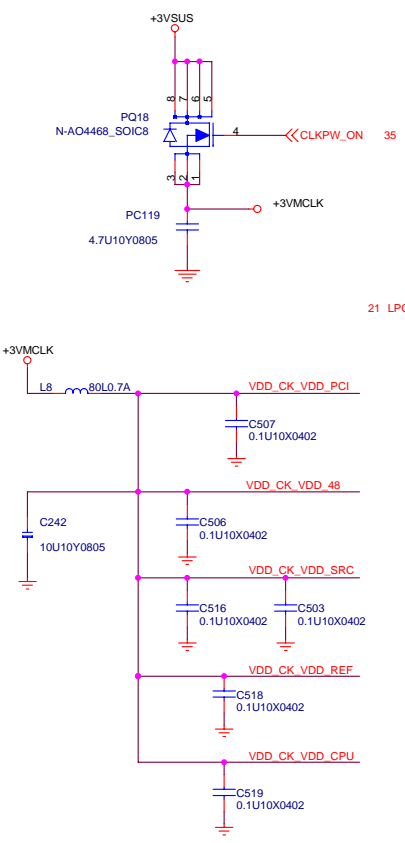
M_A_A[13:0] <<M_A_A[13:0] 7,11
 M_B_A[13:0] <<M_B_A[13:0] 7,12



Layout note: Place one cap close to every 2 pullup resistors terminated to +SMDDR_VTERN.

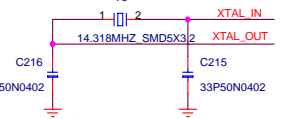
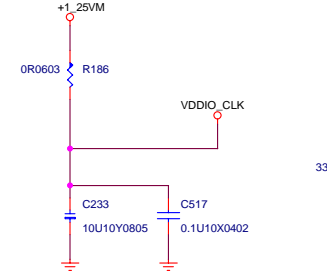
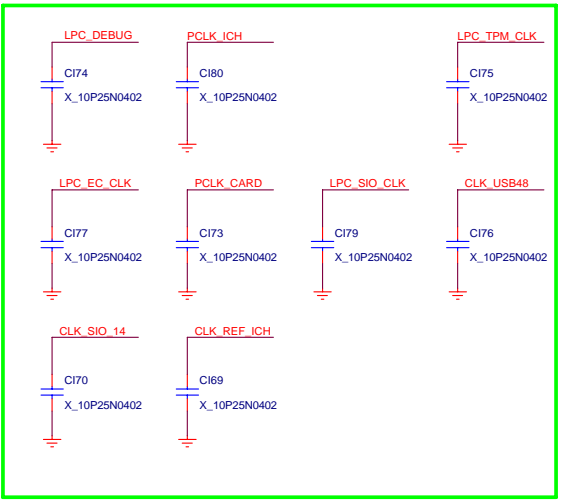
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| MSI CORPORATION | | | |
| Title | | | |
| DDR2 TREMINATION | | | |
| Size | Document Number | | Rev |
| Custom | MS-14211 | | 0A |
| Date: | Monday, December 25, 2006 | Sheet | 13 of 49 |



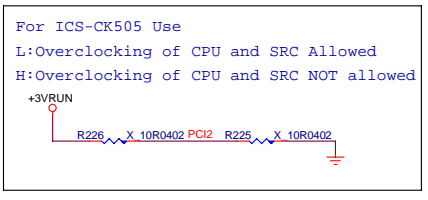


| PCIF_5/ITP_EN | |
|---------------|---------|
| 0 | SRC_8 |
| 1 | CPU_ITP |

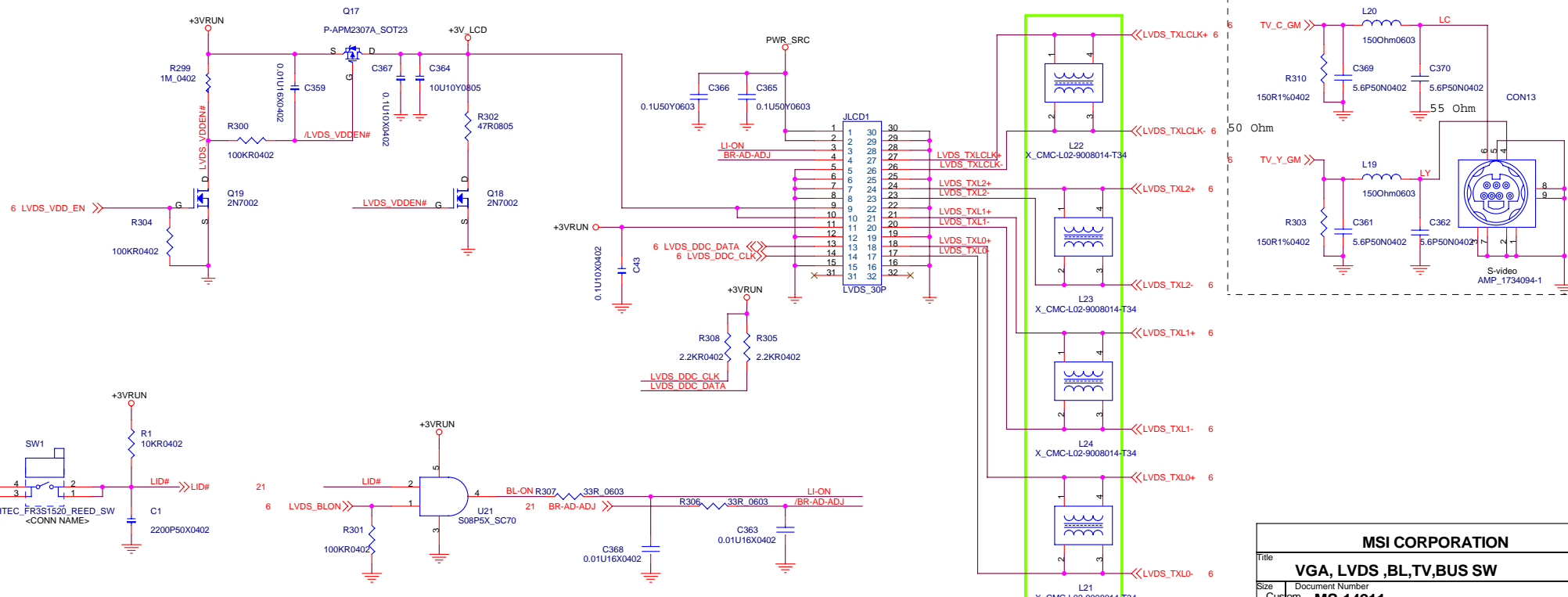
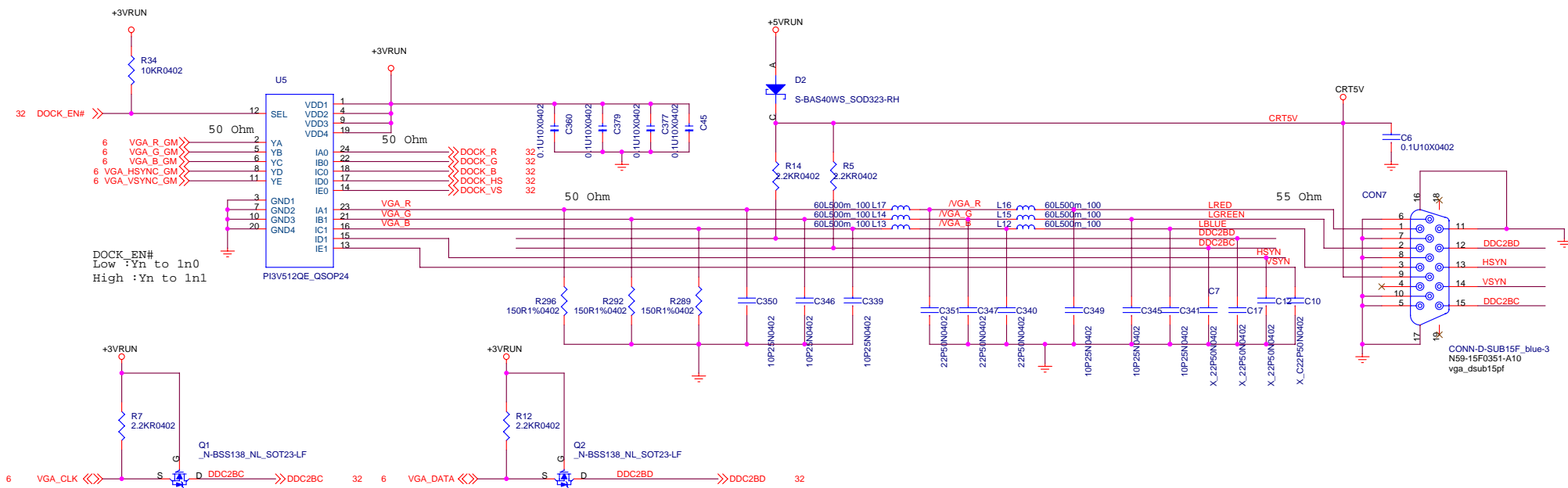
| PCI4/SEL_LCDCLK | | |
|-----------------|------------------|------------------|
| SEL_LCDCLK# | Pin 13/14 | Pin 17/18 |
| PIN6:LOW | DOT_96 / DOT_96# | LCDCLK / LCDCLK# |
| PIN6:High | SRC_0 / SRC_0# | 27M / 27M_SS |



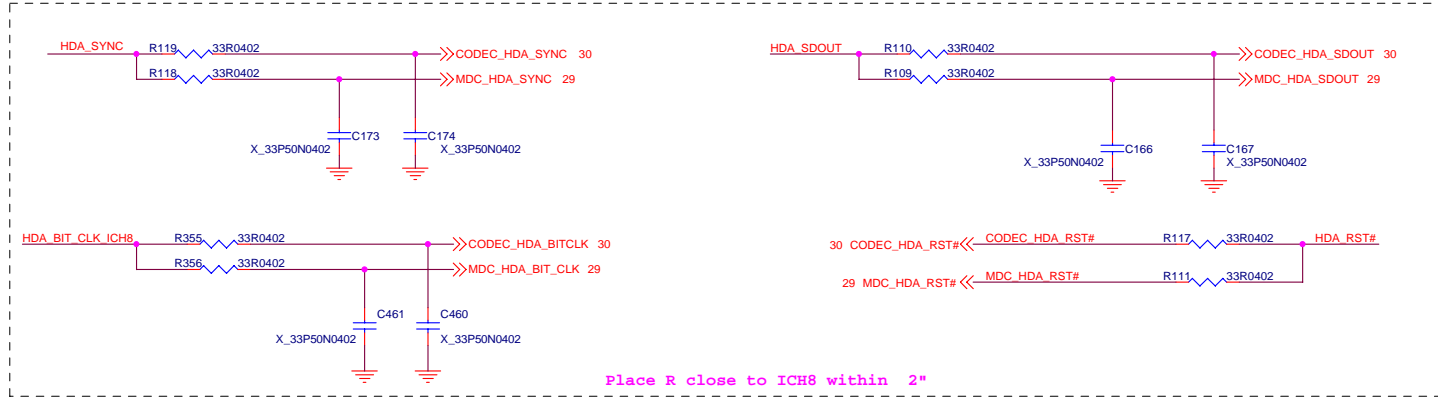
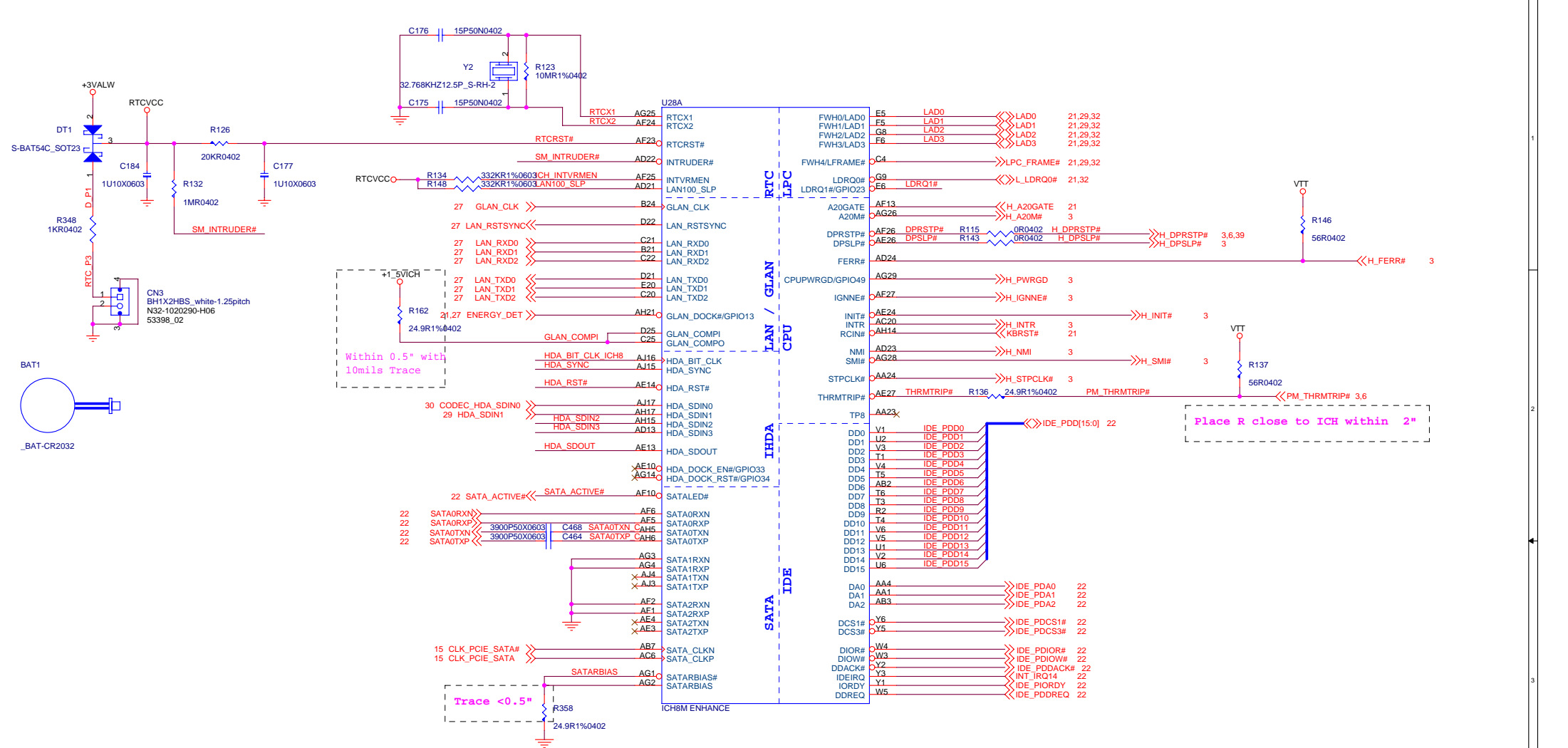
| CPU Table | | | FSB Freq (MHz) |
|-----------|---------|---------|----------------|
| BSEL[2] | BSEL[1] | BSEL[0] | |
| L | H | H | 667 MHz |
| L | H | L | 800 MHz |



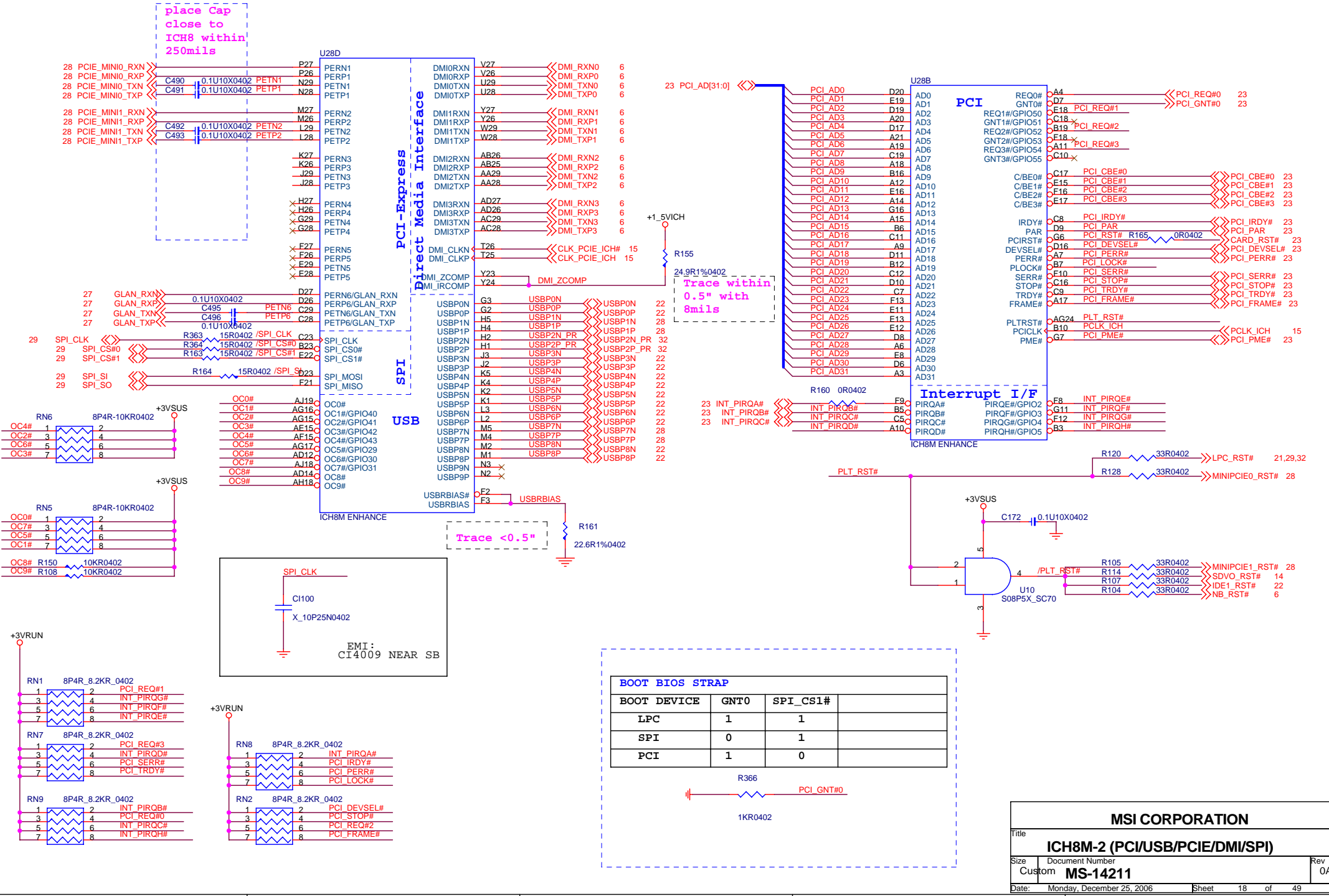
| Description/Function | Mapping | Power up condition |
|------------------------------------------------------------------------------------------------------|------------------------------------|--------------------|
| CLKREQ_A# enable 0 = Configure pin 1 as PCI_0 output 1 = Configure pin 1 as CLKREQ_A# input | CLKREQ_A# control SRC_2 output | 0 |
| CLKREQ_H# enable 0 = Configure pin 33 as SRC_11 output 1 = Configure pin 33 as CLKREQ_H# input | CLKREQ_H# control SRC_10 output | 0 |



| | | |
|----------------------------------|-----------------|-------|
| MSI CORPORATION | | |
| VGA, LVDS, BL, TV, BUS SW | | |
| Title | Document Number | Rev |
| Size | MS-14211 | 0A |
| Date: Monday, December 25, 2006 | Sheet 16 | of 49 |



| | | |
|---------------------------------|---------------------------|----------------|
| MSI CORPORATION | | |
| Title | | |
| ICH8M-1 (CPU/IDE/Azalia) | | |
| Size | Document Number | Rev |
| Custom | MS-14211 | 0A |
| Date: | Monday, December 25, 2006 | Sheet 17 of 49 |



BOOT BIOS STRAP

| BOOT DEVICE | GNT0 | SPI_CS1# |
|-------------|------|----------|
| LPC | 1 | 1 |
| SPI | 0 | 1 |
| PCI | 1 | 0 |

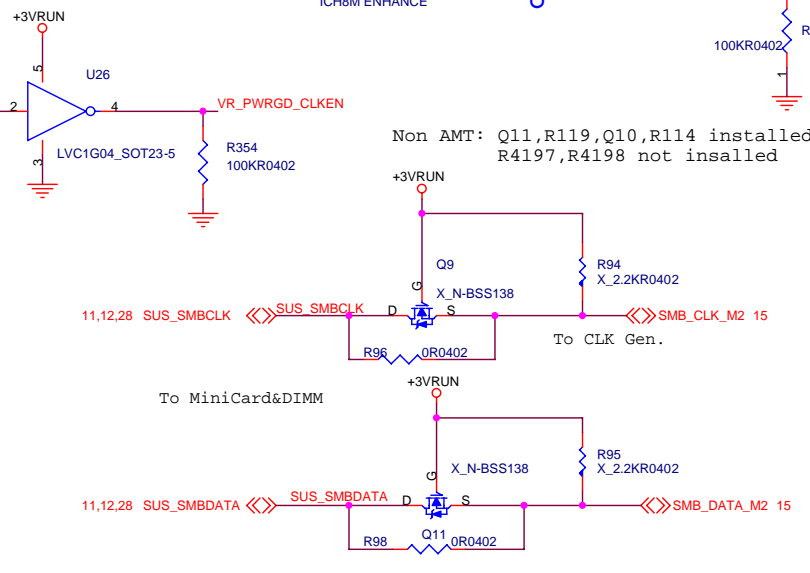
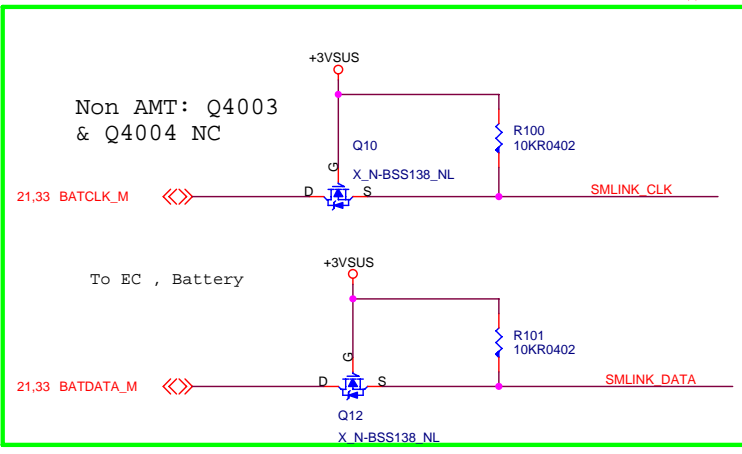
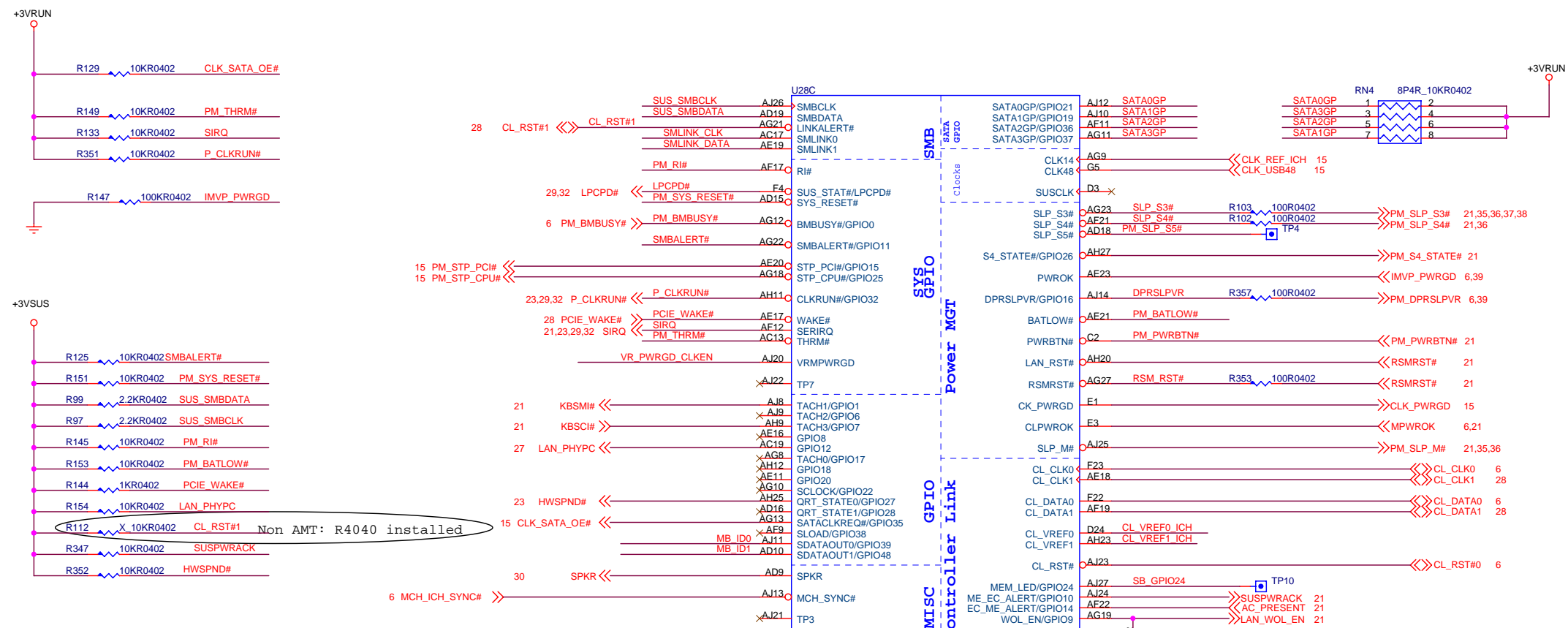


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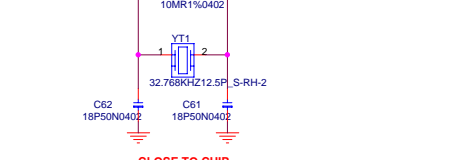
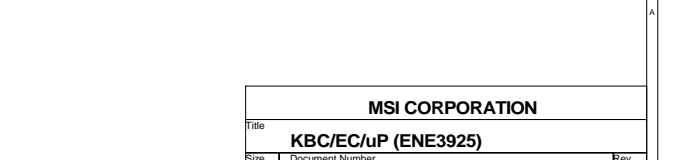
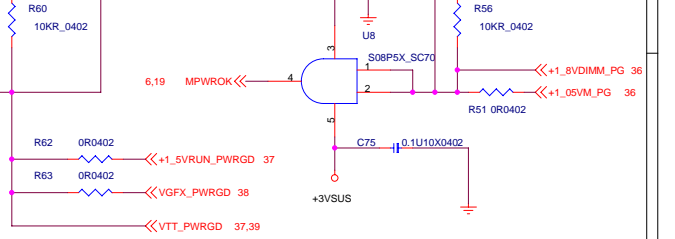
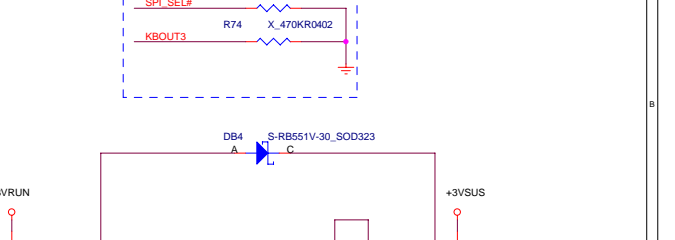
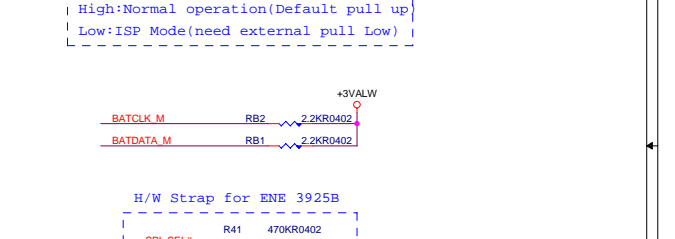
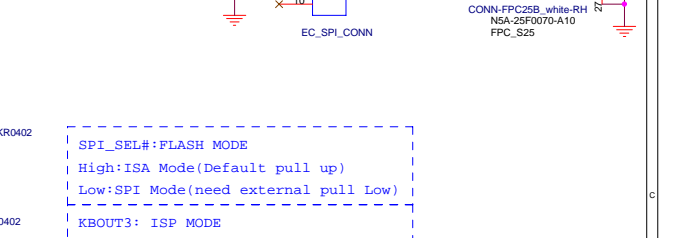
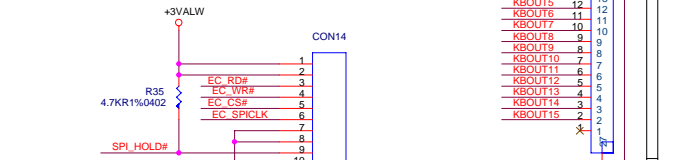
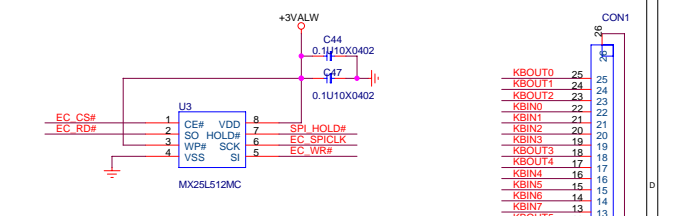
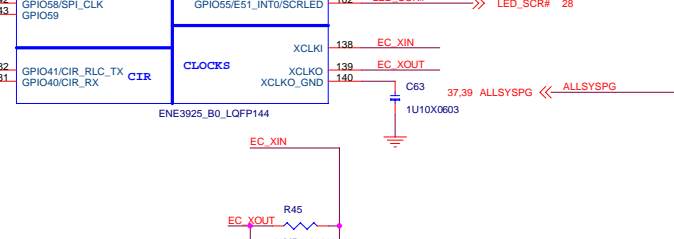
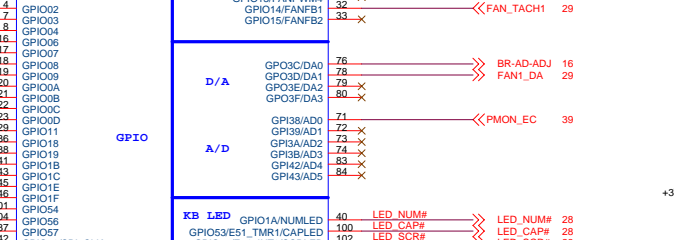
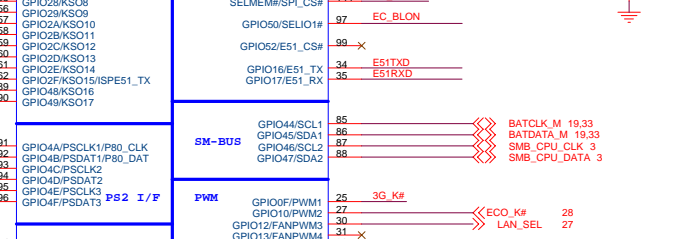
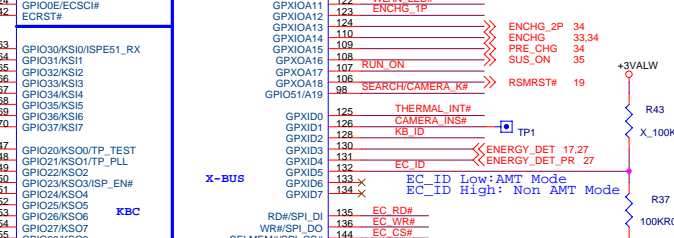
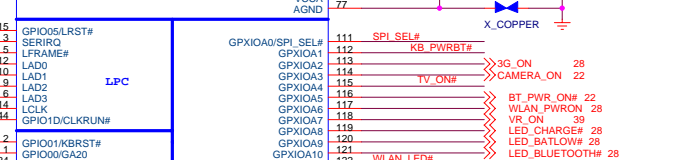
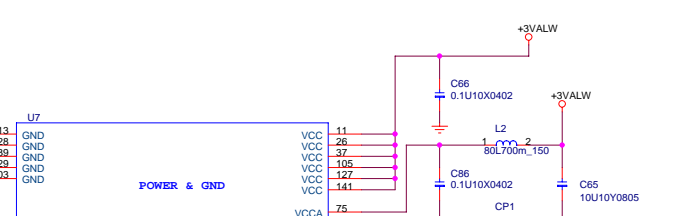
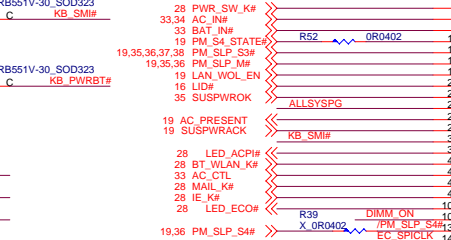
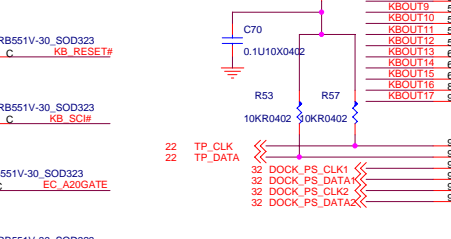
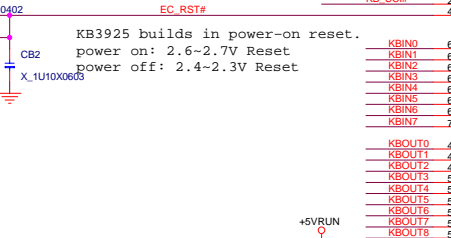
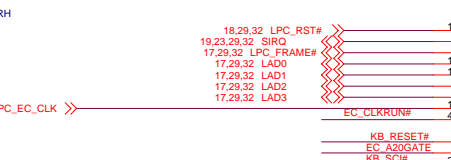
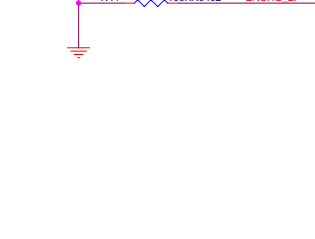
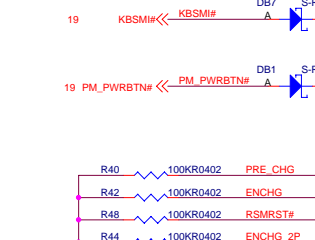
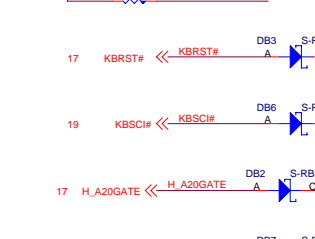
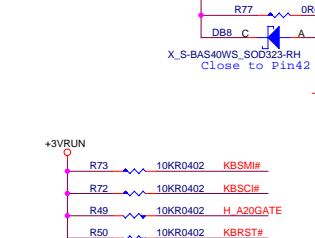
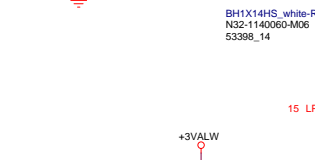
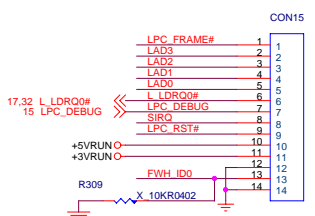
Title: **ICH8M-2 (PCI/USB/PCIE/DMI/SPI)**

| | | |
|--------|-----------------|-----|
| Size | Document Number | Rev |
| Custom | MS-14211 | 0A |

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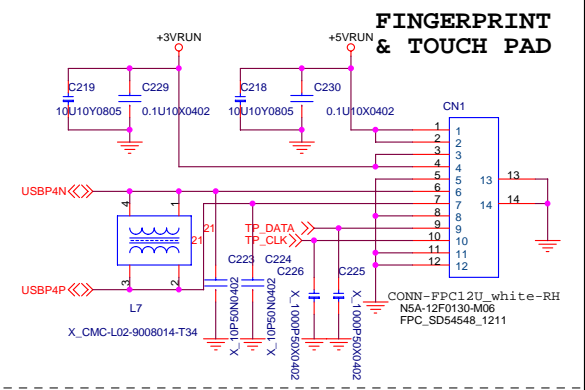
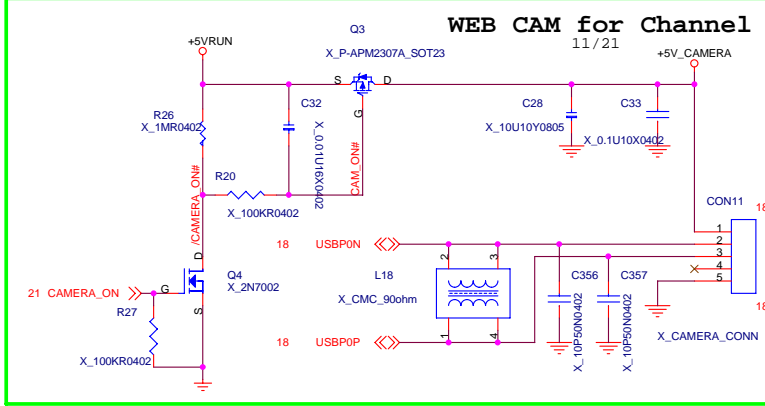
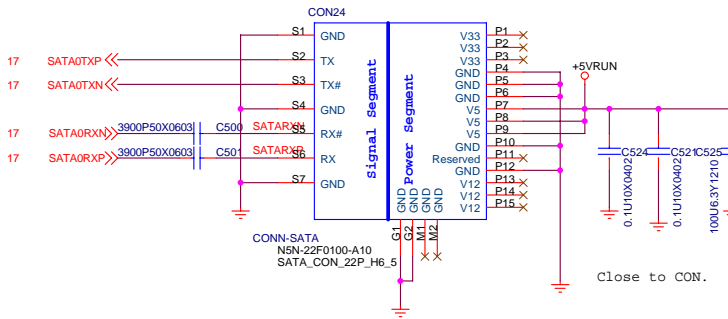
| MSI CORPORATION | | |
|---------------------------------------|------------------------------------|-----------|
| Title ICH8M-3 (SM BUS/GPIO) | | |
| Size Custom | Document Number MS-14211 | Rev 0A |
| Date: Monday, December 25, 2006 | Sheet 19 | of 49 |



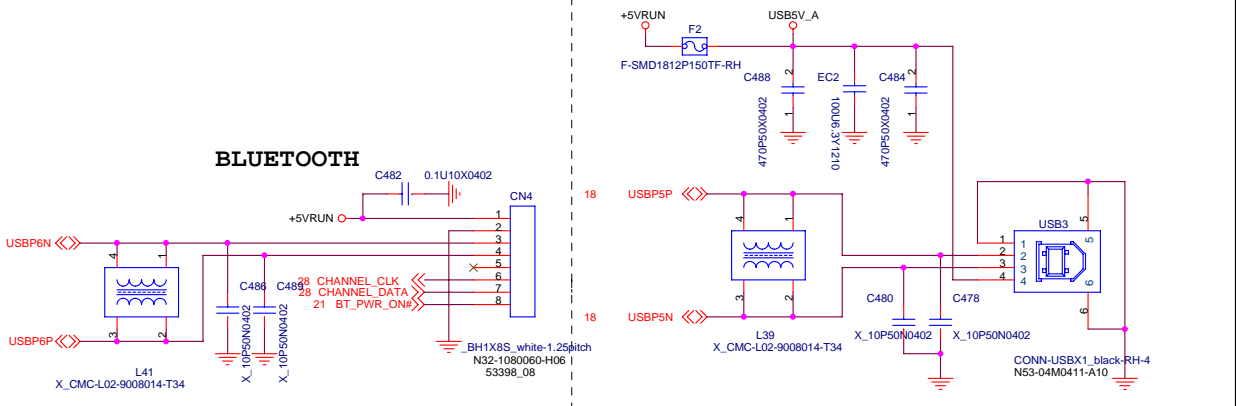
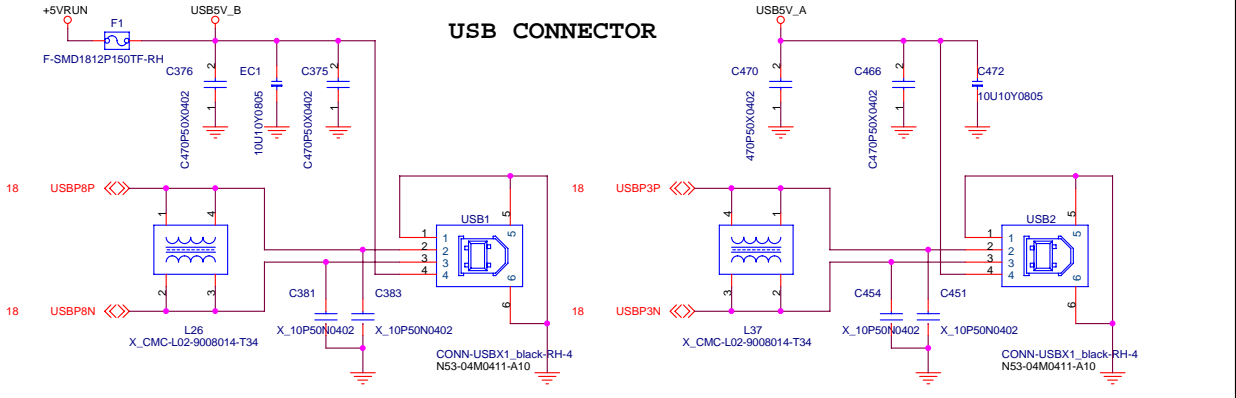
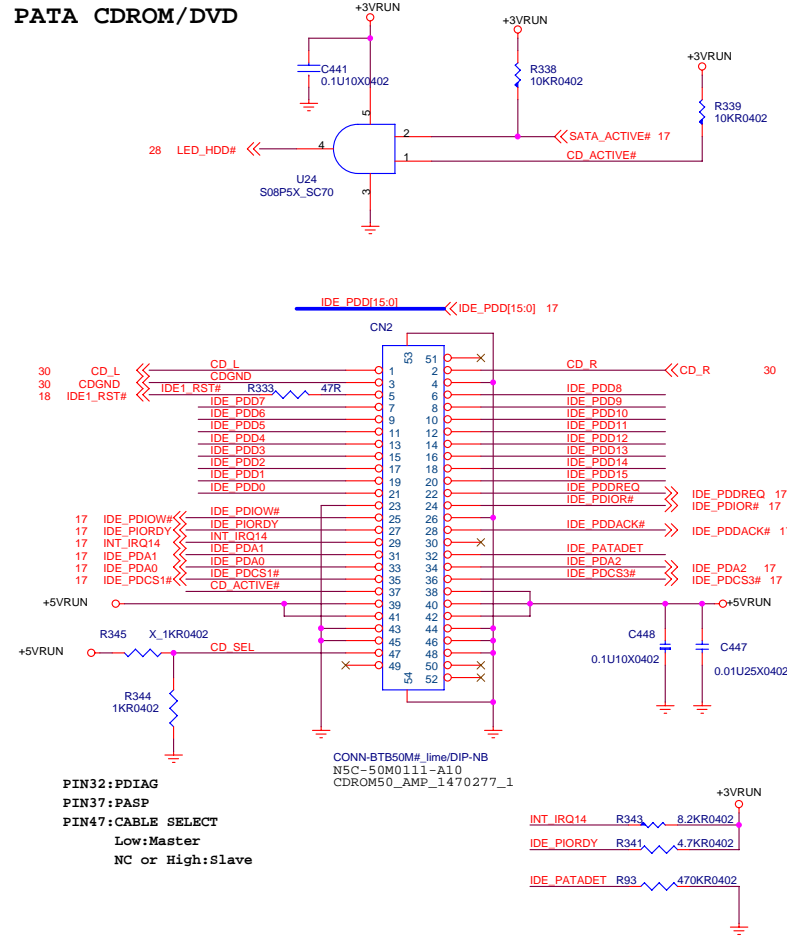
CLOSE TO CHIP

| | | | |
|------------------------|---------------------------|-------|----------|
| MSI CORPORATION | | | |
| File | KBC/EC/uP (ENE3925) | | |
| Size | Document Number | Rev | 0A |
| Custom | MS-14211 | | |
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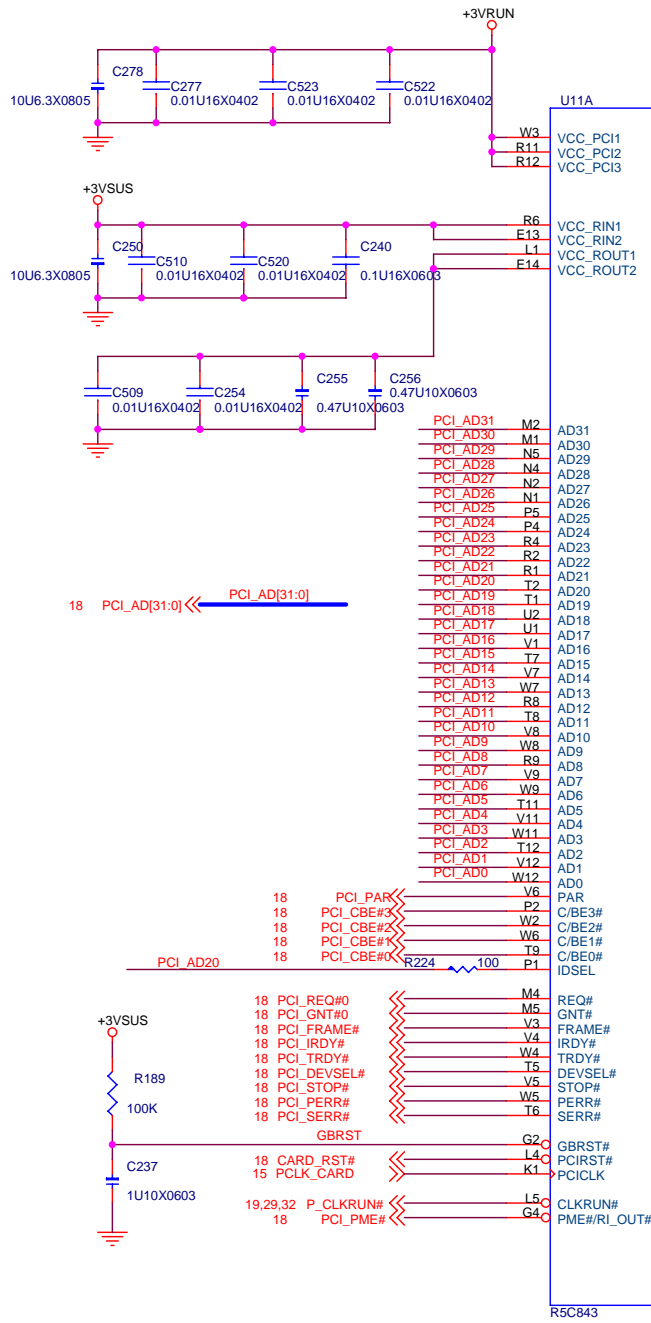
SATA HDD



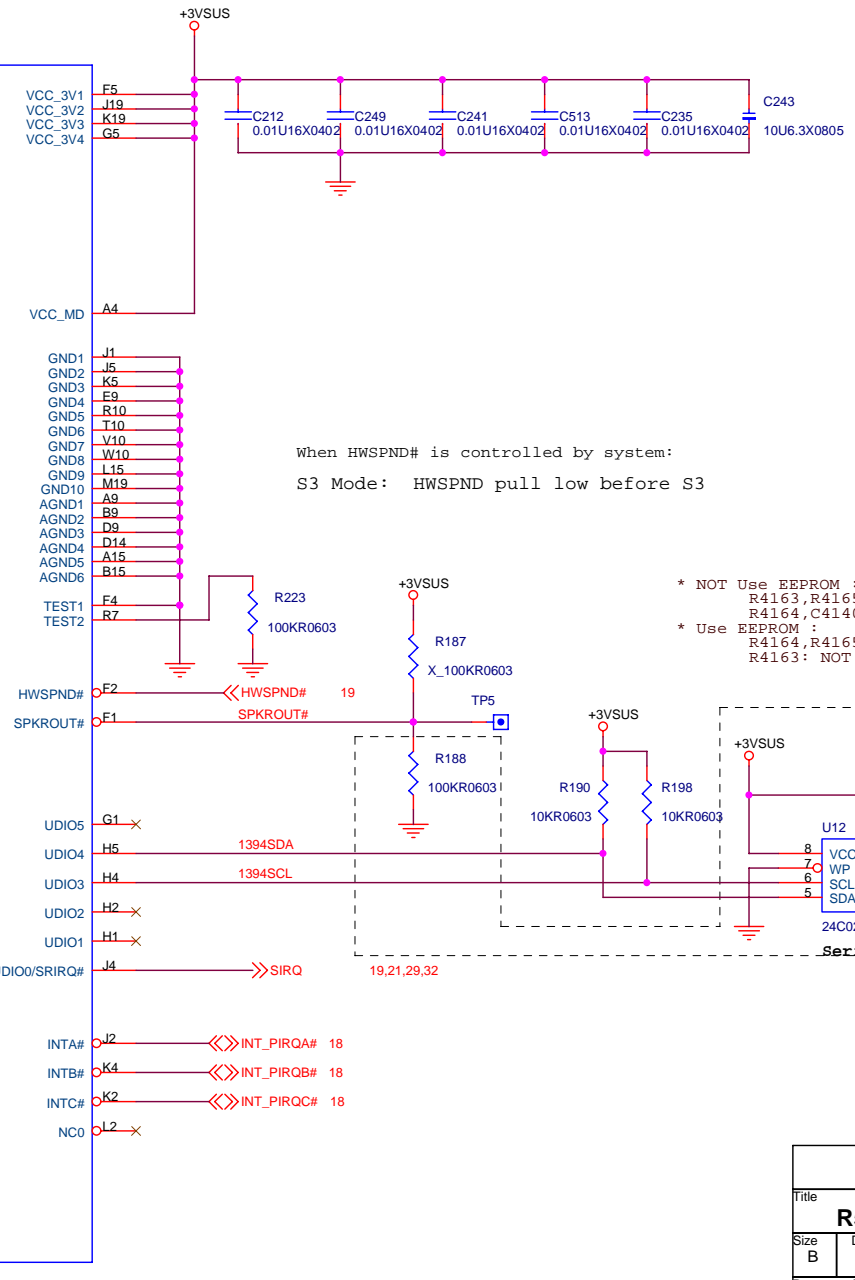
PATA CDRM/DVD



| | | |
|------------------------|--------------------------------------|----------------|
| MSI CORPORATION | | |
| Title | HDD,CDROM,BLUETOOTH,USB CONN. | |
| Size | Document Number | Rev |
| Custom | MS-14211 | 0A |
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PCI / OTHER

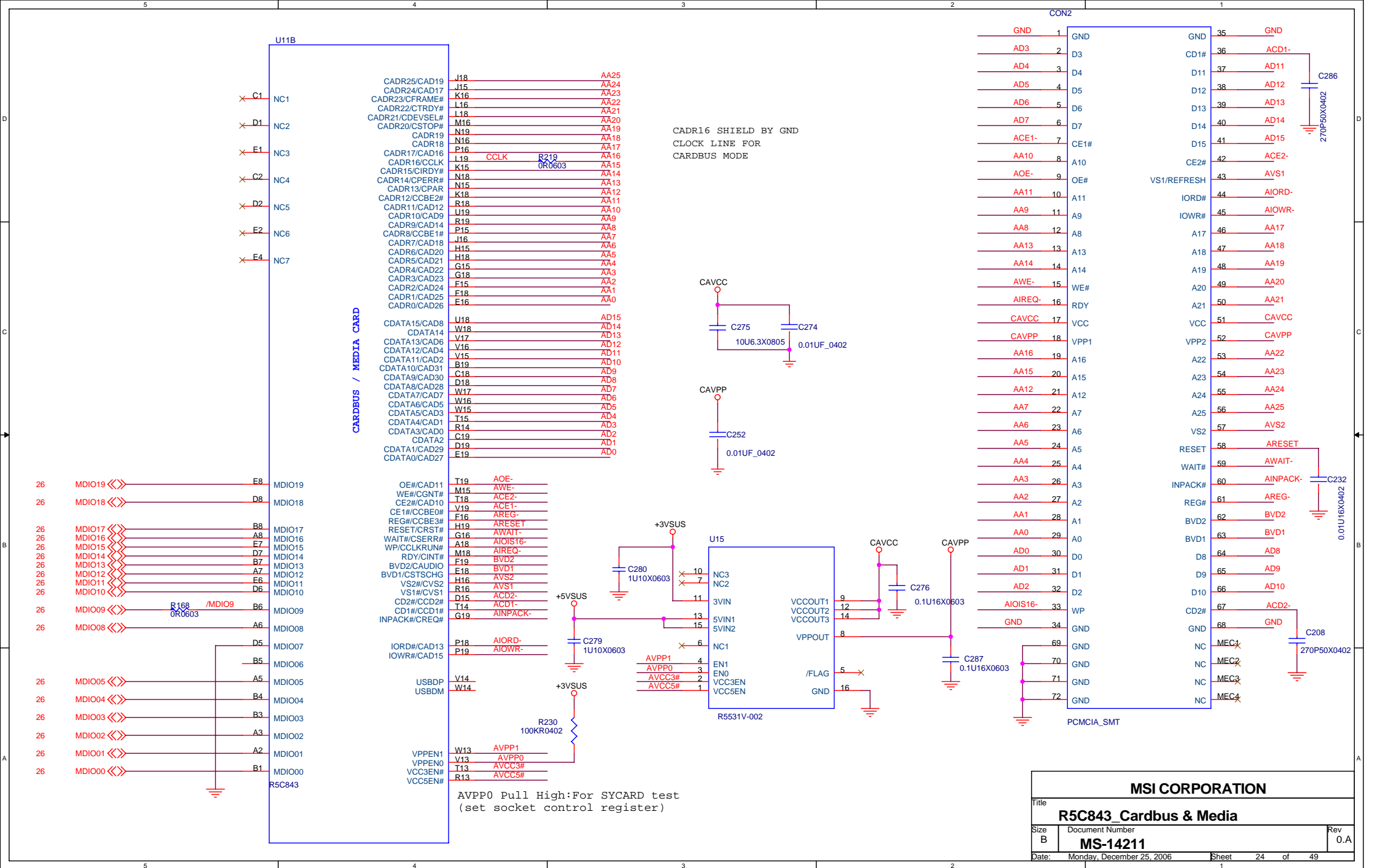


When HWSPND# is controlled by system:
S3 Mode: HWSPND pull low before S3

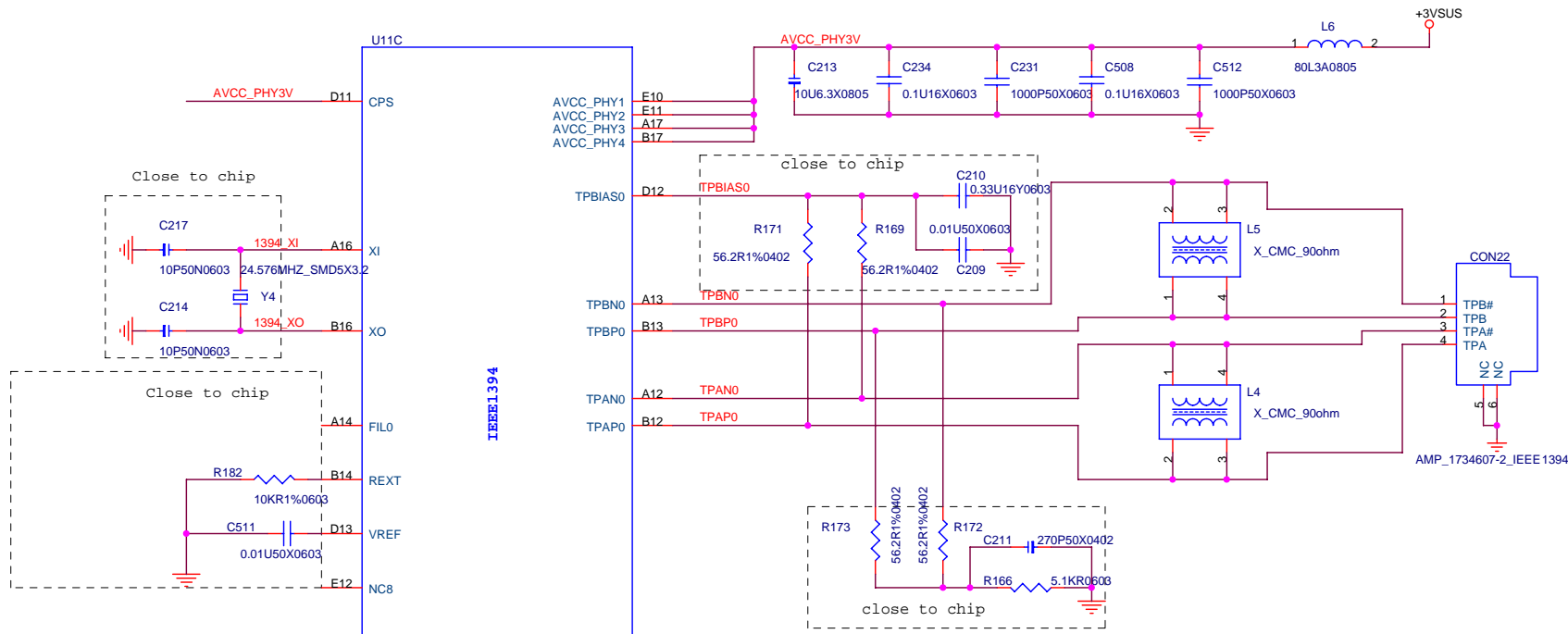
* NOT Use EEPROM :
R4163, R4165, R4166 : installed
R4164, C4140, U4019 : NOT installed

* Use EEPROM :
R4164, R4165, R4166, C4140, U4019 : installed
R4163: NOT installed

| | | |
|------------------------|---------------------------|----------------|
| MSI CORPORATION | | |
| Title | | |
| R5C843_PCI | | |
| Size | Document Number | Rev |
| B | MS-14211 | 0.A |
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| | | |
|--------------------------------------------------|------------------------------------|-------------------|
| MSI CORPORATION | | |
| Title R5C843_Carbus & Media | | |
| Size B | Document Number MS-14211 | Rev 0.A |
| Date: Monday, December 25, 2006 | Sheet 24 | of 49 |



*TPA/TPA#,TPB/TPB# pair trace : As close as possible.
 *TPA/TPA#,TPB/TPB# pair trace : Same length electrically.
 *Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).

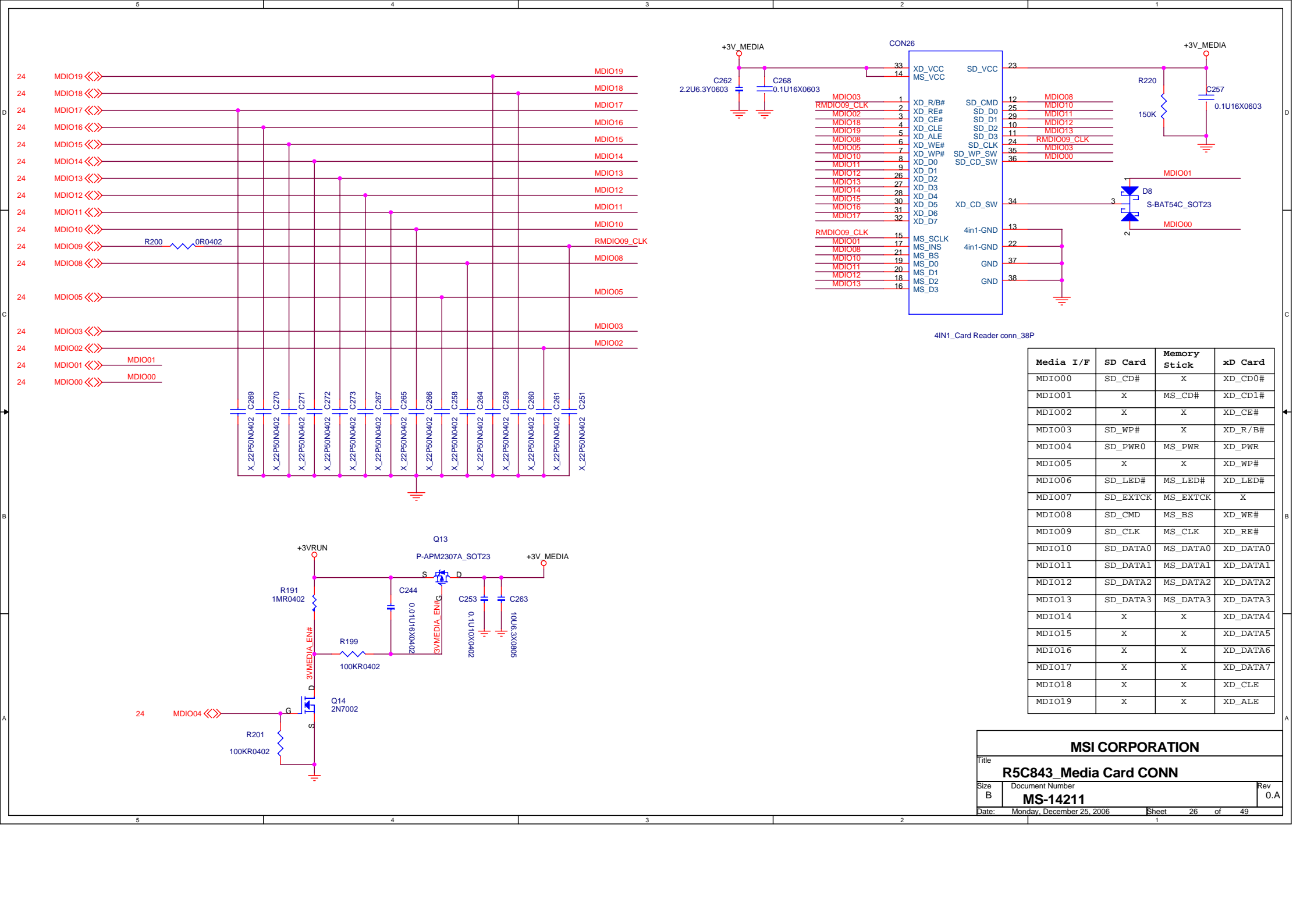
RICOH RECOMMEND ! (For TPAxx and TPBxx)

Please confirm whether or not signal meets these conditions.

- Layout these signals on top or bottom layer
- No via-hole for these signal lines
- Shield GND for TPAxx and TPBxx separately
- Impedance control required for TPAxx and TPBxx
- Use choke coils dedicated for IEEE1394

| | | |
|---------------------------------|---------------------------------|---------|
| MSI CORPORATION | | |
| Title R5C843_1394 | | |
| Size B | Document Number MS-14211 | Rev 0.A |
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R5C843



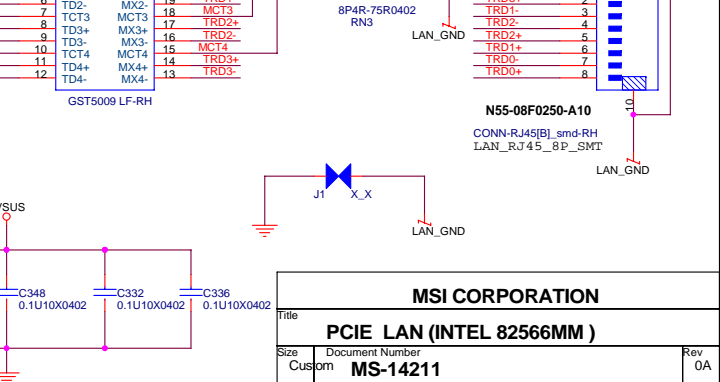
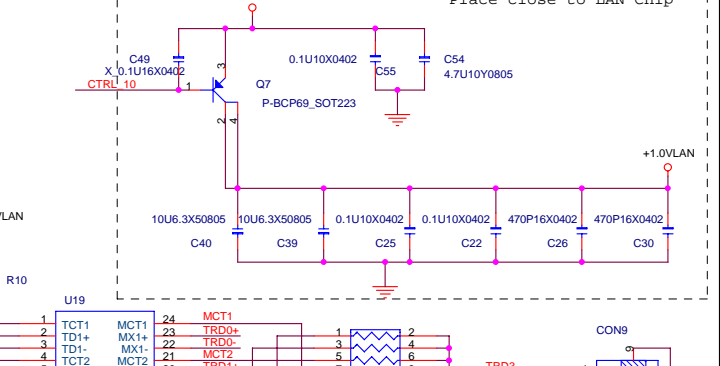
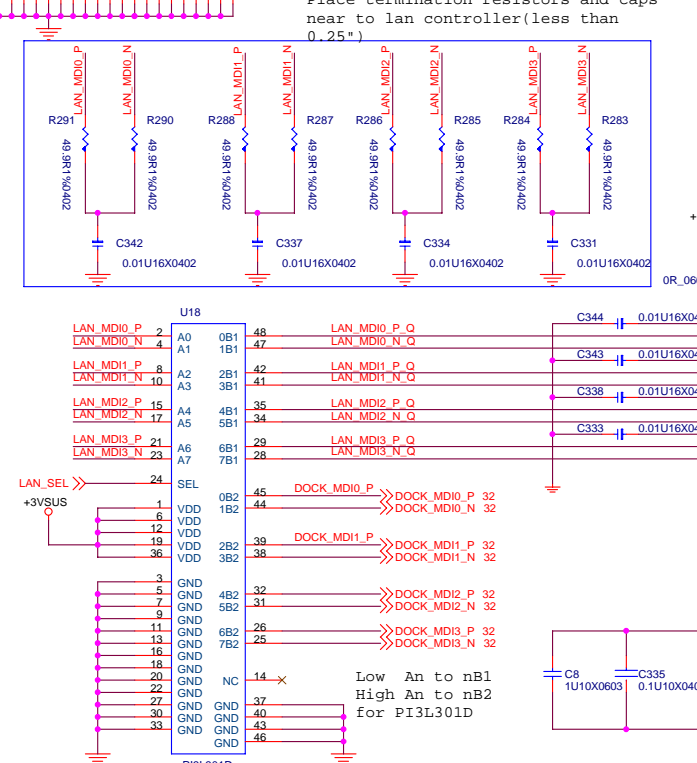
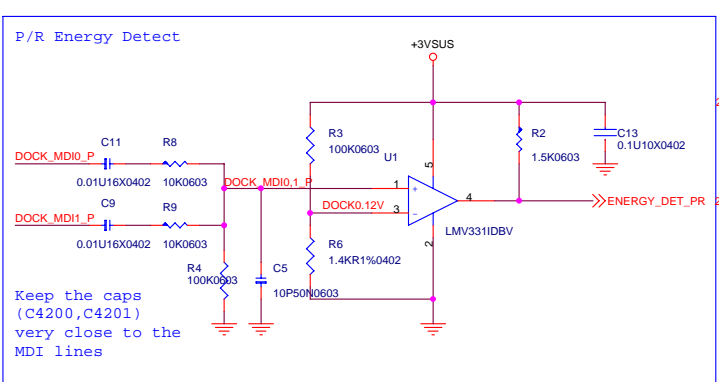
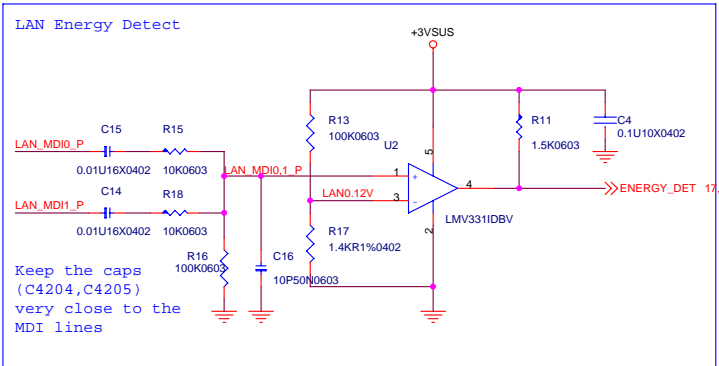
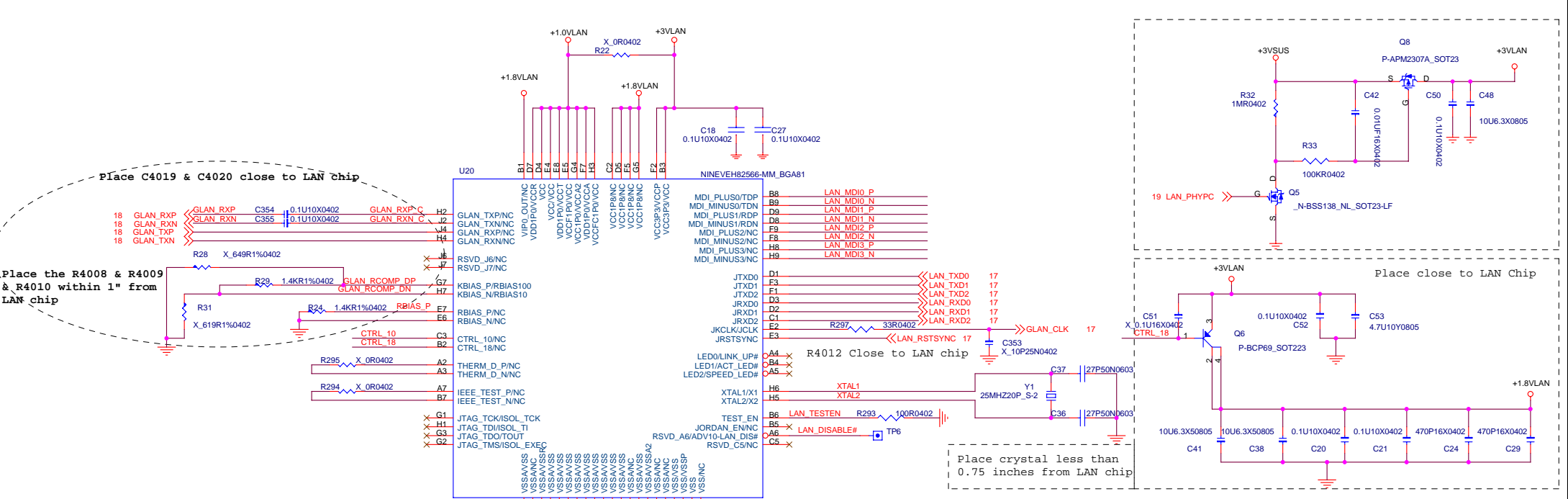
| Media I/F | SD Card | Memory Stick | xD Card |
|-----------|----------|--------------|----------|
| MDIO00 | SD_CD# | X | XD_CD0# |
| MDIO01 | X | MS_CD# | XD_CD1# |
| MDIO02 | X | X | XD_CE# |
| MDIO03 | SD_WP# | X | XD_R/B# |
| MDIO04 | SD_PWR0 | MS_PWR | XD_PWR |
| MDIO05 | X | X | XD_WP# |
| MDIO06 | SD_LED# | MS_LED# | XD_LED# |
| MDIO07 | SD_EXTCK | MS_EXTCK | X |
| MDIO08 | SD_CMD | MS_BS | XD_WE# |
| MDIO09 | SD_CLK | MS_CLK | XD_RE# |
| MDIO10 | SD_DATA0 | MS_DATA0 | XD_DATA0 |
| MDIO11 | SD_DATA1 | MS_DATA1 | XD_DATA1 |
| MDIO12 | SD_DATA2 | MS_DATA2 | XD_DATA2 |
| MDIO13 | SD_DATA3 | MS_DATA3 | XD_DATA3 |
| MDIO14 | X | X | XD_DATA4 |
| MDIO15 | X | X | XD_DATA5 |
| MDIO16 | X | X | XD_DATA6 |
| MDIO17 | X | X | XD_DATA7 |
| MDIO18 | X | X | XD_CLE |
| MDIO19 | X | X | XD_ALE |

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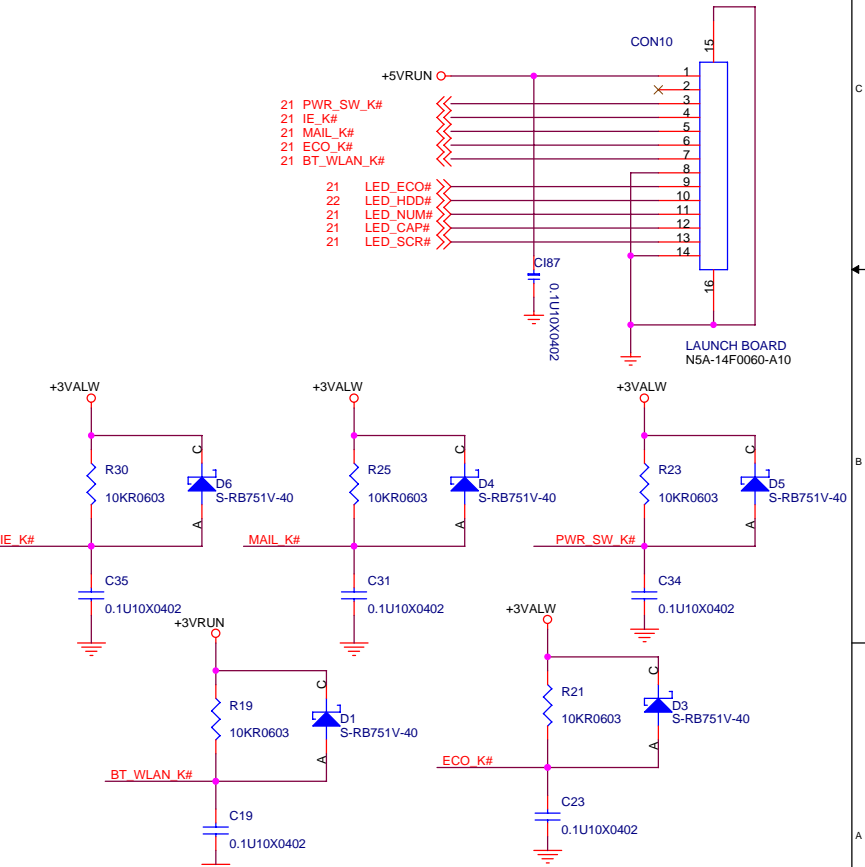
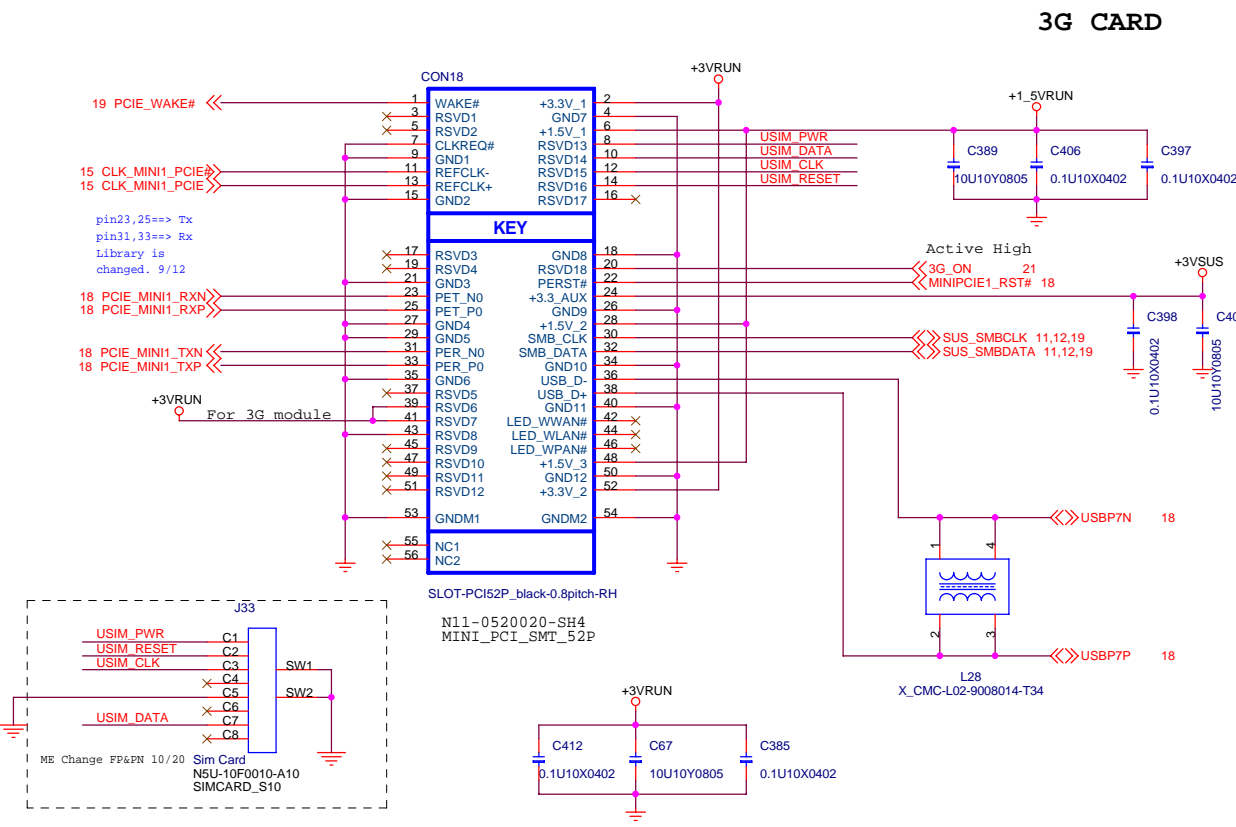
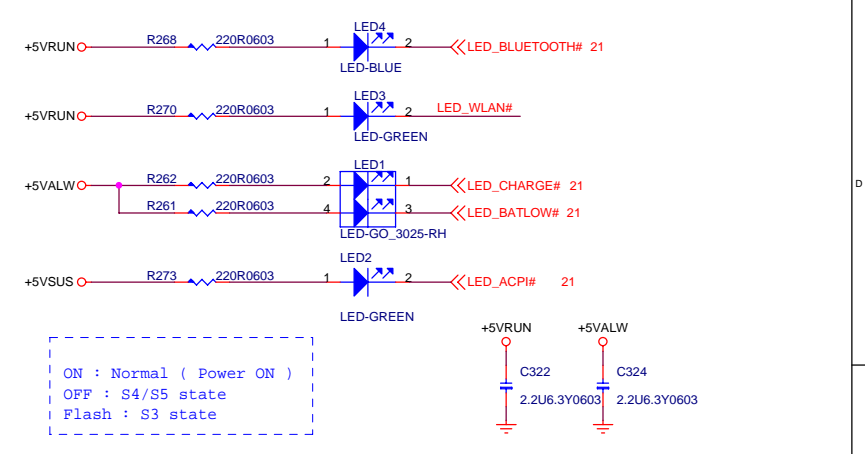
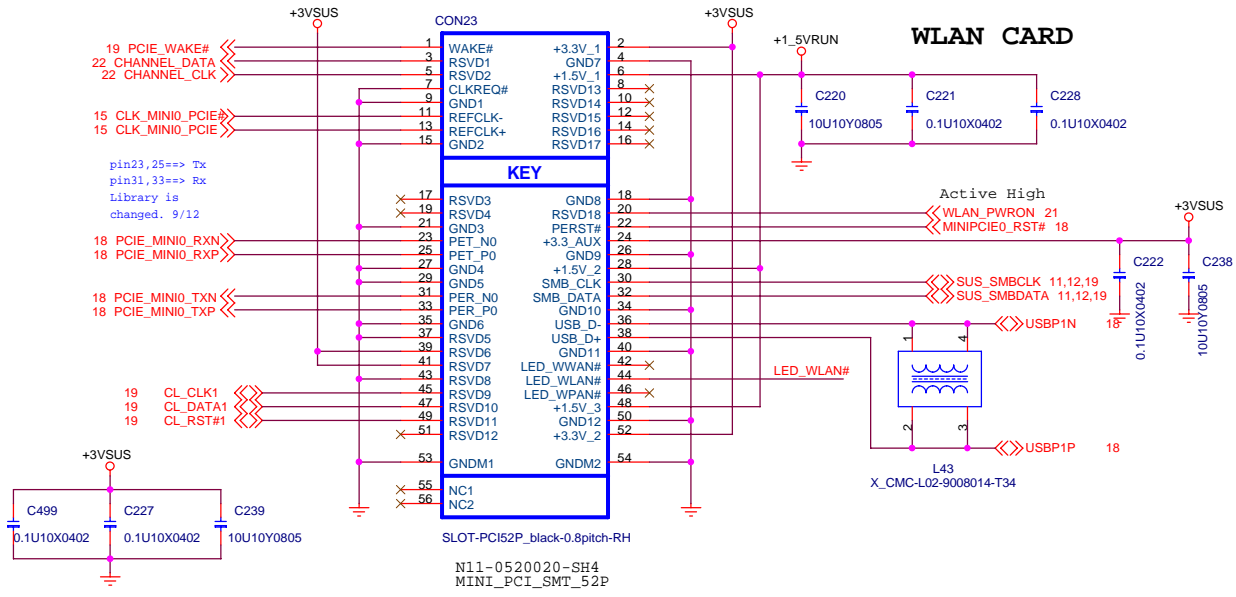
Title: **R5C843 Media Card CONN**

| | | |
|--------|------------------------------------|------------|
| Size B | Document Number MS-14211 | Rev 0.A |
|--------|------------------------------------|------------|

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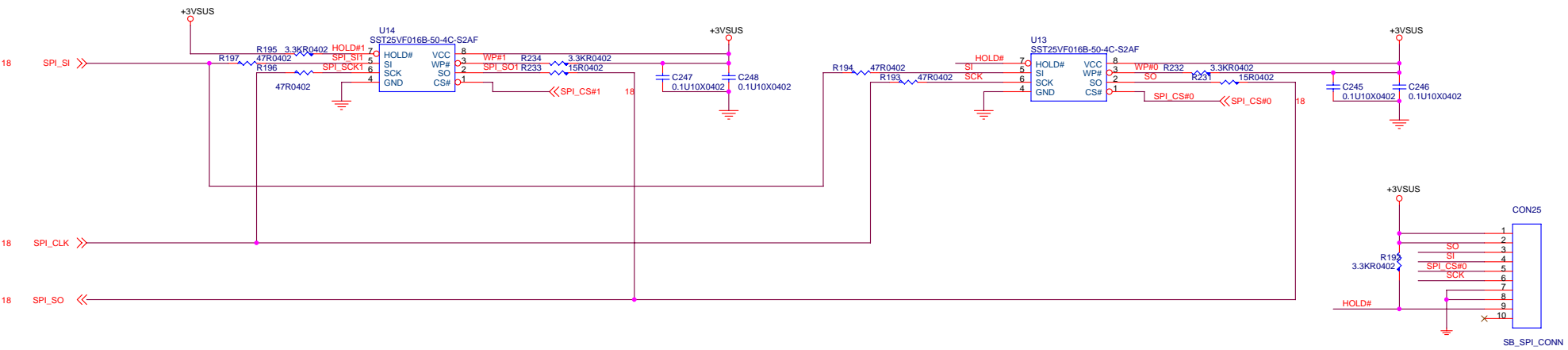


| | | |
|---------------------------------|-----------------|-----|
| MSI CORPORATION | | |
| PCIE LAN (INTEL 82566MM) | | |
| Document Number | MS-14211 | Rev |
| Size | Custom | 0A |
| Date: Monday, December 25, 2006 | Sheet 27 of 49 | |

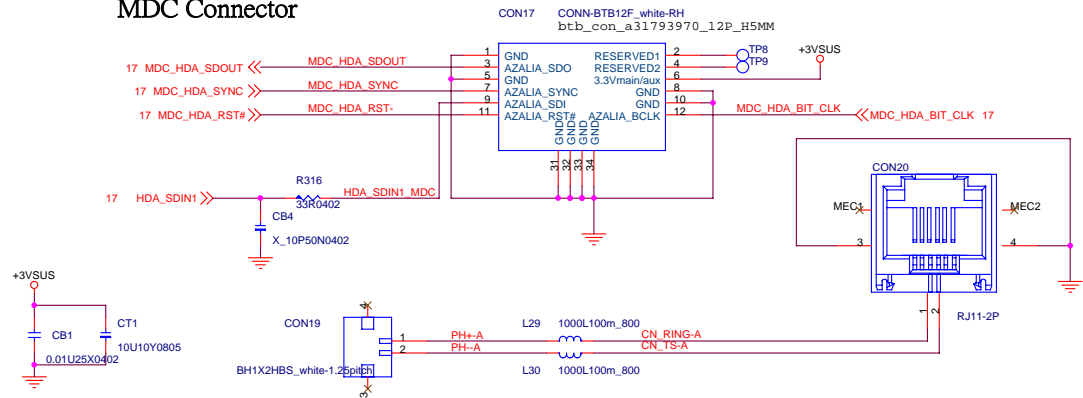


| | | |
|---------------------------------|---------------------------|----------------|
| MSI CORPORATION | | |
| Title MINI_PCIE, LED, SW | | |
| Size | Document Number | Rev |
| Custom | MS-14211 | 0A |
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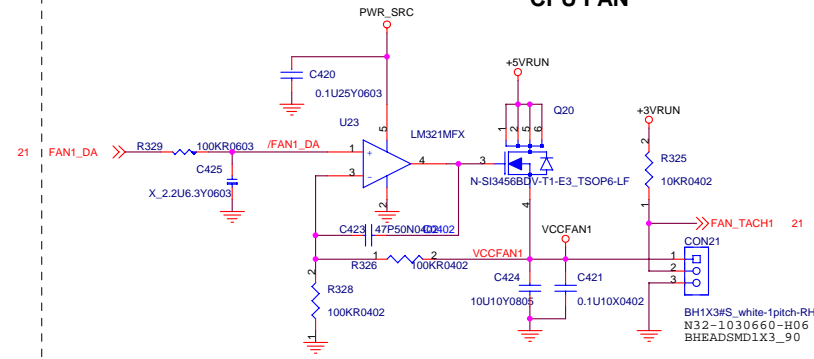
SPI FLASH(16M)



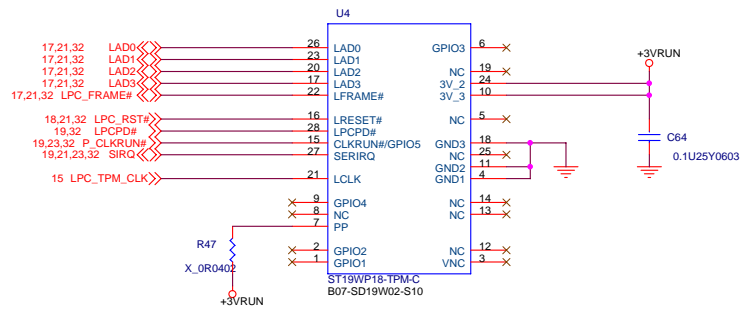
MDC Connector



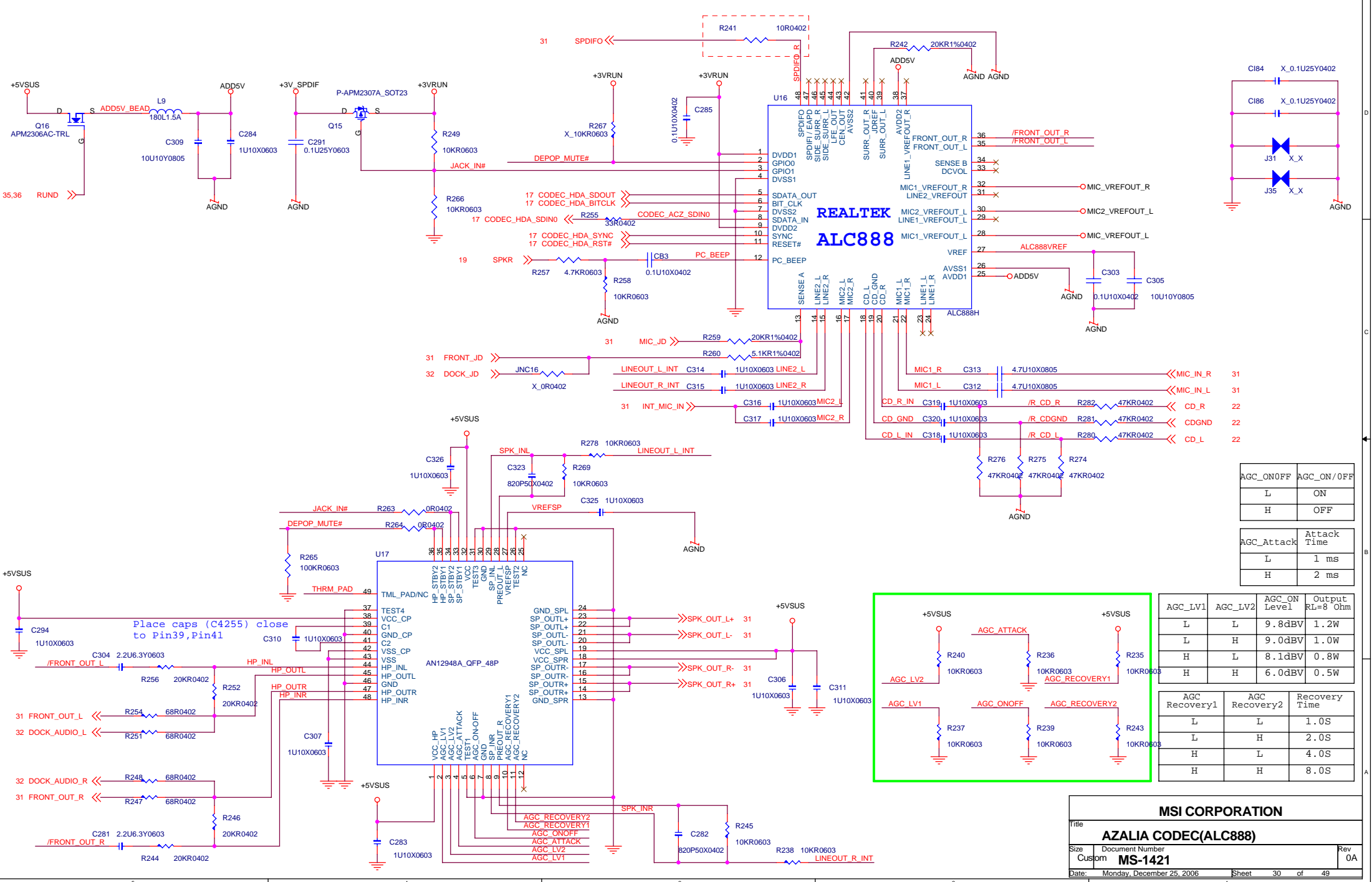
CPU FAN



TPM 1.2



| MSI CORPORATION | | |
|-----------------|------------------------------|----------------|
| Title | MDC, TPM, FAN, SPI FLASH ROM | |
| Size | Document Number | Rev |
| Custom | MS-1421 | 0A |
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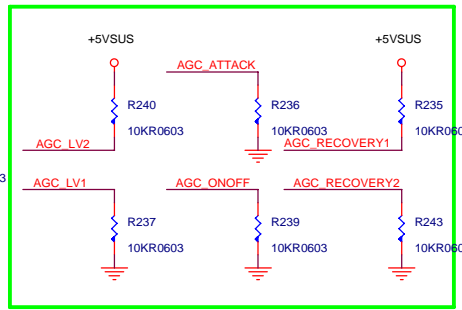


| | |
|-----------|------------|
| AGC_ON0FF | AGC_ON/0FF |
| L | ON |
| H | OFF |

| | |
|------------|-------------|
| AGC_Attack | Attack Time |
| L | 1 ms |
| H | 2 ms |

| | | | |
|---------|---------|--------------|-----------------|
| AGC_LV1 | AGC_LV2 | AGC_ON Level | Output RL=8 Ohm |
| L | L | 9.8dBV | 1.2W |
| L | H | 9.0dBV | 1.0W |
| H | L | 8.1dBV | 0.8W |
| H | H | 6.0dBV | 0.5W |

| | | |
|---------------|---------------|---------------|
| AGC Recovery1 | AGC Recovery2 | Recovery Time |
| L | L | 1.0S |
| L | H | 2.0S |
| H | L | 4.0S |
| H | H | 8.0S |

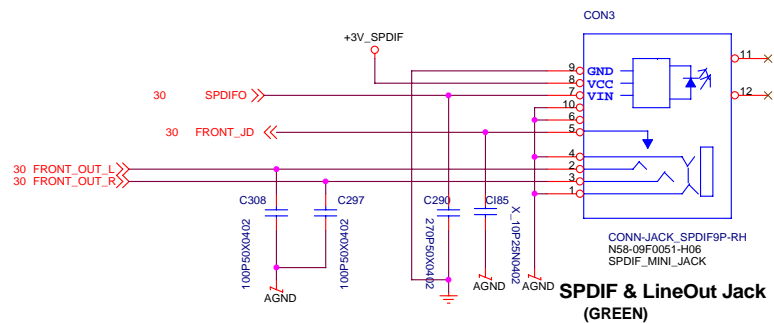
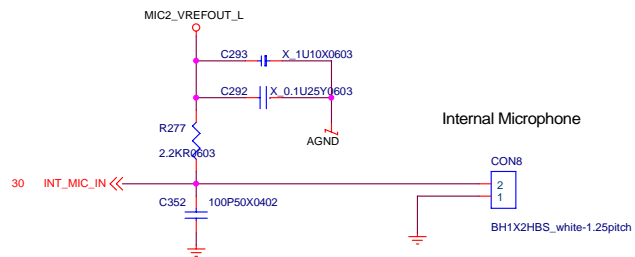
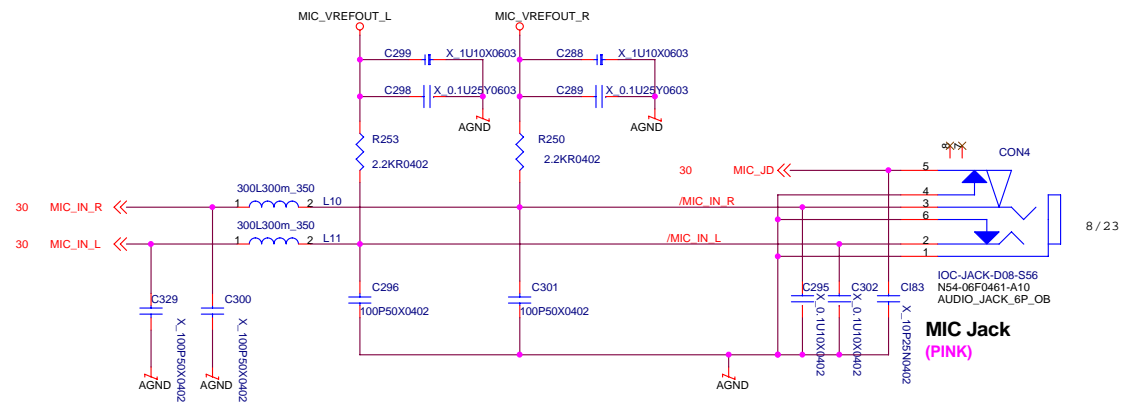
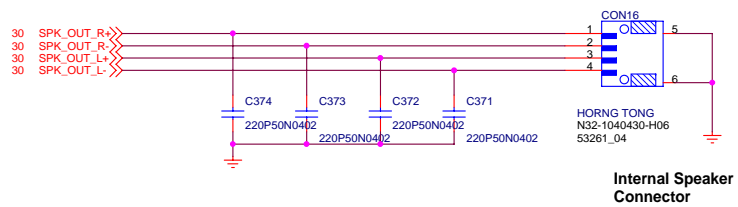


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Title AZALIA CODEC(ALC888)

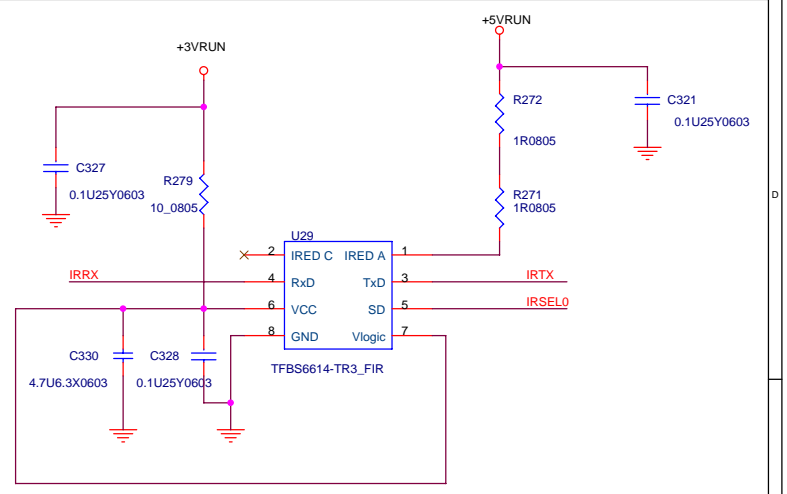
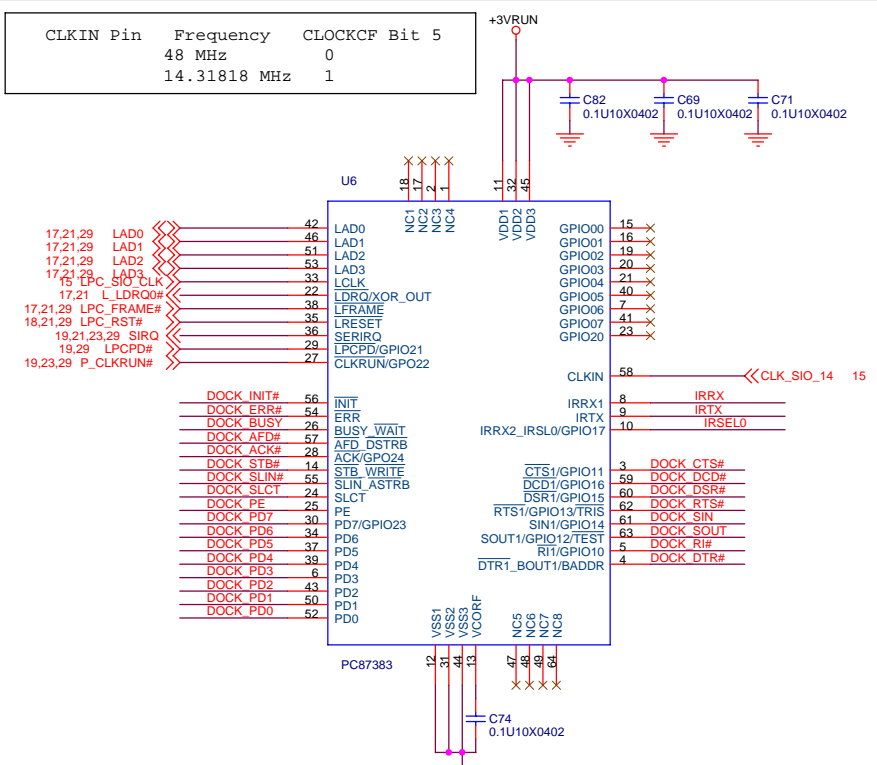
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|--------|-----------------|-----|
| Size | Document Number | Rev |
| Custom | MS-1421 | 0A |

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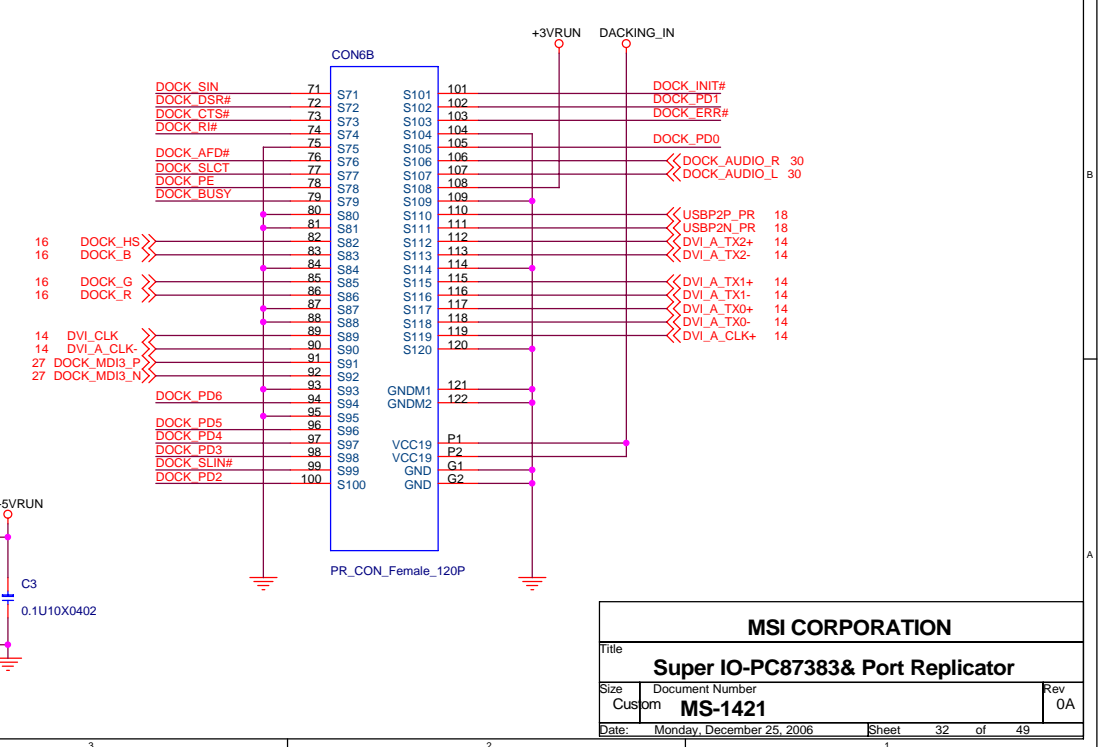
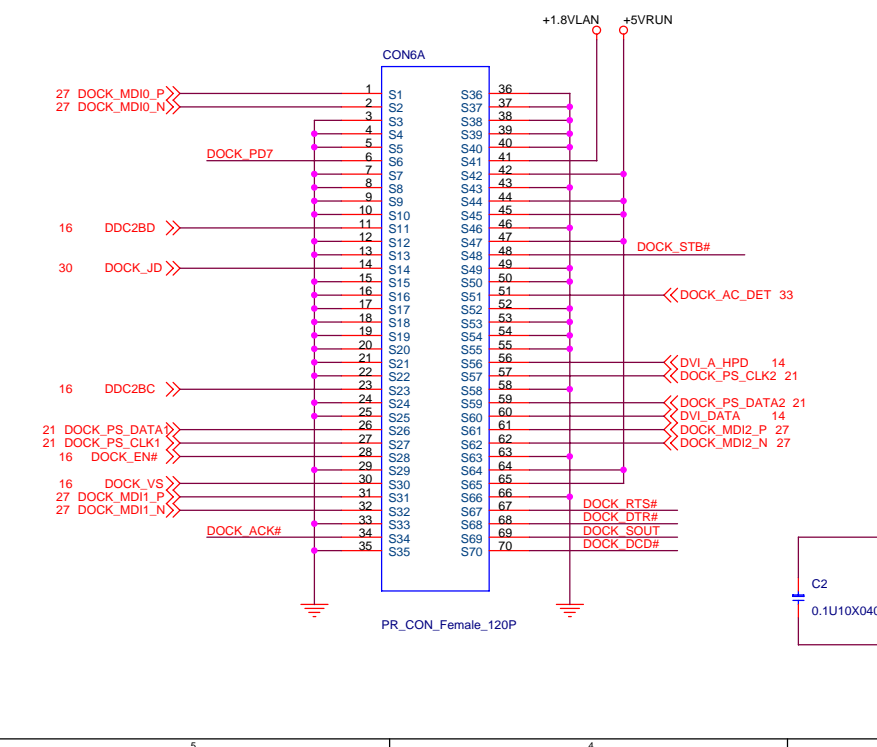


| | | |
|-------------------------------------|---------------------------|----------------|
| MSI CORPORATION | | |
| Title Audio Amp. & Jacks | | |
| Size | Document Number | Rev |
| Custom | MS-1421 | 0A |
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| | | | |
|-----------|--------------|---------|-------|
| CLKIN Pin | Frequency | CLOCKCF | Bit 5 |
| | 48 MHz | 0 | |
| | 14.31818 MHz | 1 | |



| BADDR Strapping Options | | |
|-------------------------|----------------|---------------|
| BADDR | I/O Address | |
| | Index Register | Data Register |
| 0 | 2Eh | 2Fh |
| 1 (default) | 164Eh | 164Fh |

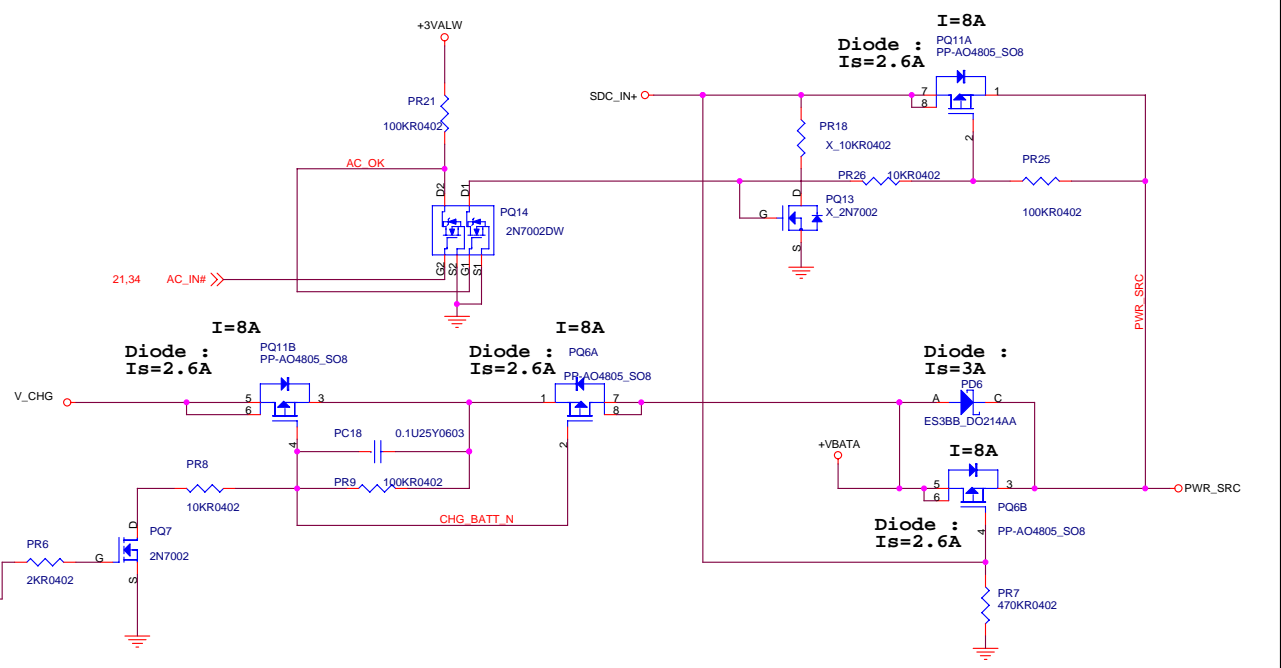
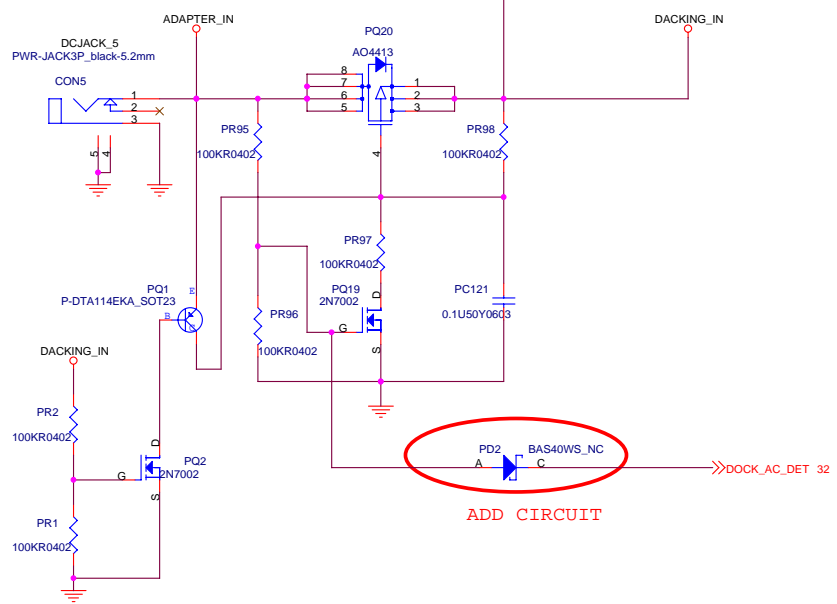
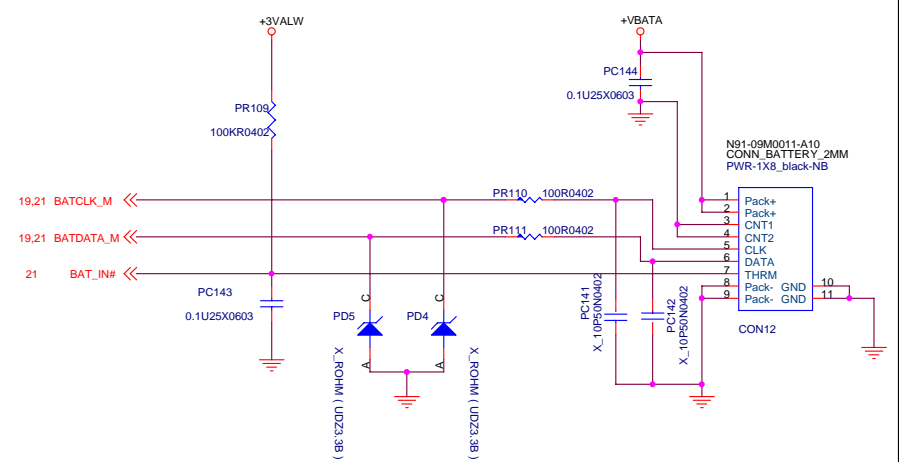
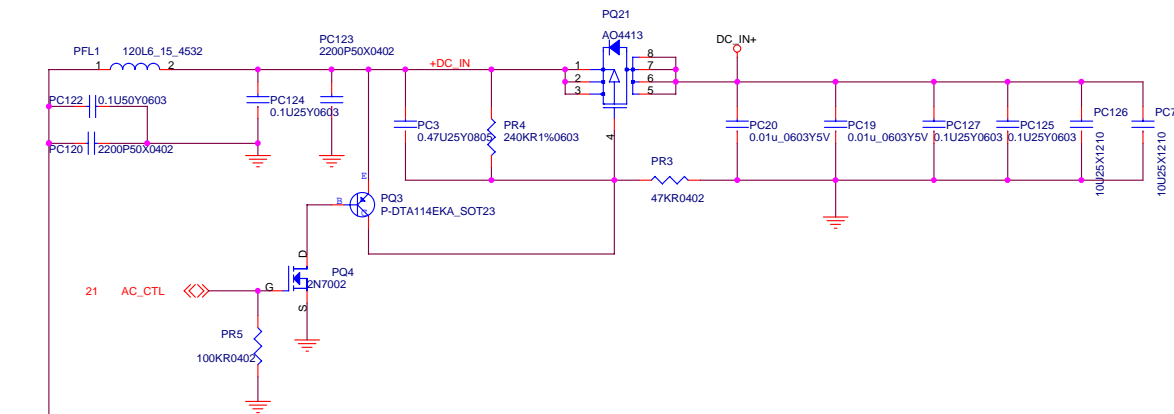


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Title: **Super IO-PC87383& Port Replicator**

| | | |
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| Size | Document Number | Rev |
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| | | |
|------------------------|---------------------------|----------------|
| MSI CORPORATION | | |
| Title | Battery Select | |
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Adapter= 90 W
 Adapter input voltage set 17.4 Voltage
 $2.048/7.15 * (53.6 + 7.15) = 17.4V$

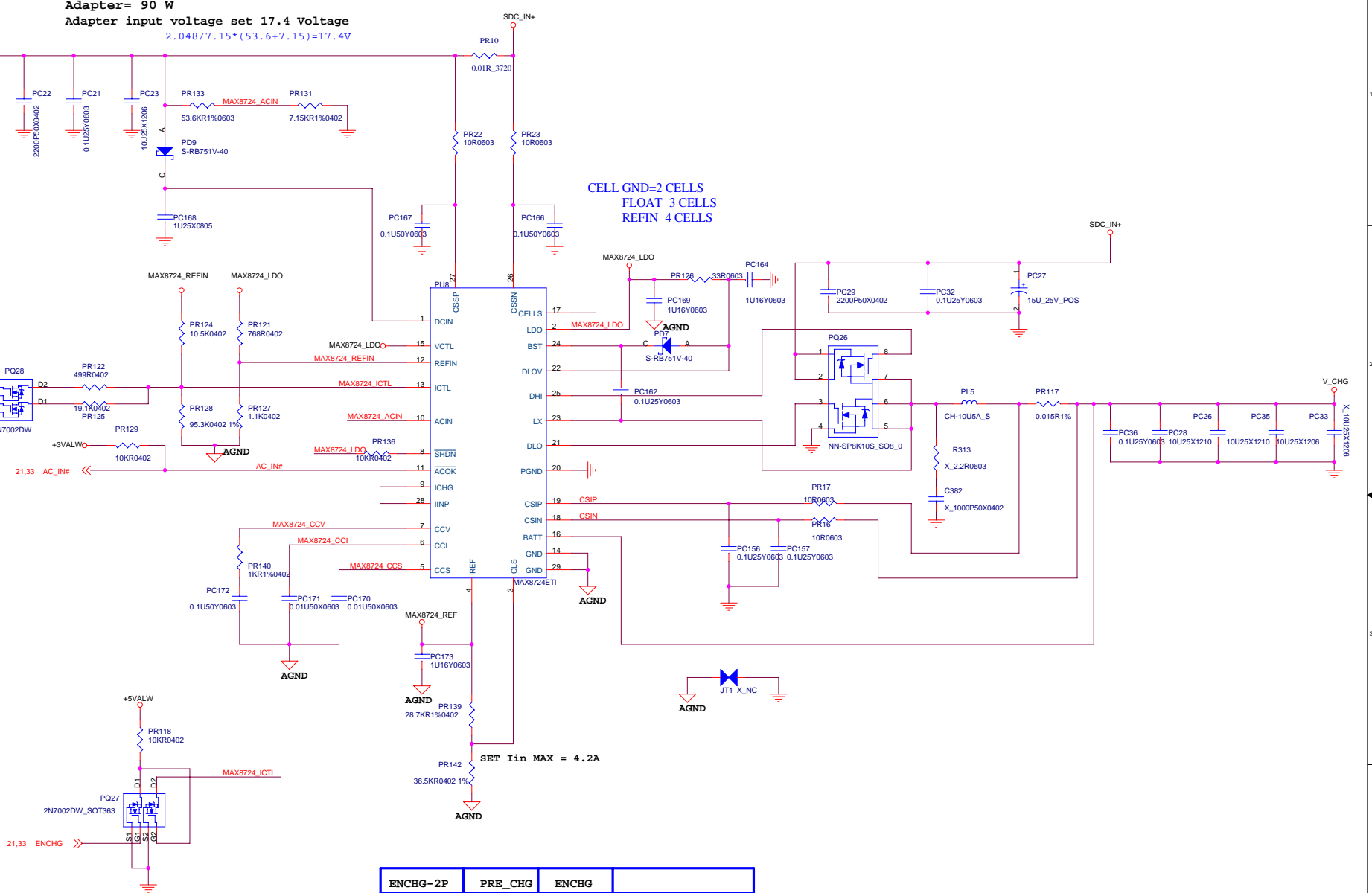
CELL GND=2 CELLS
 FLOAT=3 CELLS
 REFIN=4 CELLS

| ENCHG-2P | PRE_CHG | ENCHG | |
|----------|---------|-------|------------------|
| 0 | 1 | 1 | Pre-charge |
| 1 | 0 | 1 | 3S2P-Fast charge |
| 0 | 0 | 1 | 3S3P-Fast charge |
| 0 | 0 | 0 | STOP CHARGE |

| | | |
|------------------------------|---------------------------|----------------|
| MSI CORPORATION | | |
| Title Battery Charger | | |
| Size | Document Number | Rev |
| Custom | MS-1412 | 0A |
| Date: | Monday, December 25, 2006 | Sheet 34 of 49 |

3S2P: Charge current set 3 Amp
 3S3P: Charge current set 4.5 Amp
 Pre-charger: Charge current set 220mA

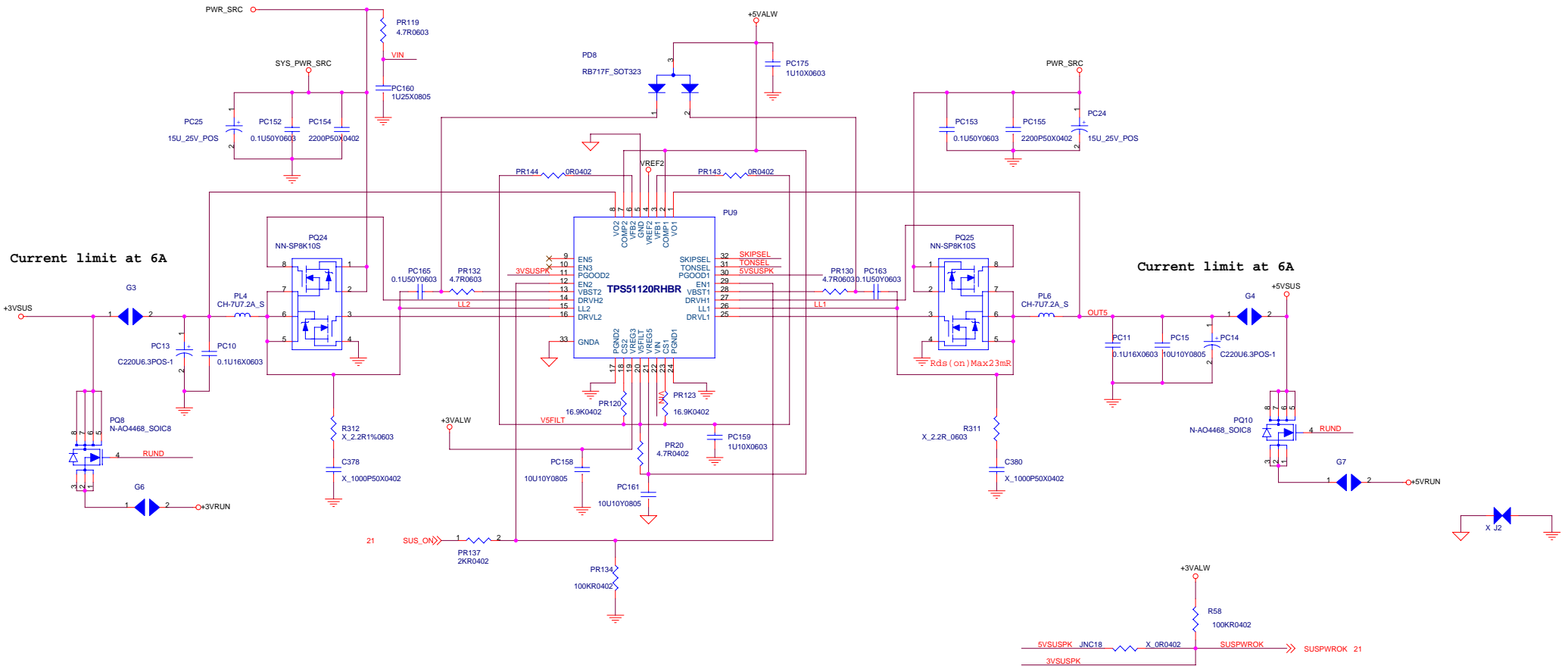
21 PRE_CHG
 21 ENCHG_2P



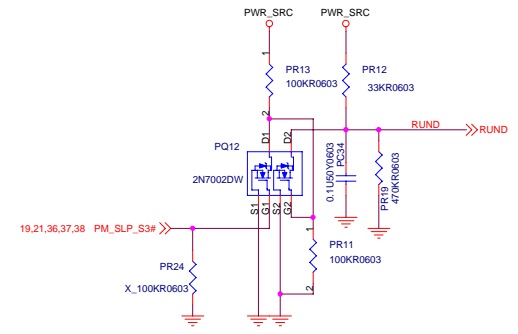
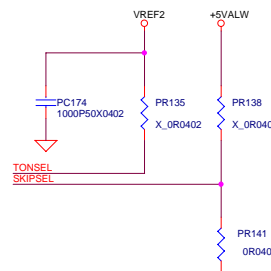
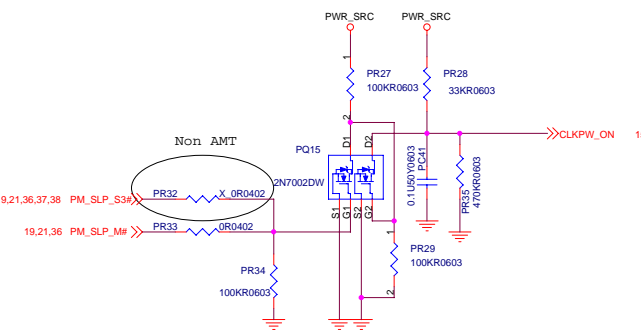
SET Iin MAX = 4.2A

Current limit at 6A

Current limit at 6A



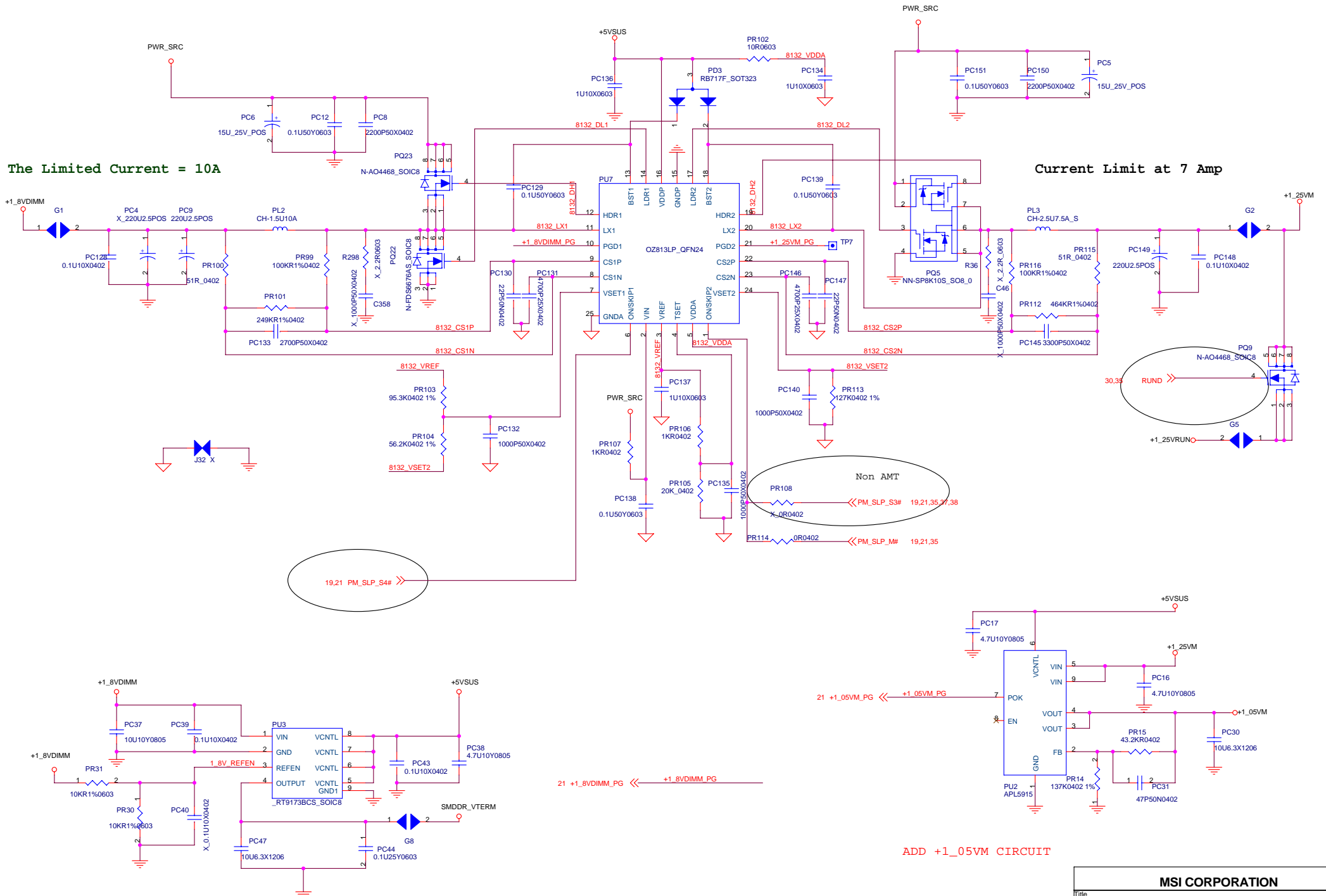
Non AMT
 19.21,36,37,38 PM_SLP_S3#
 19.21,36 PM_SLP_M#



| | | |
|--------------------------|---------------------------|----------------|
| MSI CORPORATION | | |
| Title | | |
| SYSTEM POWER 3/5V | | |
| Size | Document Number | Rev |
| Custom | MS-1412 | 0A |
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The Limited Current = 10A

Current Limit at 7 Amp

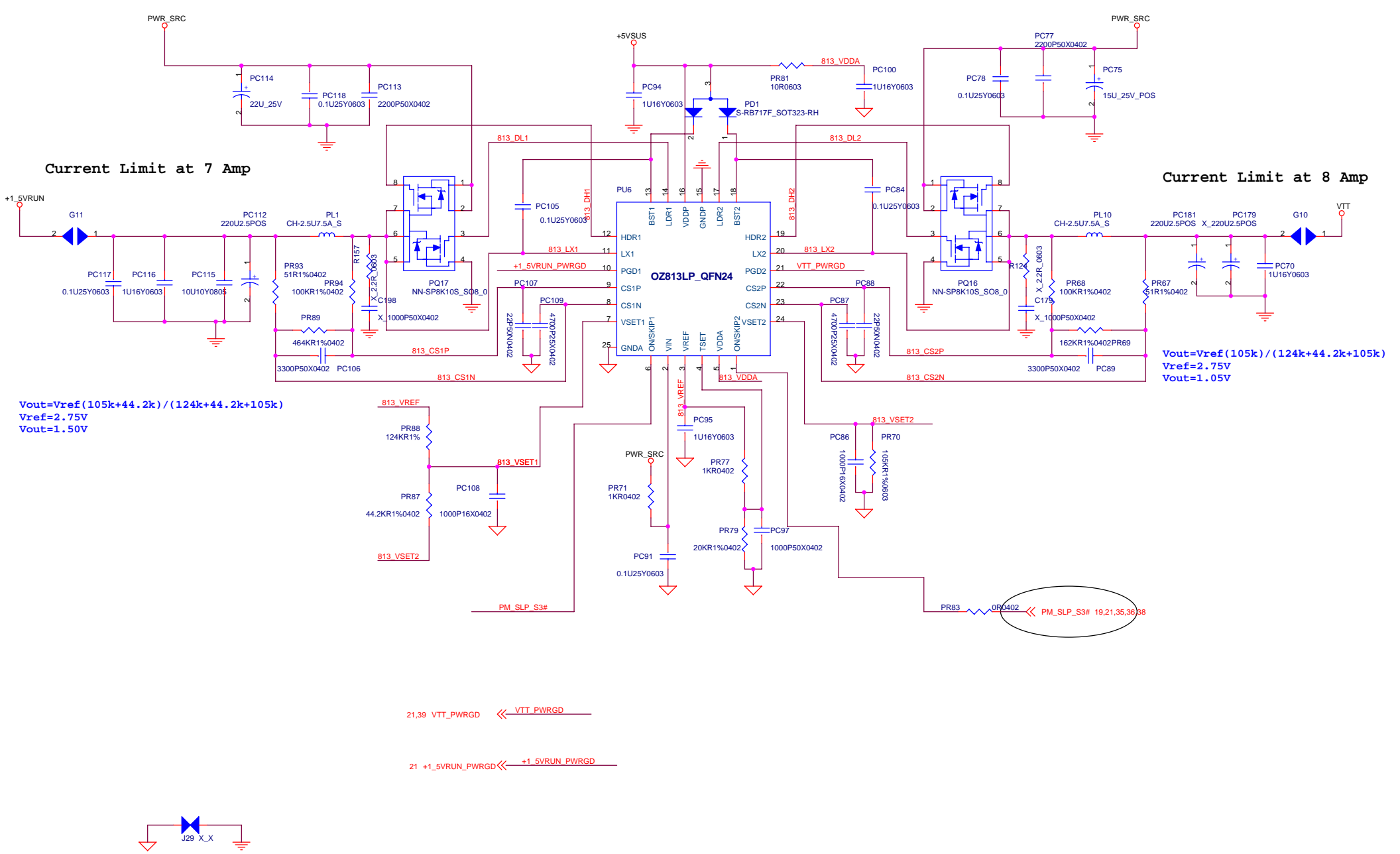


19,21 PM_SLP_S4#

Non AMT
PR108 1000P50X0402 << PM_SLP_S3# 19,21,35,37,38
X_0R0402
PR114 0R0402 << PM_SLP_M# 19,21,35

ADD +1_05VM CIRCUIT

| | | |
|------------------------|-------------------------------|----------------|
| MSI CORPORATION | | |
| Title | DDR2 RAM POWER, +1.25V | |
| Size | Document Number | Rev |
| Cusom | MS-1421 | 0A |
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Current Limit at 7 Amp

Current Limit at 8 Amp

$$V_{out} = \frac{V_{ref}(105k + 44.2k)}{(124k + 44.2k + 105k)}$$

$$V_{ref} = 2.75V$$

$$V_{out} = 1.50V$$

$$V_{out} = \frac{V_{ref}(105k)}{(124k + 44.2k + 105k)}$$

$$V_{ref} = 2.75V$$

$$V_{out} = 1.05V$$

21,39 VTT_PWRGD << VTT_PWRGD

21 +1_5VRUN_PWRGD << +1_5VRUN_PWRGD

PR83 0R0402 << PM_SLP_S3# 19,21,35,36,38

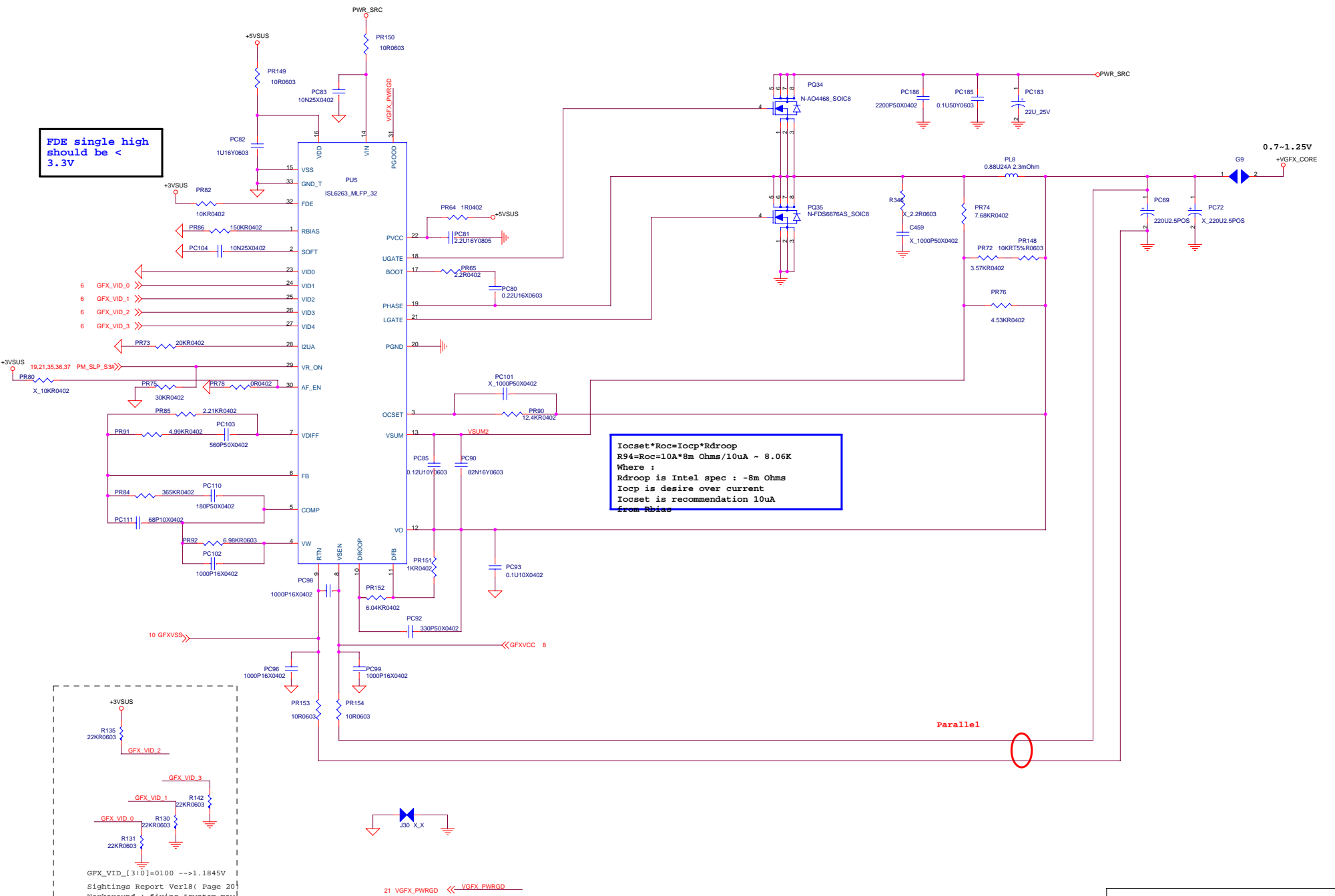
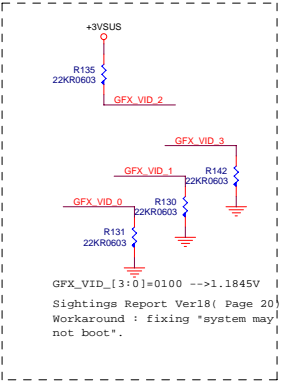


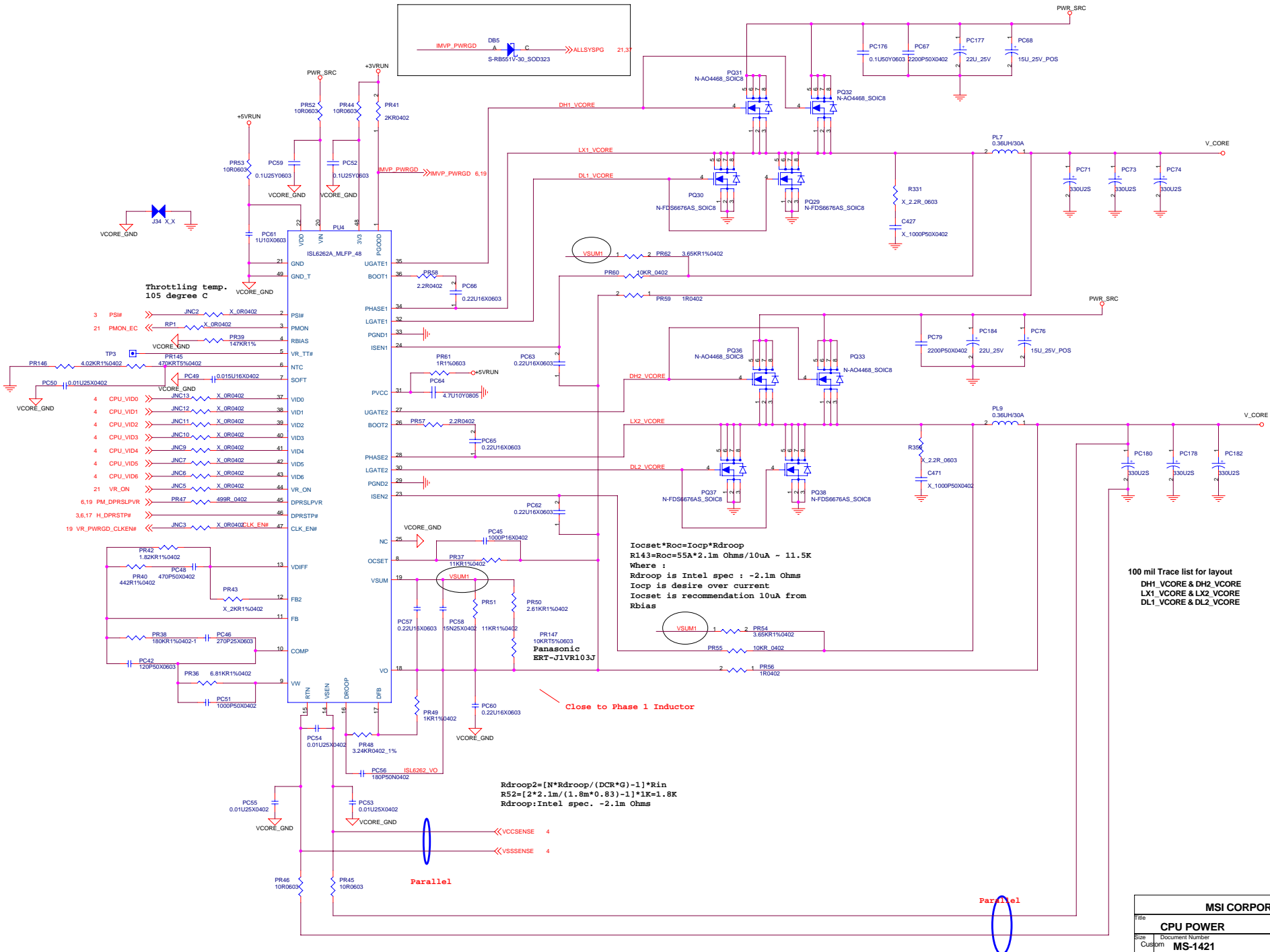
| | | | |
|-----------------------------|---------------------------|-------|----------|
| MSI CORPORATION | | | |
| Title | | | |
| +1_5VRUN , VTT POWER | | | |
| Size | Document Number | Rev | |
| Custom | MS-1421 | 0A | |
| Date: | Monday, December 25, 2006 | Sheet | 37 of 49 |

FDE single high should be < 3.3V

$I_{ocset} * R_{oc} = I_{ocp} * R_{droop}$
 $R_{94} = R_{oc} = 10A * 8m\ Ohms / 10uA \sim 8.06K$
 Where :
 Rdroop is Intel spec : -8m Ohms
 Iocp is desire over current
 Iocset is recommendation 10uA
 from Rbias

Parallel





Throttling temp.
105 degree C

- 3 PSIF JNC2 X_0R0402 2 PSIF
- 21 PMON_EC RP1 X_0R0402 3 PMON
- VCORE_GND PR39 147KR1% 4 RBIAS
- 5 VR_TT# PR145 470KRTS%0402 5 VR_TT#
- 6 NTC PR146 4.02KR1%0402 6 NTC
- 7 SOFT PC49 0.015U16X0402 7 SOFT
- 4 CPU_VID0 JNC13 X_0R0402 37 VID0
- 4 CPU_VID1 JNC12 X_0R0402 38 VID1
- 4 CPU_VID2 JNC11 X_0R0402 39 VID2
- 4 CPU_VID3 JNC10 X_0R0402 40 VID3
- 4 CPU_VID4 JNC9 X_0R0402 41 VID4
- 4 CPU_VID5 JNC7 X_0R0402 42 VID5
- 4 CPU_VID6 JNC6 X_0R0402 43 VID6
- 21 VR_ON JNC5 X_0R0402 44 VR_ON
- 6.19 PM_DPRSLPVR PR47 499R_0402 45 DPRSLPVR
- 3.6,17 H_DPRSTP# PR48 3.24KR0402_1% 46 DPRSTP#
- 19 VR_PWRGD_CLKEN# JNC3 X_0R0402CLK_EN# 47 CLK_EN#

$I_{ocset} * R_{oc} = I_{ocp} * R_{droop}$
 $R_{143} = R_{oc} = 55A * 2.1m \text{ Ohms} / 10\mu A \sim 11.5K$
 Where :
 R_{droop} is Intel spec : -2.1m Ohms
 I_{ocp} is desire over current
 I_{ocset} is recommendation 10uA from Rbias

$R_{droop2} = [N * R_{droop} / (DCR * G) - 1] * R_{in}$
 $R_{52} = [2 * 2.1m / (1.8m * 0.83) - 1] * 1K = 1.8K$
 R_{droop} : Intel spec. -2.1m Ohms

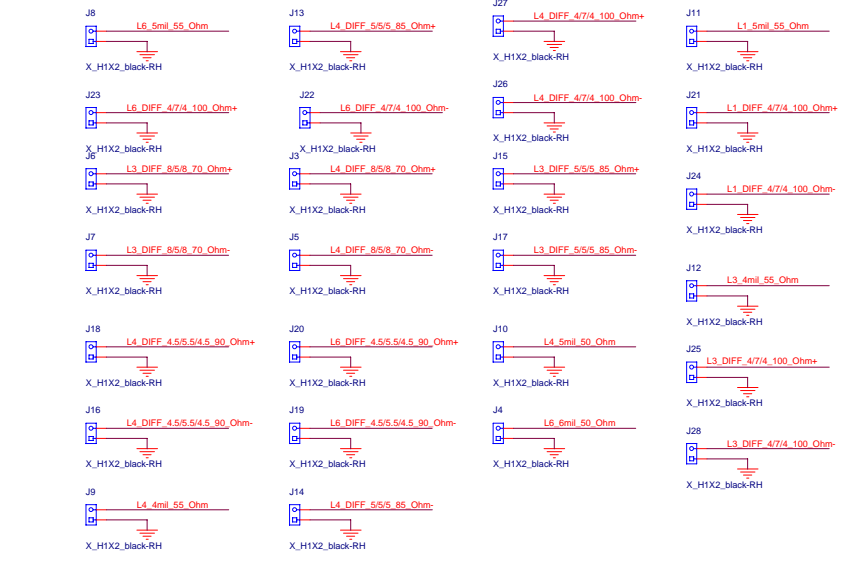
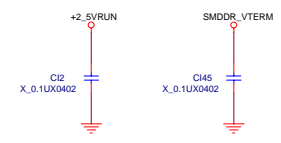
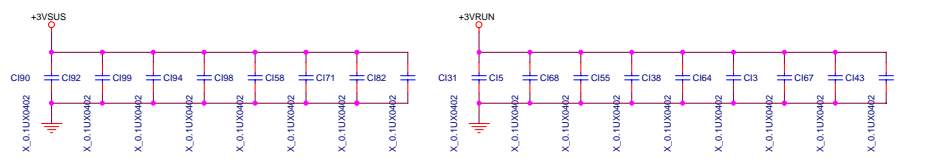
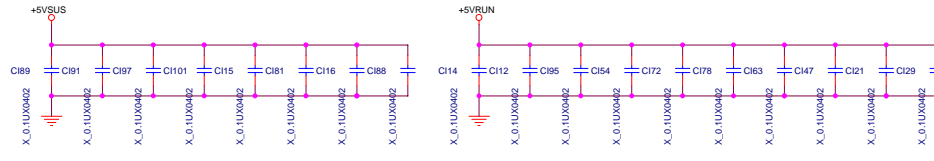
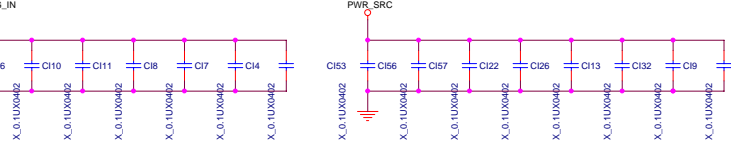
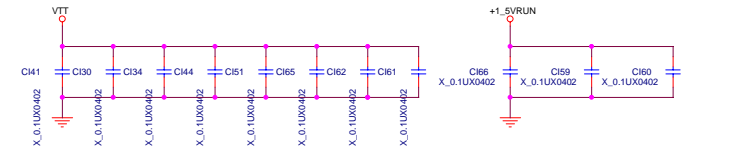
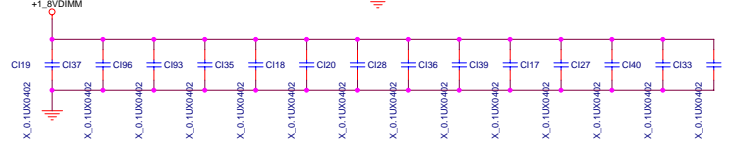
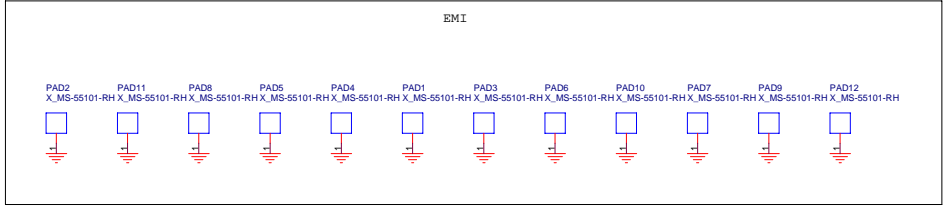
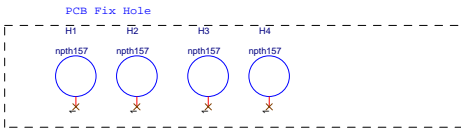
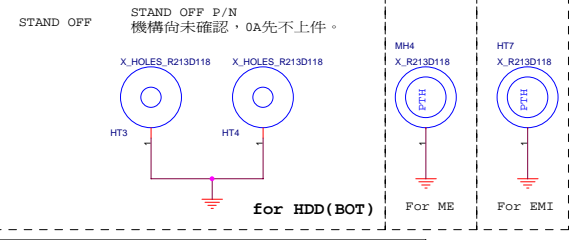
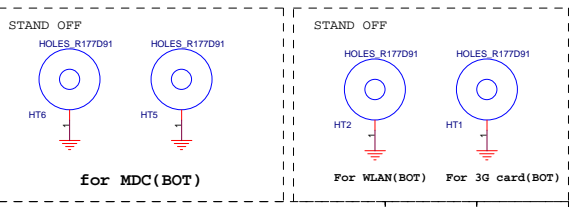
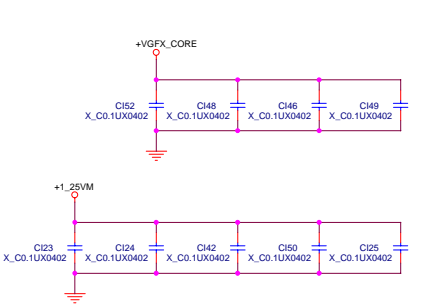
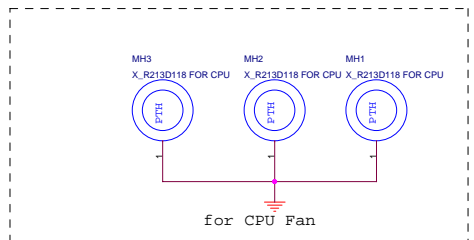
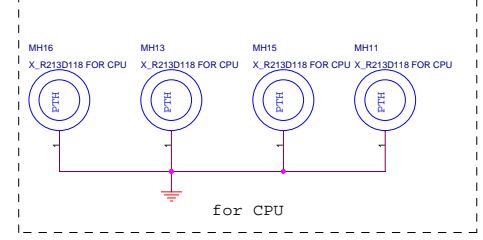
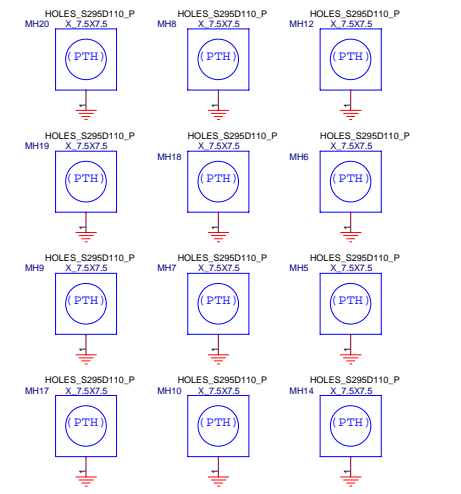
100 mil Trace list for layout
 DH1_VCORE & DH2_VCORE
 LX1_VCORE & LX2_VCORE
 DL1_VCORE & DL2_VCORE

Close to Phase 1 Inductor

Parallel

Parallel

| | | |
|-----------------|---------------------------|----------------|
| MSI CORPORATION | | |
| File | CPU POWER | |
| Size | Document Number | Rev |
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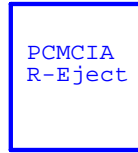


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|------------------------|---------------------------|----------------|
| MSI CORPORATION | | |
| File | | |
| Screw & EMI | | |
| Size | Document Number | Rev |
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瀚宇博德_NC

UME3003



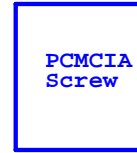
PCMCIA-EJECT
E21-1022010-H21

SCREW1

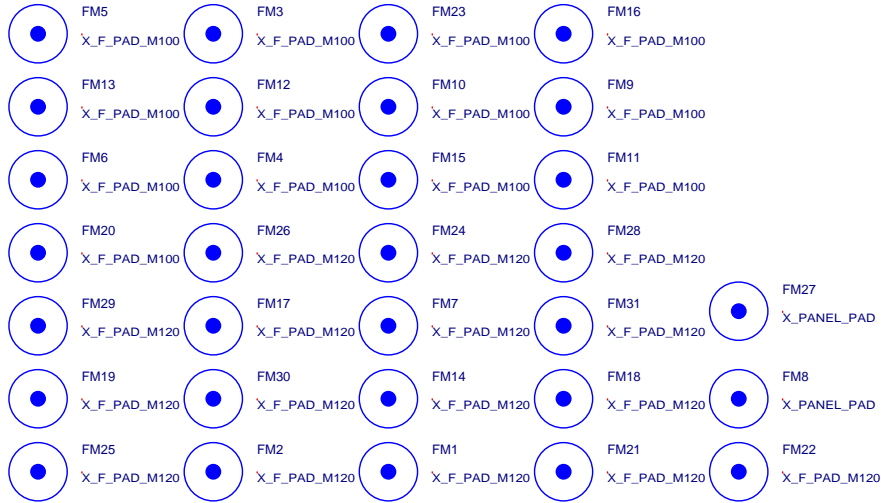


PCMCIA Screw

SCREW2



PCMCIA Screw



| | | |
|------------------------------|---------------------------|----------------|
| MSI CORPORATION | | |
| Title | | |
| Non-Footprint for BOM | | |
| Size | Document Number | Rev |
| B | MS-1421 | 0A |
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G3 -> M1/SX -> M0/S0(AC Mode)

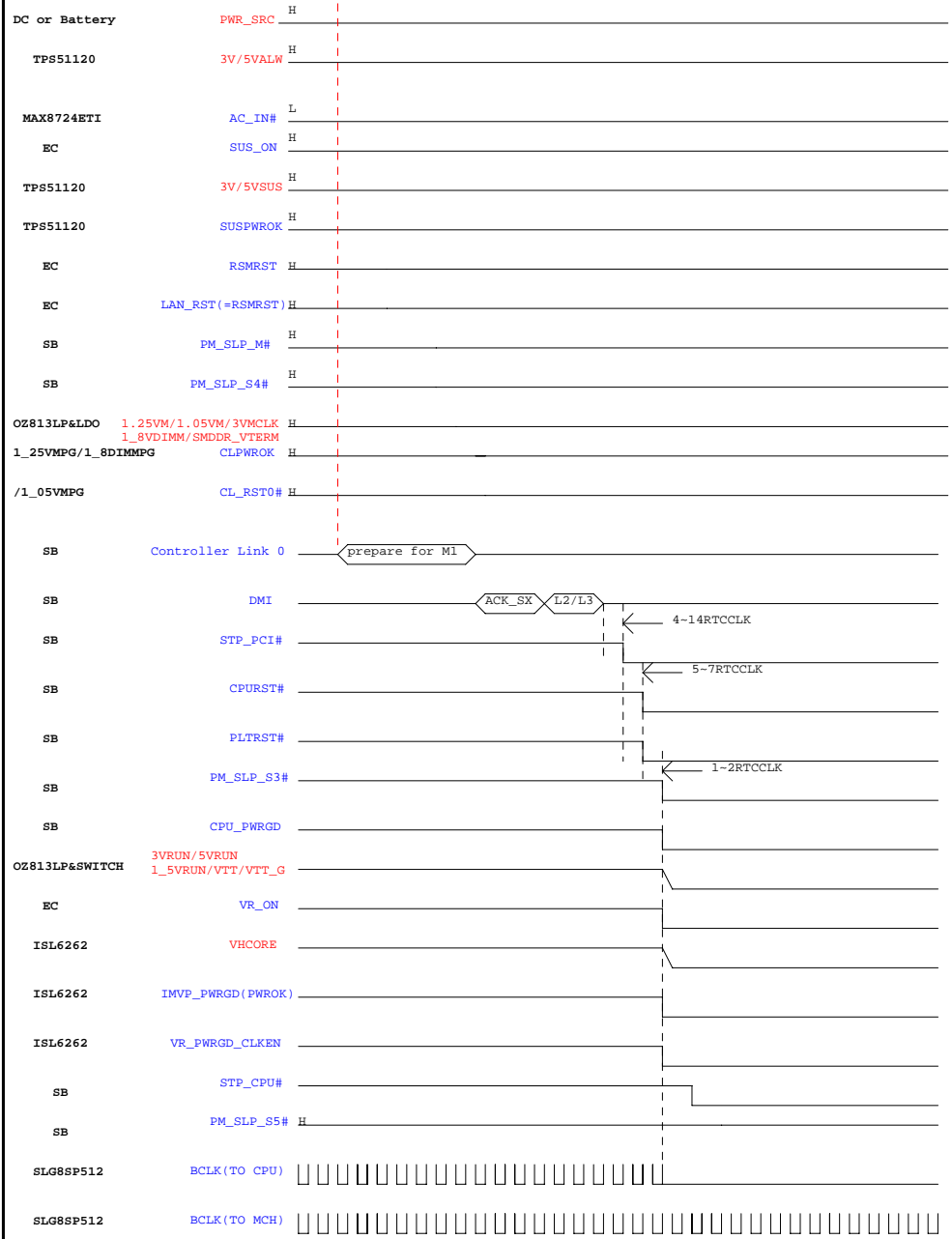
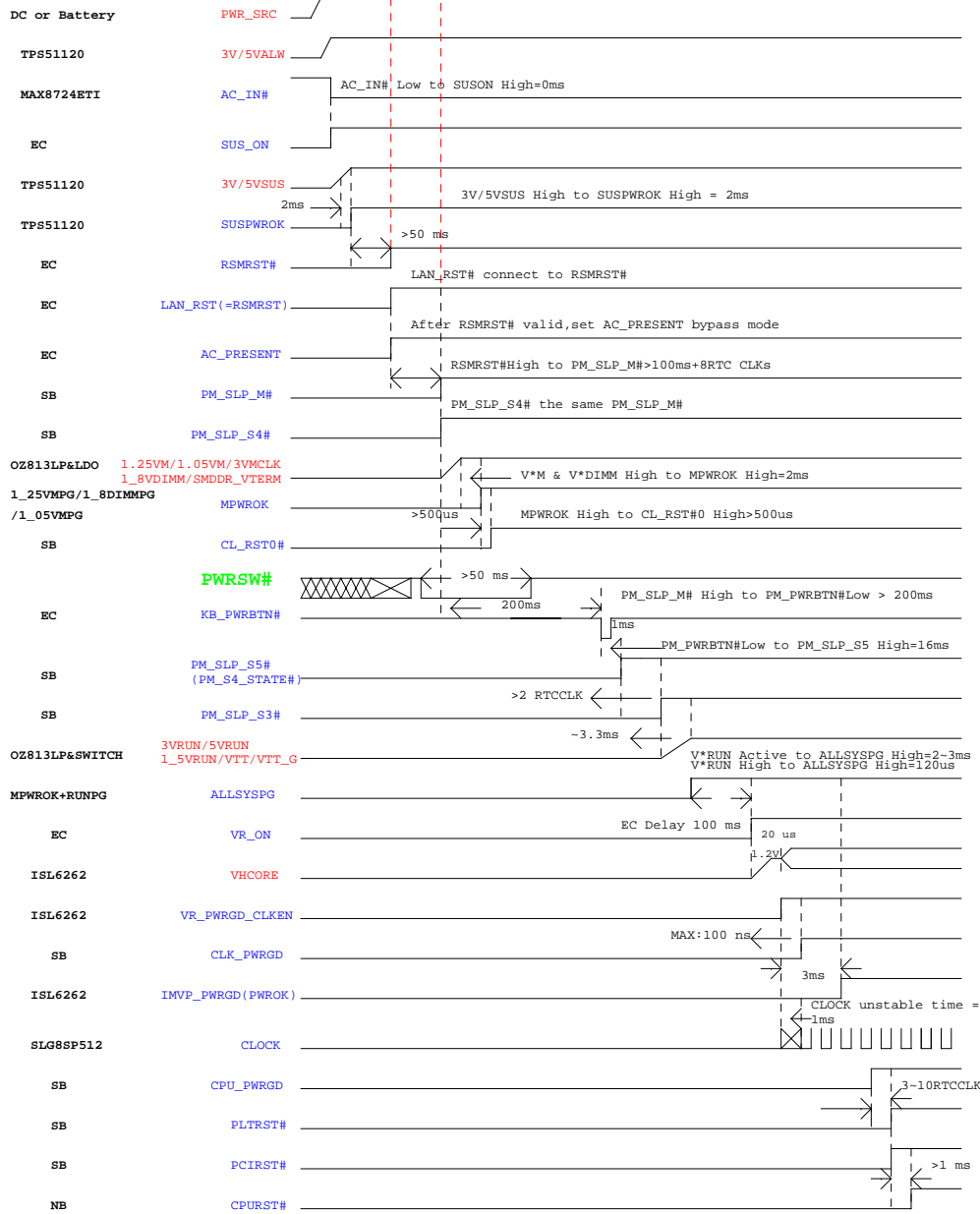
M0/S0->M1/S3(AC Mode)

System State

System State

Drive Source

Drive Source



G3->M0/S0 (Battery Mode)

M0/S0->MOff/S3 (Battery Mode)

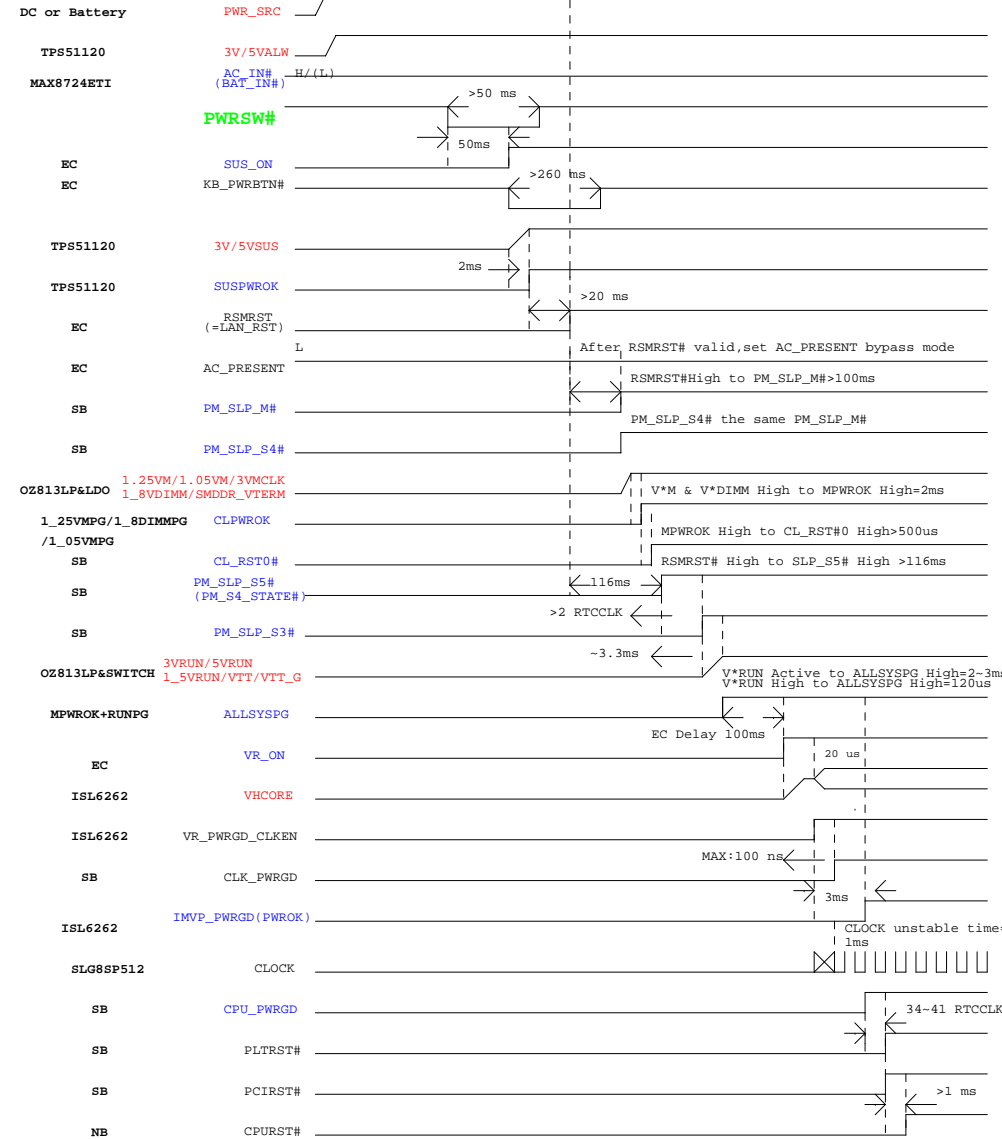
System State

G3 X S5/Moff -> S0/M0

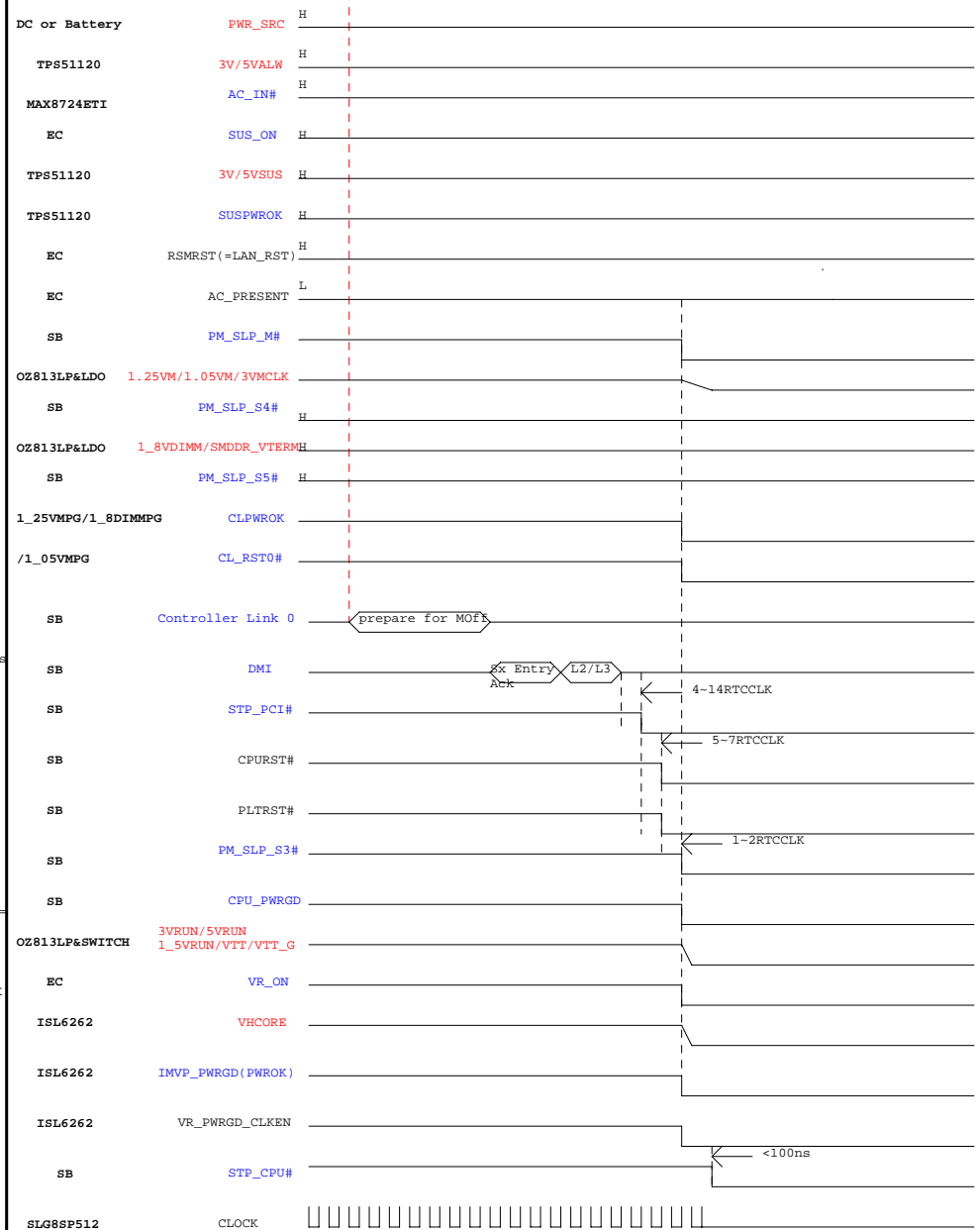
System State

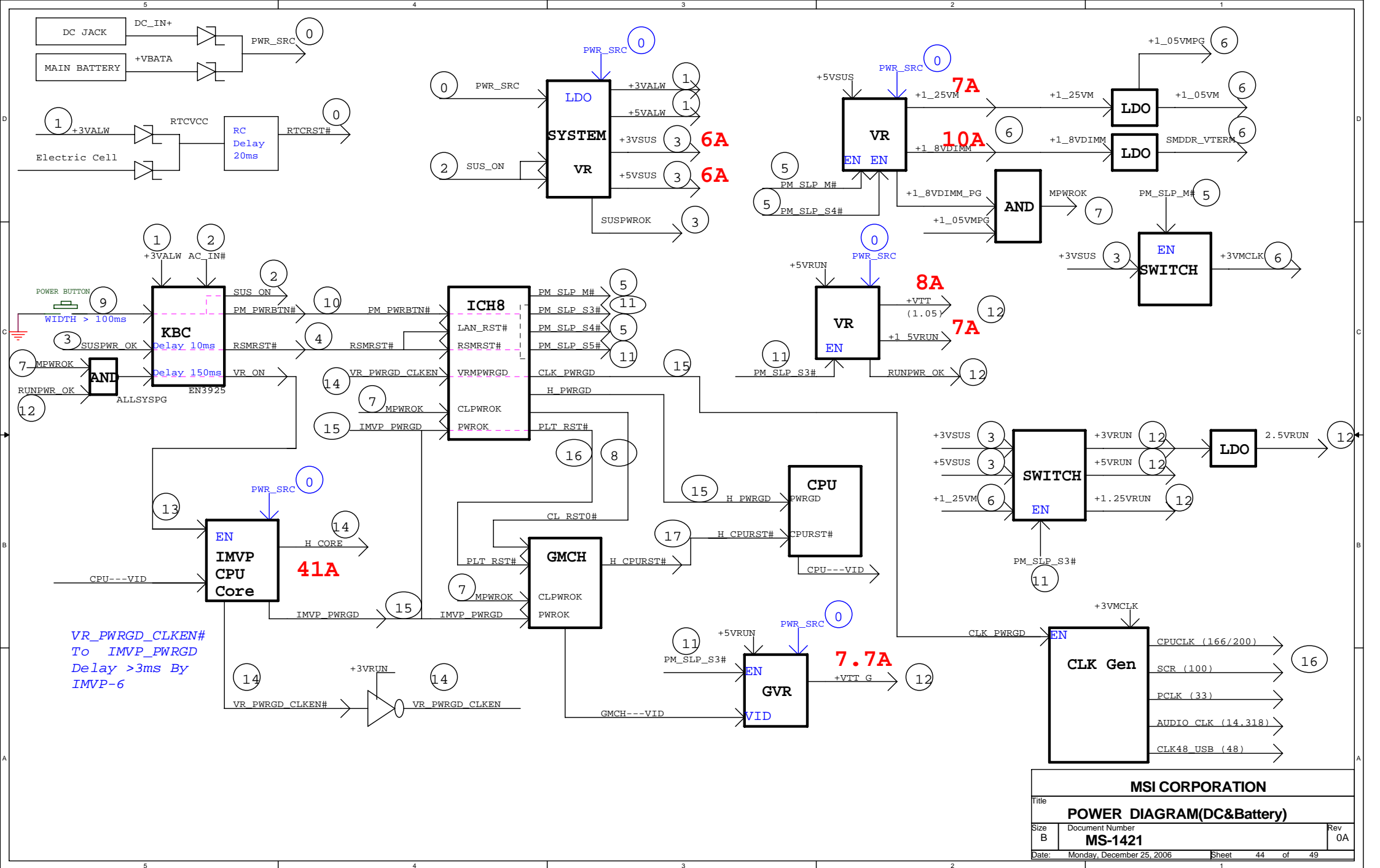
M0/S0 X MOff / S3

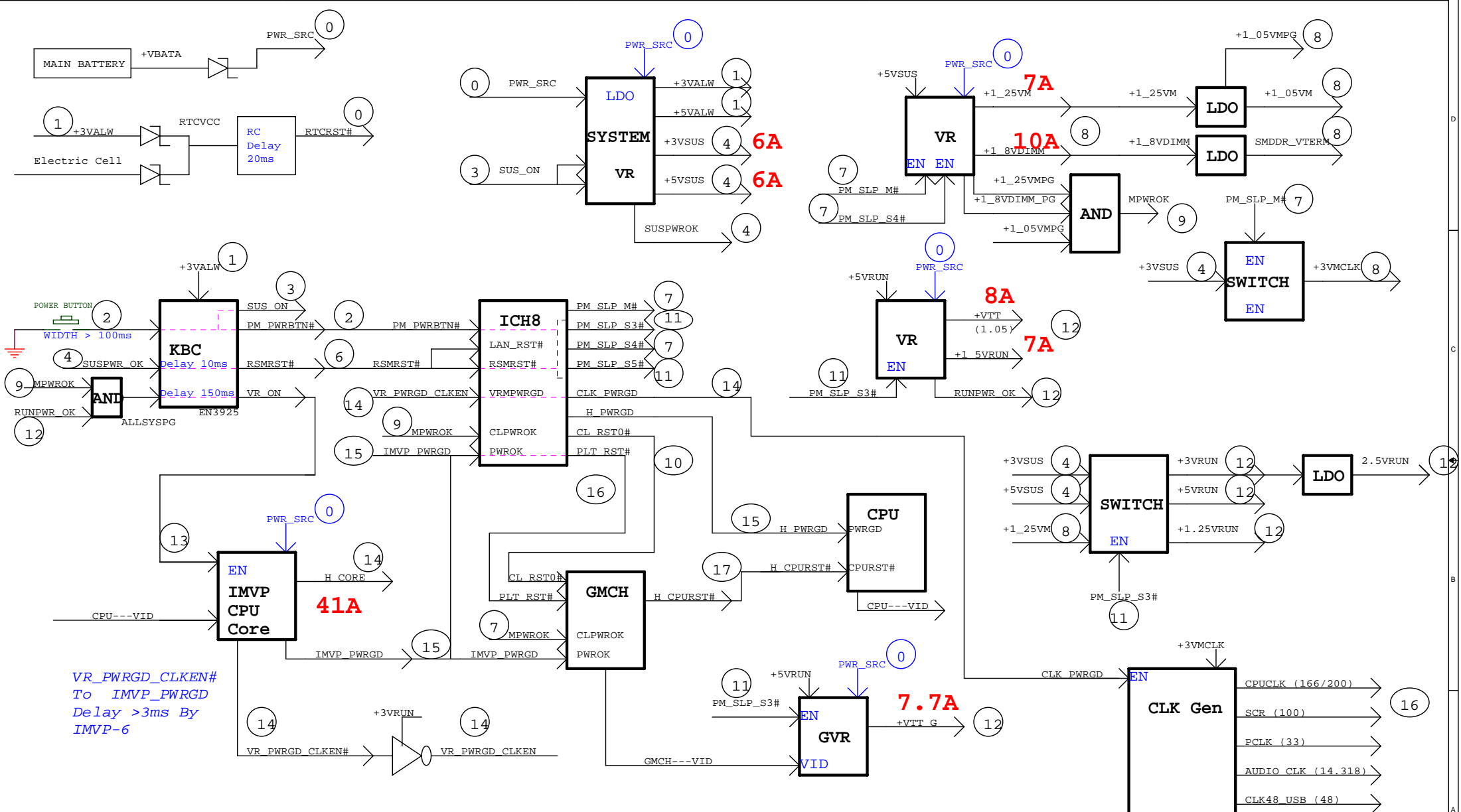
Drive Source



Drive Source

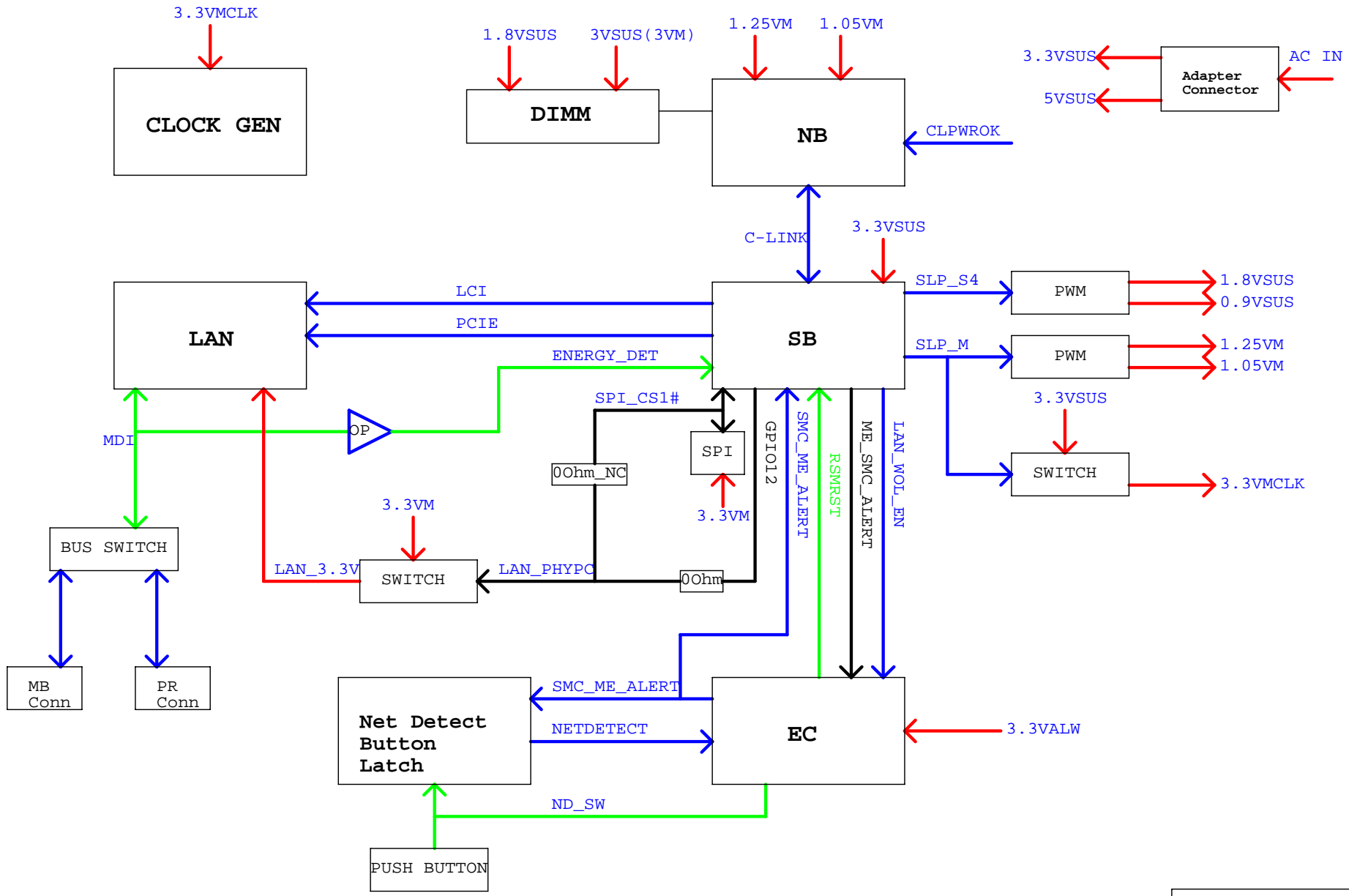






VR_PWRGD_CLKEN#
To IMVP_PWRGD
Delay >3ms By
IMVP-6

| | | |
|---------------------------------------------|-----------------------------------|-----------|
| MSI CORPORATION | | |
| Title POWER DIAGRAM(Only Battery) | | |
| Size B | Document Number MS-1421 | Rev 0A |
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| | | |
|--------------------------|---------------------------|----------------|
| MSI CORPORATION | | |
| Title | | |
| AMT BLOCK DIAGRAM | | |
| Size | Document Number | Rev |
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MS1421-0A

11/30: Add Mini PCI-E Stand off * 2-----Page 28
11/30: CAMERA# Change to CAMERA (High active)-----Page 21 & Page 22
11/30: CHRONTEL recommend RG2014,RG2015 2.2KOhm Change to 5.6KOhm-----Page 14
12/04: Modified Card reader P/N & Footprint-----Page 26
12/04: Add MS1421A(FINGERPRINT&TOUCHPAD)-----Page 48
12/04: Add MS1421B(FINGERPRINT)-----Page 49
12/04: Add MS1421C(LAUNCH BOARD)-----Page 50
12/04: Modified MINI-PCIE Footprint-----Page 28
12/04: Del PD9,C4071,C437,C249,PC96
12/04: C206(220UF) Change to 100UF
12/04: C146(330UF) Change to 220UF
12/04: DIMM1 Connector P/N & Footprint change to N13-2000180-A10 & DDR_II_SODIMM_STD---Page 12
12/04: DIMM0 Connector P/N change to N13-2000190-A10----Page 11
12/04: C3274,C4113,CG1,CG10,EC1 change to 100UF/6.3V MLCC
12/05: Del R340(PM_BMBUSY# Pull high resistor),This signal does not require external pull-up---Page 19
12/05: Intel check list recommend R353(IMVP_PWRGD) 100KOhm Change to 10KOhm-----Page 19
12/05: Change PCMCIA Connector P/N-----Page 24
12/05: Add PCMCIA R-Eject & Screw *2-----Page 41
12/06: PR64(S3# Pull low resistor) NC-----Page 35
12/06: Add RJ11 Connector-----Page 29
12/07: Change LID Switch P/N & Footprint-----Page 29
12/07: Change CON2 P/N & Footprint-----Page 28
12/11: R2206,R2214,R2217,R2222,R2225-R2228,C2253,C2259,C2264,C2272 caps near to lan controller(less than 0.25")---Page 27
12/13: Change Audio AMP circuit--Page 30,31
12/14: R4264 connect to +1_25VM ,Change to 3VMCLK--Page 15
12/14: Change LED8 P/N to green light--Page 28
12/14: Del MS1421B(Fingerprint board)
12/14: Swap P/R trace for layout request-----Page 32
12/15: R4264 connect to 3VMCLK ,Change to 3VRUN--Page 15
12/15: PR131,PR132(0Ohm/0402) Change to 100Ohm/0603
12/18: Intel-WW48 recommend RG2014,RG2015 2.2KOhm Change to 4KOhm(CHRONTEL recommend 5.6k)-----Page 14
12/18: Panasonic recommend R4275,R4287 10KOhm Change to 20KOhm , C4256,C4260 1UF change to 2.2uf-----Page 30
12/18: Intel-WW48 recommend RG2014,RG2015 2.2KOhm Change to 4KOhm(CHRONTEL recommend 5.6k)-----Page 14
12/19: Del R284, C4106,C301,C288,C302,C290 Change to 100pf(REALTEK commend)-----Page 30,31
12/19: U4015 Vlogic(pin 7) connect to 5VRUN-----Page 32
12/19: ADD HDD STAND OFF-----Page 40
12/20: R4135 connect voltage from 5VRUN change to 3VRUN----Page 32
12/20: Add C4265,C4266,Del C4111 ----Page 32
12/20: Swap DDR termination for layout request-----Page 13

| | | |
|------------------------|---------------------------|----------------|
| MSI CORPORATION | | |
| Title | | |
| Change History | | |
| Size | Document Number | Rev |
| B | MS-1421 | OA |
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