TPS775xx with $\overline{\text{RESET}}$ Output, TPS776xx with PG Output
FAST-TRANSIENT-RESPONSE 500mA LOW-DROPOUT VOLTAGE REGULATORS

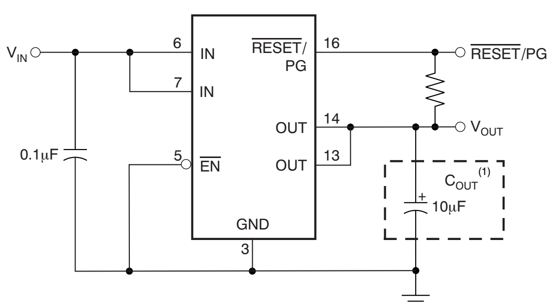
FEATURES

- **Open Drain Power-On Reset with 200ms Delay (TPS775xx)**
- **Open Drain Power Good (TPS776xx)**
- **500mA Low-Dropout Voltage Regulator**
- **Available in Fixed Output and Adjustable Versions**
- **Dropout Voltage to 169mV (Typ) at 500mA (TPS77x33)**
- **Ultralow 85µA Typical Quiescent Current**
- **Fast Transient Response**
- **2% Tolerance Over Specified Conditions for Fixed-Output Versions**
- **8-Pin SOIC and 20-Pin TSSOP PowerPAD™ (PWP) Packages**
- **Thermal Shutdown Protection**

APPLICATIONS

- **FPGA Power**
- **DSP Core and I/O Voltages**

Typical Application Circuit (Fixed Voltage Options)



DESCRIPTION

The TPS775xx and TPS776xx devices are designed to have a fast transient response and be stable with a 10µF low ESR capacitor. This combination provides high performance at a reasonable cost.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 169mV at an output current of 500mA for the TPS77x33) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 85µA over the full range of output current, 0mA to 500mA). These two key specifications yield a significant improvement in operating life for battery-powered systems. This LDO family also features a sleep mode; applying a TTL high signal to $\overline{\text{EN}}$ (enable) shuts down the regulator, reducing the quiescent current to 1µA at T_J = +25°C.

The $\overline{\text{RESET}}$ output of the TPS775xx initiates a reset in microcomputer and microprocessor systems in the event of an undervoltage condition. An internal comparator in the TPS775xx monitors the output voltage of the regulator to detect an undervoltage condition on the regulated output voltage.

Power good (PG) of the TPS776xx is an active high output, which can be used to implement a power-on reset or a low-battery indicator.

The TPS775xx and TPS776xx are offered in 1.5V, 1.6V (TPS77516 only), 1.8V, 2.5V, 2.8V (TPS77628 only), and 3.3V fixed-voltage versions and in an adjustable version (programmable over the range of 1.5V to 5.5V for the TPS77501 and 1.2V to 5.5V for the TPS77601). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges. The TPS775xx and TPS776xx families are available in 8-pin SOIC and 20-pin TSSOP packages.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT} (2)
TPS775**xx*yyyz***, TPS776**xx*yyyz***	**XX** is nominal output voltage (for example, 28 = 2.8V, 285 = 2.85V, 01 = Adjustable). **YYY** is package designator. **Z** is package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Custom fixed output voltages are available; minimum order quantities may apply. Contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS

Over operating temperature range (unless otherwise noted)(1)

PARAMETER	TPS775xx, TPS776xx	UNIT
Input voltage range, V_{IN} (2)	–0.3 to +13.5	V
Voltage range at $\overline{EN}$	–0.3 to +16.5	V
Maximum $\overline{RESET}$ voltage (TPS775xx)	16.5	V
Maximum PG voltage (TPS776xx)	16.5	V
Peak output current	Internally limited	
Voltage range at OUT, FB	7	V
Continuous total power dissipation	See Dissipation Ratings Table	
Operating junction temperature range, T_J	–40 to +125	°C
Storage junction temperature range , T_{STG}	–65 to +150	°C
ESD rating, HBM	2	kV

(1) Stresses above these ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) All voltages are with respect to network terminal ground.

DISSIPATION RATINGS

BOARD	PACKAGE	AIRFLOW (CFM)	T_A < +25°C (mW)	DERATING FACTOR ABOVE T_A = +25°C	T_A = +70°C (mW)	T_A = +85°C (mW)
—	D	0	568	5.68mW/°C	312	227
		250	904	9.04mW/°C	497	362
Low-K(1)	PWP	0	2350	23.5mW/°C	1300	940
		300	3460	34.6mW/°C	1900	1400
High-K(2)	PWP	0	2380	23.8mW/°C	1300	952
		300	5790	57.9mW/°C	3200	2300

(1) This parameter is measured with the recommended copper heat sink pattern on a 1-layer, 5in × 5in printed circuit board (PCB), 1-ounce copper, 2in × 2in coverage ($4in^2$).
(2) This parameter is measured with the recommended copper heat sink pattern on a 8-layer, 1.5in × 2in PCB, 1-ounce copper with layers 1, 2, 4, 5, 7, and 8 at 5% coverage ($0.9in^2$) and layers 3 and 6 at 100% coverage ($6in^2$). For more information, refer to TI technical brief SLMA002.

ELECTRICAL CHARACTERISTICS

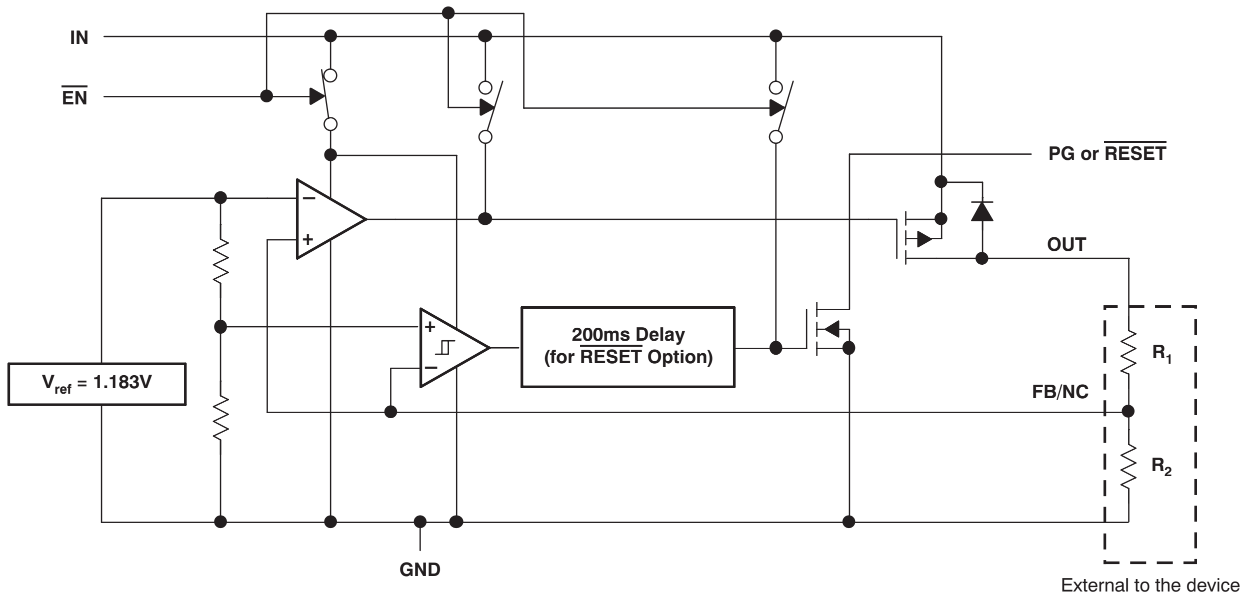
Over recommended operating temperature range (T_J = –40°C to +125°C), $V_{IN} = V_{OUT(TYP)}$ + 1V; I_{OUT} = 1mA, $V_{\overline{EN}}$ = 0V, C_{OUT} = 10µF, unless otherwise noted. Typical values are at T_J = +25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range			2.7		10	V
V_{OUT}	Output voltage range	TPS77501		1.5		5.5	V
		TPS77601		1.2		5.5	V
V_{OUT}	Accuracy		V_{OUT} + 1V ≤ V_{IN} ≤ 10V(1) 10µA < I_{OUT} < 500mA	–2.0		+2.0	%
I_{GND}	Ground pin current		I_{OUT} = 10mA		85		µA
			I_{OUT} = 500mA			125	
$\Delta V_{OUT}\%/\Delta V_{IN}$	Output voltage line regulation		V_{OUT} + 1V ≤ V_{IN} ≤ 10V(1)		0.01		%/V
$\Delta V_{OUT}\%/\Delta I_{OUT}$	Load regulation				3		mV
V_N	Output noise voltage BW = 200Hz to 100kHz	TPS77x18	I_C = 500mA, C_{OUT} = 10µF		53		$µV_{RMS}$
V_{DO}	Dropout voltage(2)	TPS77628	I_{OUT} = 500mA		285	410	mV
		TPS77533	I_{OUT} = 500mA		169	287	mV
		TPS77633	I_{OUT} = 500mA		169	287	mV
I_{CL}	Output current limit		V_{OUT} = 0V	1.2	1.6	1.9	A
T_{SD}	Shutdown temperature				150		°C
T_J	Operating junction temperature range			–40		+125	°C
I_{STBY}	Standby current		$\overline{EN}$ = V_{IN}, at T_J = +25°C, 2.7V < V_{IN} < 10V		1		µA
			$\overline{EN}$ = V_{IN}, 2.7V < V_{IN} < 10V			10	
I_{FB}	FB input current	TPS77x01	FB = 1.5V		2		nA
$V_{EN(HI)}$	High-level enable input voltage			1.7			V
$V_{EN(LO)}$	Low-level enable input voltage					0.9	V
PSRR	Power-supply ripple rejection		f = 100Hz, C_{OUT} = 10µF		60		dB
RESET (TPS775xx)	Minimum input voltage for valid $\overline{RESET}$		$I_{OUT(RESET)}$ = 300µA		1.1		V
	Trip threshold voltage		V_{OUT} decreasing	92		98	$\%V_{OUT}$
	Hysteresis voltage		Measured at V_{OUT}		0.5		$\%V_{OUT}$
	Output low voltage		V_{IN} = 2.7V, $I_{OUT(RESET)}$ = 1mA		0.15	0.4	V
	Leakage current		$V_{(RESET)}$ = 5V			1	µA
	RESET time-out delay				200		ms
PG (TPS776xx)	Minimum input voltage for valid PG		$I_{OUT(PG)}$ = 300µA		1.1		V
	Trip threshold voltage		V_{OUT} decreasing	92		98	$\%V_{OUT}$
	Hysteresis voltage		Measured at V_{OUT}		0.5		$\%V_{OUT}$
	Output low voltage		V_{IN} = 2.7V, $I_{OUT(PG)}$ = 1mA		0.15	0.4	V
	Leakage current		$V_{(PG)}$ = 5V			1	µA
	Input current ($\overline{EN}$)		$\overline{EN}$ = 0V	–1	0	1	µA
			$\overline{EN}$ = V_{IN}	–1		1	

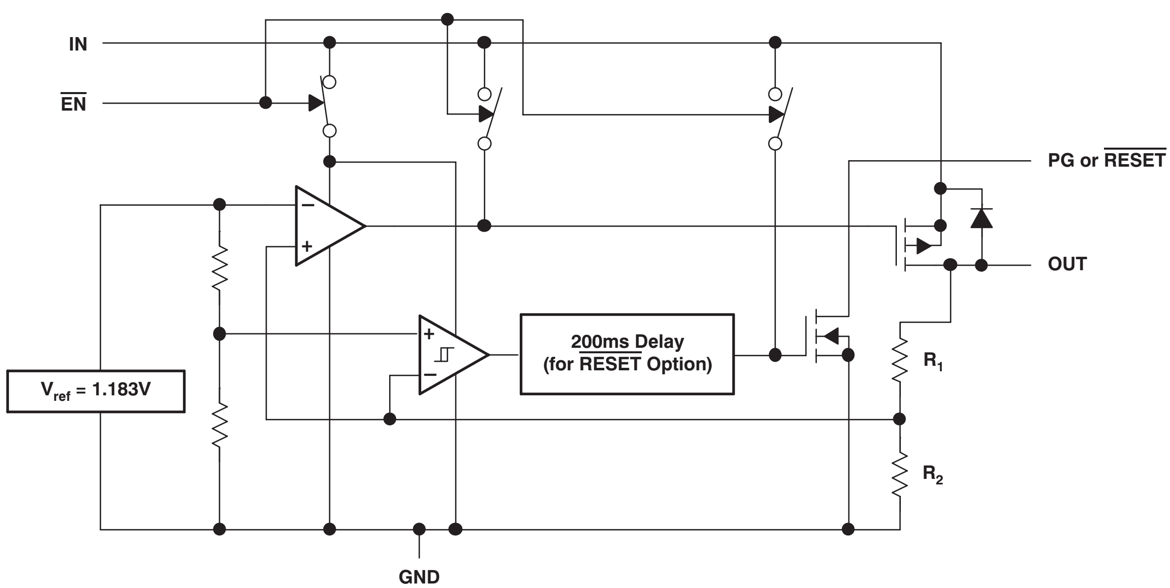
(1) Minimum $V_{IN} = V_{OUT} + V_{DO}$ or 2.7V, whichever is greater.
(2) V_{DO} is not measured for fixed output versions with $V_{OUT(NOM)}$ < 2.8 V because mimimum V_{IN} = 2.7V.

FUNCTIONAL BLOCK DIAGRAMS

Adjustable Voltage Versions

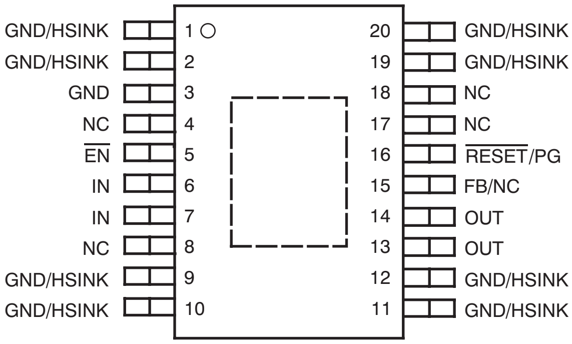


Fixed Voltage Versions



PIN CONFIGURATIONS

TSSOP-20
PWP
(TOP VIEW)



SOIC-8
D
(TOP VIEW)

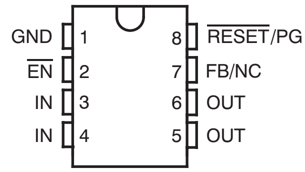
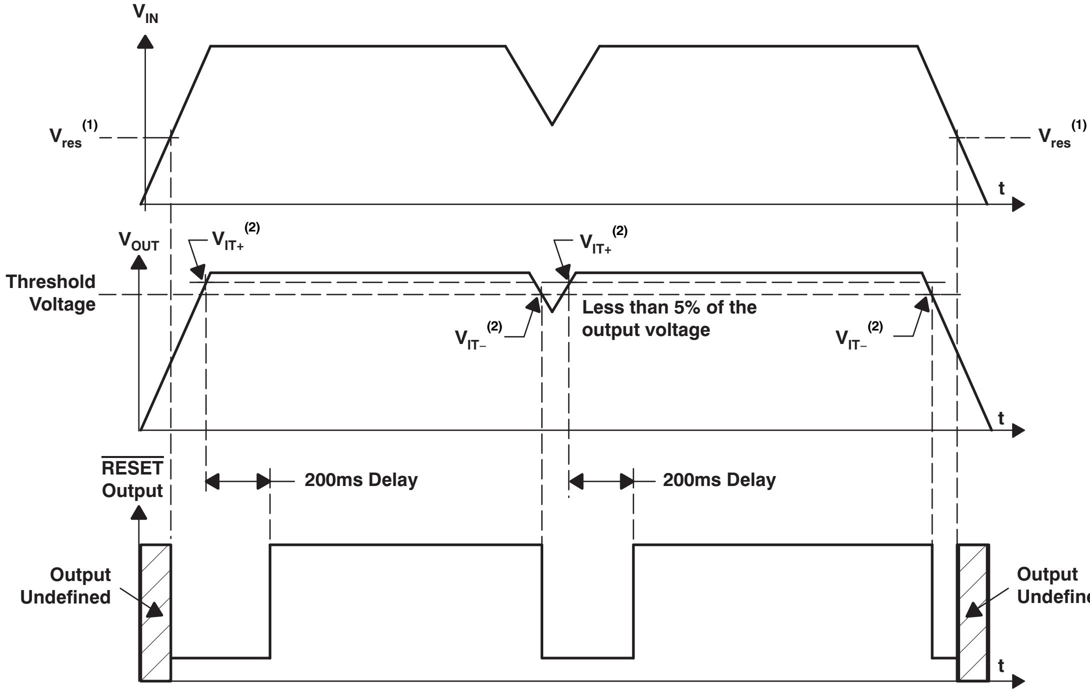


Table 1. PIN DESCRIPTIONS

TPS775xx, TPS776xx			
NAME	SOIC-8 (D) PIN NO.	TSSOP-20 (PWP) PIN NO.	DESCRIPTION
$\overline{EN}$	2	5	Negative polarity enable ($\overline{EN}$) input
FB	7	15	Adjustable voltage version only; feedback voltage for setting output voltage of the device. Not internally connected on adjustable versions.
GND	1	1, 2, 3, 9, 10, 11, 12, 19, 20	Ground
IN	3, 4	6, 7	Input voltage
OUT	5, 6	13, 14	Regulated output voltage
$\overline{RESET}$	8	16	TPS775xx devices only; open-drain $\overline{RESET}$ output.
PG	8	16	TPS776xx devices only; open-drain power-good (PG) output.
NC	—	4, 8, 17, 18	No internal connection
PAD/TAB	—	—	Should be soldered to ground plane and used for heat sinking.

TPS775xx RESET Timing Diagram



(1) V_{res} is the minimum input voltage for a valid RESET. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

(2) V_{IT}: Trip voltage is typically 5% lower than the output voltage (95% V_{OUT}). V_{IT-} to V_{IT+} is the hysteresis voltage.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE NO.
V_{OUT}	Output Voltage	vs Output Current	Figure 3, Figure 4, Figure 5
		vs Free-Air Temperature	Figure 6, Figure 7, Figure 8
		vs Time	Figure 20
I_{GND}	Ground Current	vs Free-Air Temperature	Figure 9
PSRR	Power-Supply Ripple Rejection	vs Frequency	Figure 10
	Output Spectral Noise Density	vs Frequency	Figure 11
Z_{OUT}	Output Impedance	vs Frequency	Figure 12
V_{DO}	Dropout Voltage	vs Input Voltage	Figure 13
		vs Free-Air Temperature	Figure 14
V_{IN}	Input Voltage (Min)	vs Output Voltage	Figure 15
LINE	Line Transient Response		Figure 16, Figure 18
LOAD	Load Transient Response		Figure 17, Figure 19
ESR	Equivalent Series Resistance	vs Output Current	Figure 22, Figure 23

TYPICAL CHARACTERISTICS

Over operating temperature range (T_J= –40°C to +125°C) unless otherwise noted. Typical values are at T_J = +25°C.

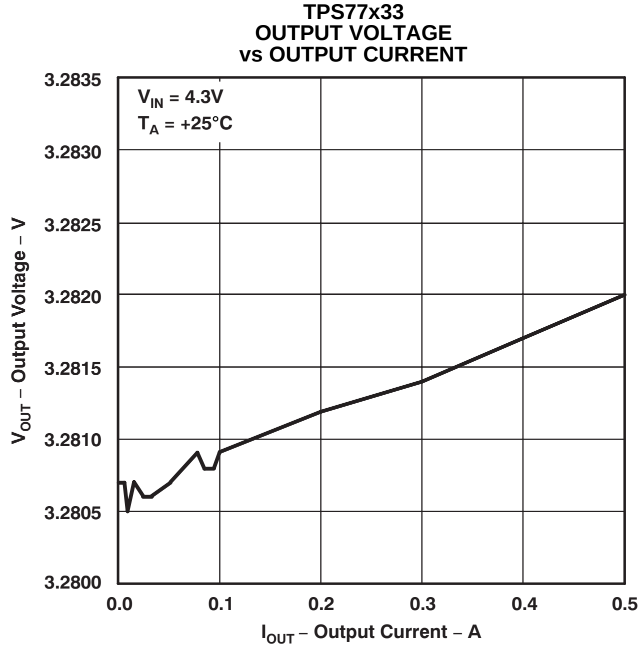


Figure 3.

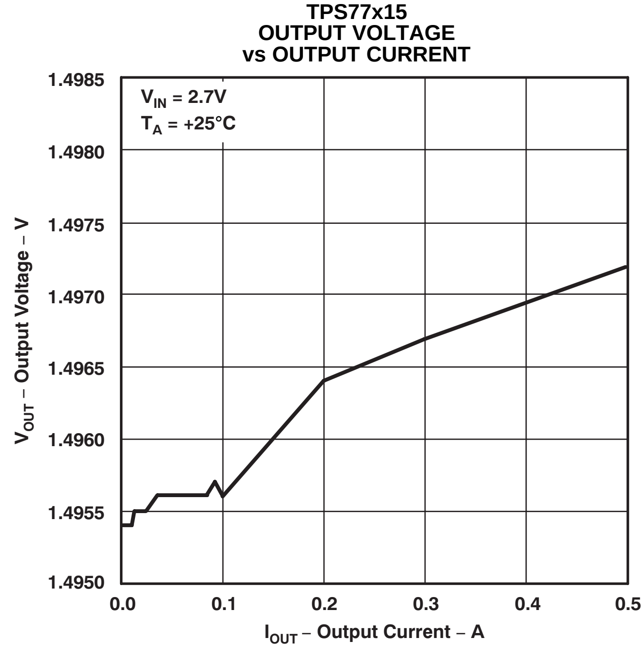


Figure 4.

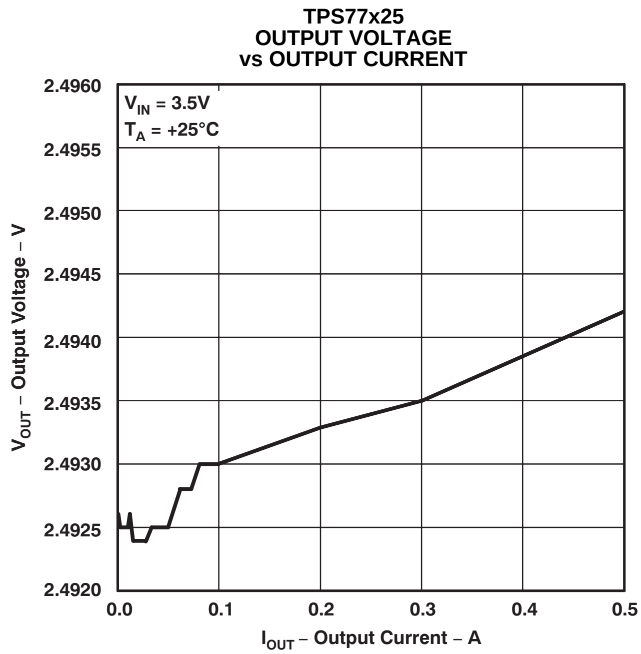


Figure 5.

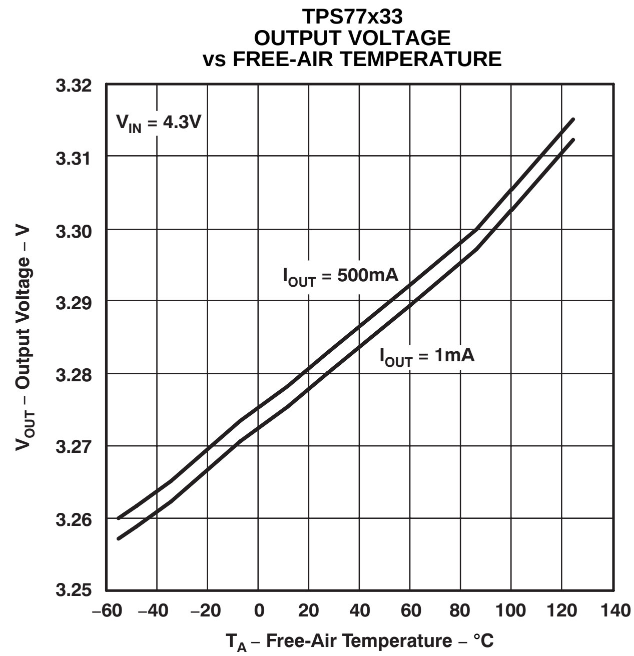


Figure 6.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J= –40°C to +125°C) unless otherwise noted. Typical values are at T_J = +25°C.

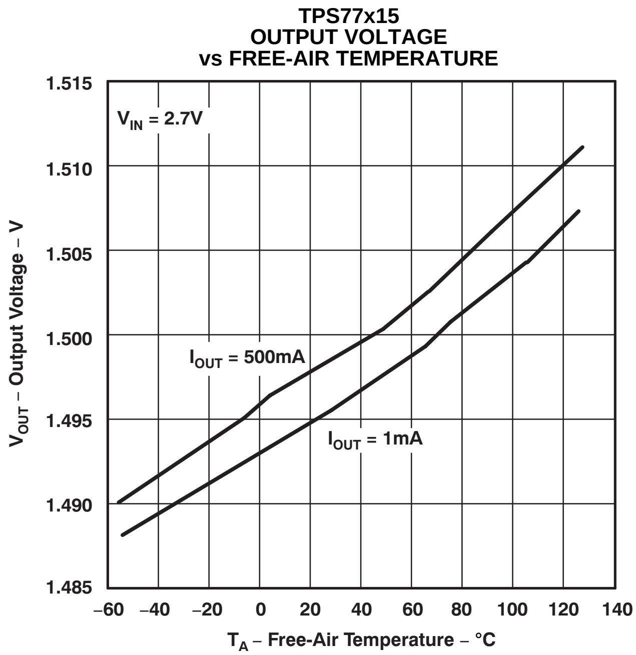


Figure 7.

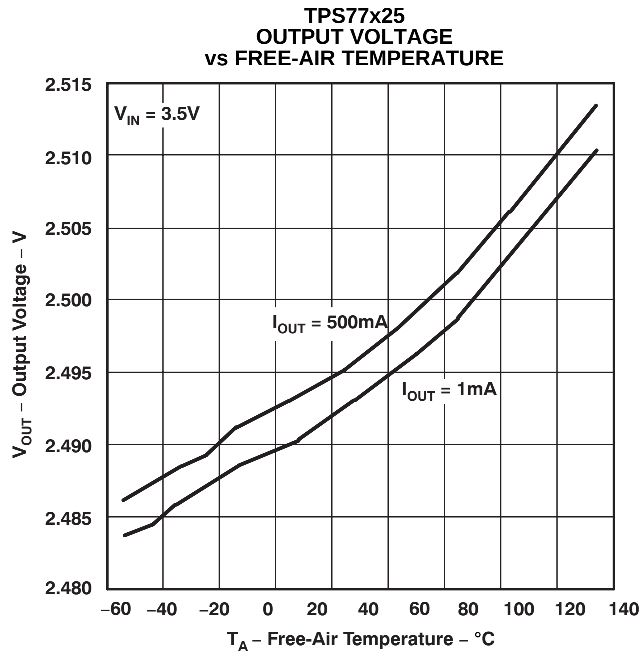


Figure 8.

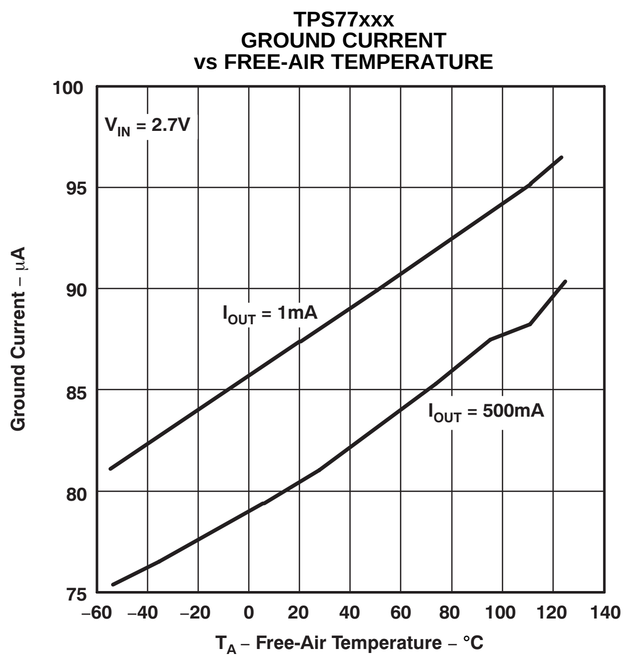


Figure 9.

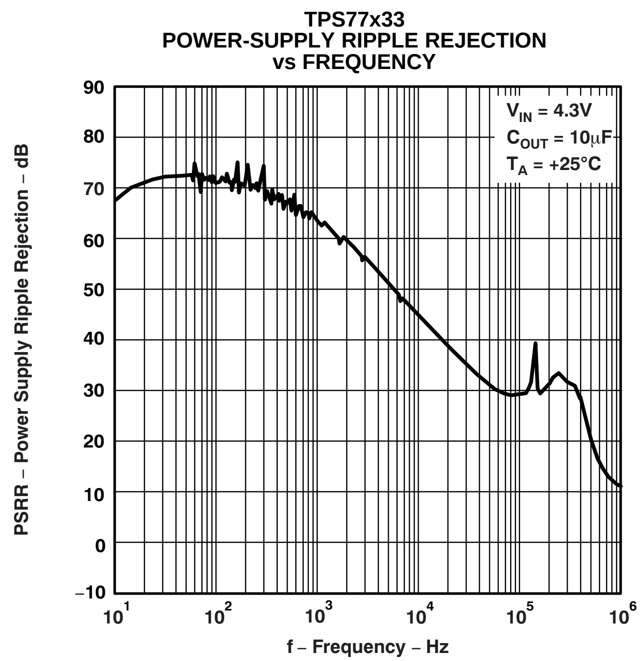


Figure 10.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J= –40°C to +125°C) unless otherwise noted. Typical values are at T_J = +25°C.

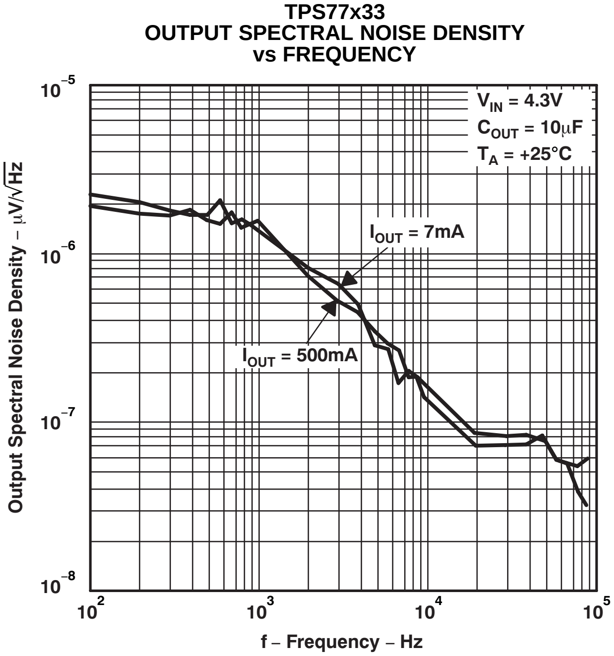


Figure 11.

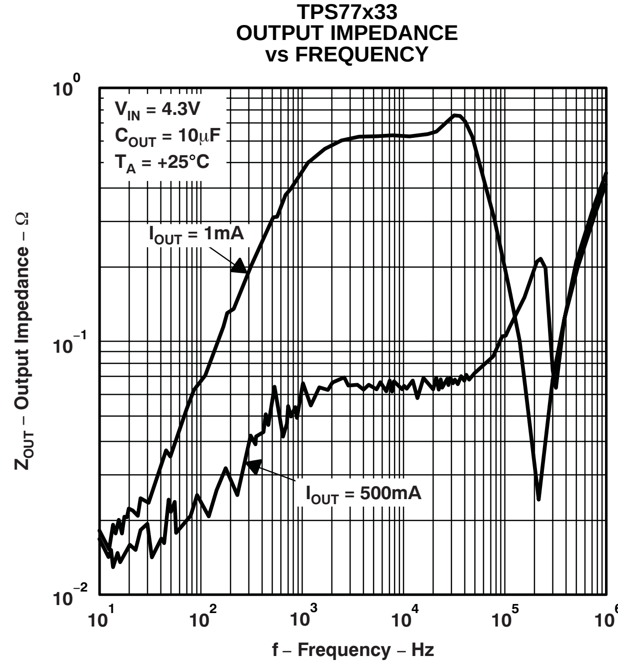


Figure 12.

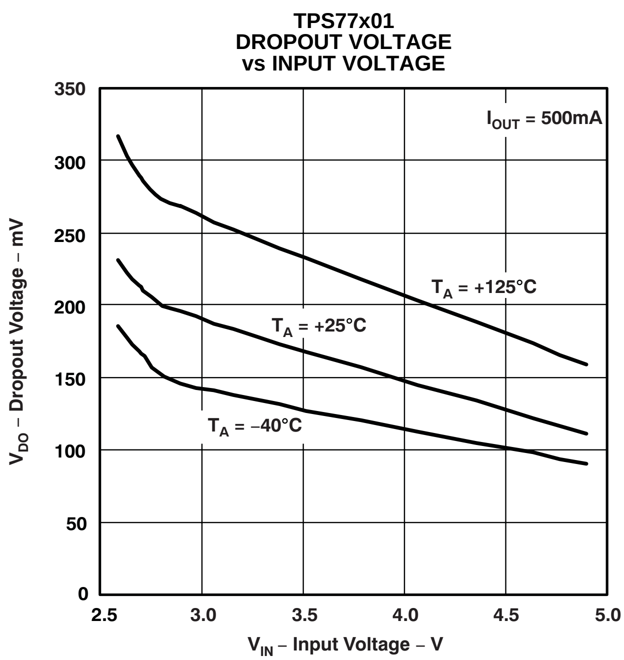


Figure 13.

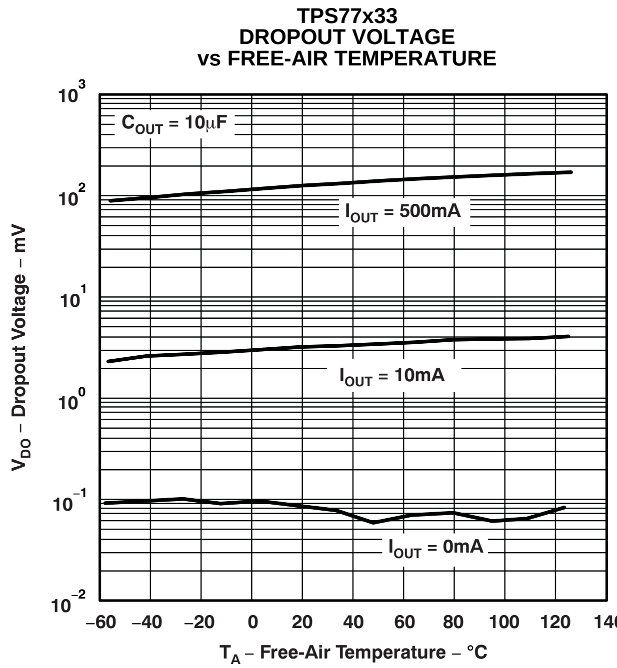


Figure 14.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J= –40°C to +125°C) unless otherwise noted. Typical values are at T_J = +25°C.

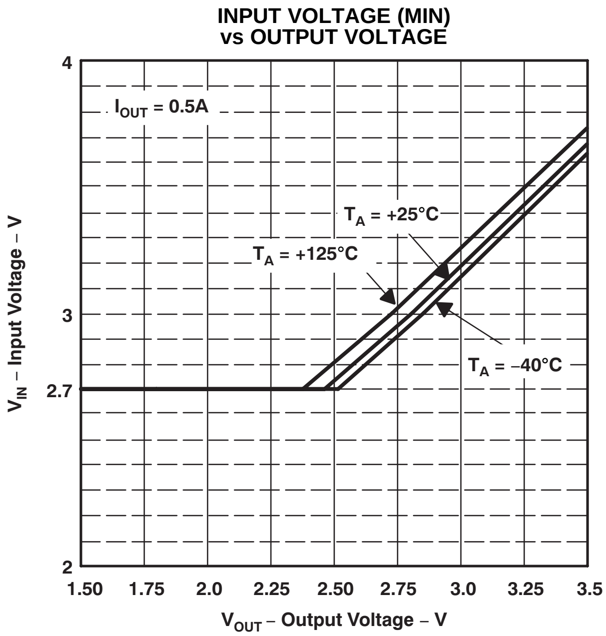


Figure 15.

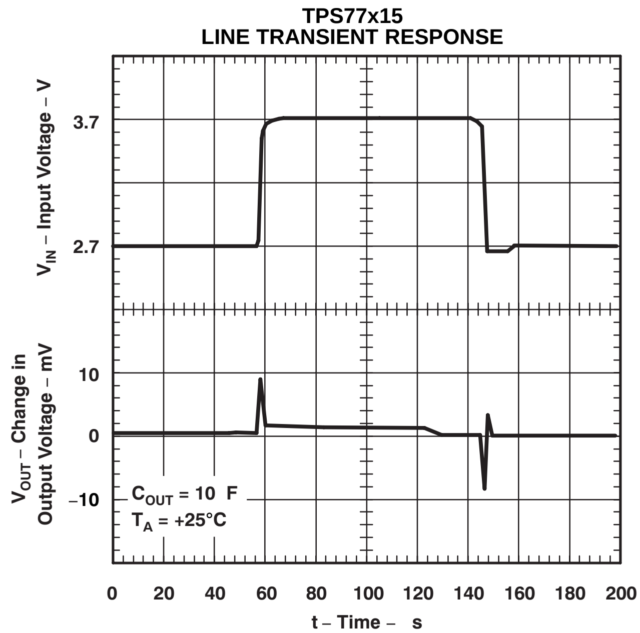


Figure 16.

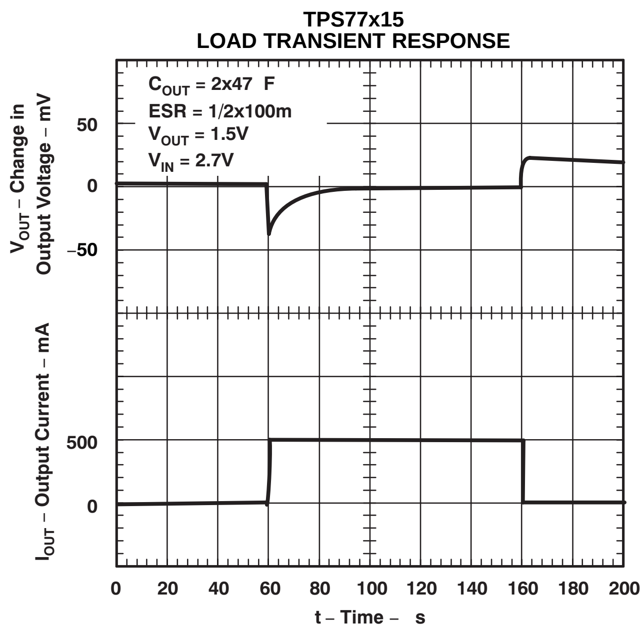


Figure 17.

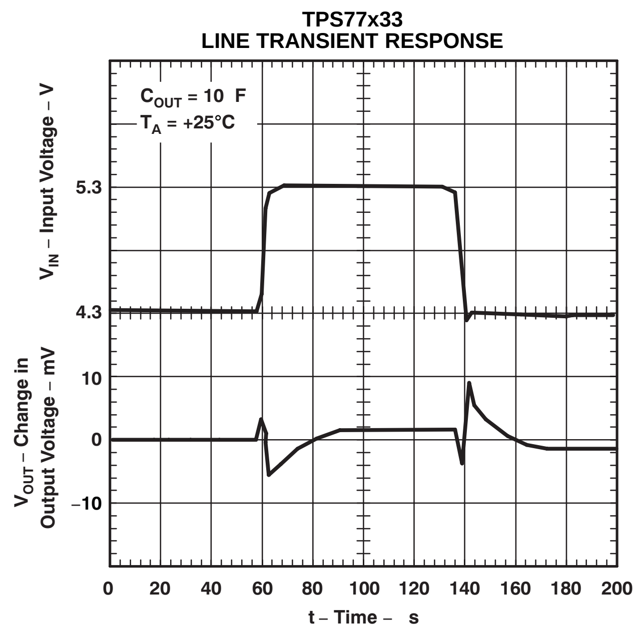


Figure 18.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J= –40°C to +125°C) unless otherwise noted. Typical values are at T_J = +25°C.

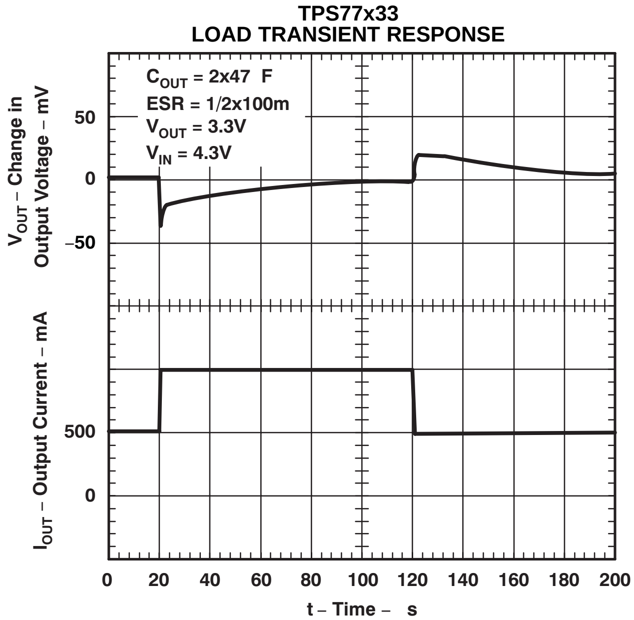


Figure 19.

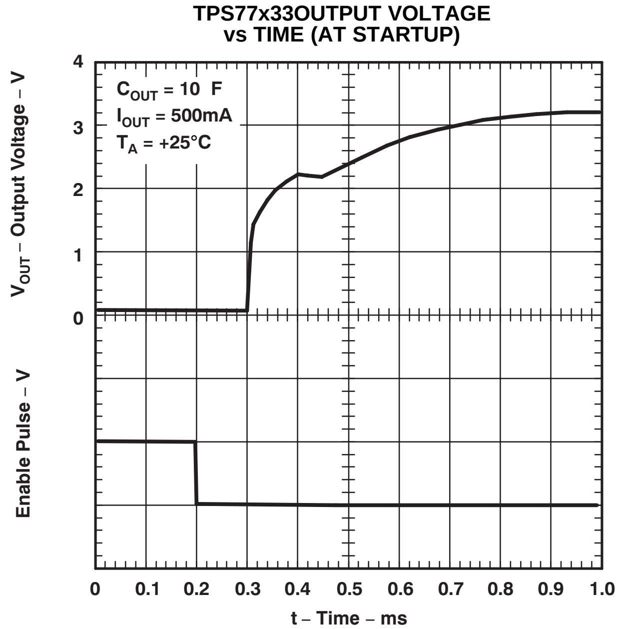


Figure 20.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J= –40°C to +125°C) unless otherwise noted. Typical values are at T_J = +25°C.

Test Circuit for Typical Regions of Stability (Figure 22 and Figure 23) (Fixed Output Options)

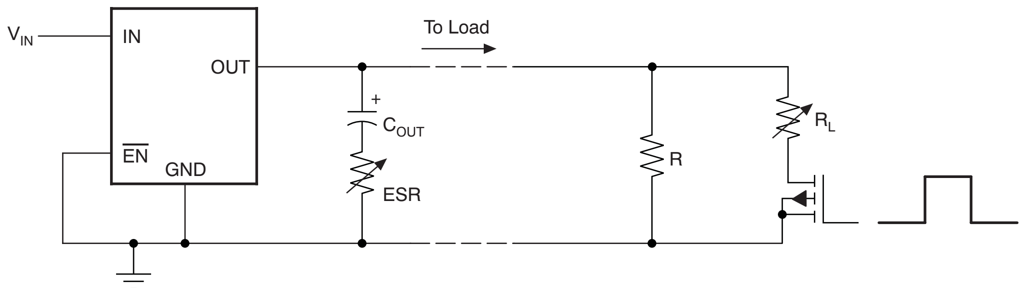
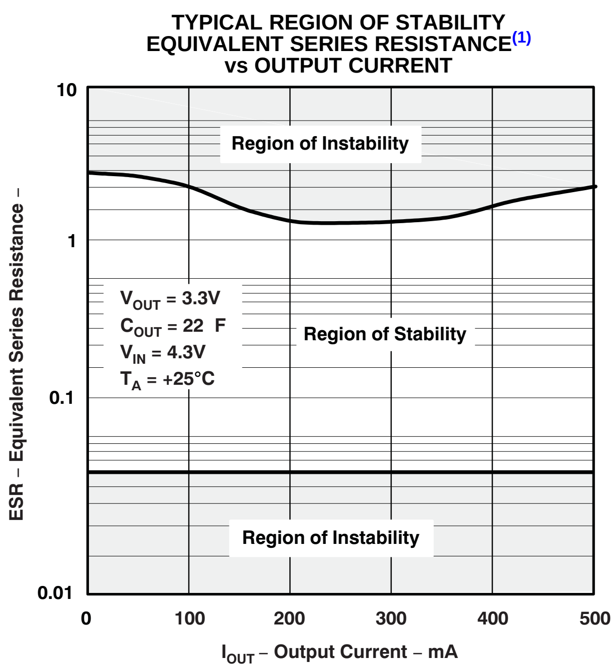
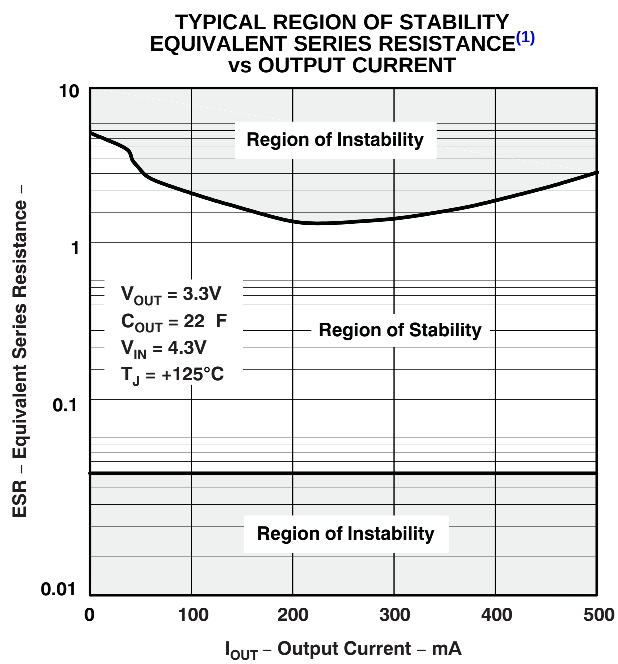


Figure 21.



(1) Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_{OUT}.

Figure 22.



(1) Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_{OUT}.

Figure 23.

APPLICATION INFORMATION

The TPS775xx and TPS776xx feature very low quiescent current, which remains virtually constant even with varying loads. Conventional LDO regulators use a pnp pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). The TPS775xx and TPS776xx use a PMOS transistor to pass current; because the gate of the PMOS is voltage driven, operating current is low and invariable over the full load range.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power up, this I_B increase translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS775xx and TPS776xx quiescent currents remain low even when the regulator drops out, eliminating both problems.

The TPS775xx and TPS776xx families also feature a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to 2μA. If the shutdown feature is not used, $\overline{EN}$ should be tied to ground.

Minimum Load Requirements

The TPS775xx and TPS776xx families are stable at zero load; no minimum load is required for operation.

FB—Pin Connection (Adjustable Version Only)

The FB pin is an input pin to sense the output voltage and close the loop for the adjustable option. The output voltage is sensed through a resistor divider network to close the loop as it is shown in Figure 25. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit to improve performance at that point. Internally, FB connects to a high-impedance wide-bandwidth amplifier and noise pickup feeds through to the regulator output. Routing the FB connection to minimize/avoid noise pickup is essential.

External Capacitor Requirements

An input capacitor is not usually required; however, a ceramic bypass capacitor (0.047μF or larger) improves load transient response and noise rejection if the TPS775xx or TPS776xx are located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

Like all low dropout regulators, the TPS775xx and TPS776xx require an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 10μF and the ESR (equivalent series resistance) must be between 50mΩ and 1.5Ω. Capacitor values 10μF or larger are acceptable, provided the ESR is less than 1.5Ω. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described previously.

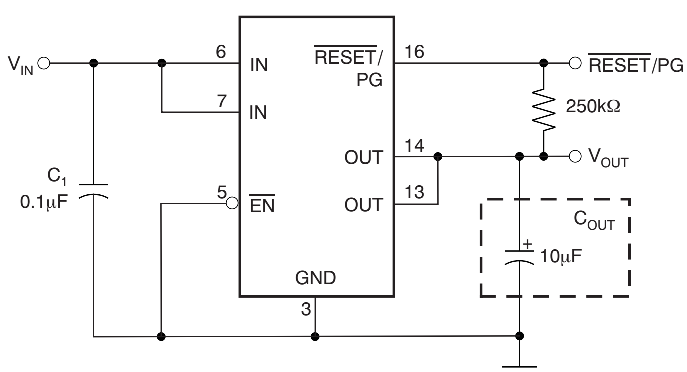


Figure 24. Typical Application Circuit (Fixed Versions)

Programming the TPS77x01 Adjustable LDO Regulator

The output voltage of the TPS77x01 adjustable regulator is programmed using an external resistor divider as shown in Figure 25. The output voltage is calculated using Equation 1:

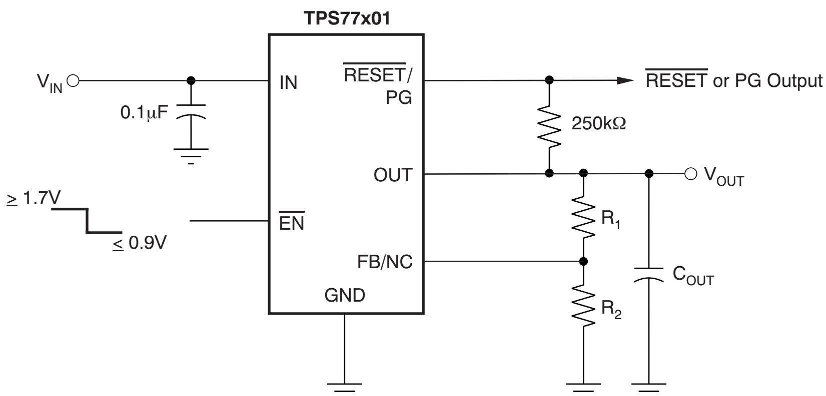
$$V_{OUT} = V_{ref} \times \left(1 + \frac{R_1}{R_2}\right) \tag{1}$$

Where:

- V_{ref} = 1.1834V typ (the internal reference voltage)

Resistors R_1 and R_2 should be chosen for approximately 10µA divider current. Lower value resistors can be used, but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R_2 = 110kΩ to set the divider current at approximately 10µA and then calculate R_1 using Equation 2:

$$R_1 = \left(\frac{V_{OUT}}{V_{ref}} - 1\right) \times R_2 \tag{2}$$



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R_1	R_2	UNIT
2.5V	121	110	kΩ
3.3V	196	110	kΩ
3.6V	226	110	kΩ
4.75V	332	110	kΩ

Figure 25. TPS77x01 Adjustable LDO Regulator Programming

Reset Indicator

The TPS775xx features a $\overline{\text{RESET}}$ output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the $\overline{\text{RESET}}$ output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. $\overline{\text{RESET}}$ can be used to drive power-on reset circuitry or as a low-battery indicator. $\overline{\text{RESET}}$ does not assert itself when the regulated output voltage falls outside the specified 2% tolerance, but instead reports an output voltage low relative to its nominal regulated value (refer to Timing Diagram for start-up sequence).

Power-Good Indicator

The TPS776xx features a power-good (PG) output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the PG output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. PG can be used to drive power-on reset circuitry or used as a low-battery indicator.

Regulator Protection

The TPS775xx and TPS776xx PMOS-pass transistors have a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (for example, during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS775xx and TPS776xx also feature internal current limiting and thermal protection. During normal operation, the TPS775xx and TPS776xx limit output current to approximately 1.7A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds +150°C(typ), thermal-protection circuitry shuts it down. Once the device has cooled below +130°C(typ), regulator operation resumes.

Power Dissipation and Junction Temperature

Specified regulator operation is assured to a junction temperature of +125°C; the maximum junction temperature should be restricted to +125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

where:

- $T_{J(max)}$ is the maximum allowable junction temperature
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, and is calculated as $\frac{1}{\text{derating factor}}$ from the dissipation rating tables
- T_A is the ambient temperature

The regulator dissipation is calculated using:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.