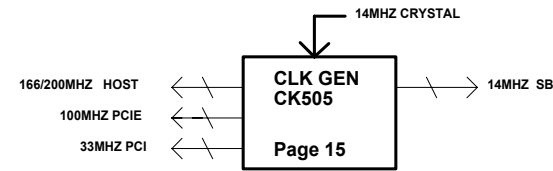
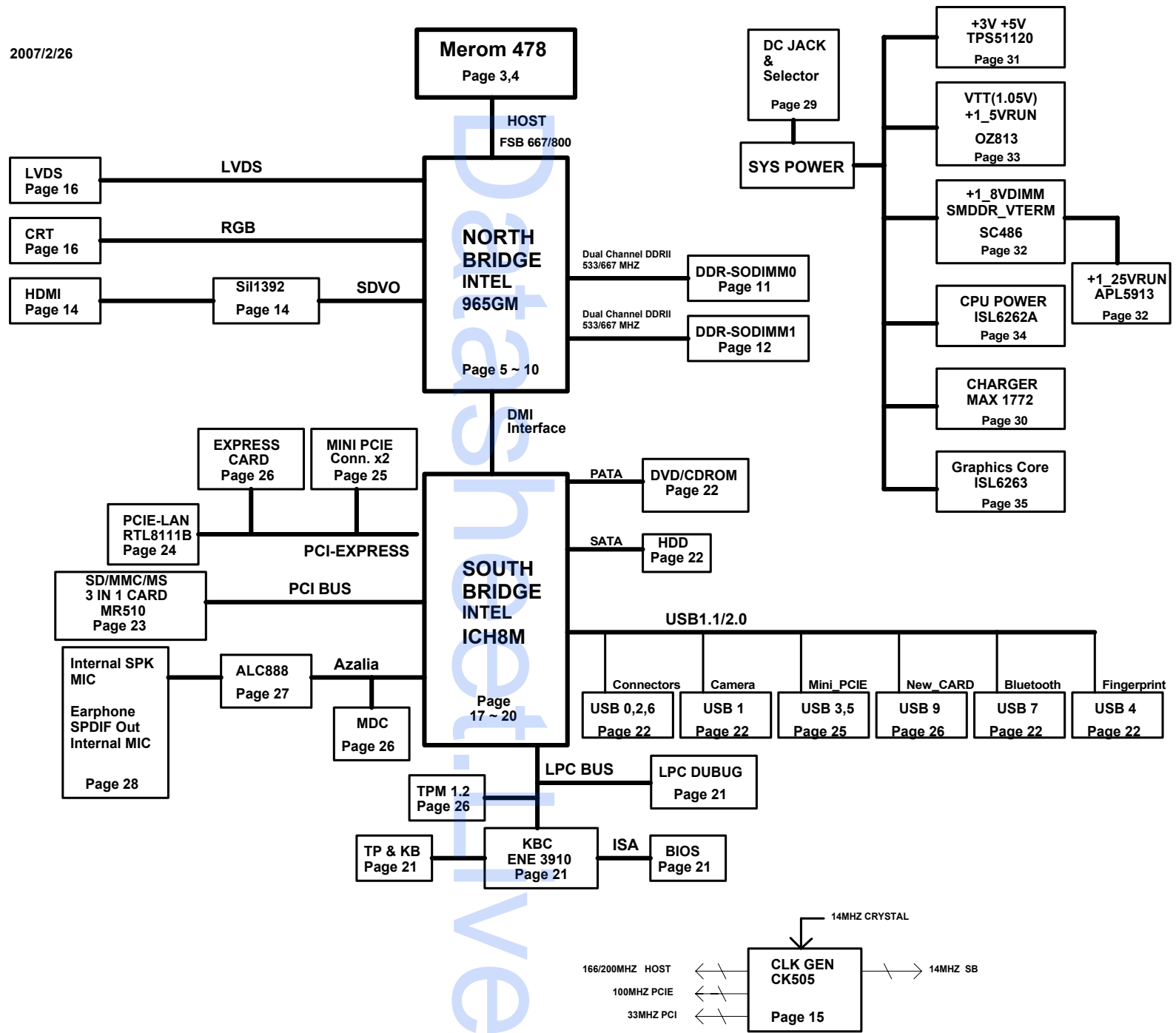


- 01 : BLOCK DIAGRAM
- 02 : PLATFORM
- 03 : Merom-1 CPU (HOST BUS)
- 04 : Merom-2 CPU (POWER/GND)
- 05 : 965GM-1 (HOST)
- 06 : 965GM-2 (DMI / VGA)
- 07 : 965GM-3 (DDR2)
- 08 : 965GM-4 (Power-1)
- 09 : 965GM-5 (Power-2)
- 10 : 965GM-6 (GND)
- 11 : DDR2\_SODIMM0
- 12 : DDR2\_SODIMM1
- 13 : DDR2\_Termination
- 14 : SDVO- SiI1392
- 15 : CLOCK GEN (CK505)
- 16 : VGA, LVDS ,BL
- 17 : ICH8M-1 (CPU/IDE/Azalia)
- 18 : ICH8M-2 (PCI/USB/PCIE/DMI)
- 19 : ICH8M-3 (SM BUS/GPIO)
- 20 : ICH8M-4 (POWER/GND)
- 21 : ENE3910( KBC ) & BIOS
- 22 : HDD,CDROM,CIR,USB CONN.
- 23 : Card Reader (MR510)
- 24 : PCIE LAN (RTL 8111B)
- 25 : MINI\_PCIE, LED, SW
- 26 : NEWCARD, MDC, TPM, FAN
- 27 : AZALIA CODEC(ALC888)
- 28 : Audio Amp. & Jacks
- 29 : M\_Battery Select
- 30 : M\_Battery Charger
- 31 : M\_System Power
- 32 : DDR2 RAM POWER, +1.25V
- 33 : M\_VTT, +1.5V
- 34 : M\_CPU power
- 35 : M\_Graphics Core
- 36 : Screw / EMI
- 37 : Non-Footprint for BOM
- 38 : KBC\_CTR\_PWR\_BD
- 39 : Power Sequency
- 40 : Change History



## Voltage Rails

Voltage	Description	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
VHCORE	Core Voltage for Processor	VR_ON
VTT	1.05 rail for Processor & 965GM I/O	RUN_ON
+1_5VRUN	1.5V switched power rail (off in S3-S5)	RUN_ON
+2_5VRUN	2.5V powe rail for CH7315A (off in S3-S5)	+3VRUN
+3VRUN	3.3V switched power rail (off in S3-S5)	RUN_ON
+5VRUN	5.0V switched power rail (off in S3-S5)	RUN_ON
SMDDR_VTERM	0.9V DDR Termination voltage (off in S4-S5)	DIMM_ON
+1_8VDIMM	1.8V power rail DDR (off in S4-S5)	DIMM_ON
+3VSUS	3.3V power rail (off in S4-S5)	SUS_ON
+5VSUS	5.0V power rail (off in S4-S5)	SUS_ON
+3VALW	3.3V always on power rail	PWR_SRC
+5VALW	5.0V always on power rail	PWR_SRC
ADD5V	5.0V Power rail Audio codec(off in S3-S5)	+5VRUN
+1_25VRUN	1.25V LDO power rail (off in S3-S5)	RUN_ON
+VGF_X_CORE	Graphic core of GMCH switched power rail (off in S3-S5)	GFX_VR_EN

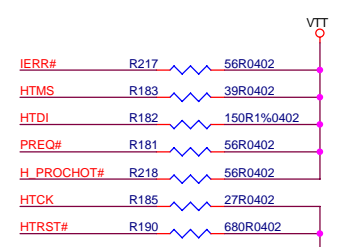
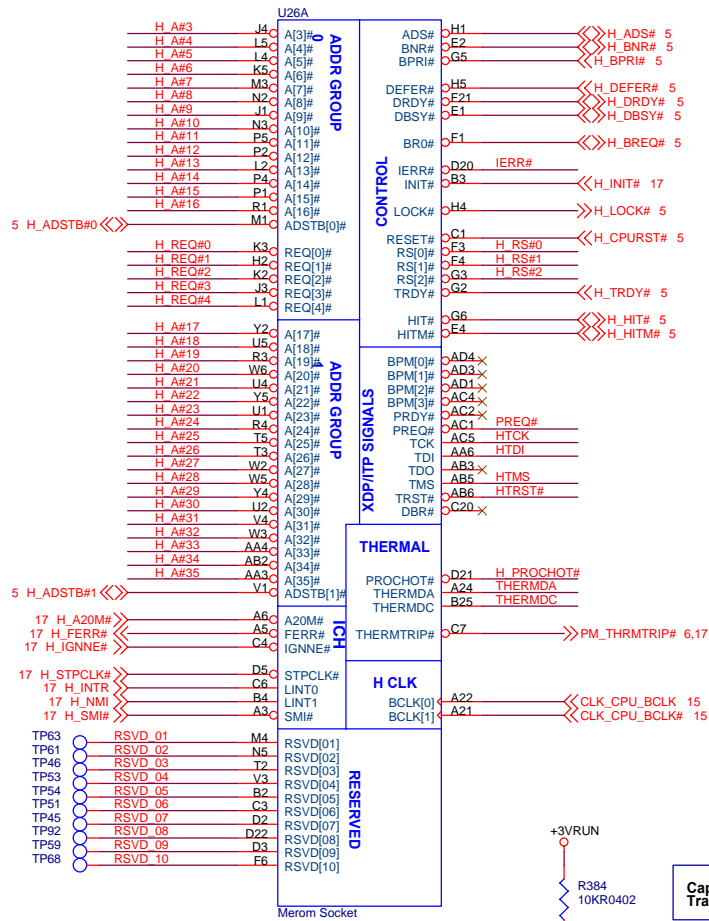
## POWER STATES

SIGNAL STATE	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALWAYS	+V*SUS	+V*RUN	Clocks
S0( Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1M(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	OFF
S3( Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4( Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 / Soft OFF	LOW	LOW	LOW	ON	OFF	OFF	OFF

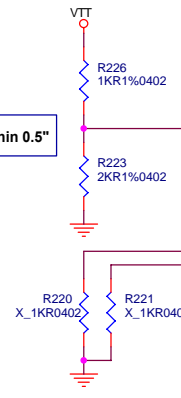
Note : WHEN AC MODE , System turn on then +V\*SUS will always keep high

<b>MSI CORPORATION</b>		
Title		
<b>PLATFORM</b>		
Size	Document Number	Rev
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5 H\_A#[35:3] <<> H\_A#[35:3]  
 5 H\_RS#[2:0] <<> H\_RS#[2:0]  
 5 H\_REQ#[4:0] <<> H\_REQ#[4:0]

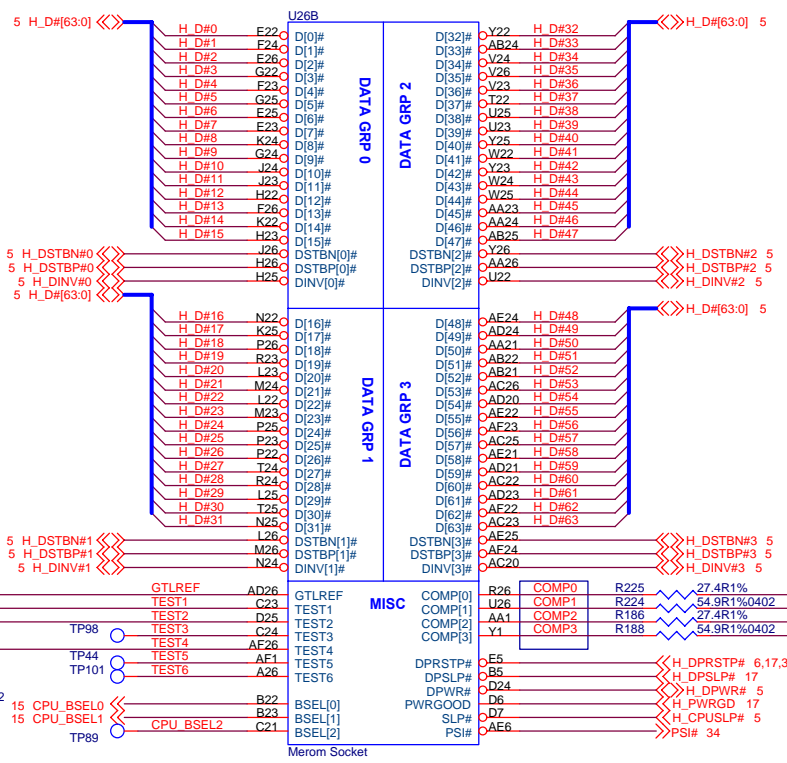
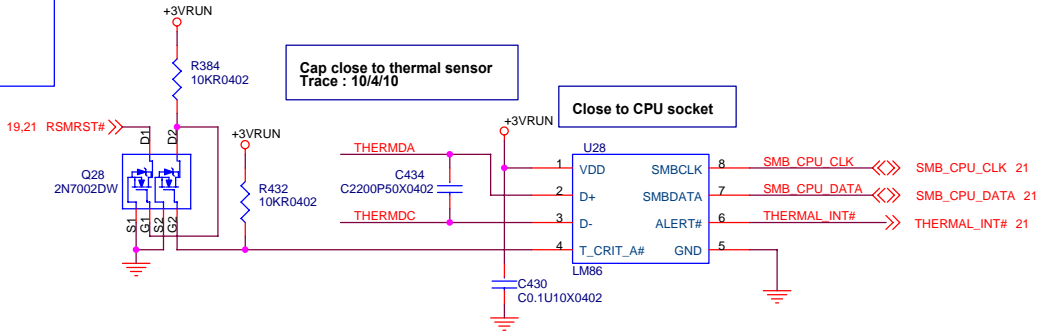


Within 0.5"



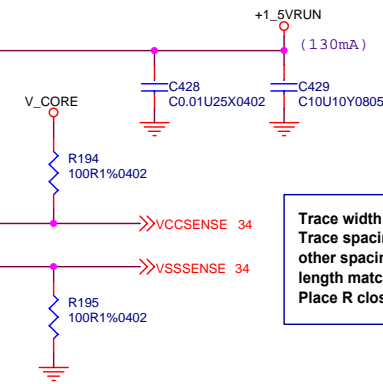
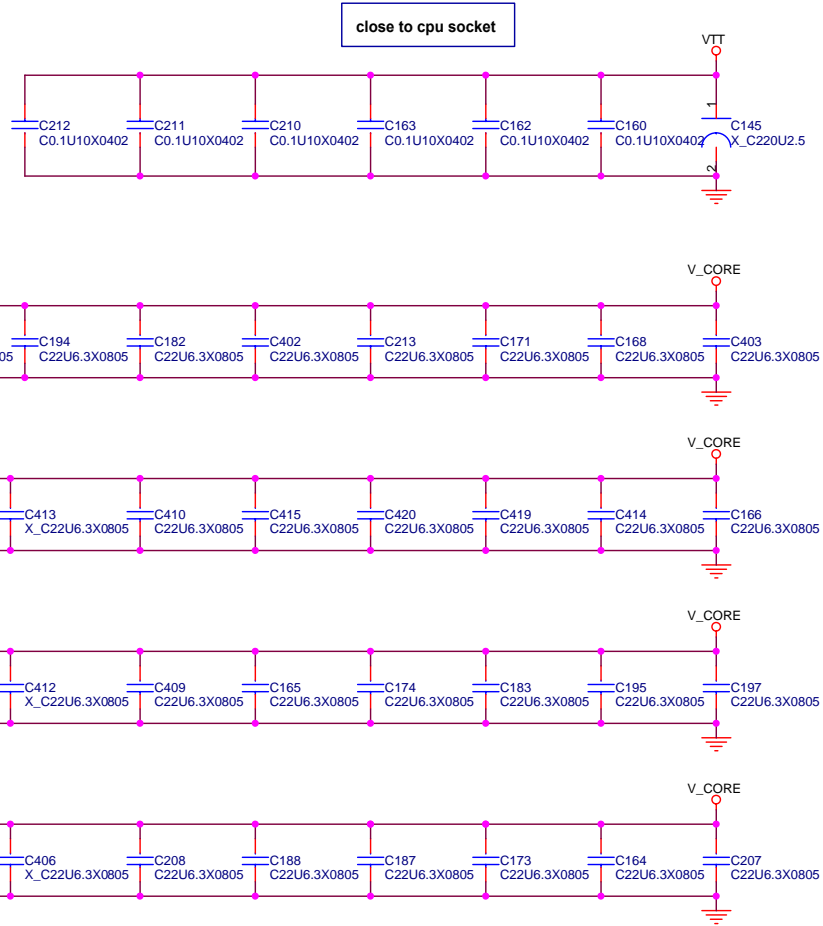
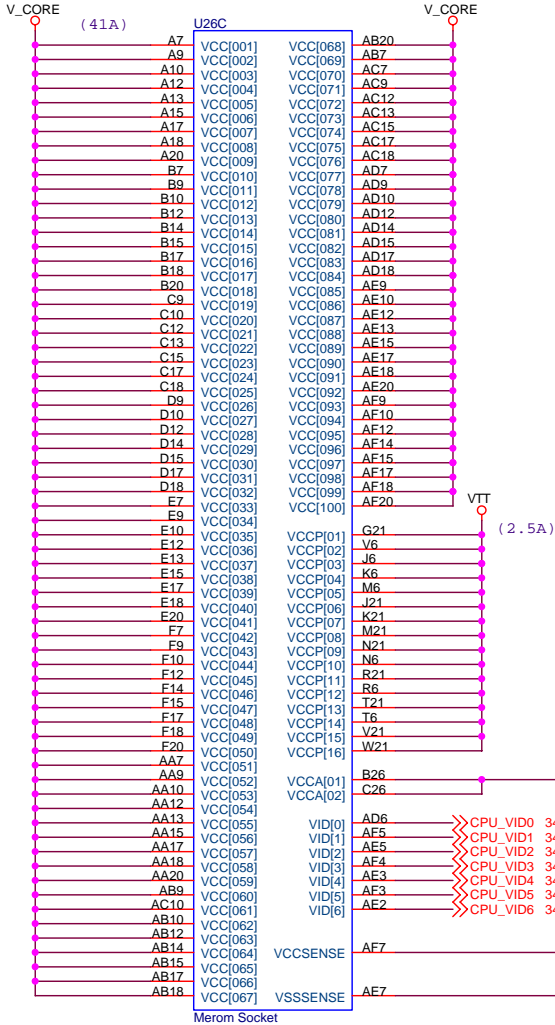
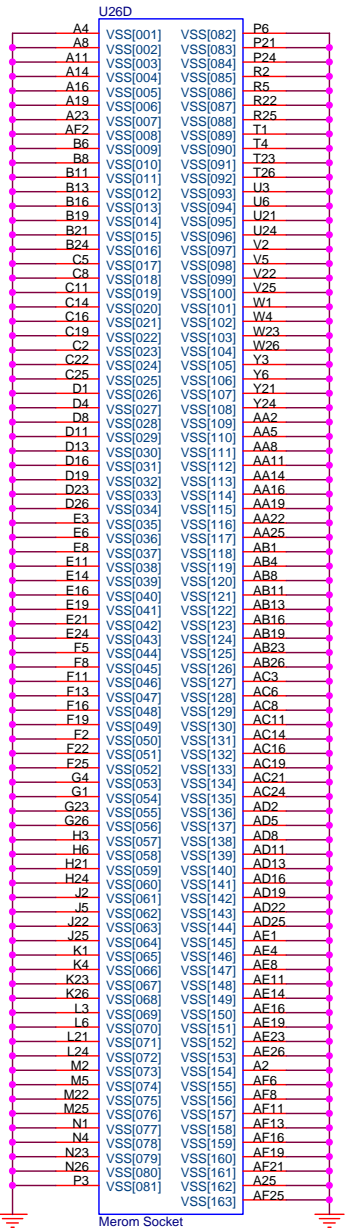
Cap close to thermal sensor  
Trace : 10/4/10

Close to CPU socket



Within 0.5"  
25mils Spacing  
COMP0,2 -> 18mils  
COMP1,3 -> 5mils

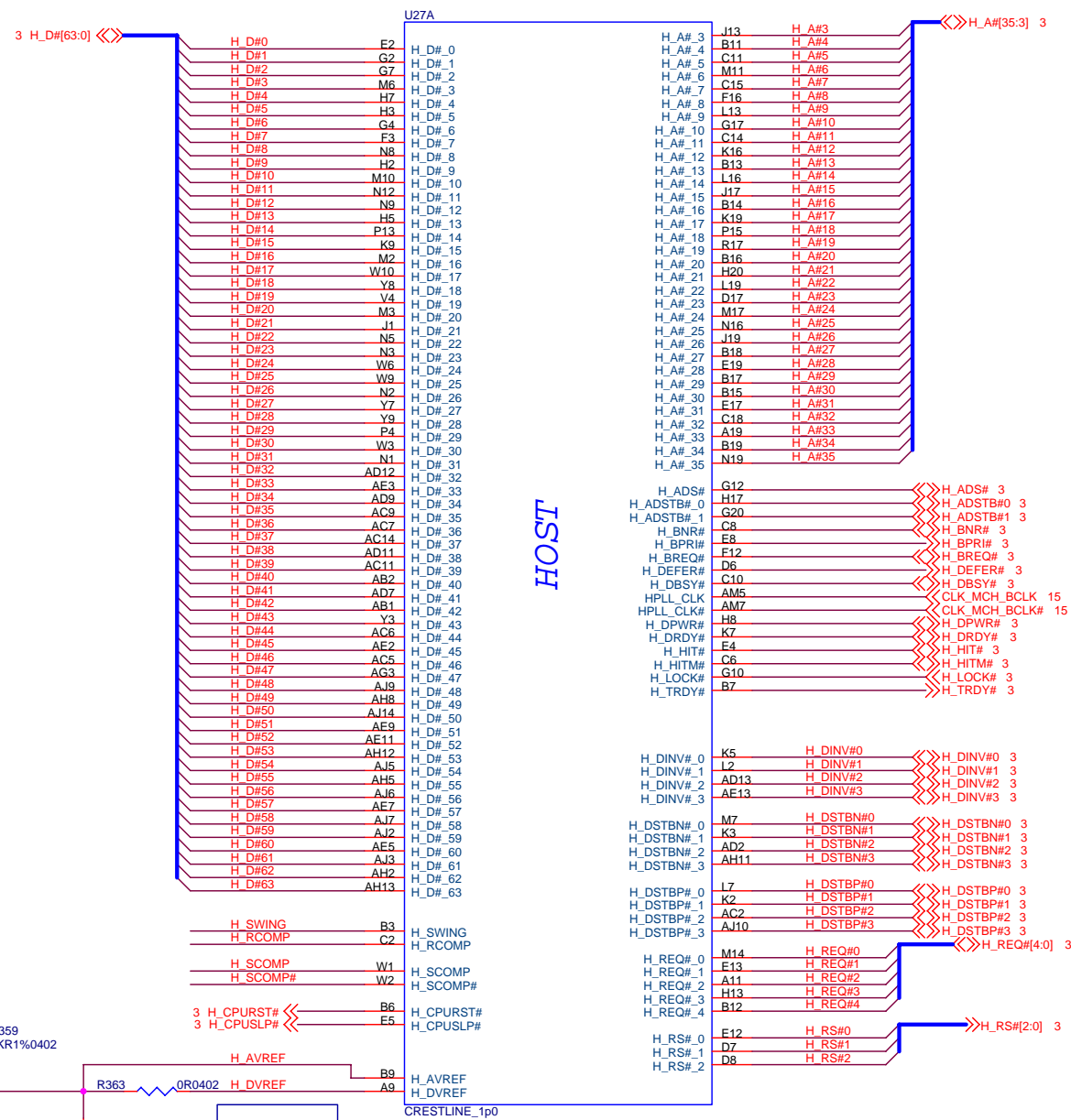
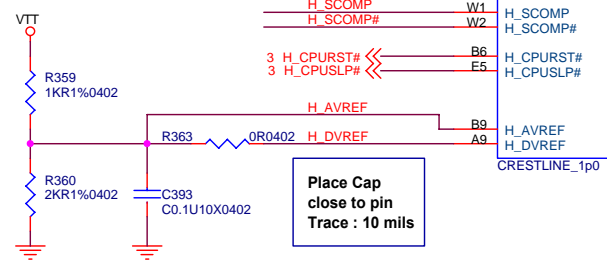
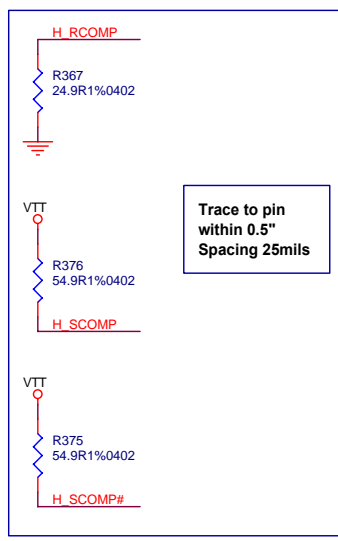
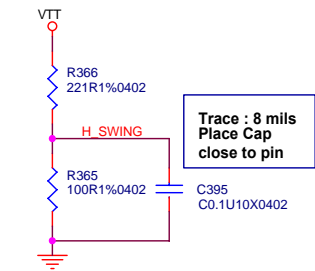
MSI CORPORATION			
Title: Merom-1 (HOST BUS)			
Size:	Document Number:	Rev: 1.0	
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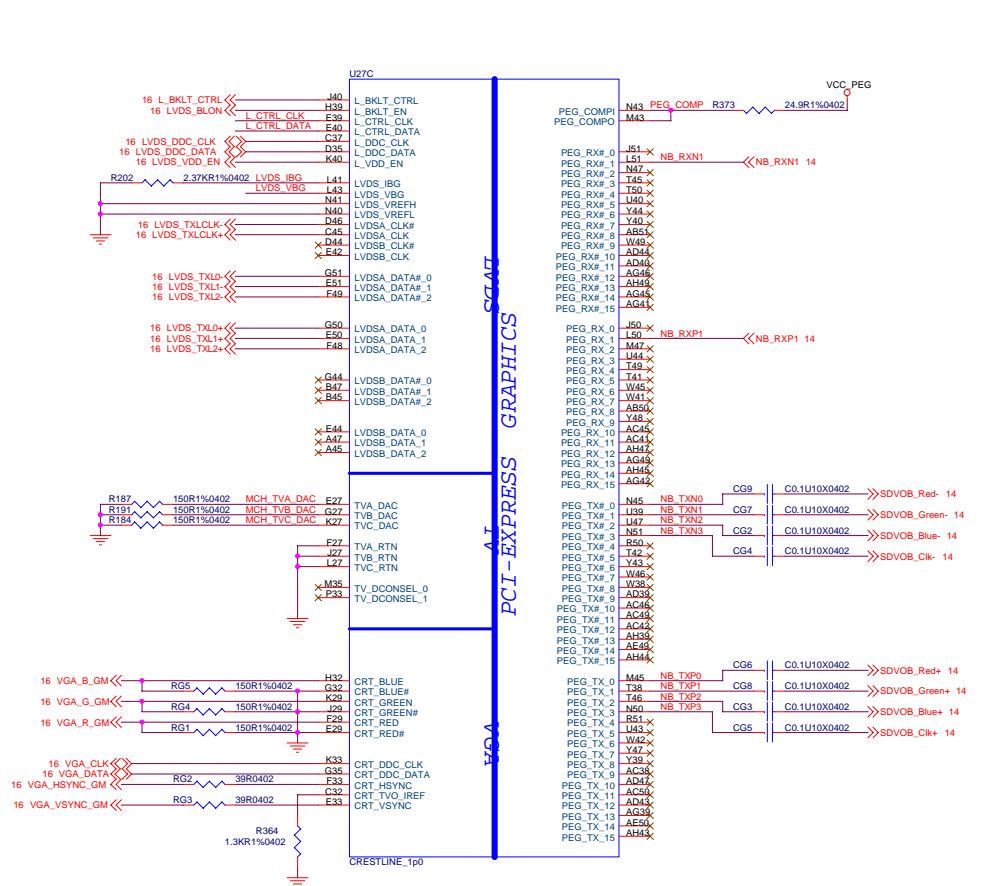
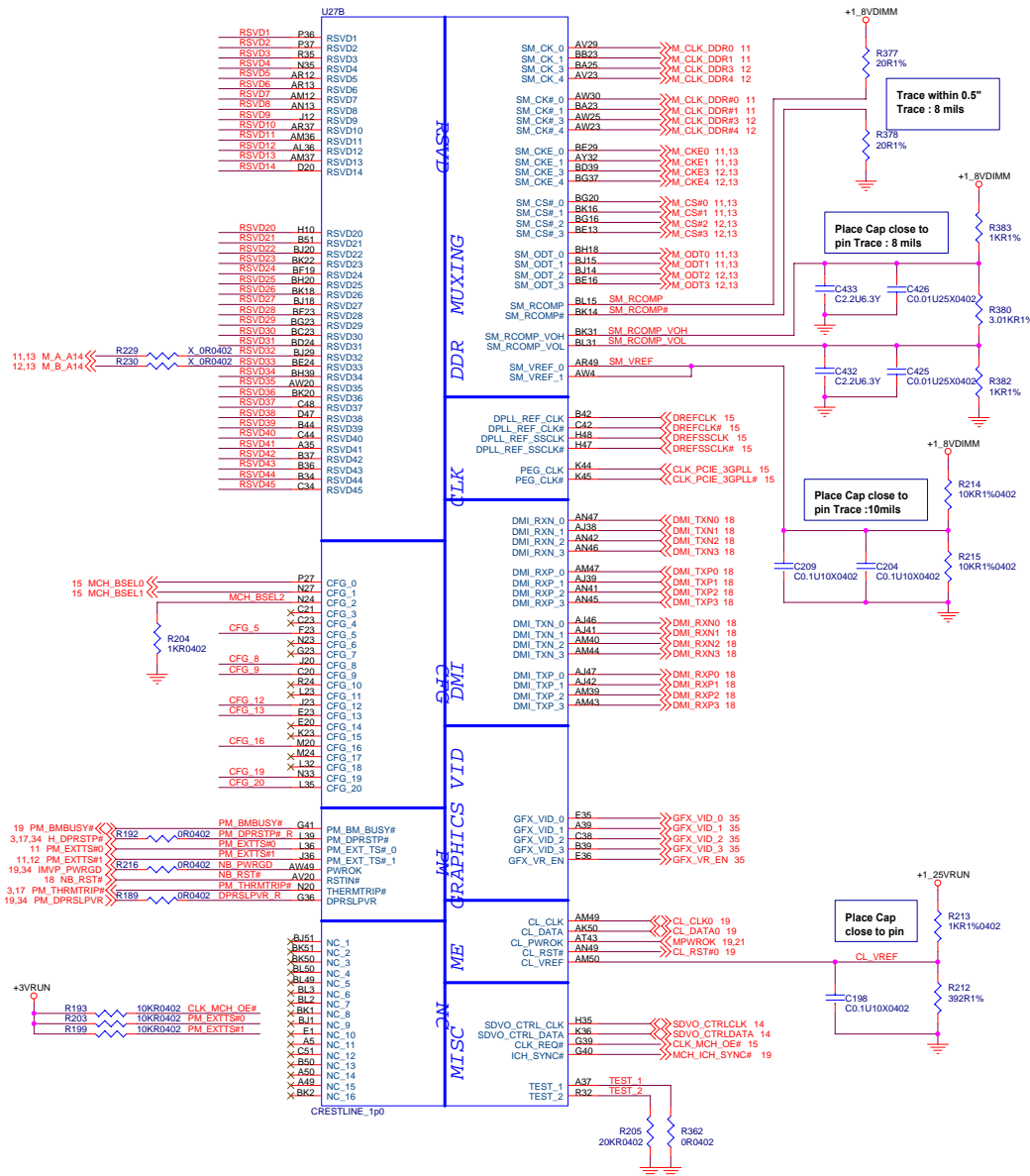
Place Cap close to pin  
Trace width > 20

Trace width = 18mils  
Trace spacing = 7mils  
other spacing = 50mils  
length matched within 25mils  
Place R close to CPU within 1"

<b>MSI CORPORATION</b>		
Title: <b>Merom-2 (POWER/GND)</b>		
Size: Custom	Document Number: <b>MS-1221</b>	Rev: 1.0
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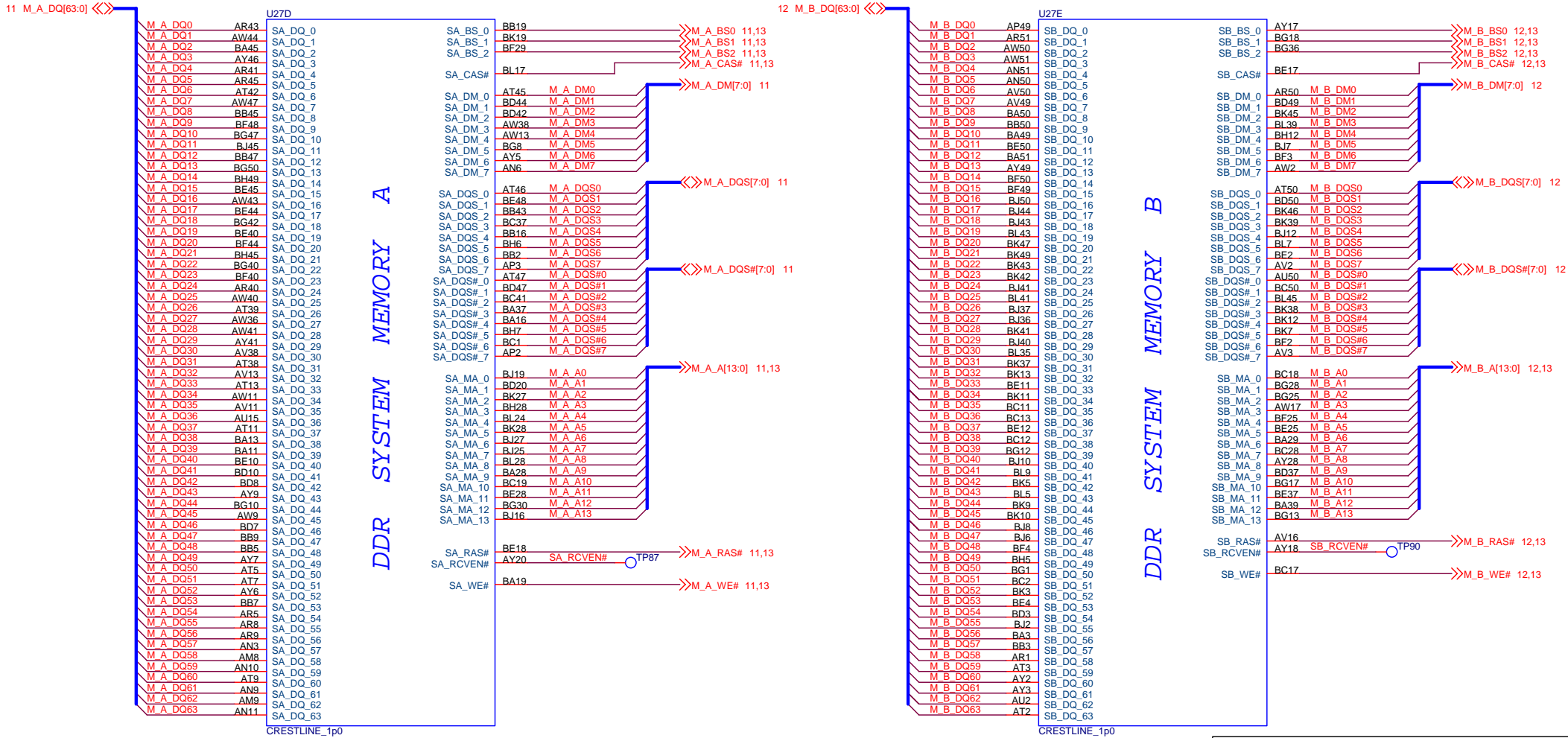
<b>MSI CORPORATION</b>		
<b>CRESTLINE-1 (HOST BUS)</b>		
Title		
Size	Document Number	Rev
B	<b>MS-1221</b>	1.0
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**Strapping Configuration**

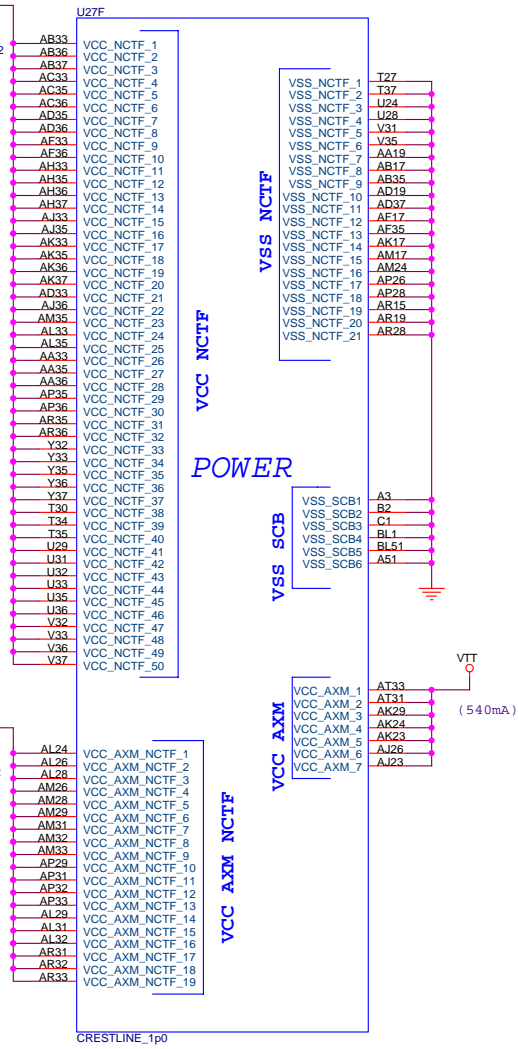
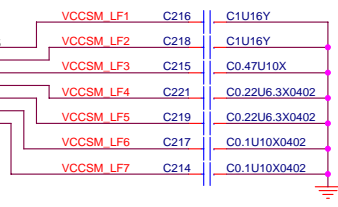
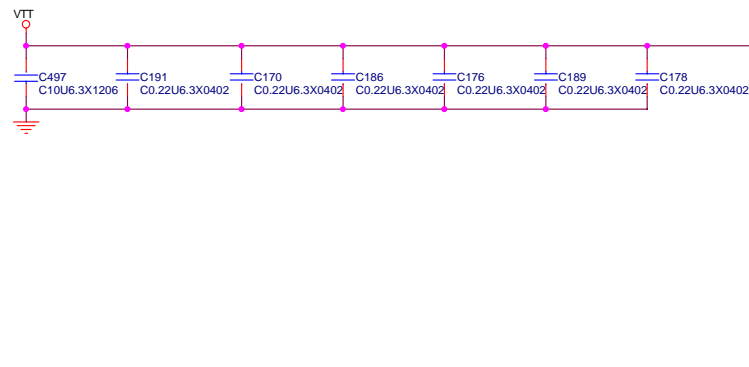
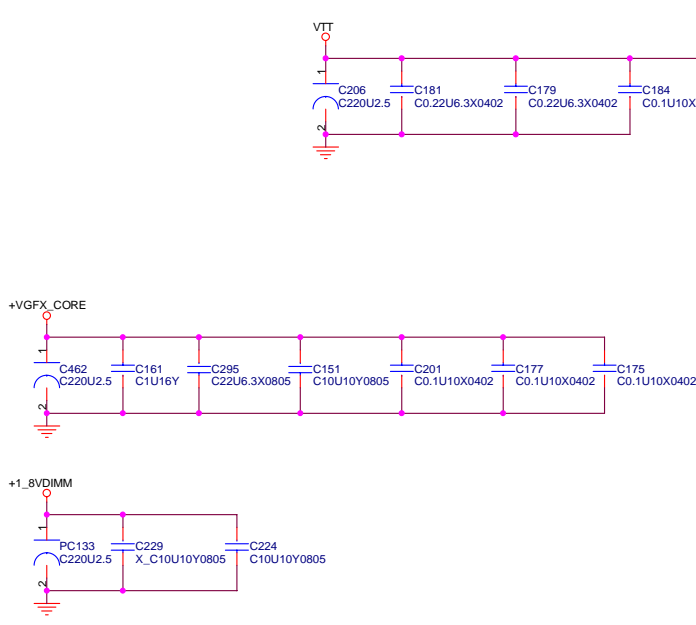
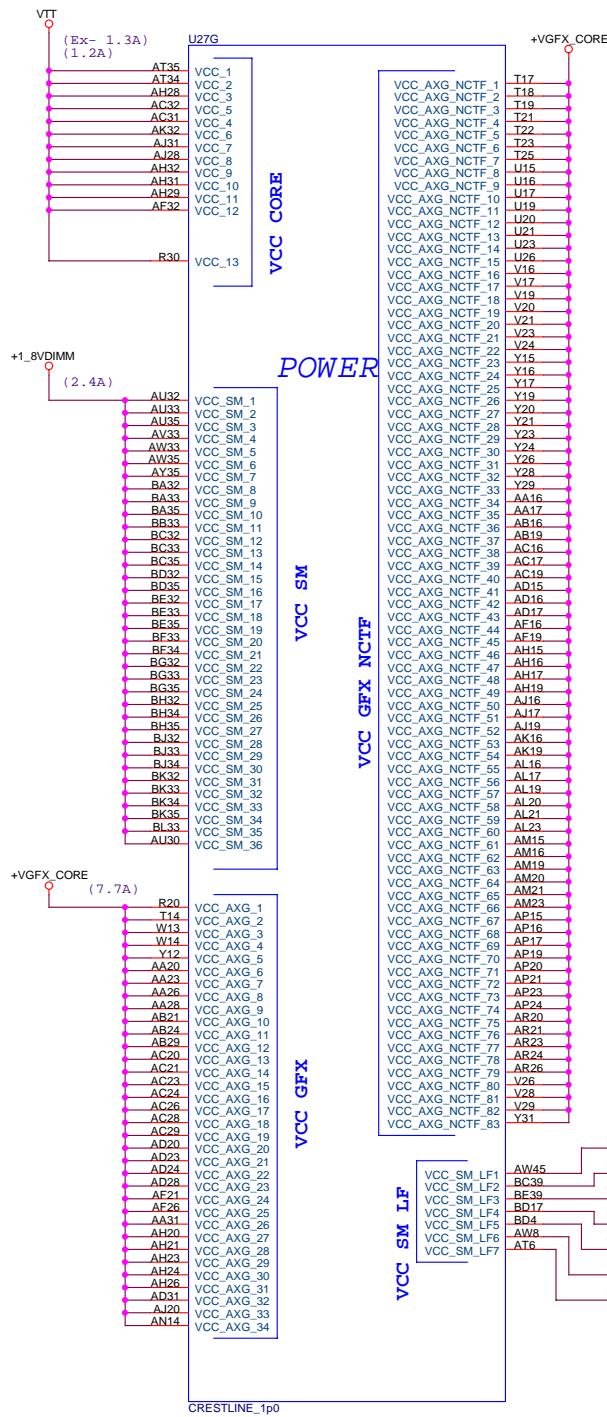
CFG5 (Default=High)	CFG9 (Default=High)	CFG16 (Default=High)	CFG19 (Default=Low)	CFG20 (Default=Low)
DMI*4	PCIe Graphics Lane: Normal Operation	Dynamic ODT Enabled	DMI Lane Reverse: Normal Operation	Only SDVO or PCIe is operational

<b>MSI CORPORATION</b>	
<b>CRESTLINE-2 (DMI/VGA)</b>	
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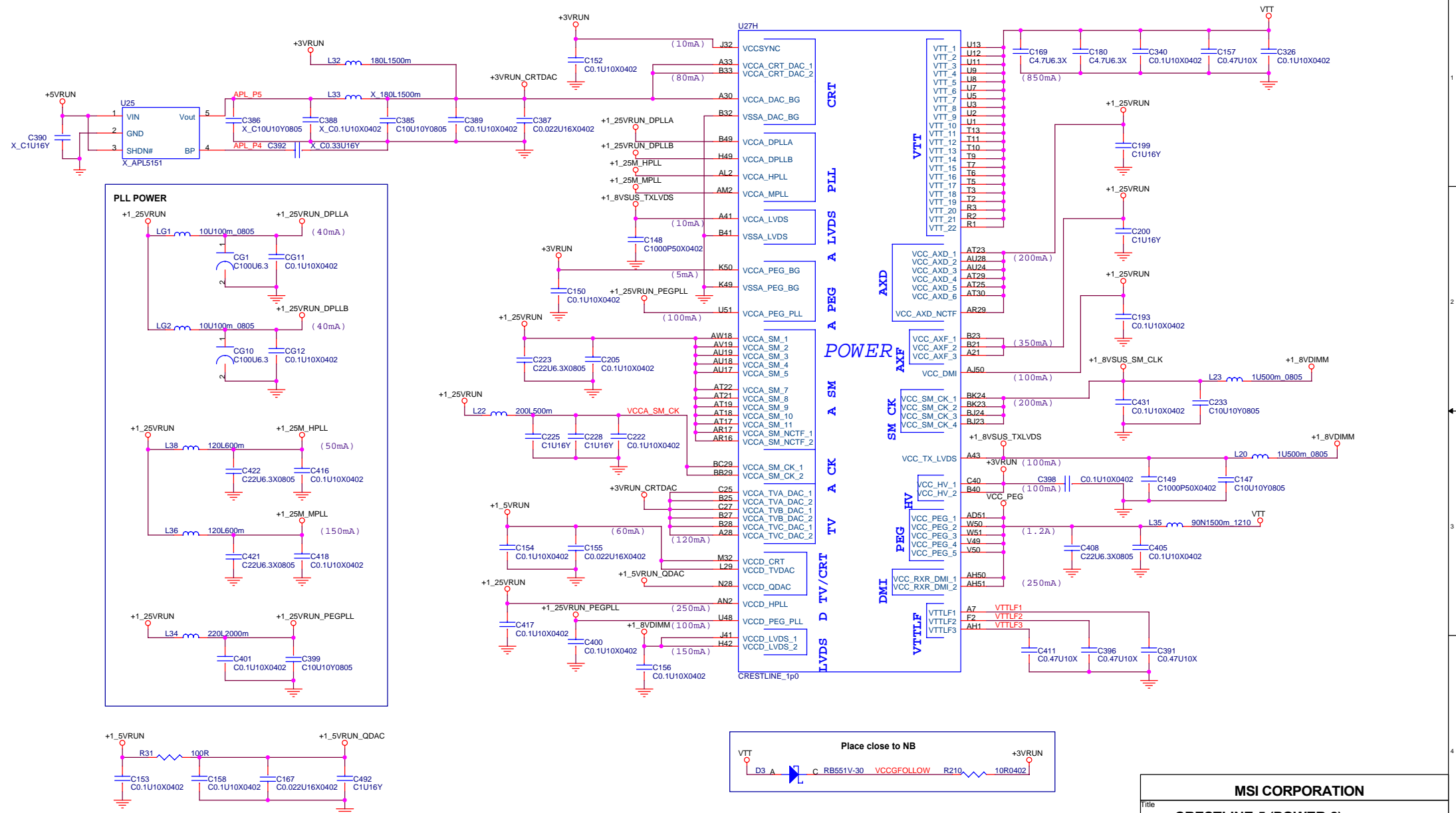
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Title			
<b>CRESTLINE-3 (DDR)</b>			
Size	Document Number	Rev	
Custom	<b>MS-1221</b>	1.0	
Date:	Friday, March 16, 2007	Sheet	7 of 41



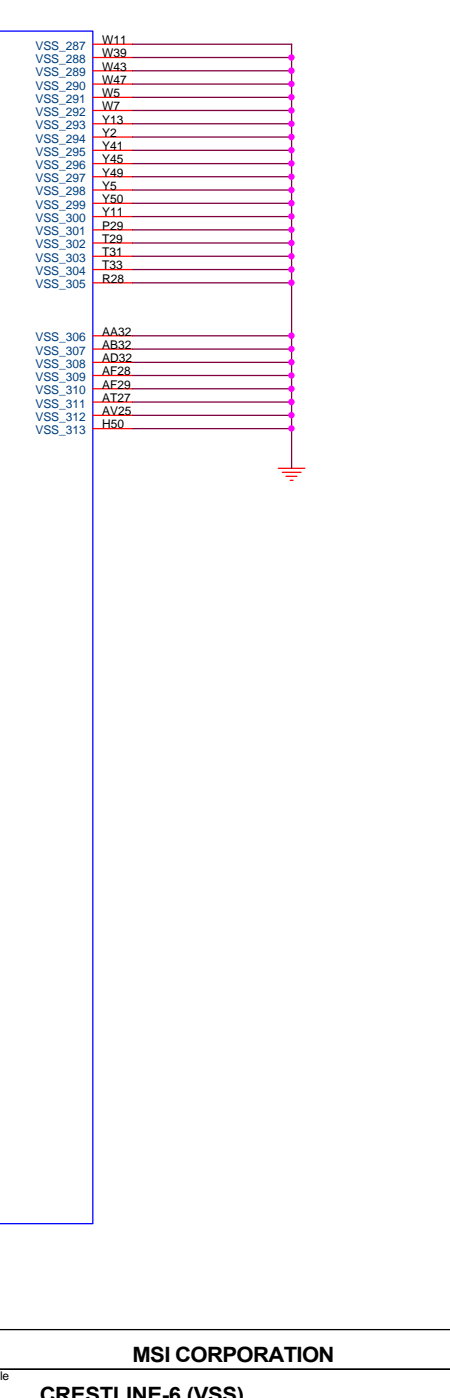
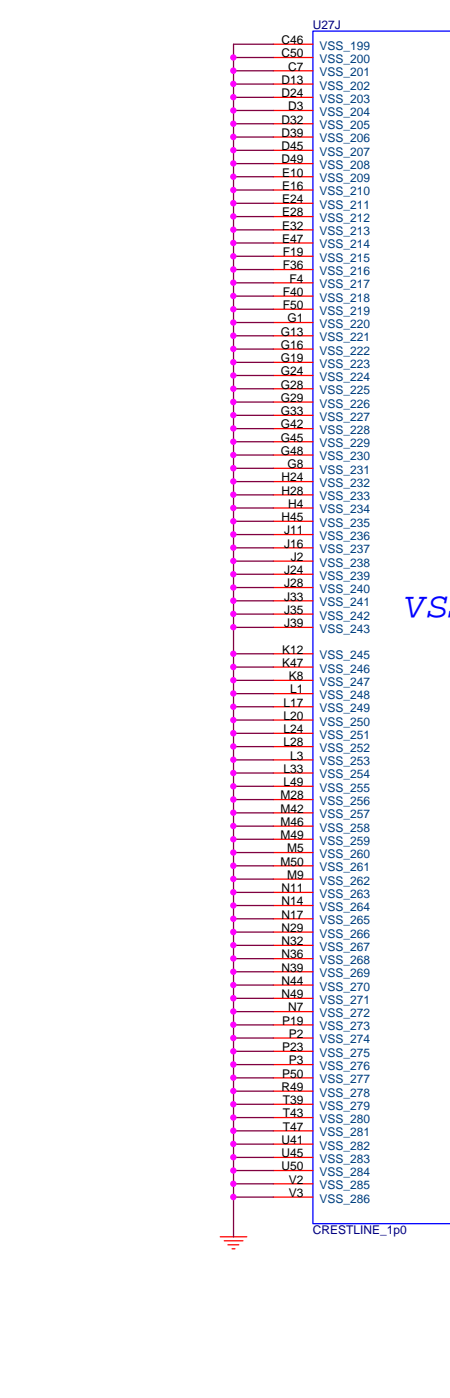
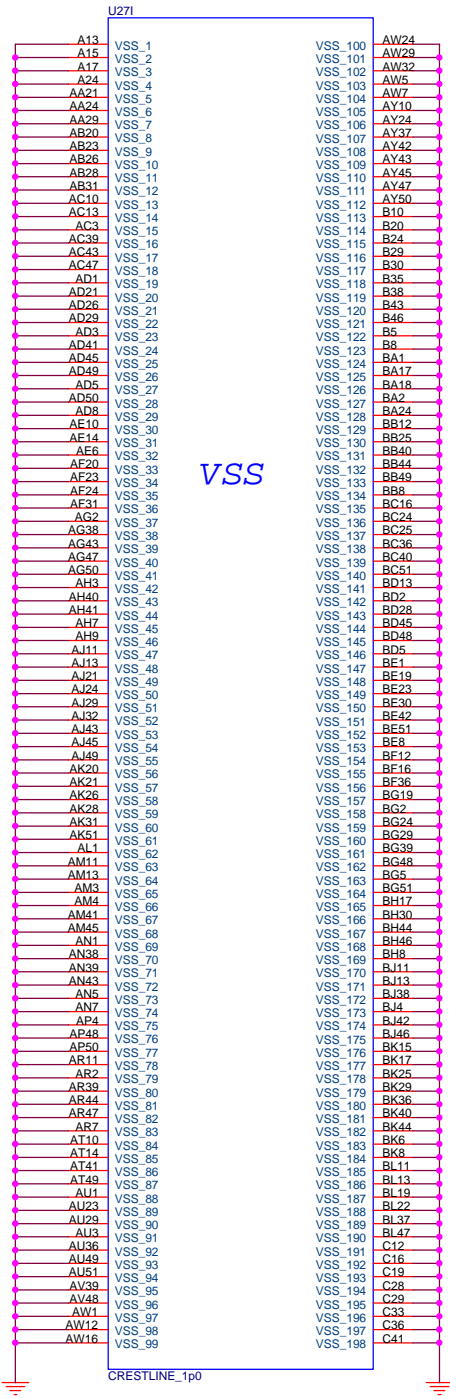


<b>MSI CORPORATION</b>			
Title			
<b>CRESTLINE-4 (POWER-1)</b>			
Size	Document Number	Rev	
Custom	<b>MS-1221</b>	1.0	
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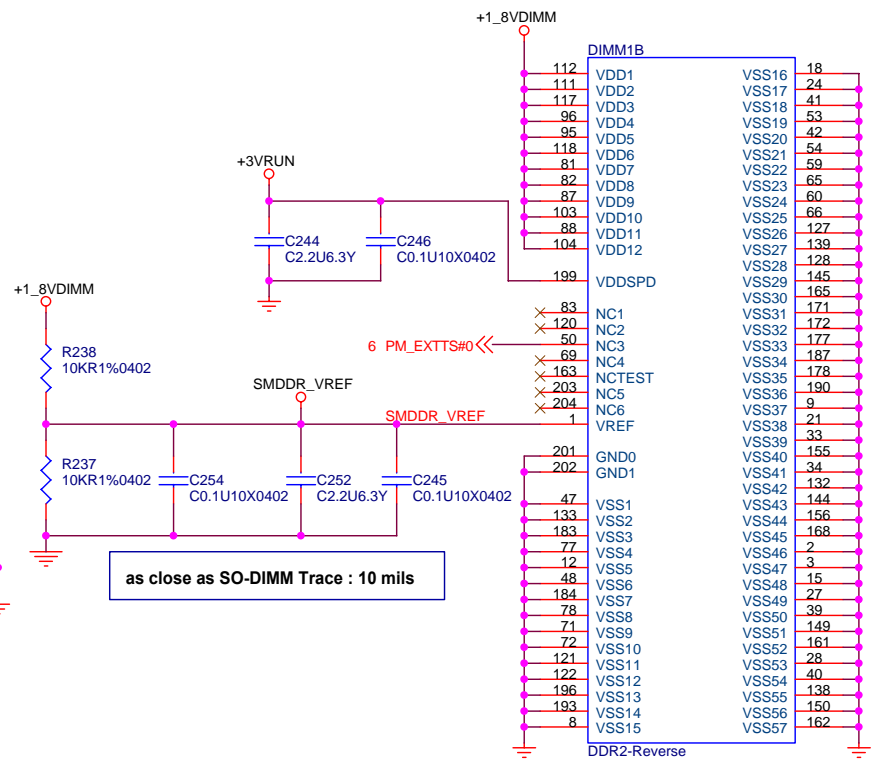
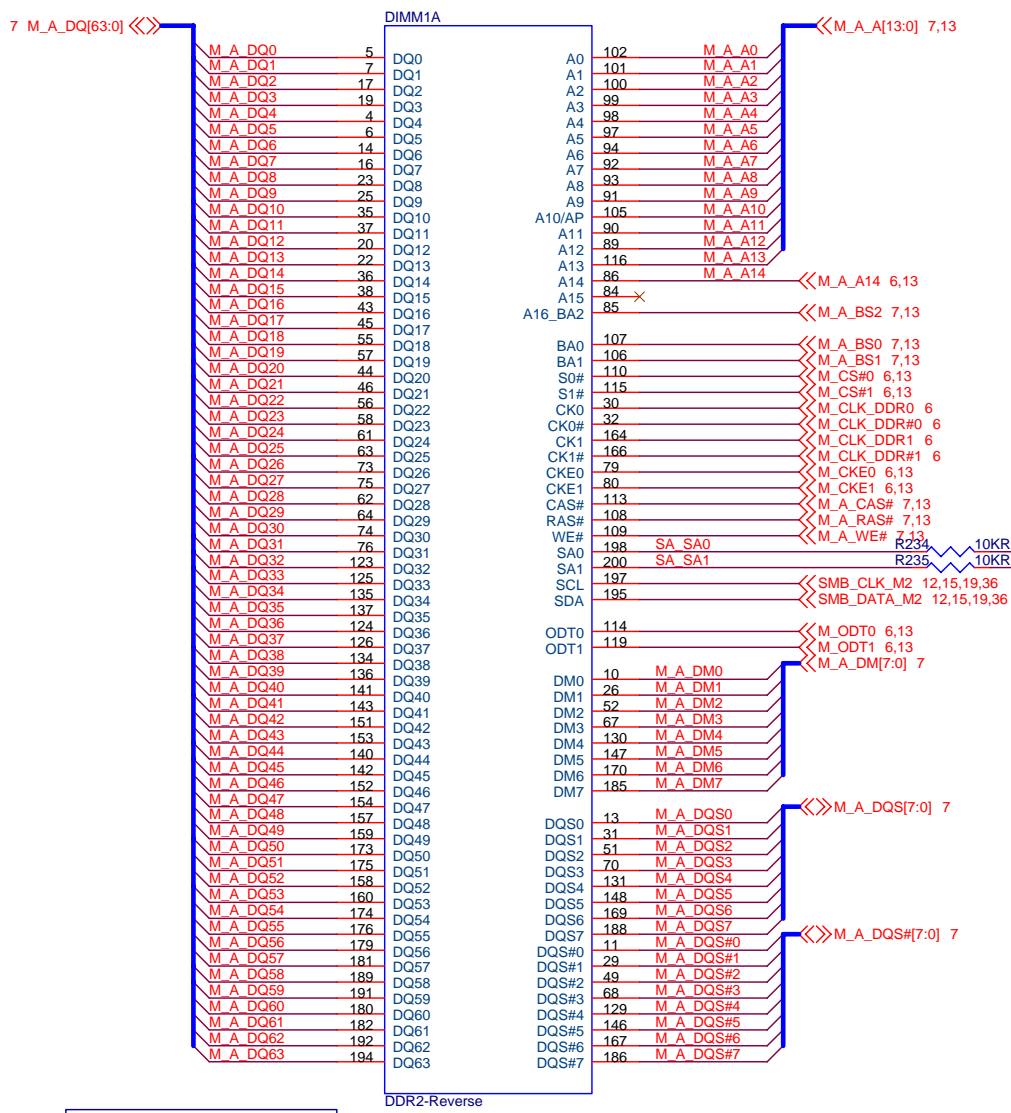




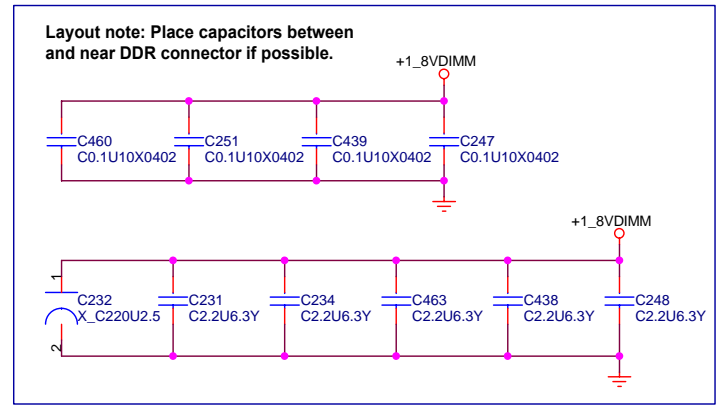
<b>MSI CORPORATION</b>		
Title		
<b>CRESTLINE-5 (POWER-2)</b>		
Size	Document Number	Rev
Custom	<b>MS-1221</b>	1.0
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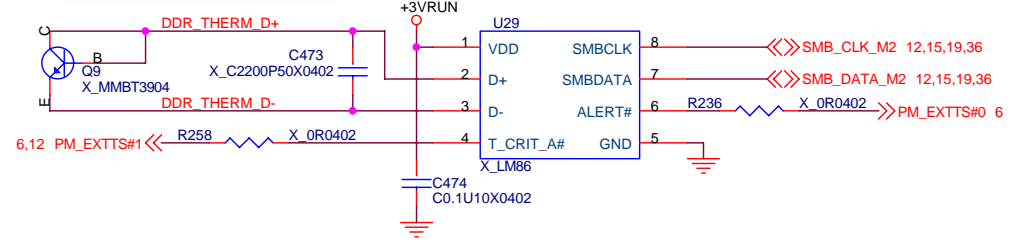
<b>MSI CORPORATION</b>		
Title		
<b>CRESTLINE-6 (VSS)</b>		
Size	Document Number	Rev
Custom	<b>MS-1221</b>	1.0
Date:	Monday, March 26, 2007	Sheet 10 of 41



as close as SO-DIMM Trace : 10 mils

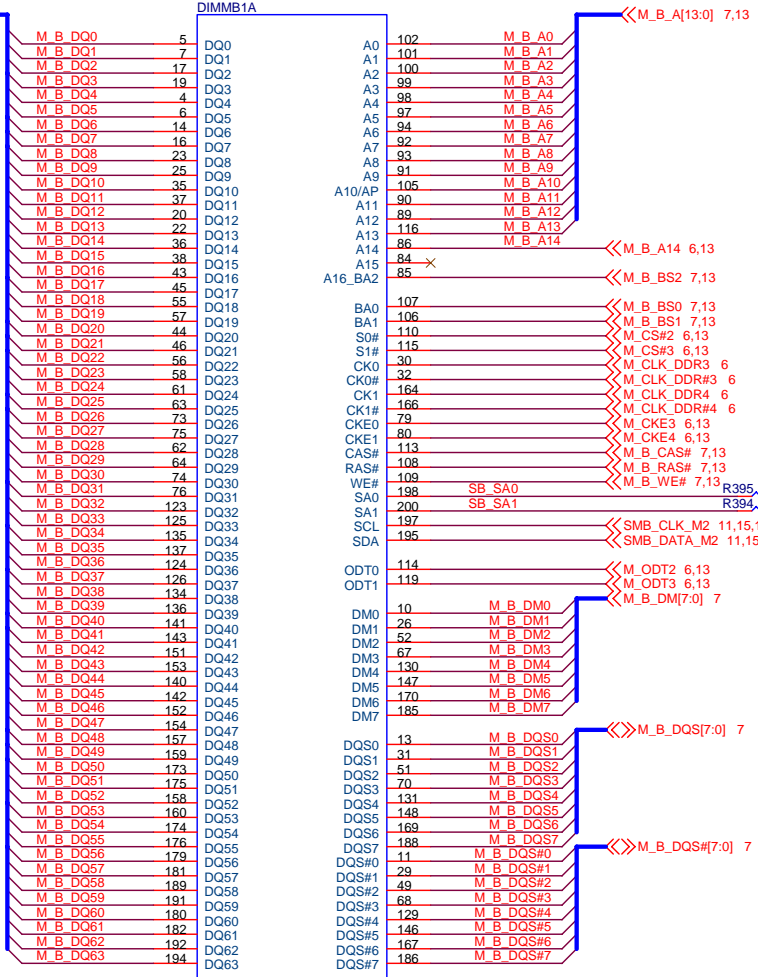


Cap close to thermal sensor  
Trace : 10/4/10

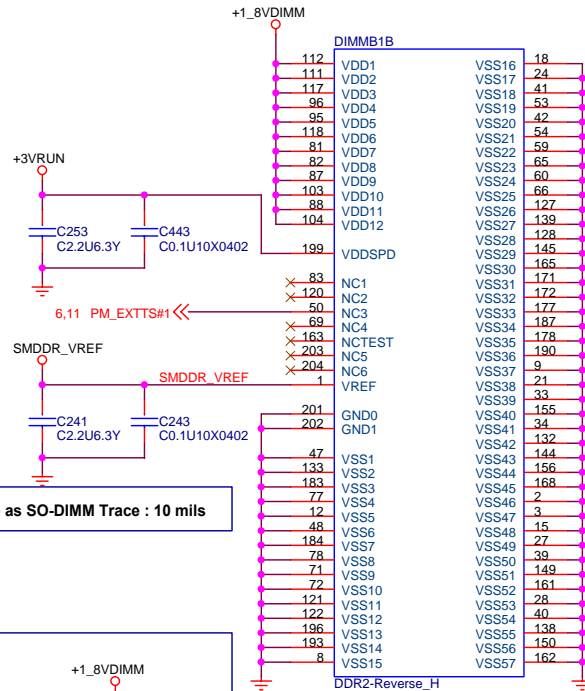


<b>MSI CORPORATION</b>		
<b>DDR2 SODIMM 0</b>		
Title	Document Number	Rev
	Custom <b>MS-1221</b>	1.0
Date:	Tuesday, March 13, 2007	Sheet 11 of 41

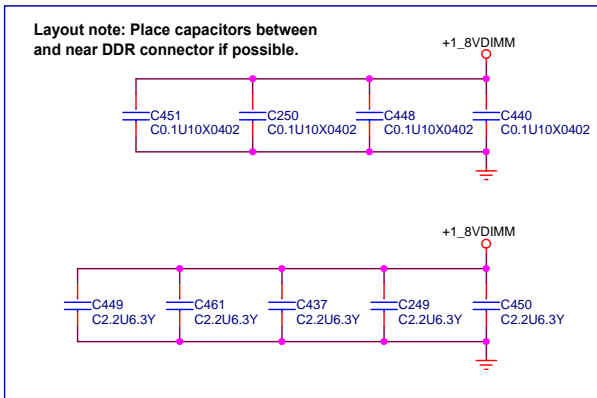
7 M\_B\_DQ[63:0] <<>



DDR2-Reverse\_H

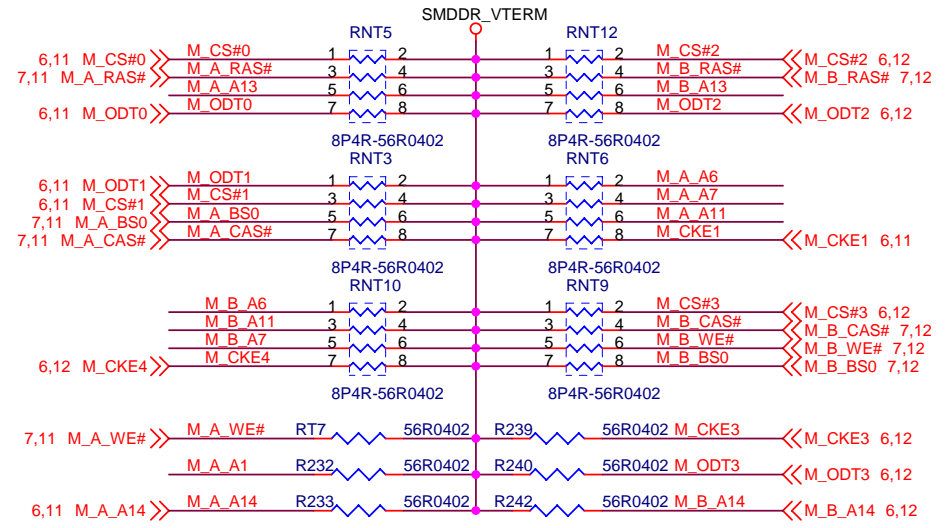
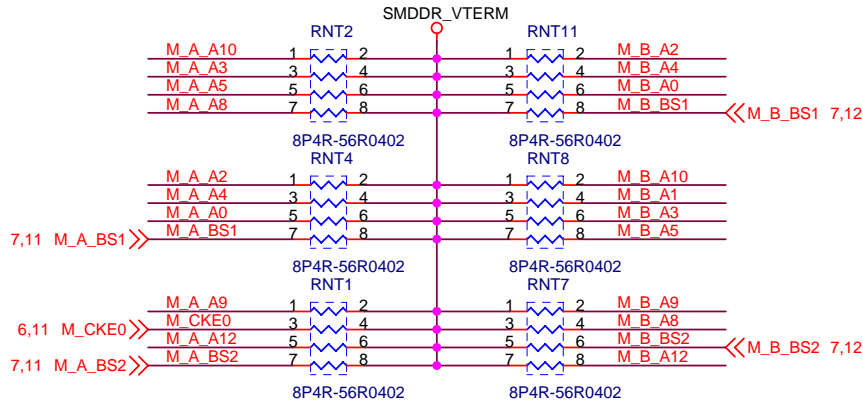


as close as SO-DIMM Trace : 10 mils

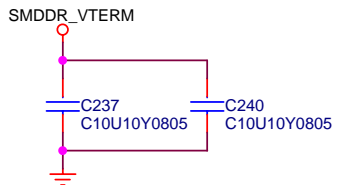
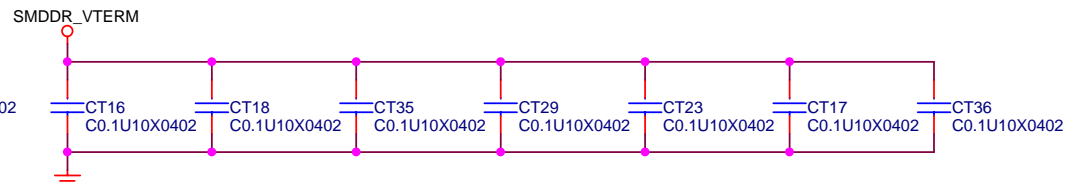
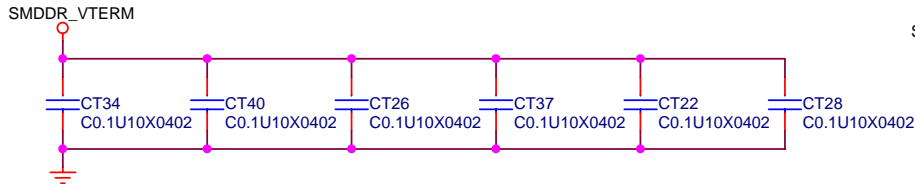
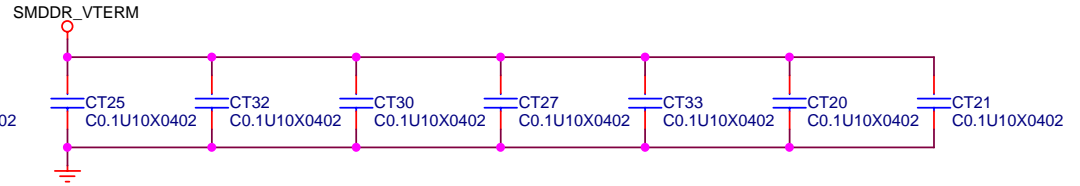
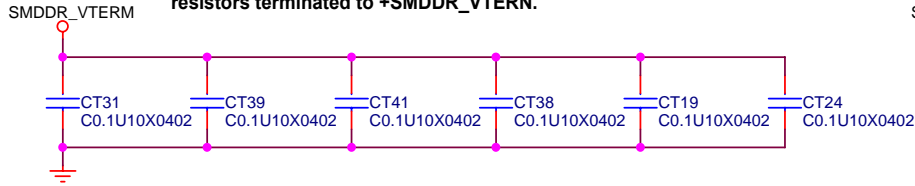


MSI CORPORATION			
Title			
DDR2 SODIMM 1			
Size	Document Number	Rev	
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M\_A A[13:0] <<M\_A\_A[13:0] 7,11  
 M\_B A[13:0] <<M\_B\_A[13:0] 7,12



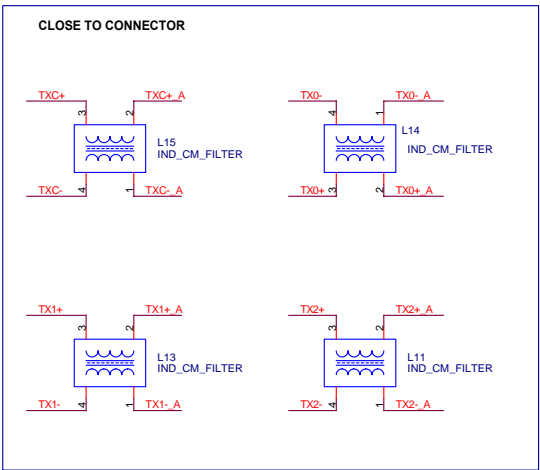
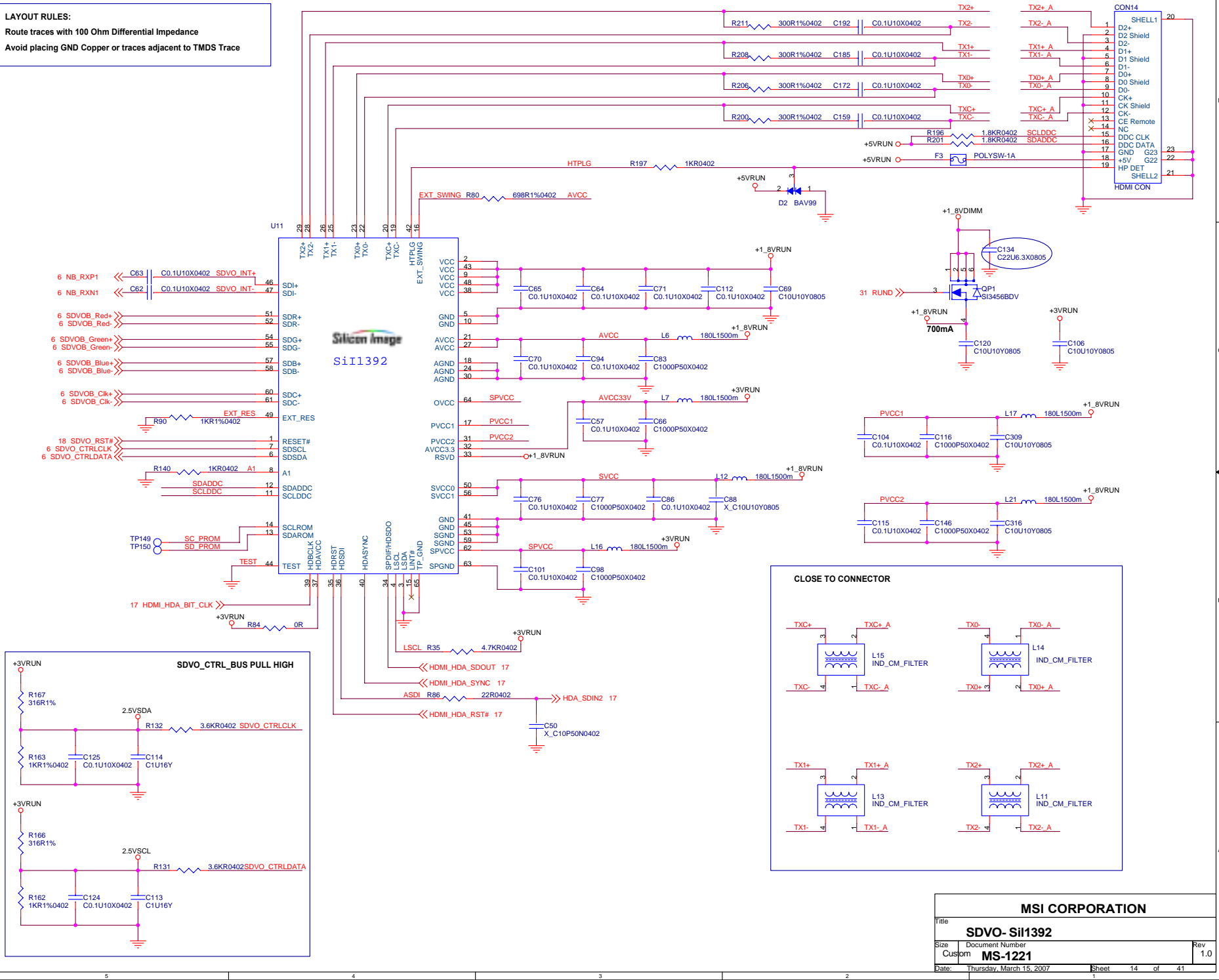
Layout note: Place one cap close to every 2 pullup resistors terminated to +SMDDR\_VTERM.



MSI CORPORATION

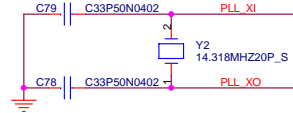
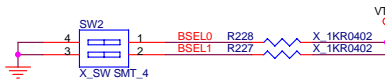
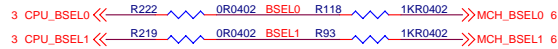
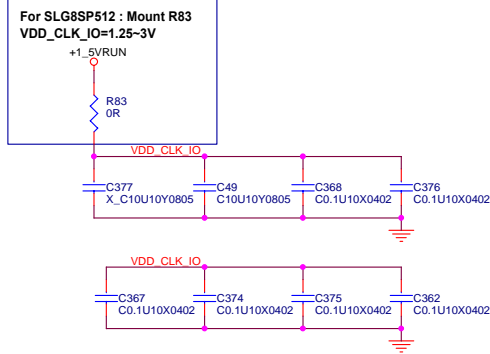
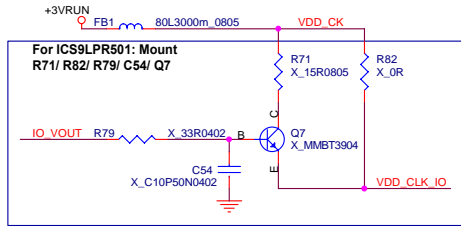
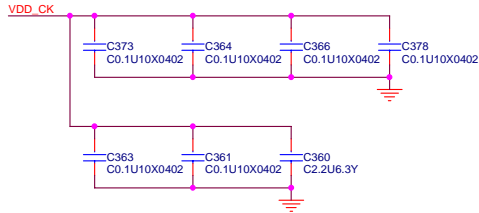
Title			Rev
DDR2 TREMINATION			
Size	Document Number		1.0
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**LAYOUT RULES:**  
Route traces with 100 Ohm Differential Impedance  
Avoid placing GND Copper or traces adjacent to TMSD Trace



<b>MSI CORPORATION</b>		
File: <b>SDVO- Sii1392</b>		
Size: Custom	Document Number: <b>MS-1221</b>	Rev: 1.0
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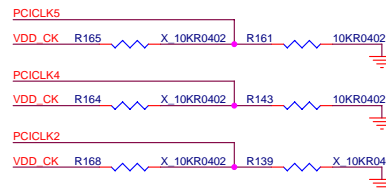
19 CLK\_PWRGD >> BSEL1

11,12,19,36 SMB\_CLK\_M2 >>  
11,12,19,36 SMB\_DATA\_M2 >>

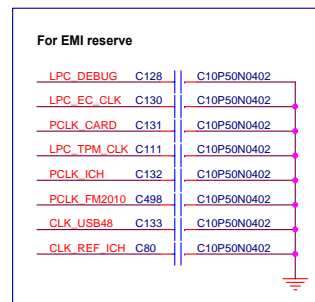
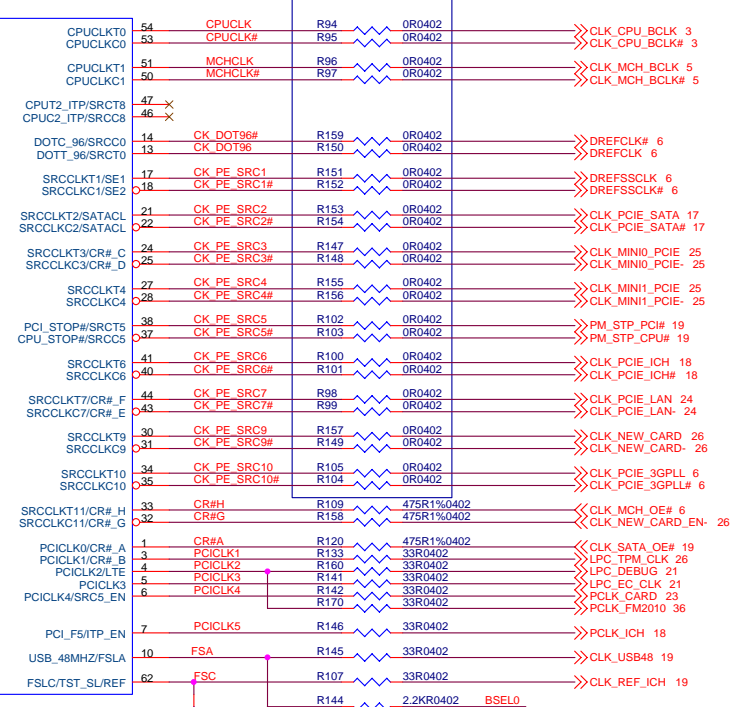


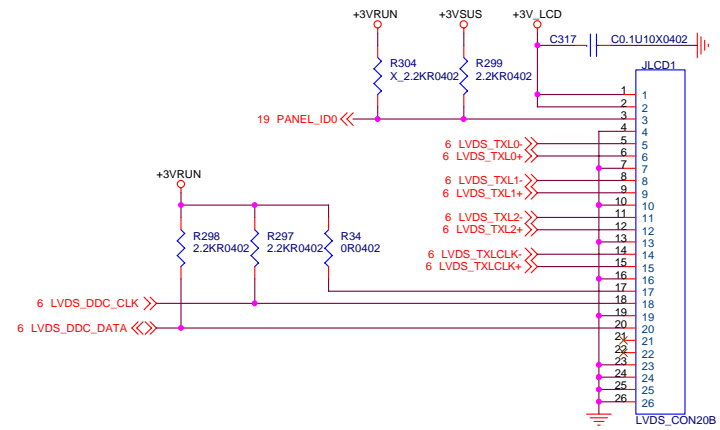
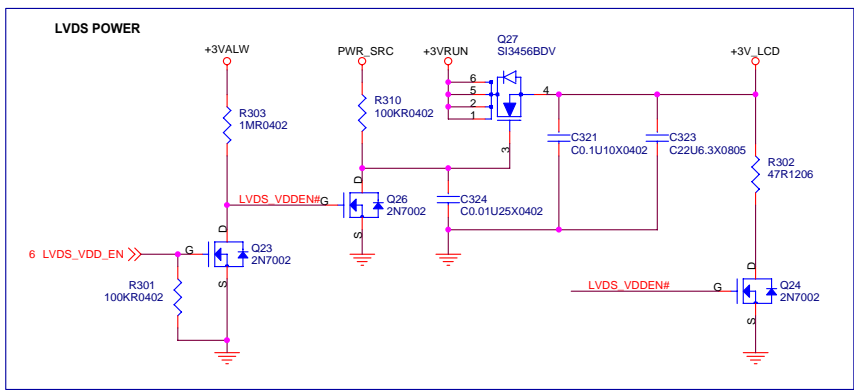
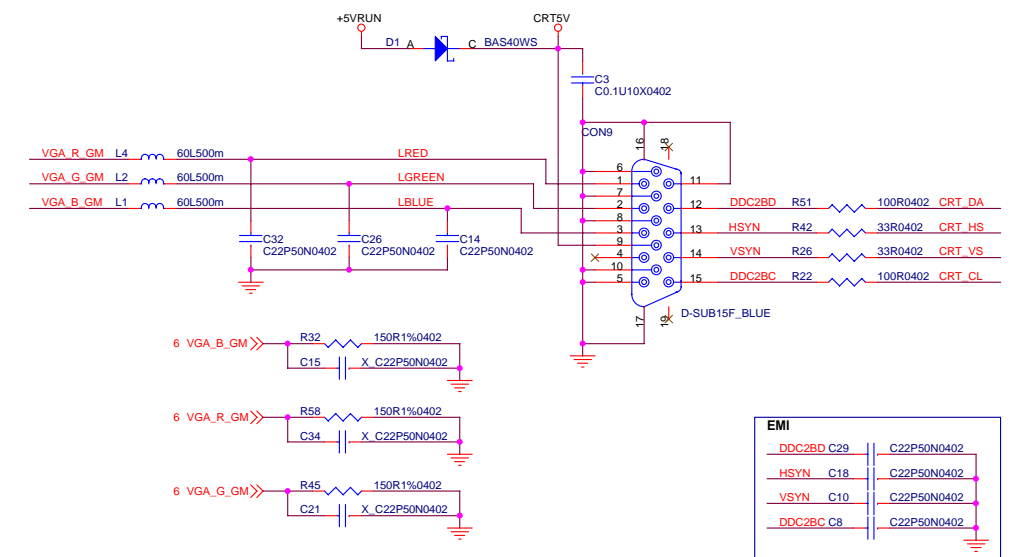
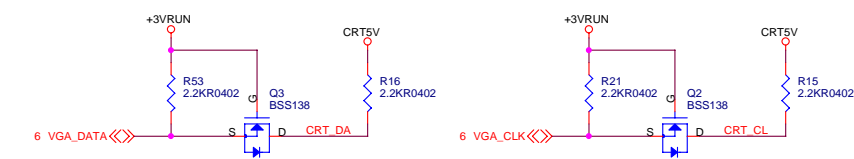
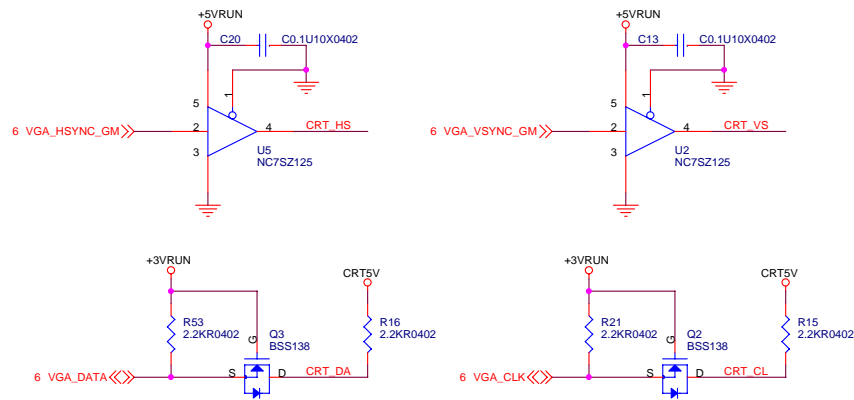
PIN#	DESCRIPTION	USAGE
1	Control SRC2 pair	CR#_A
32	Control SRC9 pair	CR#_G
33	Control SRC10 pair	CR#_H

FSC	FSB	FSA	CPU
Bit7	Bit6	Bit5	MHz
0	0	0	266.66
0	0	1	133.33
0	1	0	200.00
0	1	1	166.66
1	0	0	333.33
1	0	1	100.00
1	1	0	400.00

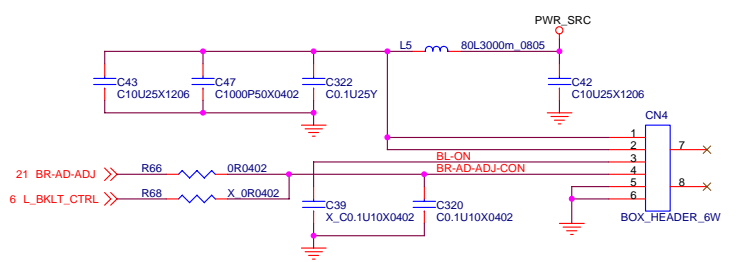
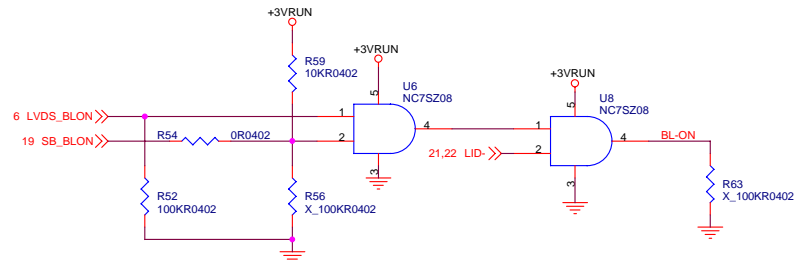


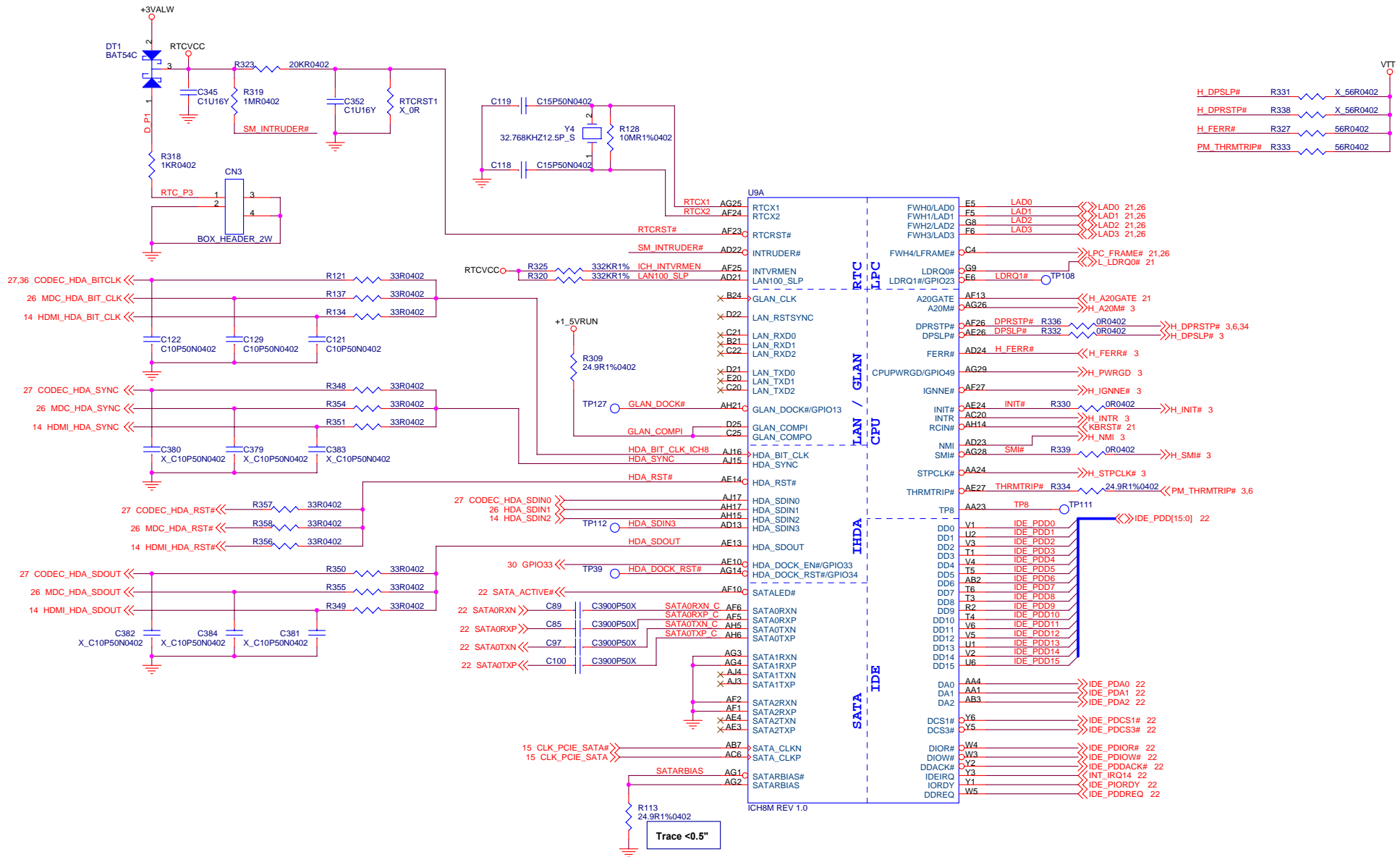
The serial resistors of differential pairs  
SLG8SP512 : pop 0R  
ICS9LP505 : pop 33R





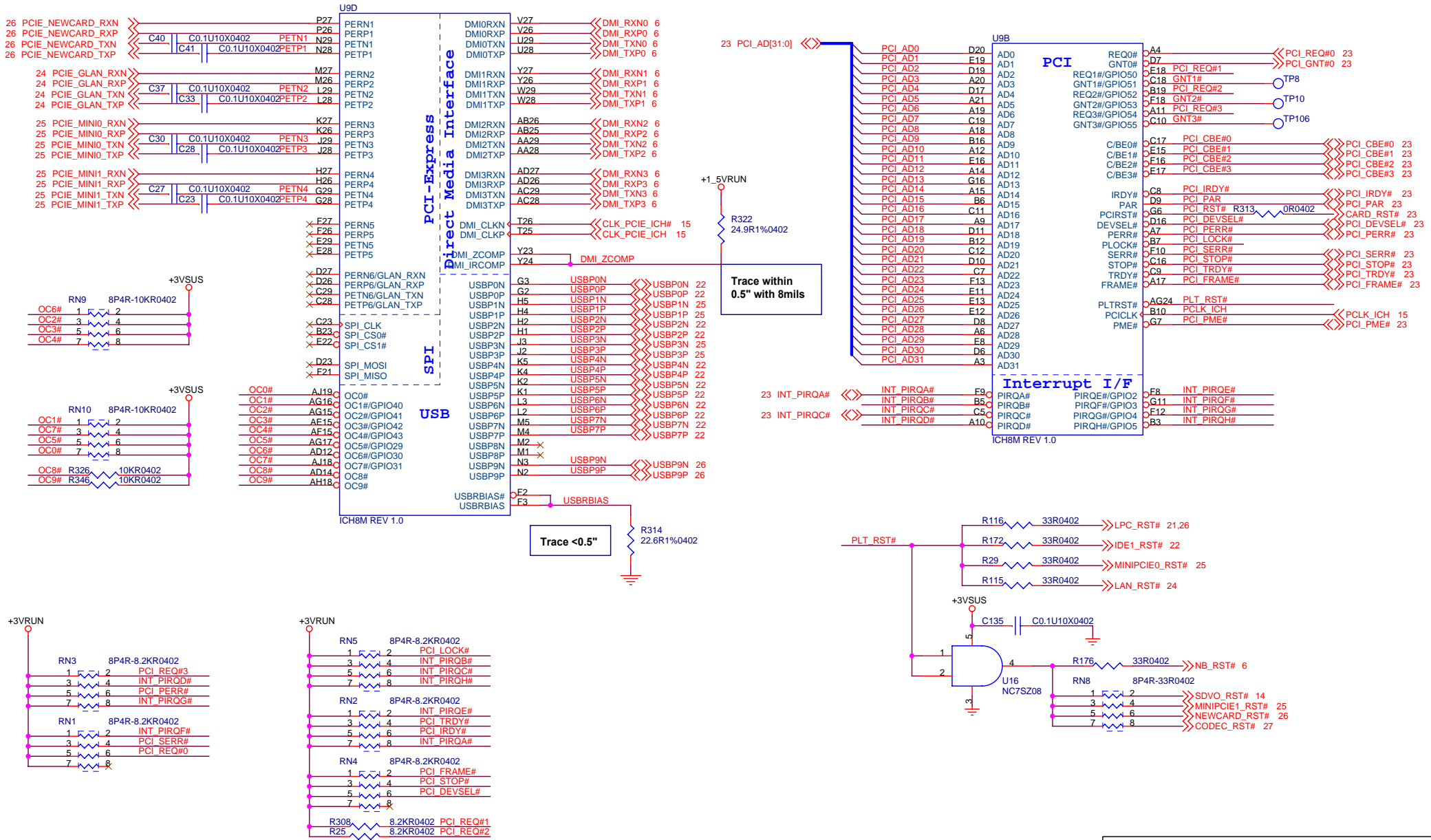
CABLE PIN DEFINE		
LCD CABLE		JLCD1
1	====>	GND
2	====>	1
3	====>	2
4	====>	17
5	====>	NC
6	====>	18
7	====>	20
8	====>	5
9	====>	6
10	====>	GND
11	====>	8
12	====>	9
13	====>	GND
14	====>	11
15	====>	12
16	====>	GND
17	====>	14
18	====>	15
19	====>	GND
20	====>	GND



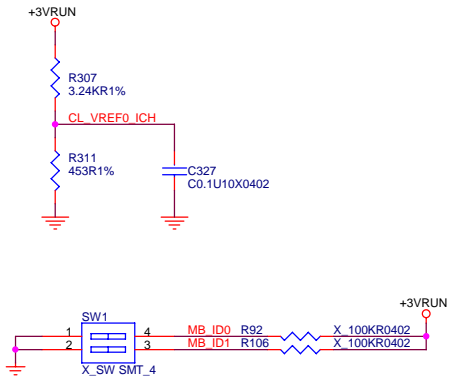
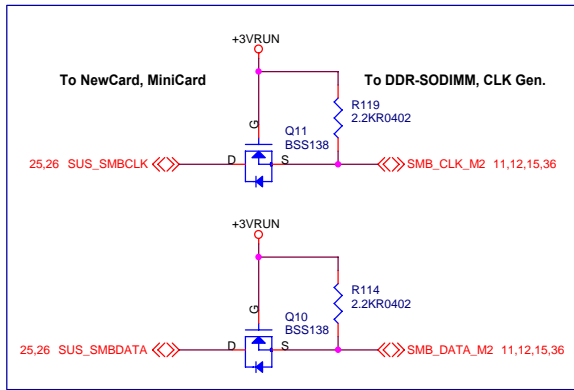
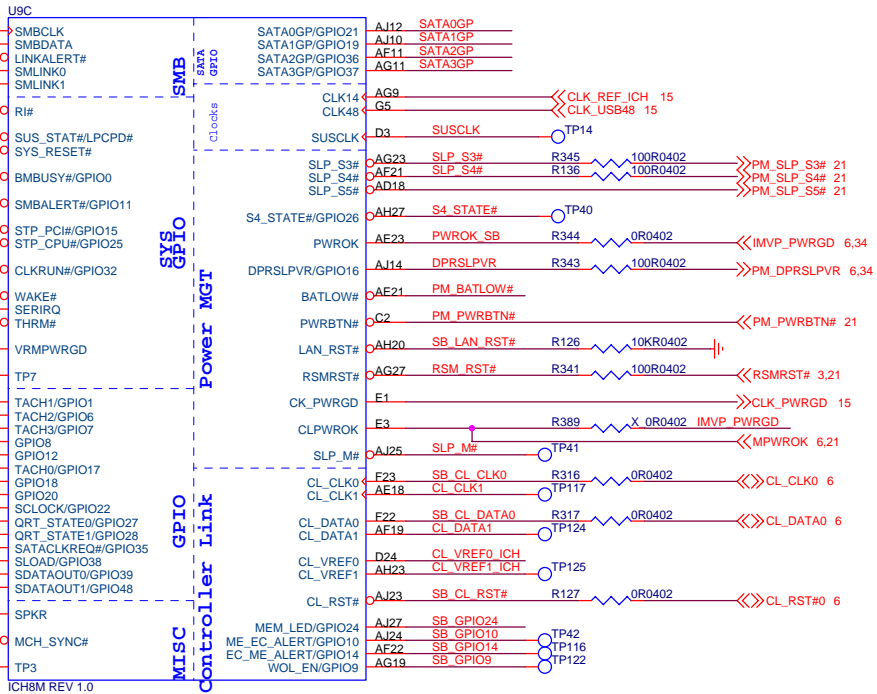
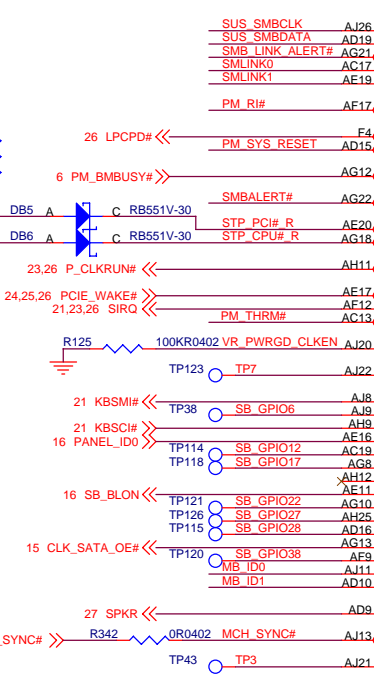
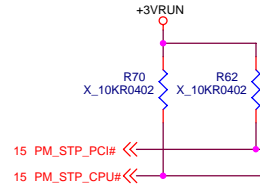
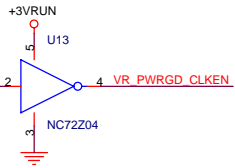
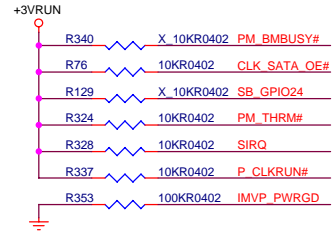
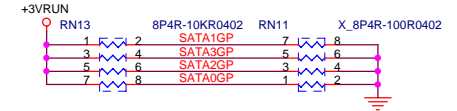
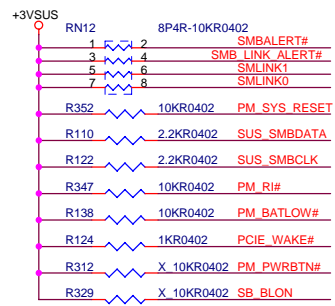


<b>MSI CORPORATION</b>			
Title			
<b>ICH8M-1 (CPU/IDE/Azalia)</b>			
Size	Document Number		Rev
Custom	<b>MS-1221</b>		1.0
Date:	Monday, March 19, 2007	Sheet	17 of 41

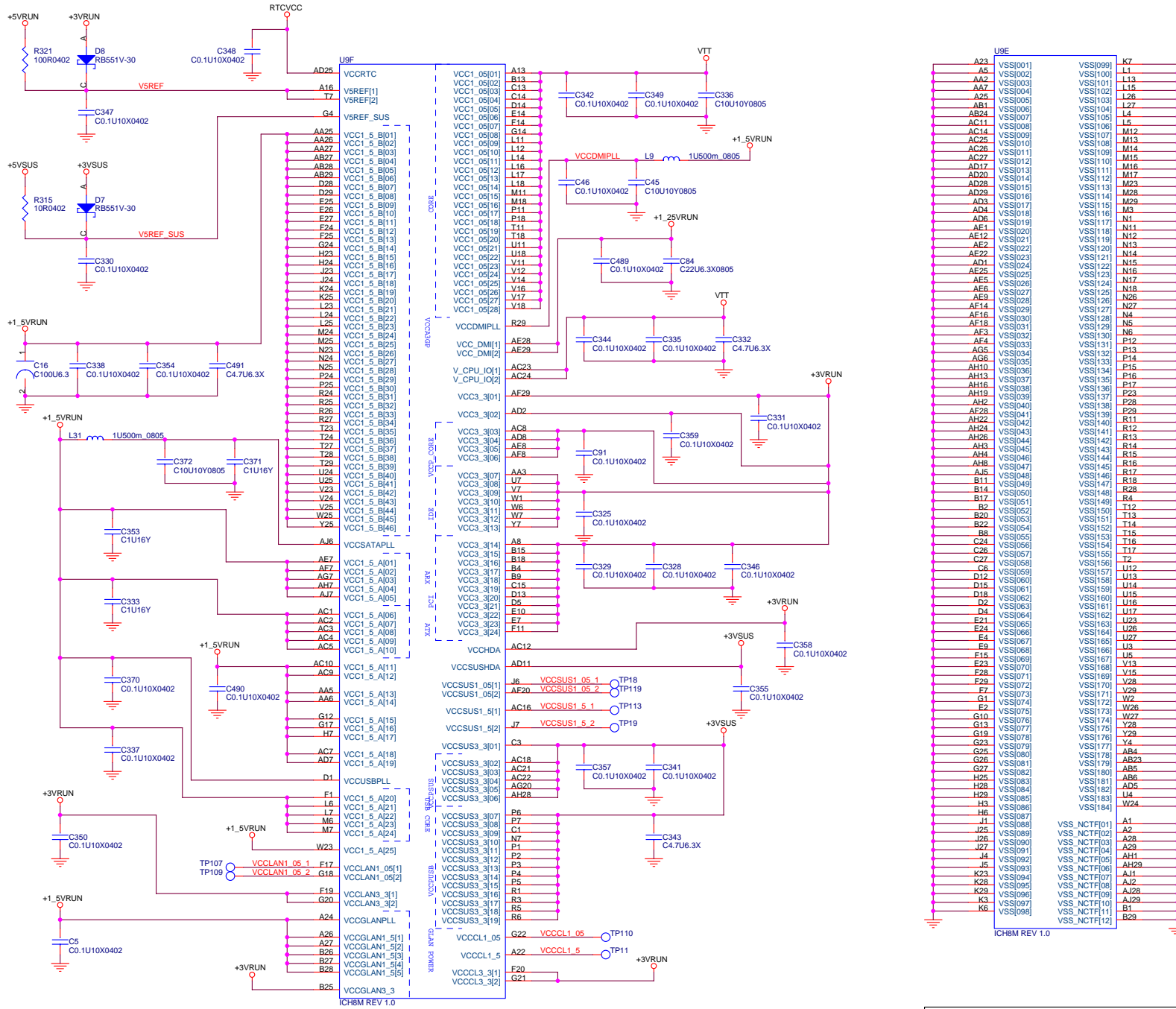
place Cap close to ICH8  
within 250mils



<b>MSI CORPORATION</b>			
Title			
<b>ICH8M-2 (PCI/USB/PCIE/DMI)</b>			
Size	Document Number	Rev	
Custom	<b>MS-1221</b>	1.0	
Date:	Monday, March 19, 2007	Sheet	18 of 41



<b>MSI CORPORATION</b>		
Title		
<b>ICH8M-3 (SM BUS/GPIO)</b>		
Size	Document Number	Rev
A3	<b>MS-1221</b>	1.0
Date:	Monday, March 19, 2007	Sheet 19 of 41



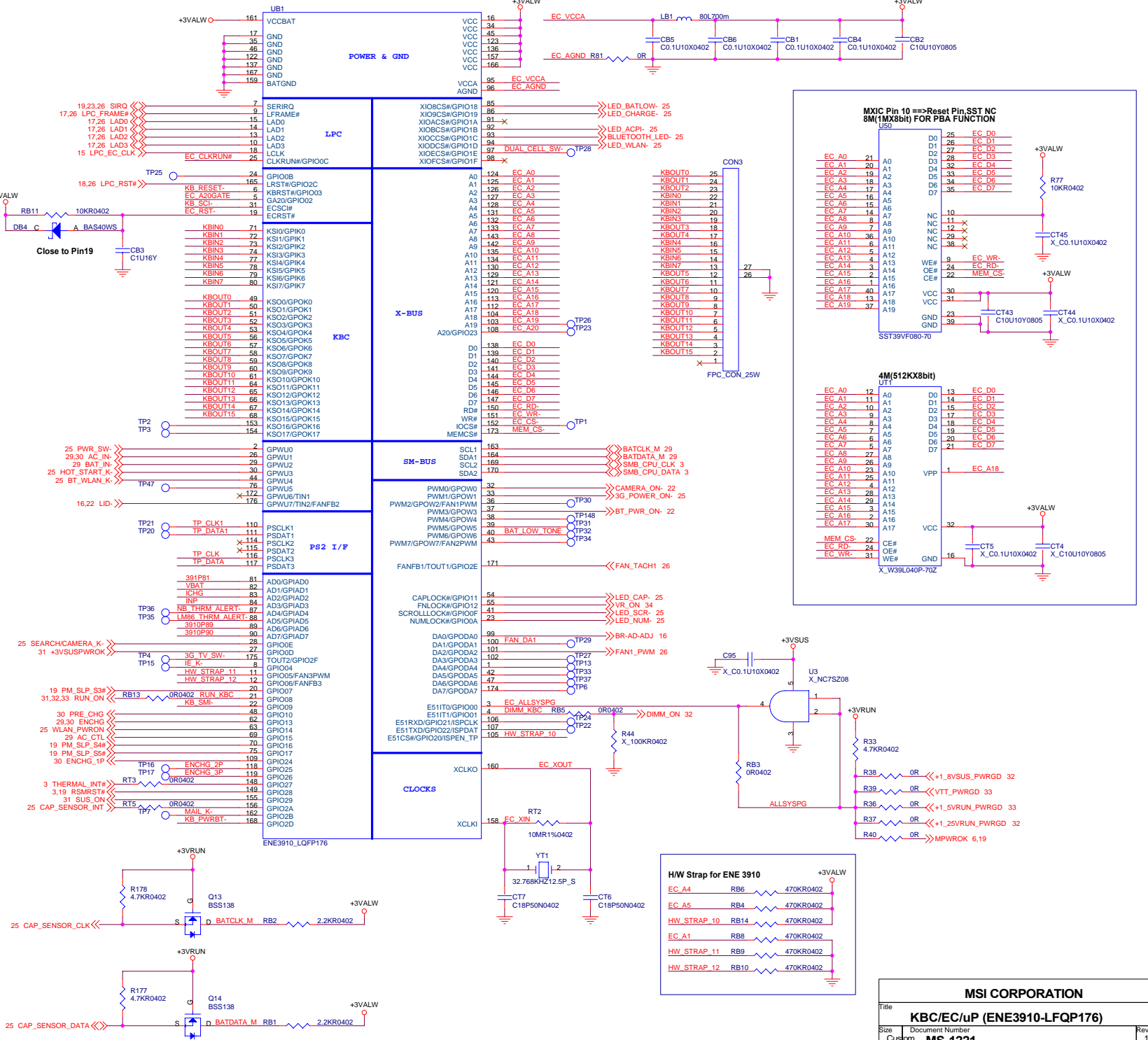
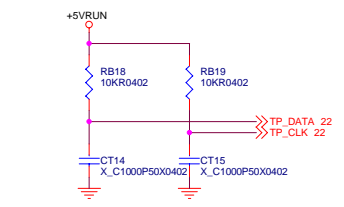
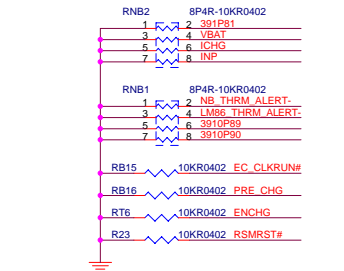
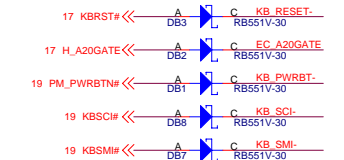
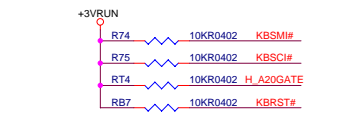
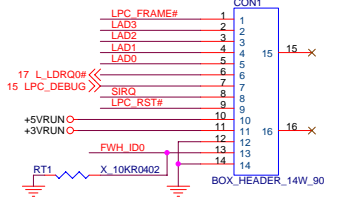
U9E	VSS	K7
A23	VSS[001]	VSS[099]
A5	VSS[002]	VSS[100]
AA7	VSS[003]	VSS[101]
AA7	VSS[004]	VSS[102]
A25	VSS[005]	VSS[103]
AB1	VSS[006]	VSS[104]
AB24	VSS[007]	VSS[105]
AC11	VSS[008]	VSS[106]
AC14	VSS[009]	VSS[107]
AC25	VSS[010]	VSS[108]
AC26	VSS[011]	VSS[109]
AC27	VSS[012]	VSS[110]
AD17	VSS[013]	VSS[111]
AD20	VSS[014]	VSS[112]
AD28	VSS[015]	VSS[113]
AD29	VSS[016]	VSS[114]
AD3	VSS[017]	VSS[115]
AD4	VSS[018]	VSS[116]
AD6	VSS[019]	VSS[117]
AE1	VSS[020]	VSS[118]
AE12	VSS[021]	VSS[119]
AE2	VSS[022]	VSS[120]
AE22	VSS[023]	VSS[121]
AD1	VSS[024]	VSS[122]
AE25	VSS[025]	VSS[123]
AE5	VSS[026]	VSS[124]
AE6	VSS[027]	VSS[125]
AE9	VSS[028]	VSS[126]
AF14	VSS[029]	VSS[127]
AF16	VSS[030]	VSS[128]
AF18	VSS[031]	VSS[129]
AF3	VSS[032]	VSS[130]
AF4	VSS[033]	VSS[131]
AG5	VSS[034]	VSS[132]
AG6	VSS[035]	VSS[133]
AH10	VSS[036]	VSS[134]
AH13	VSS[037]	VSS[135]
AH16	VSS[038]	VSS[136]
AH19	VSS[039]	VSS[137]
AH2	VSS[040]	VSS[138]
AH28	VSS[041]	VSS[139]
AH22	VSS[042]	VSS[140]
AH24	VSS[043]	VSS[141]
AH26	VSS[044]	VSS[142]
AH3	VSS[045]	VSS[143]
AH4	VSS[046]	VSS[144]
AH8	VSS[047]	VSS[145]
AJ5	VSS[048]	VSS[146]
B1	VSS[049]	VSS[147]
B14	VSS[050]	VSS[148]
B17	VSS[051]	VSS[149]
B2	VSS[052]	VSS[150]
B20	VSS[053]	VSS[151]
B22	VSS[054]	VSS[152]
B8	VSS[055]	VSS[153]
C24	VSS[056]	VSS[154]
C26	VSS[057]	VSS[155]
C27	VSS[058]	VSS[156]
D5	VSS[059]	VSS[157]
D12	VSS[060]	VSS[158]
D15	VSS[061]	VSS[159]
D18	VSS[062]	VSS[160]
D2	VSS[063]	VSS[161]
D4	VSS[064]	VSS[162]
E21	VSS[065]	VSS[163]
E4	VSS[066]	VSS[164]
E9	VSS[067]	VSS[165]
F15	VSS[068]	VSS[166]
E23	VSS[069]	VSS[167]
F28	VSS[070]	VSS[168]
F28	VSS[071]	VSS[169]
F7	VSS[072]	VSS[170]
G1	VSS[073]	VSS[171]
E2	VSS[074]	VSS[172]
G10	VSS[075]	VSS[173]
G13	VSS[076]	VSS[174]
G19	VSS[077]	VSS[175]
G23	VSS[078]	VSS[176]
G25	VSS[079]	VSS[177]
G26	VSS[080]	VSS[178]
G27	VSS[081]	VSS[179]
H25	VSS[082]	VSS[180]
H28	VSS[083]	VSS[181]
H29	VSS[084]	VSS[182]
H3	VSS[085]	VSS[183]
H6	VSS[086]	VSS[184]
J1	VSS[087]	VSS[185]
J25	VSS[088]	VSS[186]
N7	VSS[089]	VSS[187]
N7	VSS[090]	VSS[188]
J4	VSS[091]	VSS[189]
J5	VSS[092]	VSS[190]
K23	VSS[093]	VSS[191]
K28	VSS[094]	VSS[192]
K29	VSS[095]	VSS[193]
K3	VSS[096]	VSS[194]
R6	VSS[097]	VSS[195]
K6	VSS[098]	VSS[196]
VSS NCTF[01]	VSS NCTF[01]	A1
VSS NCTF[02]	VSS NCTF[02]	A2
VSS NCTF[03]	VSS NCTF[03]	A28
VSS NCTF[04]	VSS NCTF[04]	A28
VSS NCTF[05]	VSS NCTF[05]	AH1
VSS NCTF[06]	VSS NCTF[06]	AH29
VSS NCTF[07]	VSS NCTF[07]	A11
VSS NCTF[08]	VSS NCTF[08]	A12
VSS NCTF[09]	VSS NCTF[09]	AJ28
VSS NCTF[10]	VSS NCTF[10]	AJ29
VSS NCTF[11]	VSS NCTF[11]	B1
VSS NCTF[12]	VSS NCTF[12]	B29

**MSI CORPORATION**

Title	<b>ICH8M-4 (POWER/GND)</b>	
Size	Document Number	Rev
Custom	<b>MS-1221</b>	1.0
Date:	Monday, March 19, 2007	Sheet 20 of 41



**For SW Debug**



**MSI CORPORATION**

Part Number: **KBC/EC/uP (ENE3910-LFQP176)**

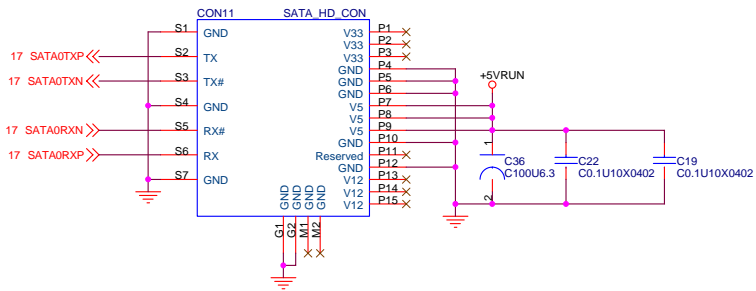
Revision: **1.0**

Document Number: **MS-1221**

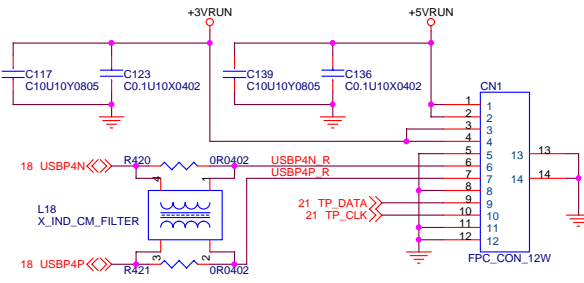
Date: Wednesday, March 14, 2007

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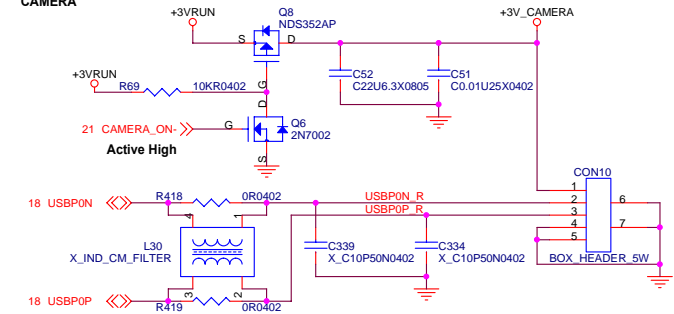
SATA HDD



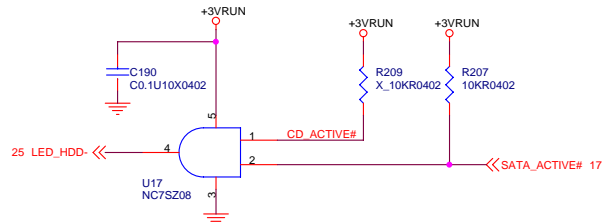
FINGERPRINT & TOUCH PAD



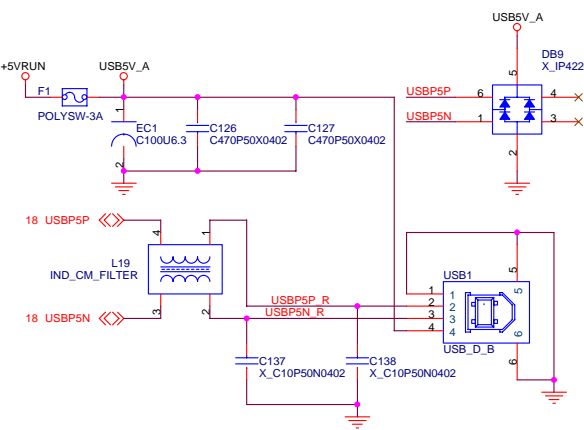
CAMERA



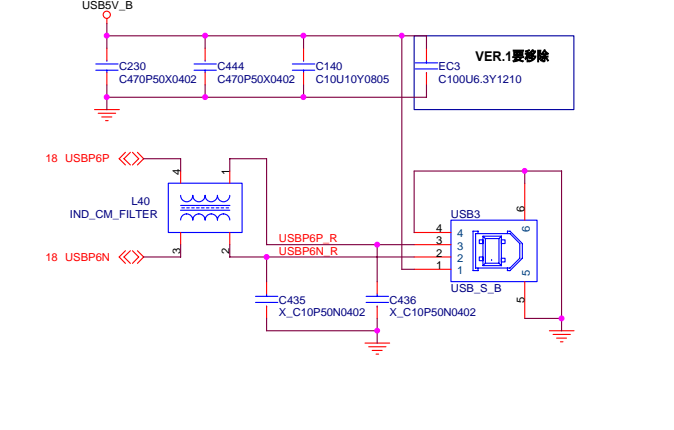
PATA CDROM/DVD



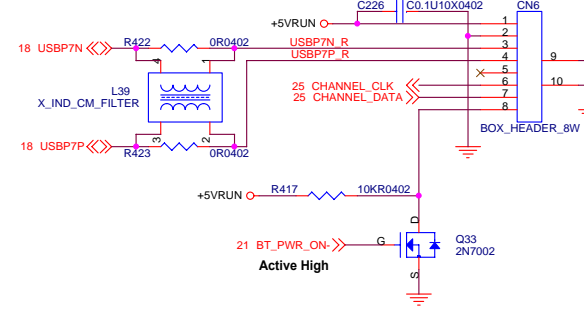
LEFT USB



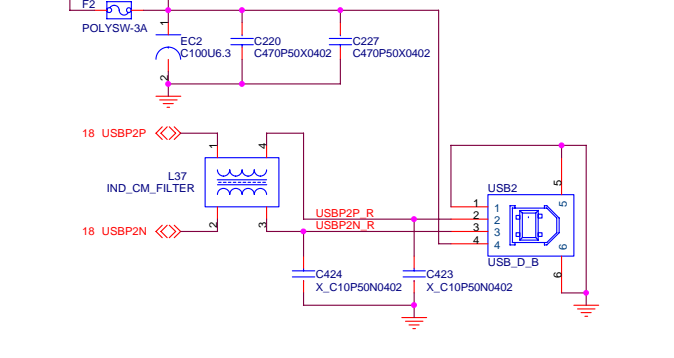
RIGHT USB



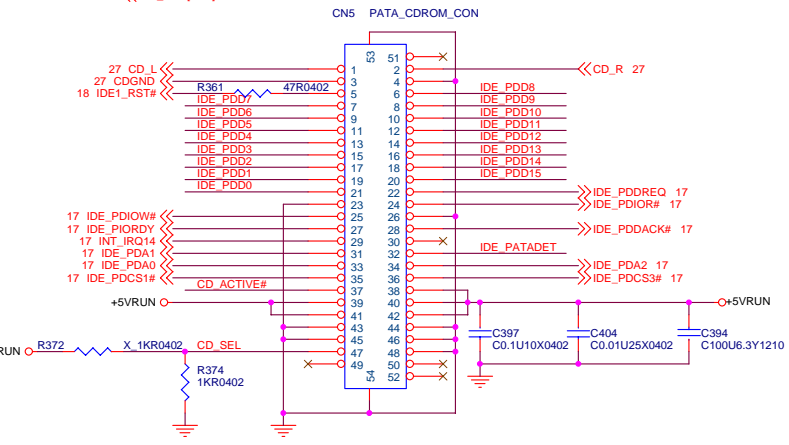
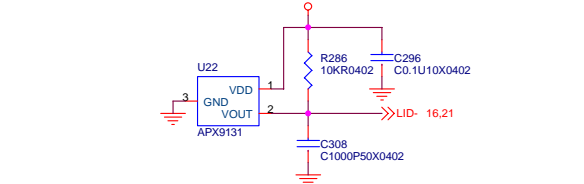
BLUETOOTH



LID



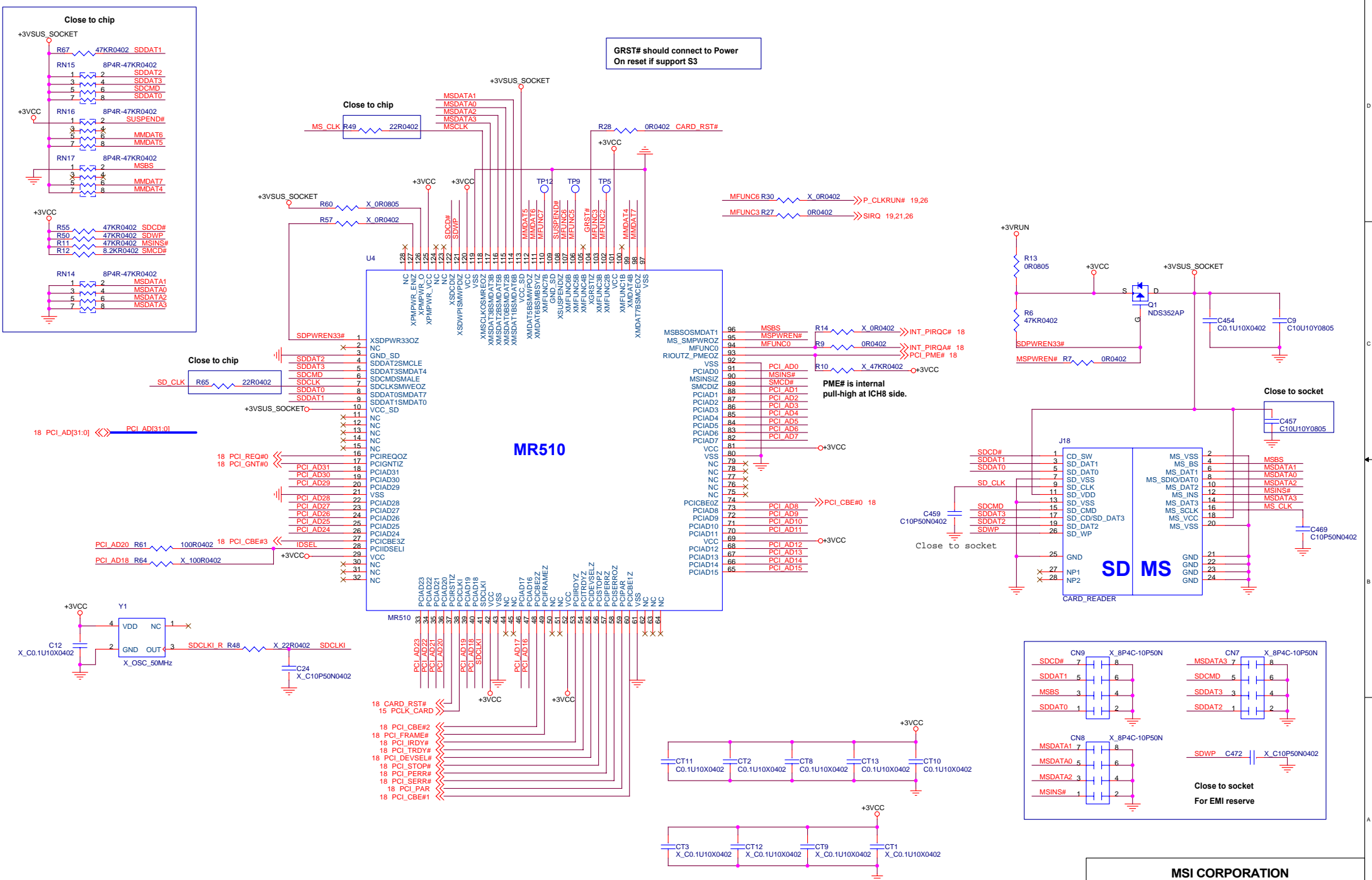
LID



PIN32:PDIAG  
PIN37:PASP  
PIN47:CABLE SELECT  
Low:Master  
NC or High:Slave

+3VRUN  
INT\_IRQ14 R370 8.2KR0402  
IDE\_PIORDY R369 4.7KR0402  
IDE\_PATADET R371 470KR0402  
IDE\_PDDREQ R368 100KR0402

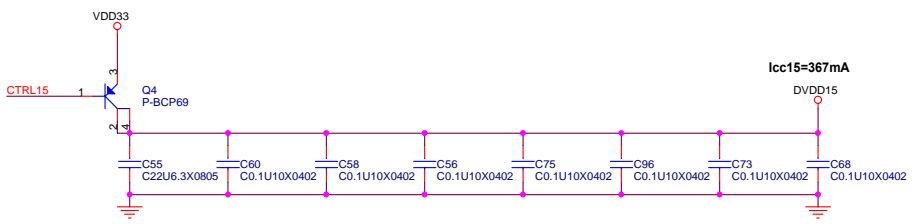
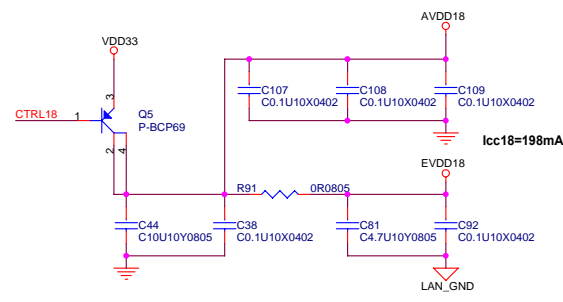
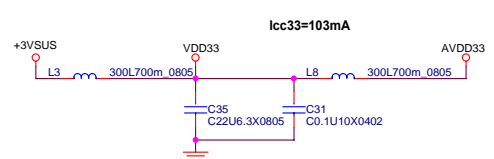
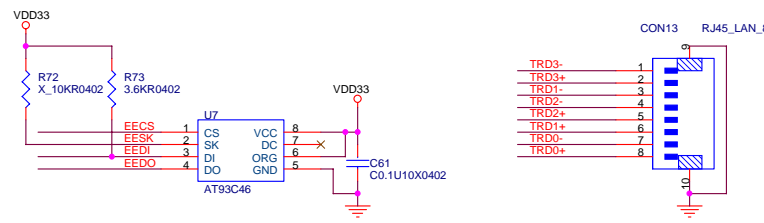
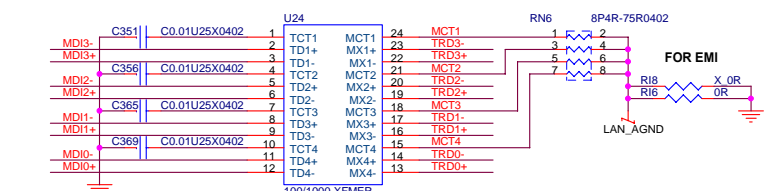
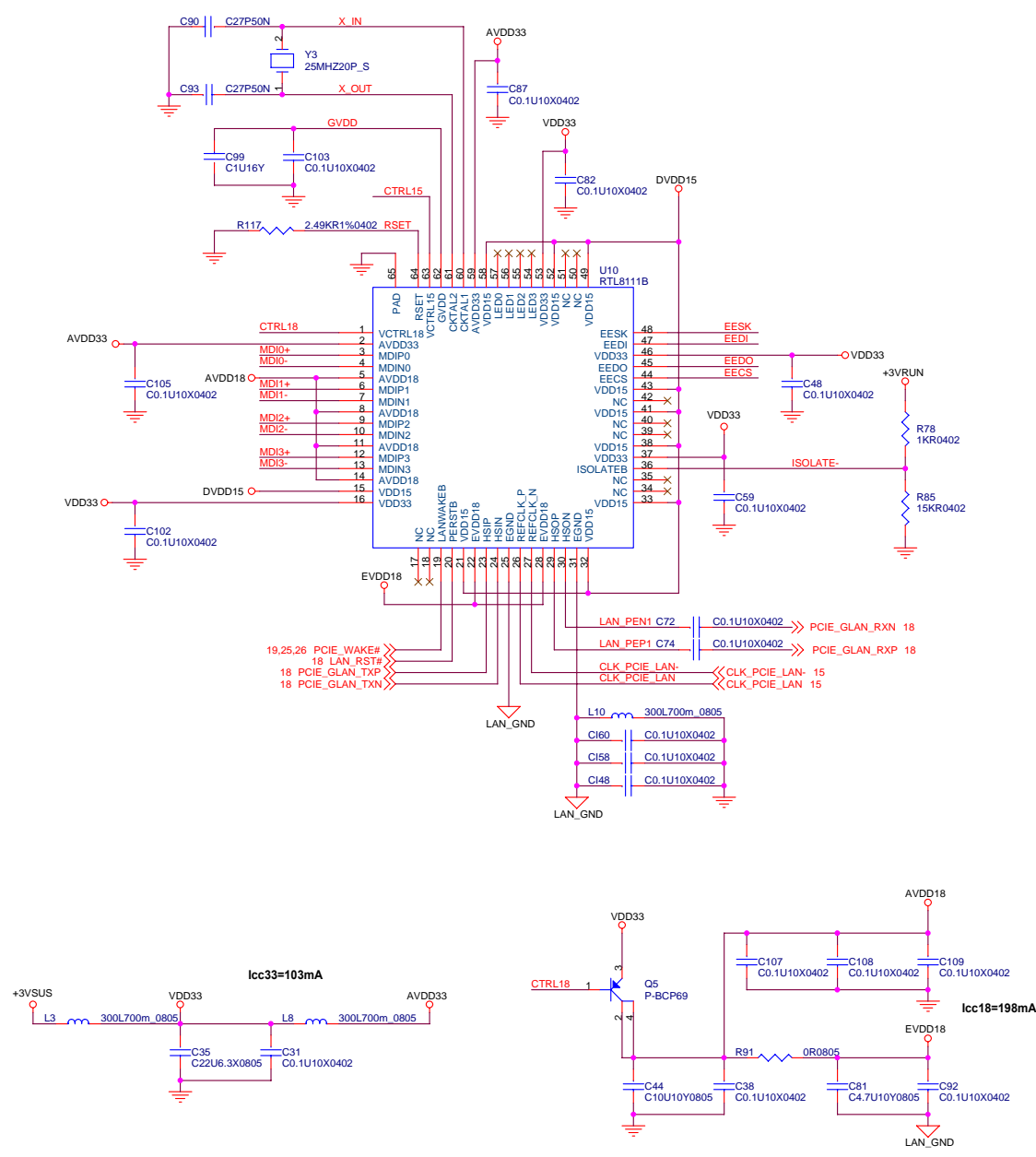
<b>MSI CORPORATION</b>		
Title <b>HDD,CDROM,LID,USB</b>		
Size Custom	Document Number <b>MS-1221</b>	Rev 1.0
Date: Monday, March 19, 2007	Sheet 22	of 41



GRST# should connect to Power On reset if support S3

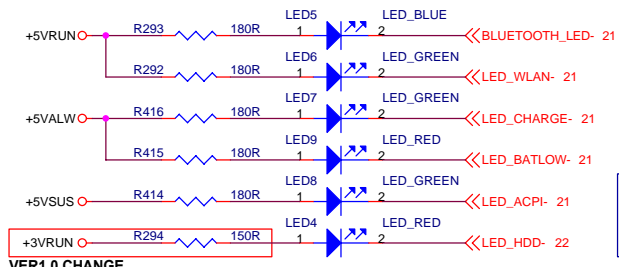
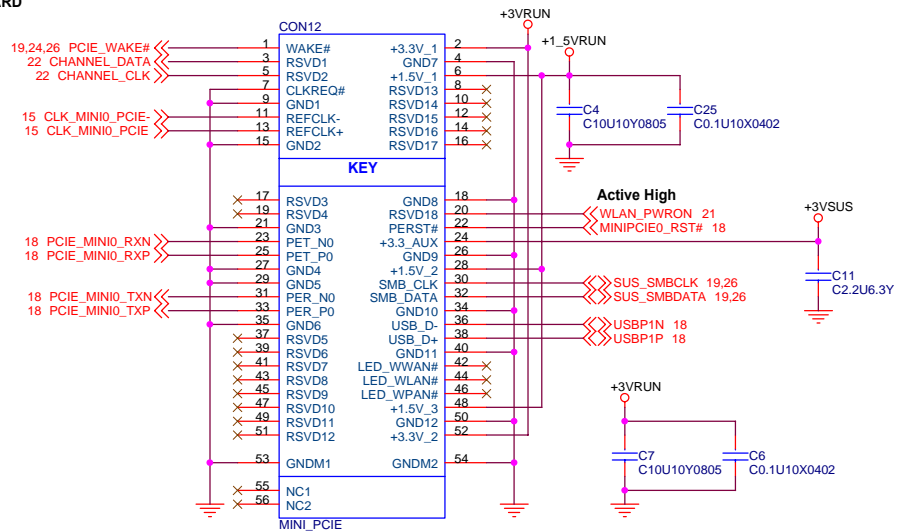
PME# is internal pull-high at ICH8 side.

MSI CORPORATION		
Title <b>Card Reader (MR510)</b>		
Size	Document Number	Rev
Custom	<b>MS-1221</b>	1.0
Date:	Tuesday, March 13, 2007	Sheet 23 of 41



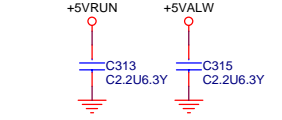
<b>MSI CORPORATION</b>		
Title <b>PCIE LAN (RTL 8111B)</b>		
Size	Document Number	Rev
Custom	<b>MS-1221</b>	1.0
Date:	Wednesday, March 14, 2007	Sheet 24 of 41

**WLAN CARD**

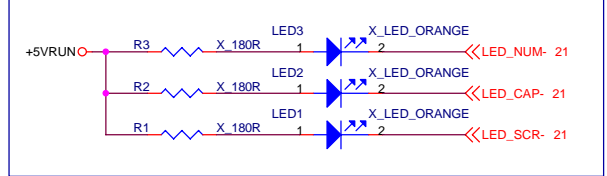


**ON : Normal ( Power ON )**  
**OFF : S4/S5 state**  
**Flash : S3 state**

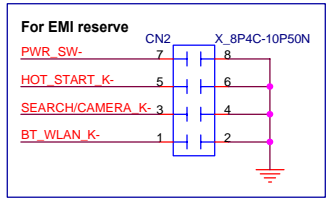
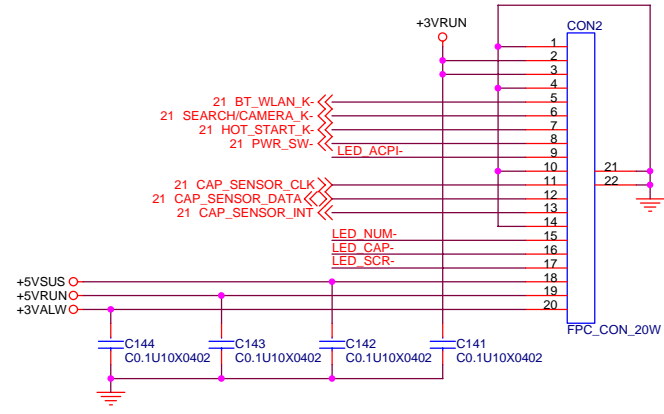
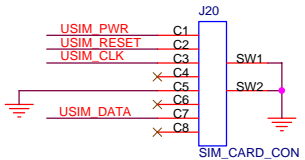
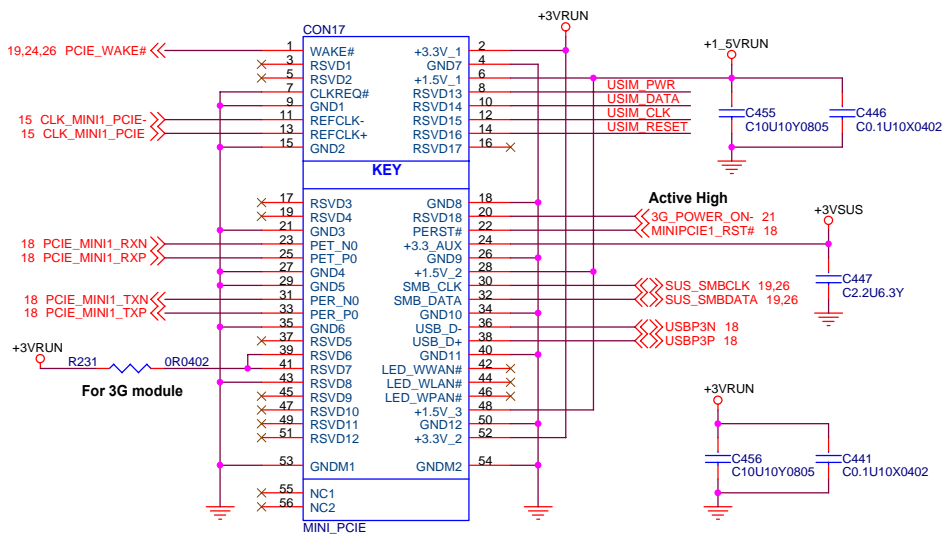
**VER1.0 CHANGE**



**FOR DIFFERENT CUSTOMER REQUEST**

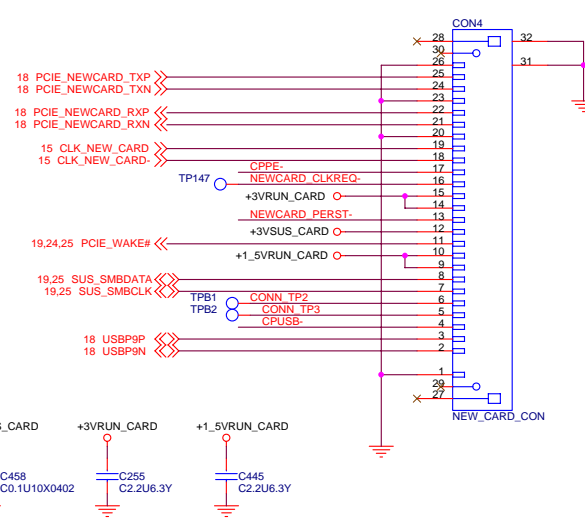
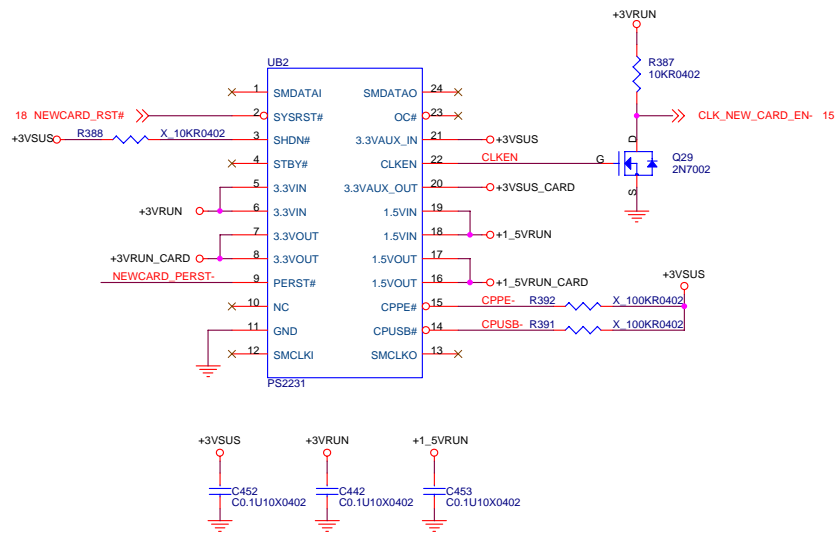


**TV TUNER /3G CARD**

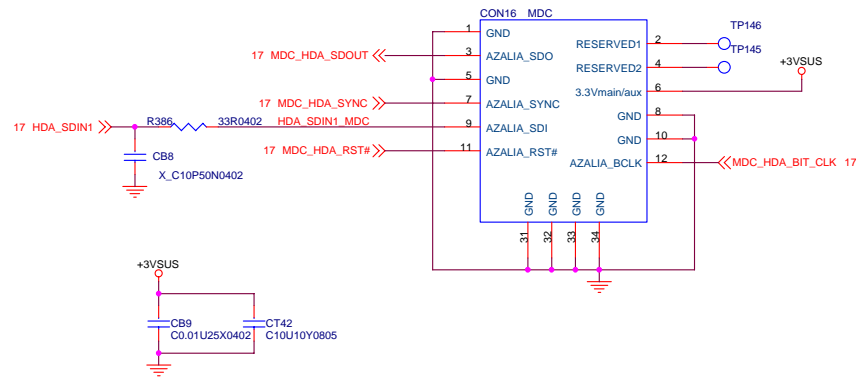


<b>MSI CORPORATION</b>		
Title		
<b>MINI_PCIE, LED, SW</b>		
Size	Document Number	Rev
Custom	<b>MS-1221</b>	0D
Date:	Tuesday, March 13, 2007	Sheet 25 of 41

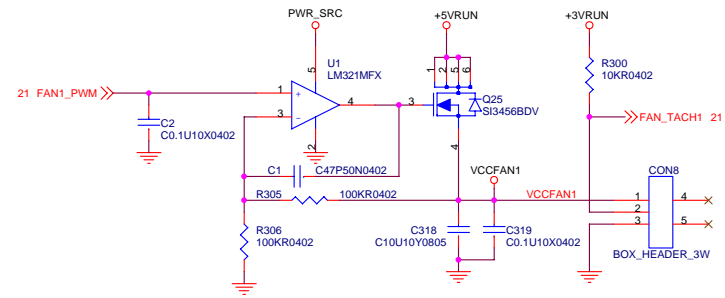
NEW CARD



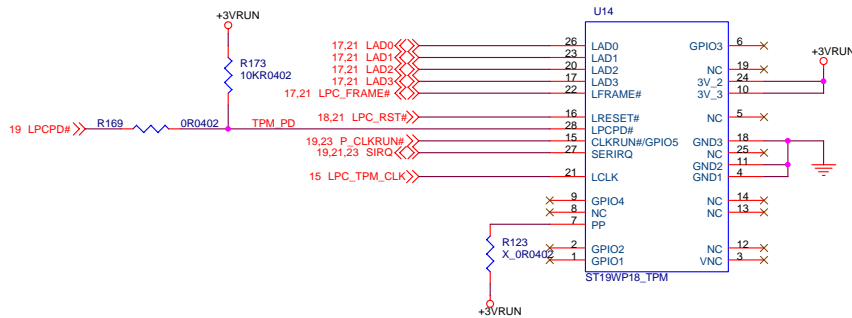
MDC Connector



CPU FAN



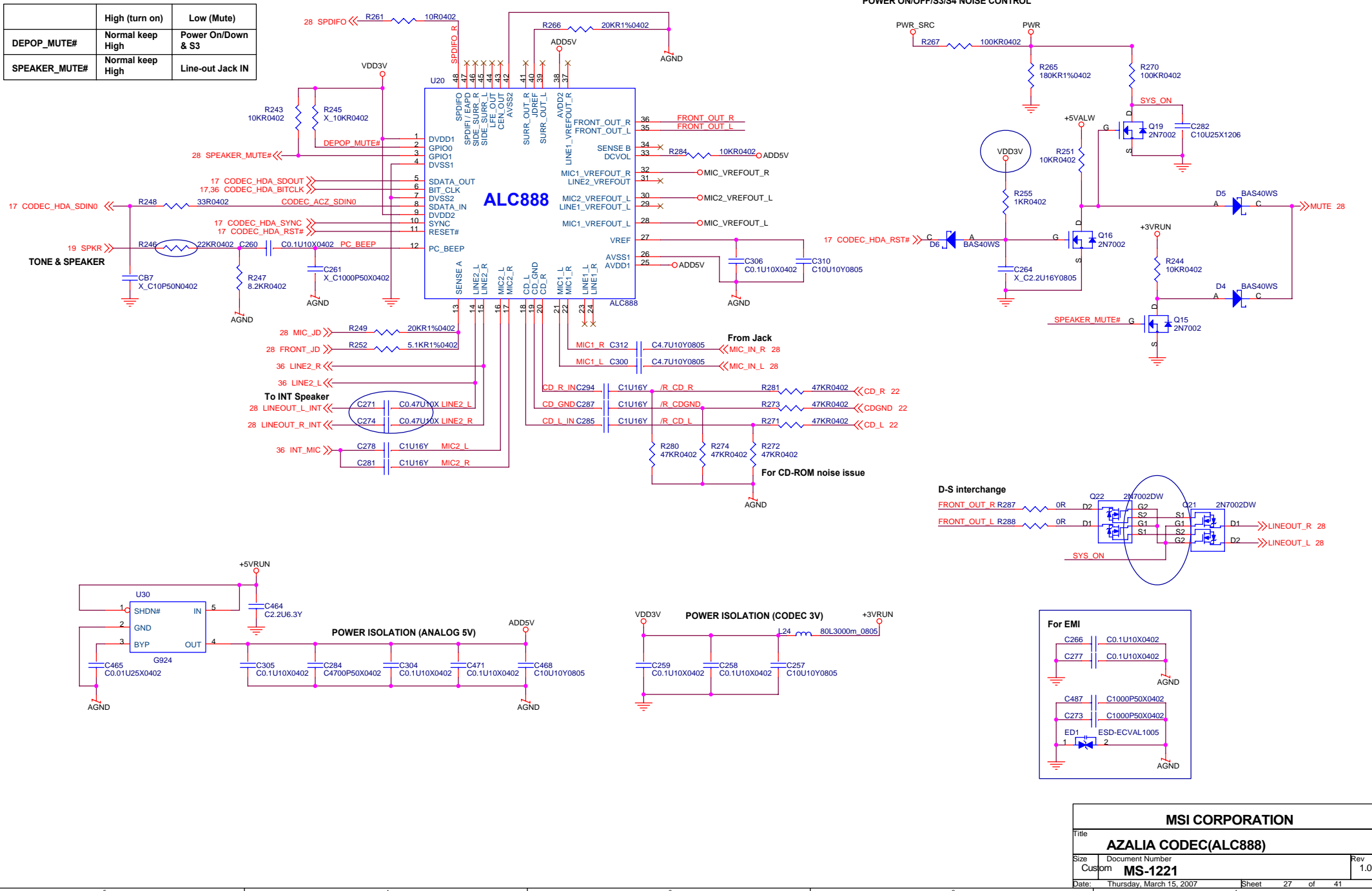
TPM 1.2



<b>MSI CORPORATION</b>		
Title	<b>NEWCARD, MDC, TPM, FAN</b>	
Size	Document Number	Rev
Custom	<b>MS-1221</b>	1.0
Date	Tuesday, March 13, 2007	Sheet 26 of 41

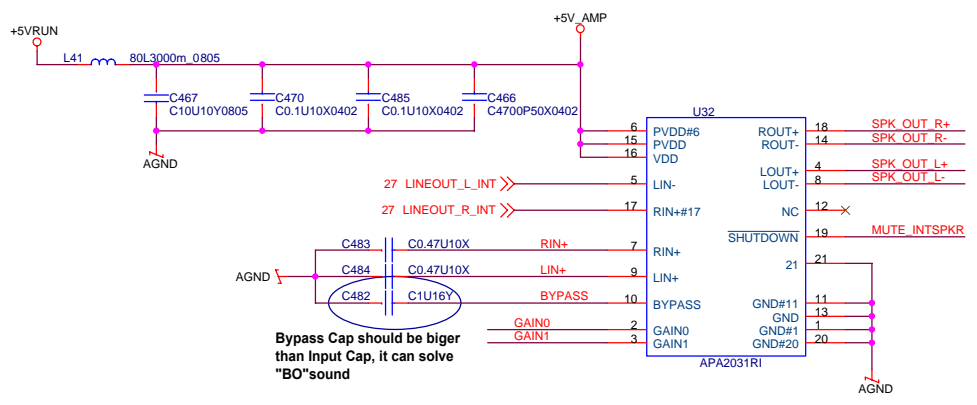


	High (turn on)	Low (Mute)
DEPOP_MUTE#	Normal keep High	Power On/Down & S3
SPEAKER_MUTE#	Normal keep High	Line-out Jack IN



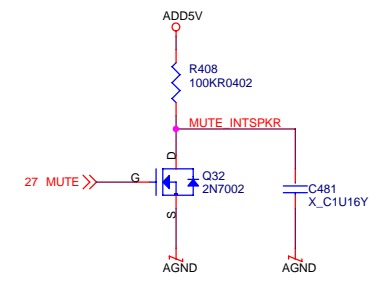
MSI CORPORATION		
Title	AZALIA CODEC(ALC888)	
Size	Document Number	Rev
Custom	MS-1221	1.0
Date:	Thursday, March 15, 2007	Sheet 27 of 41

Internal Speaker Circuit



Bypass Cap should be bigger than Input Cap, it can solve "BO" sound

(MUTE SPEAKER)

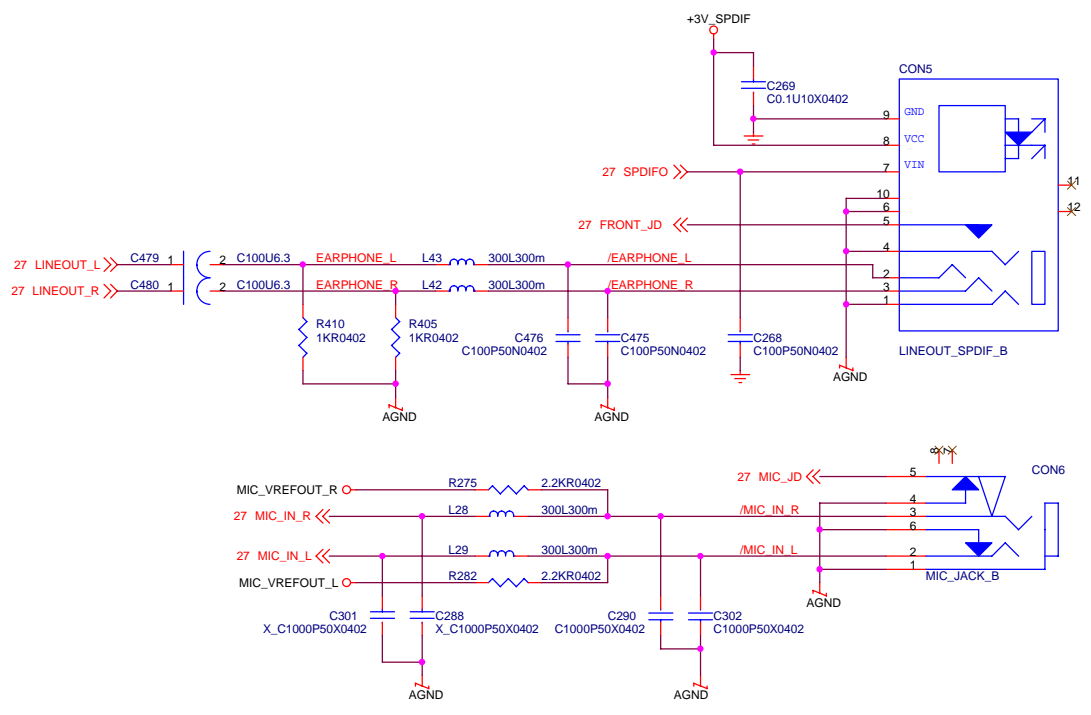
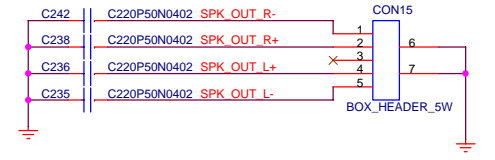


POWER ON/OFF/S3/S4 NOISE CONTROL

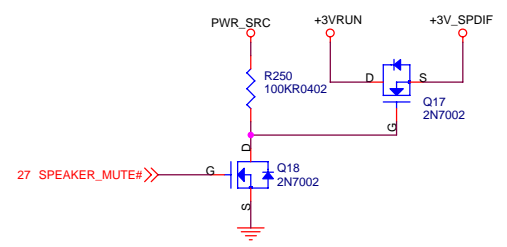
FOR APA2031

GAIN0	GAIN1
6dB	0 0
10dB	0 1
15.6dB	1 0
21.6dB	1 1
4.3dB	X X

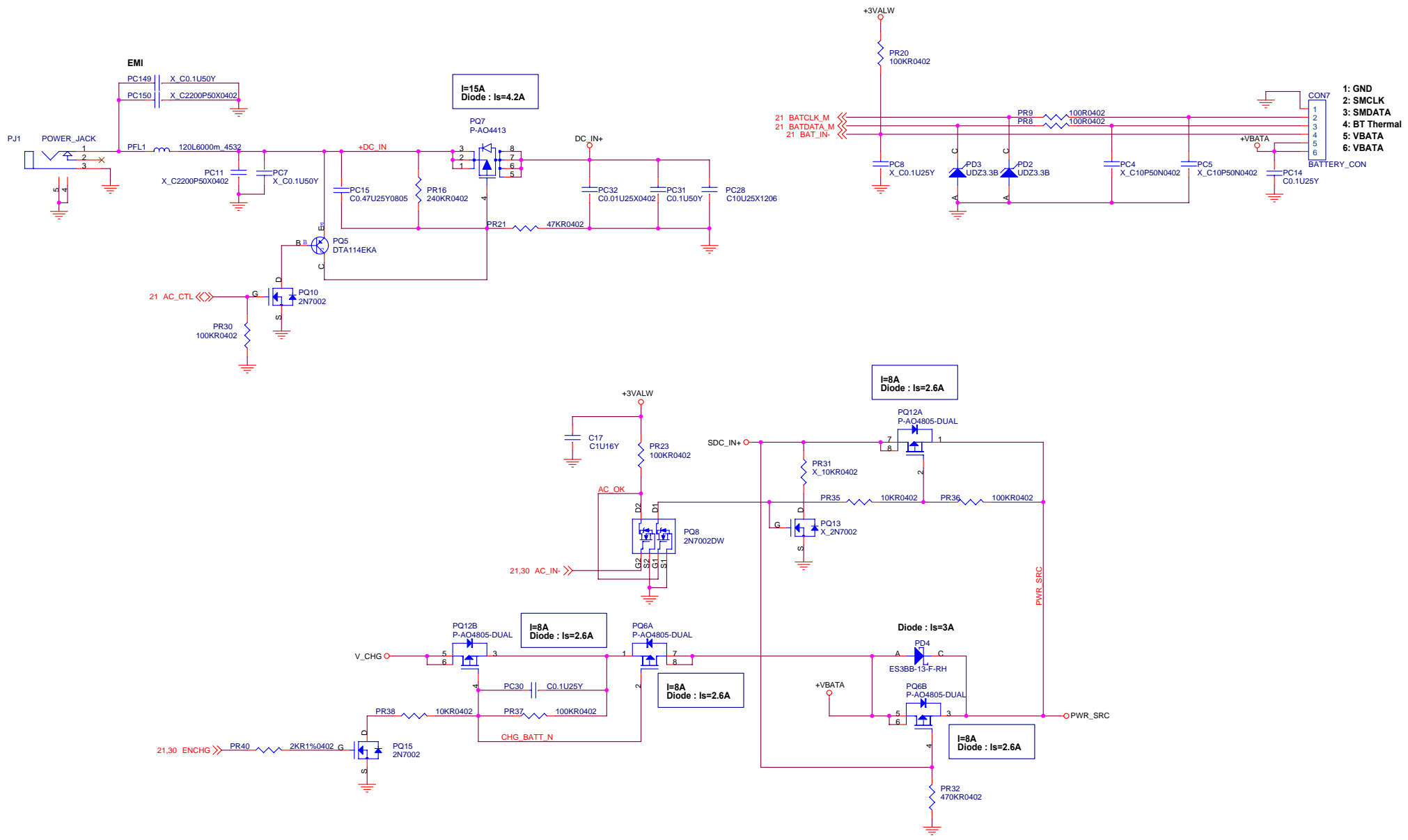
Internal Speaker Connector

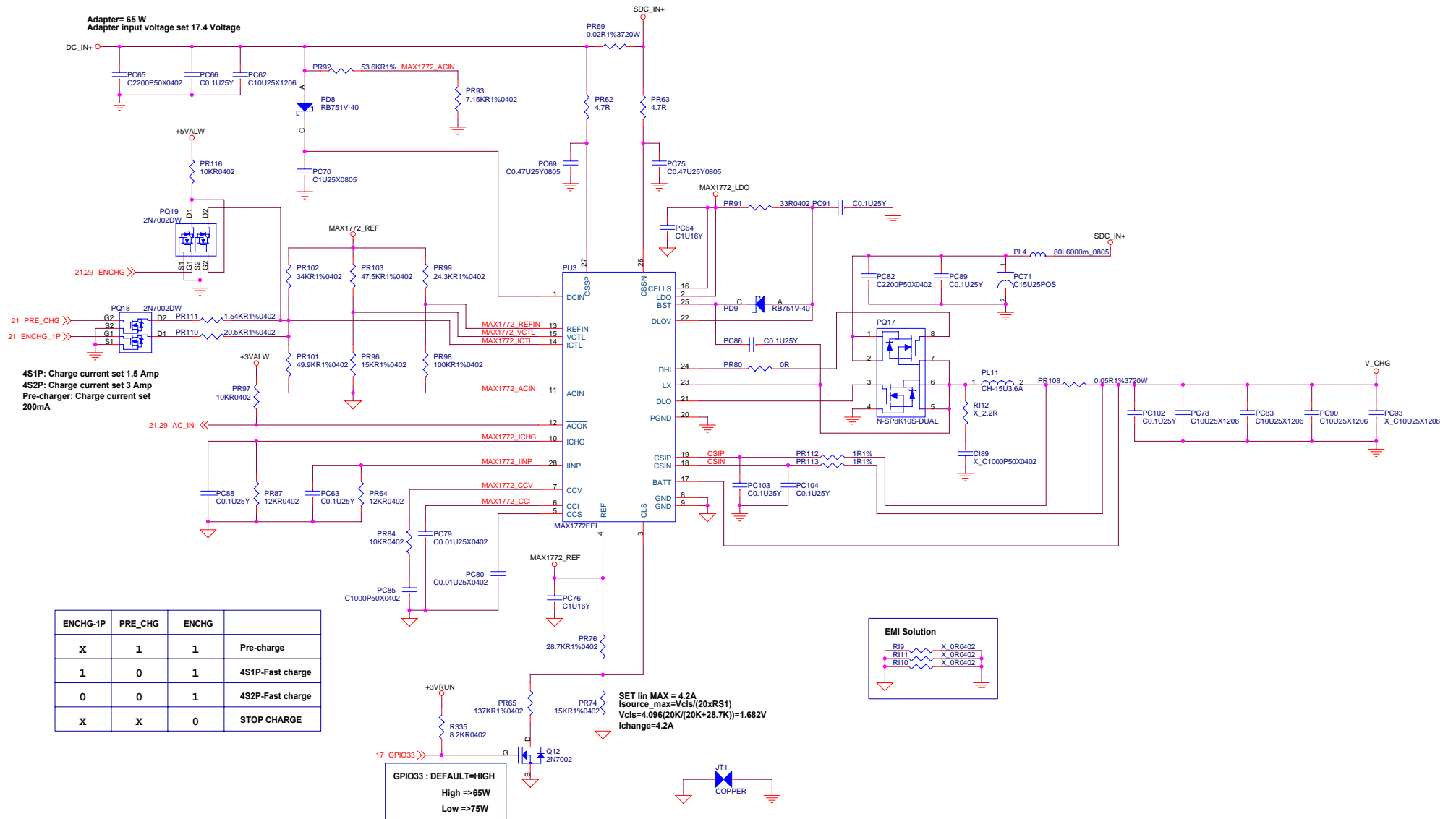


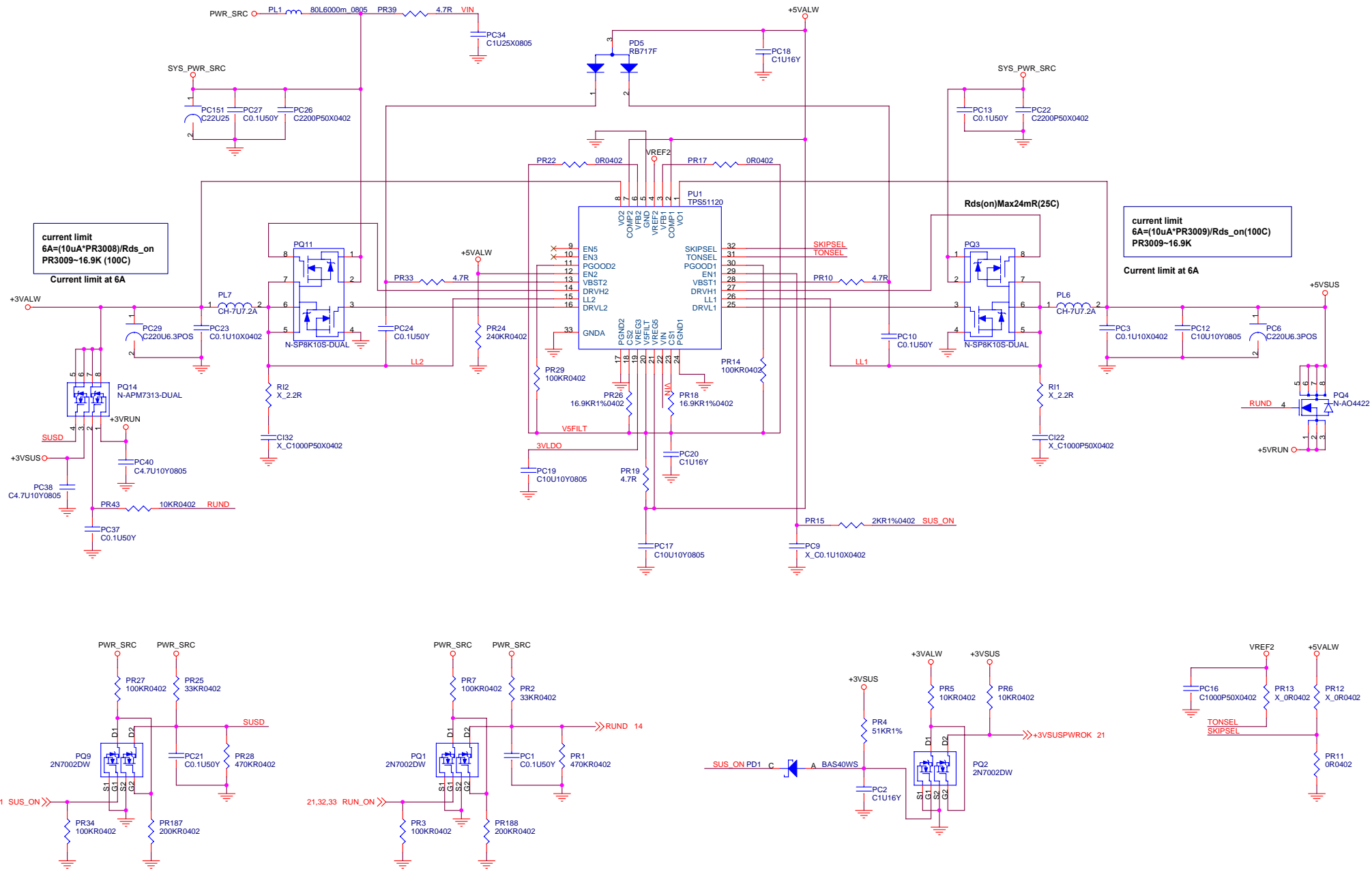
SPDIF ON/OFF CONTROL



<b>MSI CORPORATION</b>		
Title	<b>Audio Amp. &amp; Jacks</b>	
Size	Document Number	Rev
A3	<b>MS-1221</b>	1.0
Date:	Monday, March 19, 2007	Sheet 28 of 41

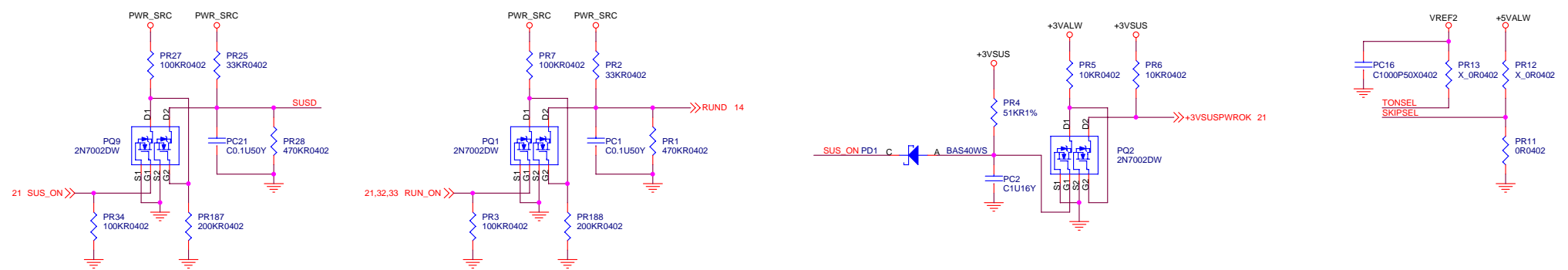




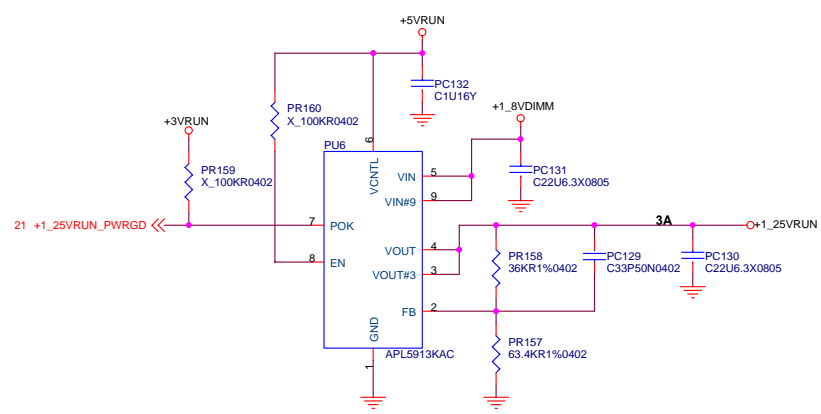
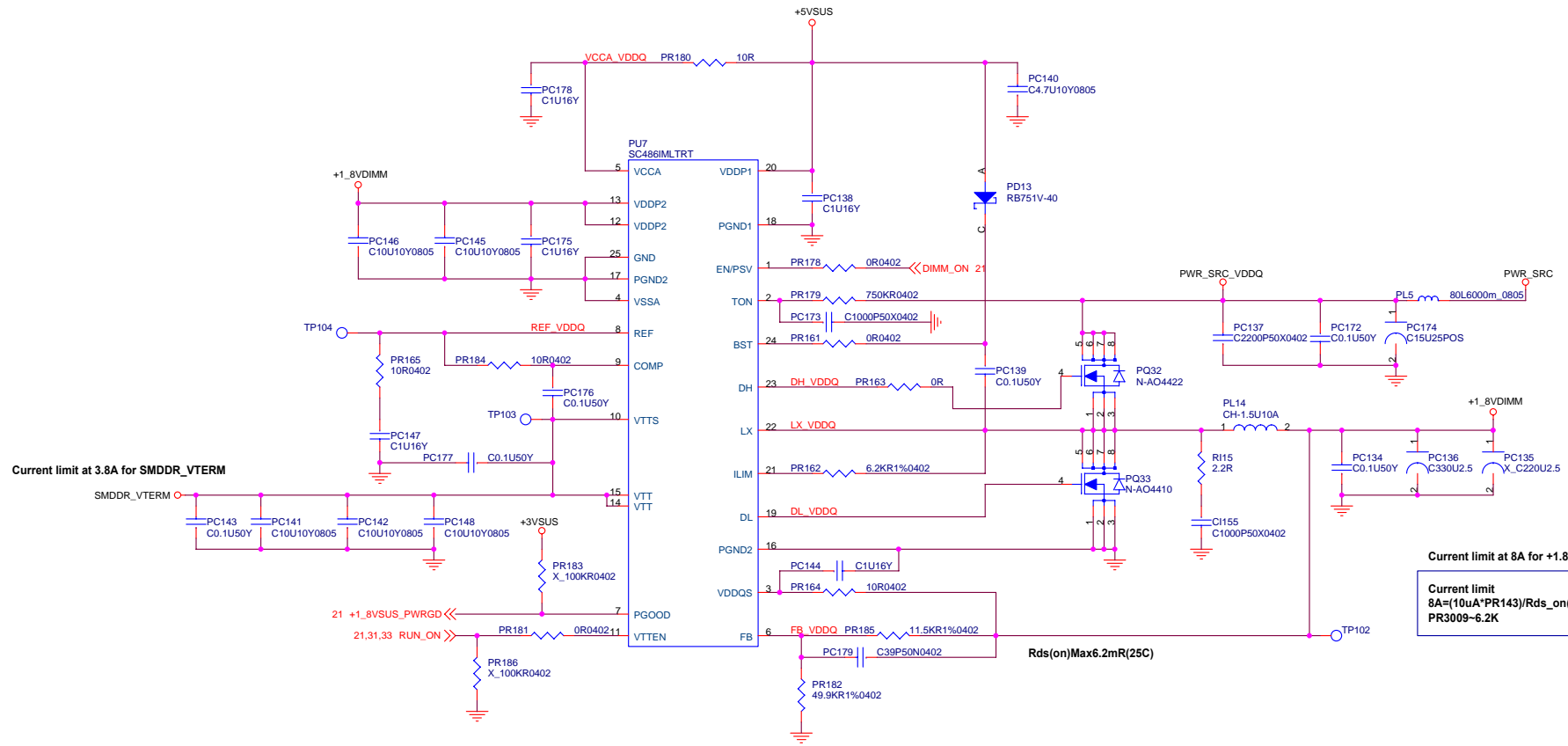


current limit  
 $6A = (10\mu A \cdot PR3008) / Rds\_on$   
 PR3009~16.9K (100C)  
 Current limit at 6A

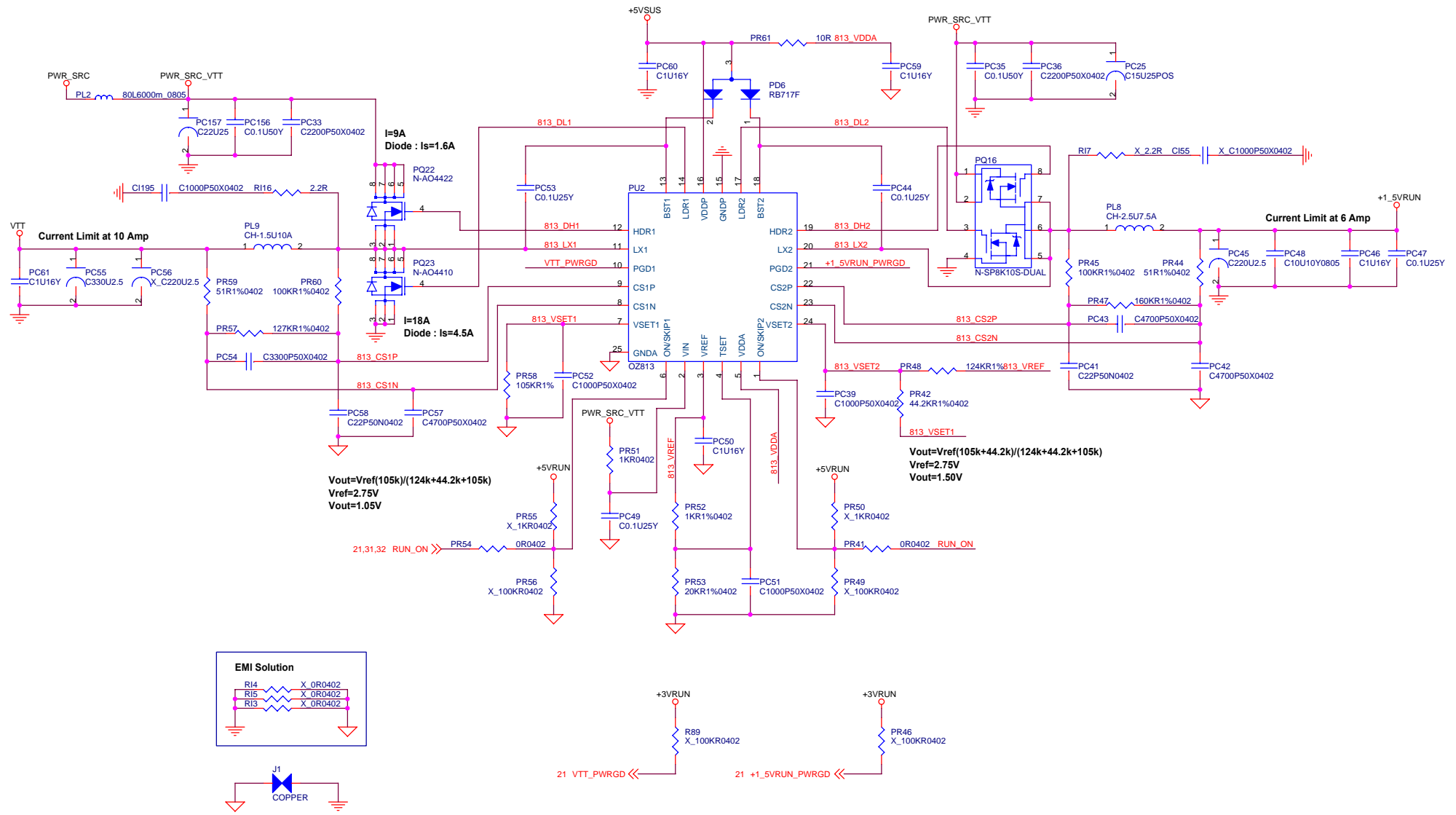
current limit  
 $6A = (10\mu A \cdot PR3009) / Rds\_on(100C)$   
 PR3009~16.9K  
 Current limit at 6A



<b>MSI CORPORATION</b>		
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Title: <b>DDR2 RAM POWER, +1.25V</b>		
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$$V_{out} = \frac{V_{ref}(105k)}{(124k + 44.2k + 105k)}$$

$$V_{ref} = 2.75V$$

$$V_{out} = 1.05V$$

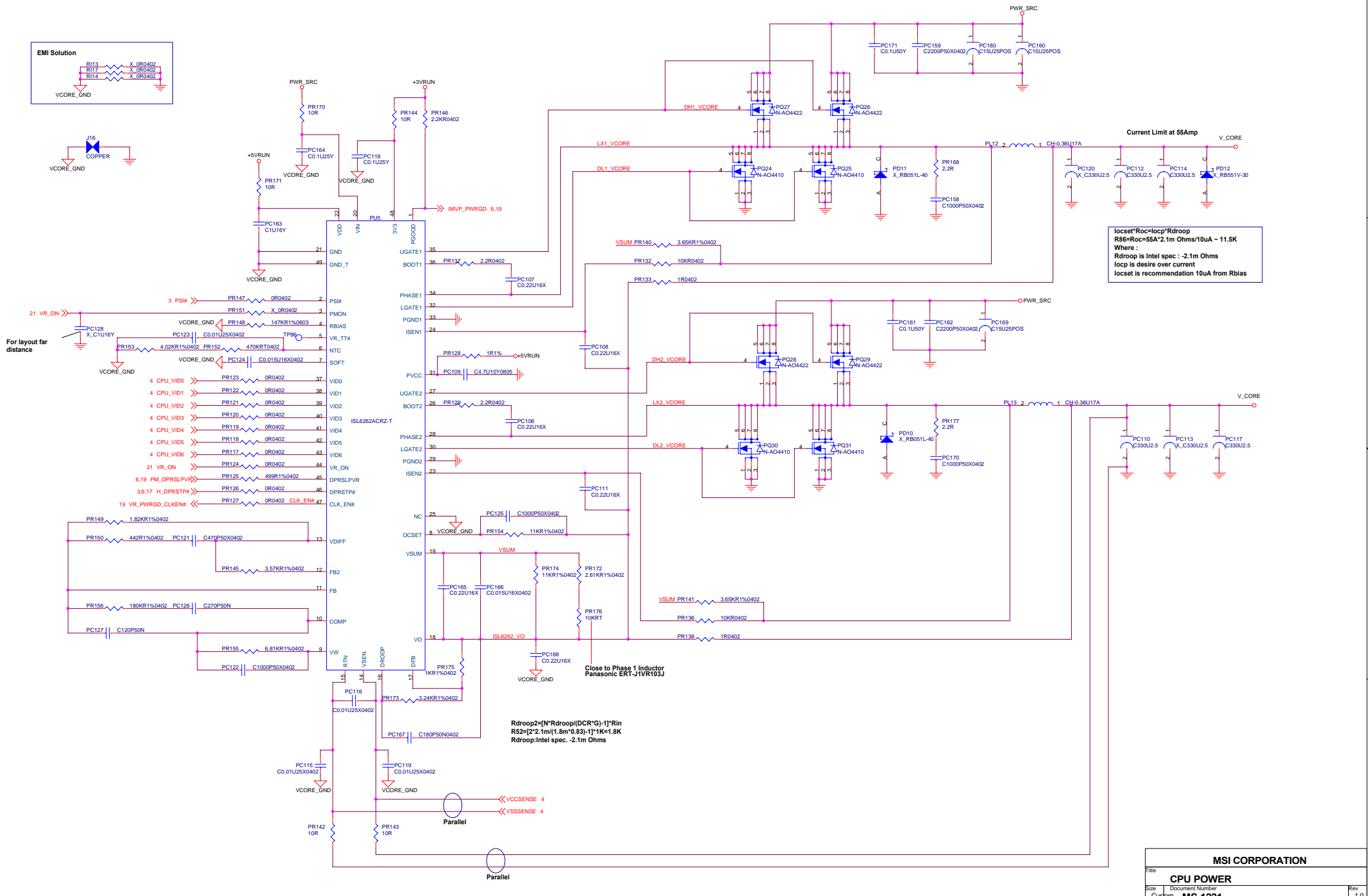
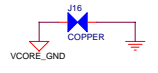
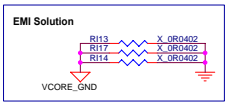
$$V_{out} = \frac{V_{ref}(105k + 44.2k)}{(124k + 44.2k + 105k)}$$

$$V_{ref} = 2.75V$$

$$V_{out} = 1.50V$$

<b>MSI CORPORATION</b>			
Title			
<b>+1.5VSRUN , VTT POWER</b>			
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For layout far distance

Current Limit at 55Amp

$l_{ocset} \cdot R_{oc} = l_{ocp} \cdot R_{droop}$   
 $R_{88} = R_{oc} = 55A \cdot 2.1m \text{ Ohms} / 10uA \sim 11.5K$   
 Where :  
 Rdroop is Intel spec : -2.1m Ohms  
 l<sub>ocp</sub> is desire over current  
 l<sub>ocset</sub> is recommendation 10uA from Rbias

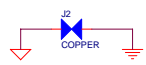
$R_{droop2} = [N \cdot R_{droop} (DCR \cdot G) - 1] \cdot R_{in}$   
 $R_{S2} = [2 \cdot 2.1m (1.8m \cdot 0.83) - 1] \cdot 1K = 1.8K$   
 Rdroop Intel spec -2.1m Ohms

Close to Phase 1 Inductor  
Panasonic ER1-J1VR103J

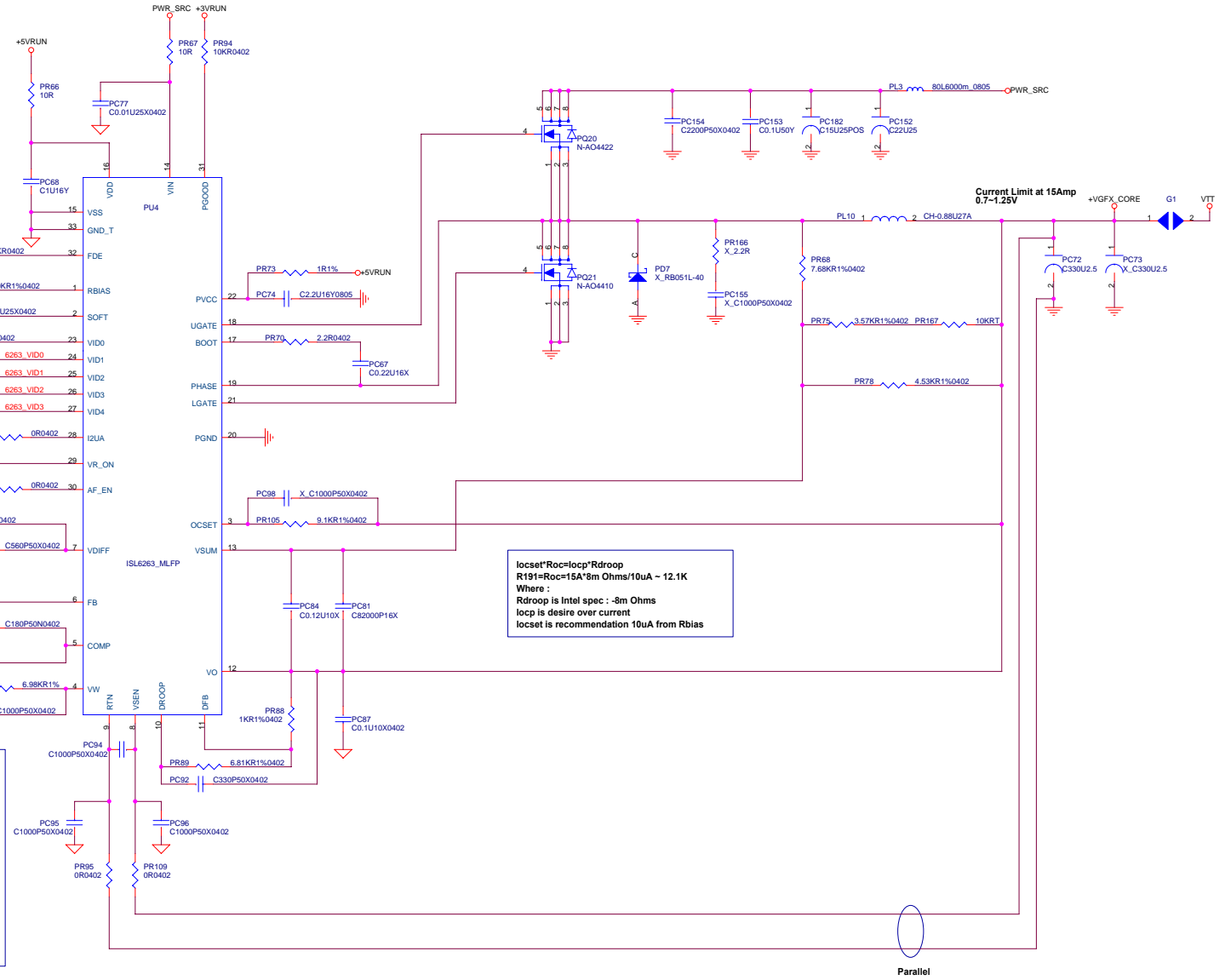
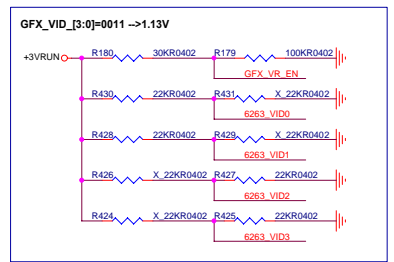
Parallel

Parallel

<b>MSI CORPORATION</b>			
Title			
<b>CPU POWER</b>			
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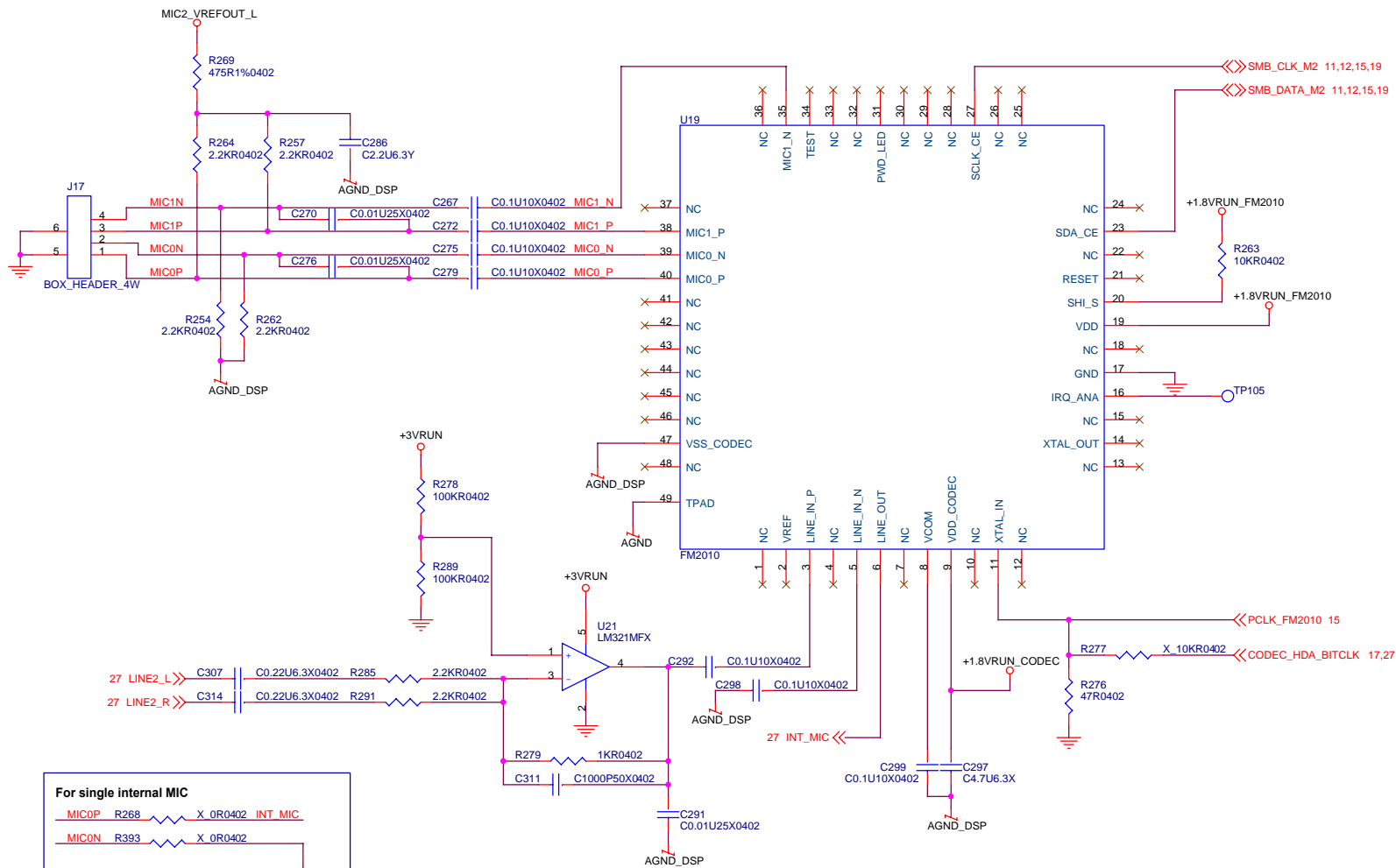
FDE single high should be < 3.3V



locset\*Roc=locp\*Rdroop  
 $R191 = Roc = 15A * 8m\ Ohms / 10uA \sim 12.1K$   
 Where :  
 Rdroop is Intel spec : -8m Ohms  
 locp is desire over current  
 locset is recommendation 10uA from Rbias

Current Limit at 15Amp  
 0.7-1.25V

Parallel

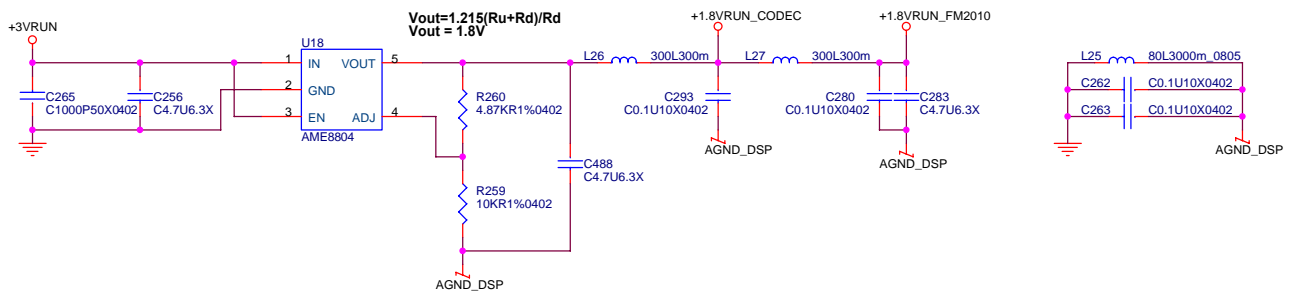


**For single internal MIC**

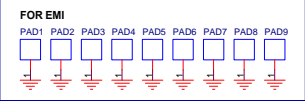
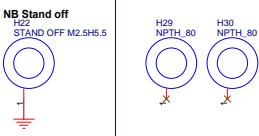
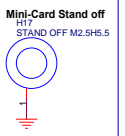
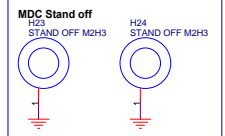
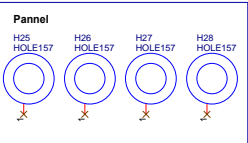
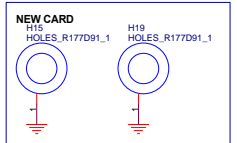
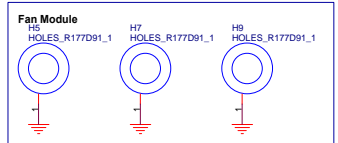
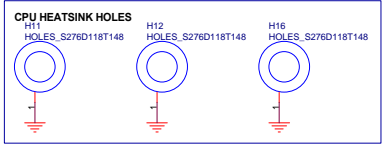
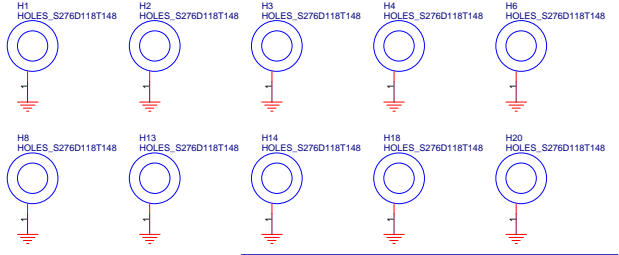
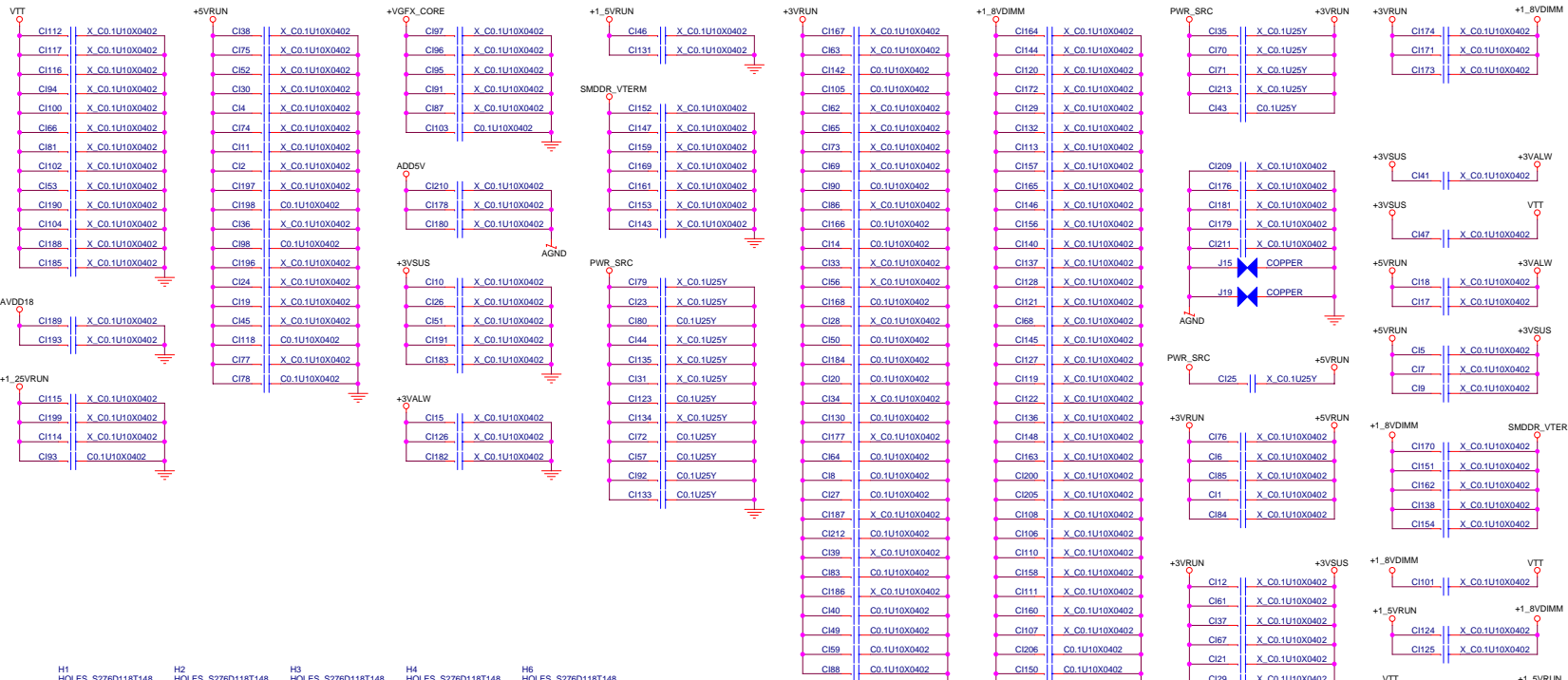
MIC0P R268 X 0R0402 INT\_MIC

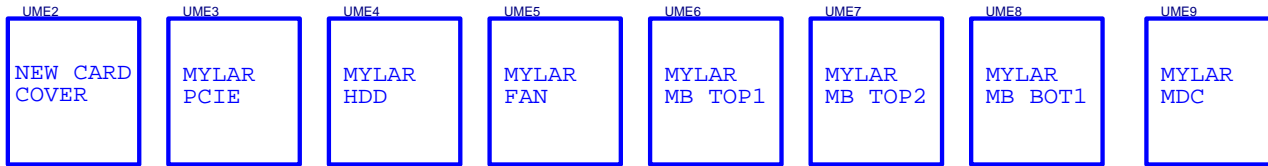
MIC0N R393 X 0R0402

AGND\_DSP

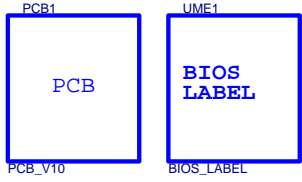


<b>MSI CORPORATION</b>		
Title		
<b>Array Mic FM2010</b>		
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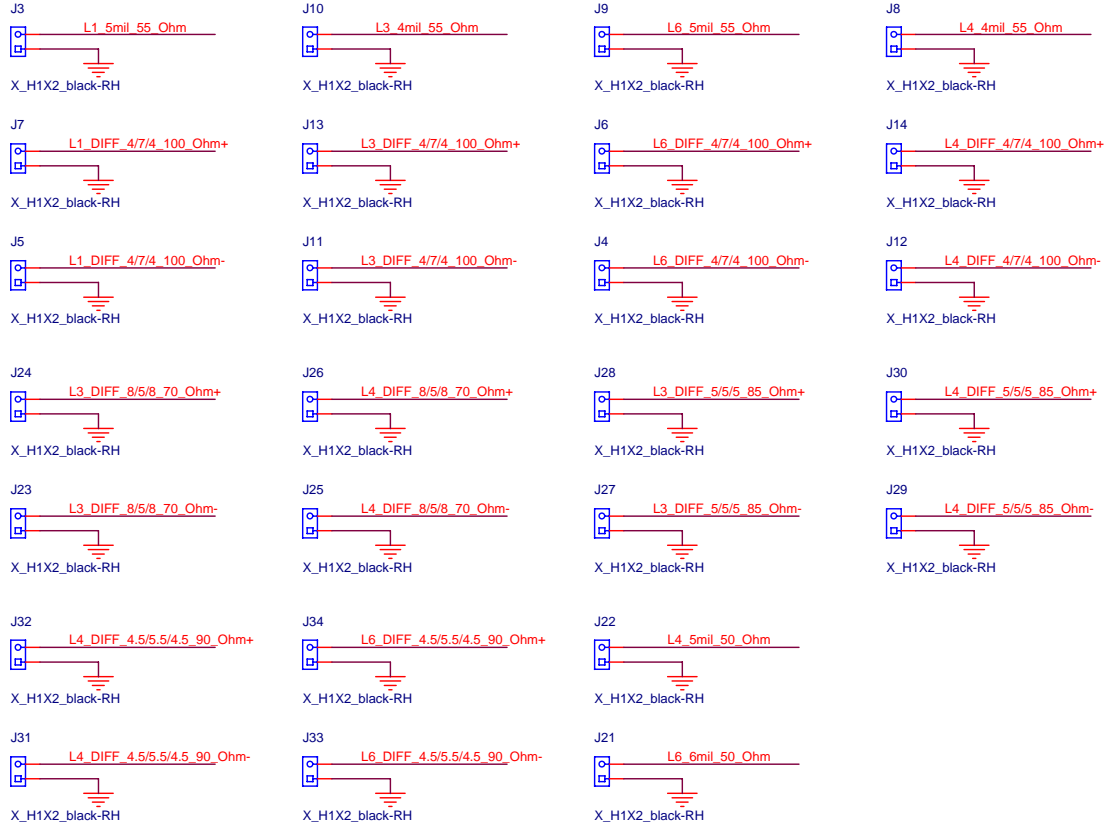
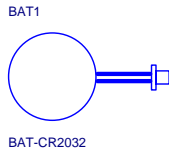
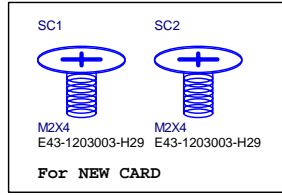




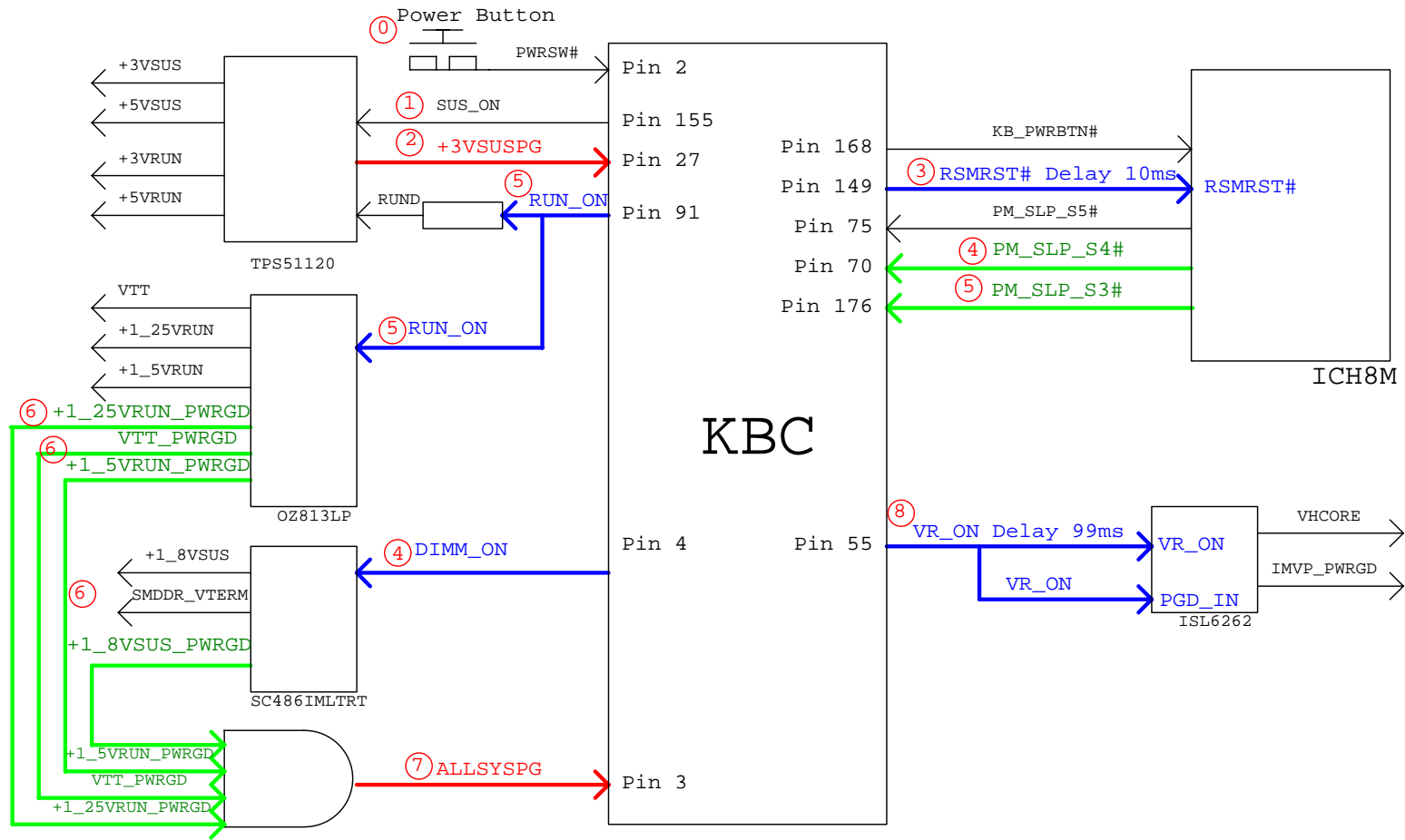
NEW CARD SHIELDING E2M-2210111-SH4  
 MYLAR PCIE E2Y-2210211-G40  
 MYLAR HDD E2Y-2210311-G40  
 MYLAR FAN E2Y-2210411-G40  
 MYLAR MB TOP1 E2P-2211611-G40  
 MYLAR MB TOP2 E2P-2211711-G40  
 MYLAR MB BOT1 E2P-2211511-G40  
 MYLAR MDC E2P-2213211-G40



P30-1221110-T53, 健鼎  
 P30-1221110-D05, 昆穎  
 P30-1221110-Y34, 元茂

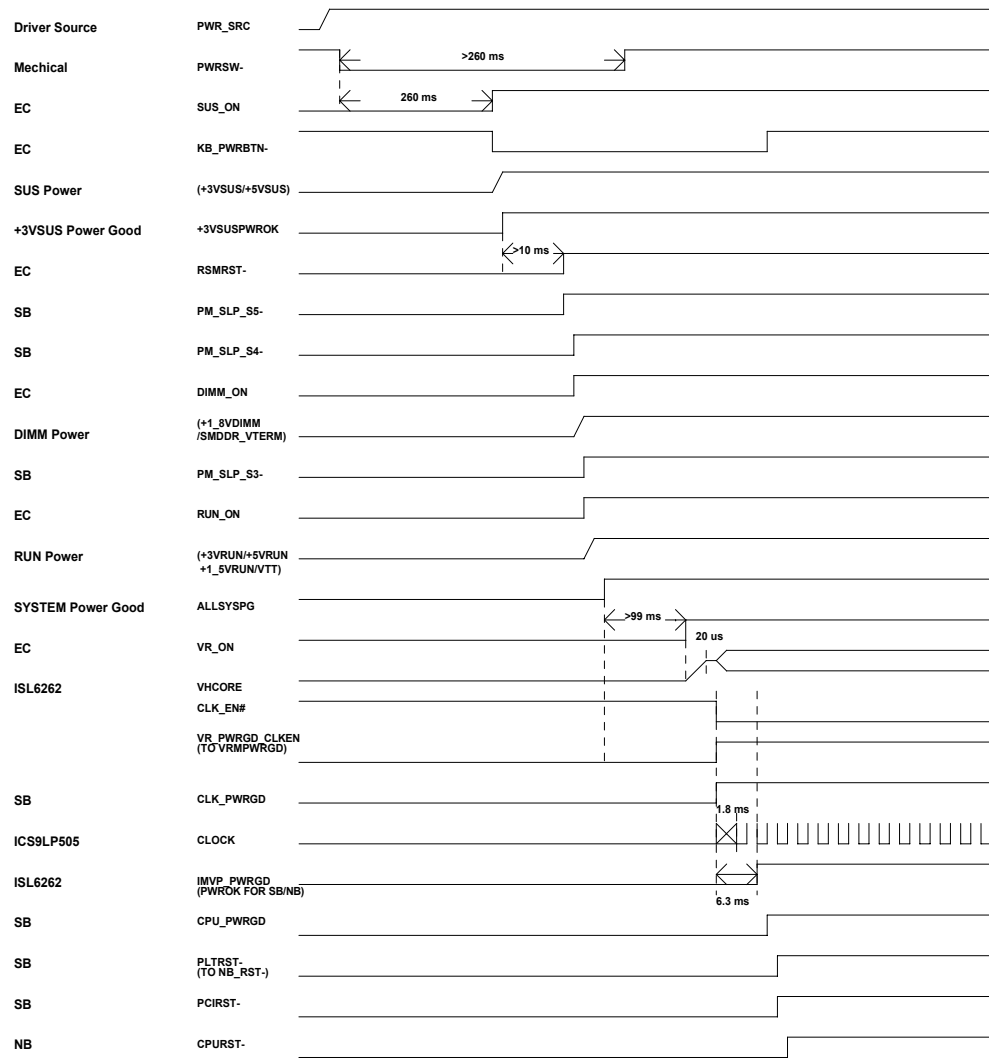


<b>MSI CORPORATION</b>		
Title		
<b>Non-Footprint for BOM</b>		
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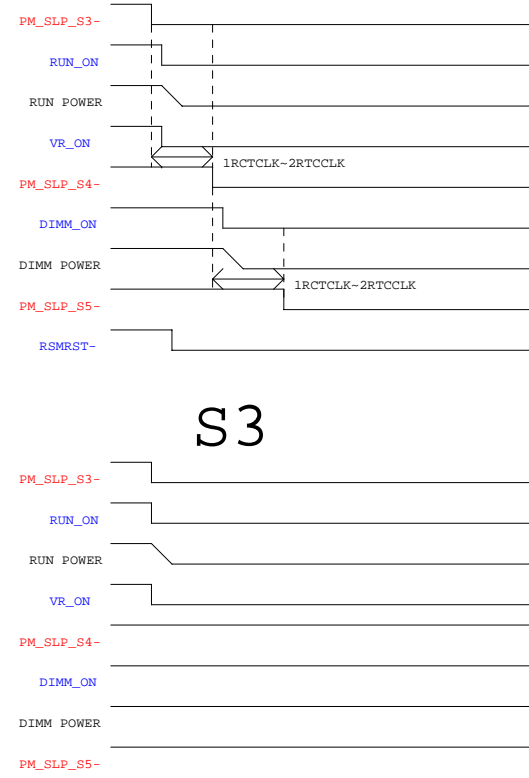


<b>MSI CORPORATION</b>			
Title			
<b>KBC_CTR_PWR_BD</b>			
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# Power Up



# Power Down





**MS-1221 Revision: 0D**

Rev	Date	Page	Description	Rev	Date	Page	Description
0A	2006/08/07		<ul style="list-style-type: none"> <li>● first version be released.</li> </ul>				
0B	2006/09/05		<ul style="list-style-type: none"> <li>● 2nd version be released.</li> </ul>				
0C	2006/10/24	- 34 -	<ul style="list-style-type: none"> <li>● change PR150 -1.4K to 442R,PR145 -2K to 3.57K ,PR156 -61.9K to 180K,PC126 -0.033U to 270p ,PC127 -390p to 120p,PR155 -4.42K to 6.81K ,PC122 -47p to 1000p,PR173 -3.6K to 3.24K ,PR154 -11.5K to 11K for load line and transient.</li> </ul>				
		- 35 -	<ul style="list-style-type: none"> <li>● change PR89 -6.04K to 6.81K,PR105 -12.1K to 9.1K for load line and transient.</li> </ul>				
		- 31 -	<ul style="list-style-type: none"> <li>● add PR187,PR188 -200K for decreasing Gate voltage of 2N7002DW.</li> </ul>				
	2006/10/31	- 27 -	<ul style="list-style-type: none"> <li>● change ALC883 to ALC888 chip.</li> </ul>				
		- 21 -	<ul style="list-style-type: none"> <li>● change R33 -100K to 4.7K for pulling up level of voltage.</li> <li>● pop R38,RB13,RB5,RT3 and no-pop RB12,RB17</li> <li>● remove UT1 -BIOS socket.</li> </ul>				
		- 34 -	<ul style="list-style-type: none"> <li>● change PR146 -100K to 2.2K for pulling up level of voltage.</li> </ul>				
		- 06 -	<ul style="list-style-type: none"> <li>● change GFX_VID[3:0] H/W strap to adjustable setting.</li> </ul>				
		- 09 -	<ul style="list-style-type: none"> <li>● change L21 to R31 -100R and add C492 -1uF to eliminate CRT/TV noise.</li> </ul>				
		- 15 -	<ul style="list-style-type: none"> <li>● change ICS9LP505 to SLG8SP512.</li> </ul>				
		- 36 -	<ul style="list-style-type: none"> <li>● change R276 -10K to 47R and no-pop R277, connect CLK_IN of FM2010 from PCI clock to fix FM2010 no function.</li> </ul>				
		- 16 -	<ul style="list-style-type: none"> <li>● add R34 for DDC power.</li> </ul>				
	2006/11/03	- 23 -	<ul style="list-style-type: none"> <li>● no-pop R10,CT1,CT3,CT9,CT12.</li> </ul>				
		- 22 -	<ul style="list-style-type: none"> <li>● change EC1,EC2,C36 to 100uF POS Cap for ME height limitation.</li> <li>● change USB3 to SMT type for ME height limitation.</li> </ul>				
		- 25 -	<ul style="list-style-type: none"> <li>● change J20 to new SIM card for ME request.</li> </ul>				
		- 21 -	<ul style="list-style-type: none"> <li>● change CON1 to R/A type for ME request.</li> </ul>				
		- 14 -	<ul style="list-style-type: none"> <li>● change U11 -Sil1390 to Sil1392 chip.</li> </ul>				
	2006/11/06	- 26 -	<ul style="list-style-type: none"> <li>● change CON8 to another P/N.</li> </ul>				
	2006/11/13	- 26 -	<ul style="list-style-type: none"> <li>● add RT5, pop R177,R178,Q13,Q14 for Cap Sense Launch board.</li> </ul>				
		- 11 -	<ul style="list-style-type: none"> <li>● add DDR2 thermal sensor circuit.</li> </ul>				
		- 22 -	<ul style="list-style-type: none"> <li>● remove CIR circuit.</li> </ul>				
		- 21 -	<ul style="list-style-type: none"> <li>● define pin-30 of UB1 to be as HOT_START_K- function. (Vista Hot Start)</li> </ul>				
	2006/11/20	- 09 -	<ul style="list-style-type: none"> <li>● pop D3,R210.</li> </ul>				
		- 19 -	<ul style="list-style-type: none"> <li>● no-pop R92,R106,R340,R129,R312,R329,R70 and pop DB6.</li> </ul>				
		- 21 -	<ul style="list-style-type: none"> <li>● no-pop UT1,CT4 and pop U50,CT43 for 8M FLASH.</li> </ul>				
0D	2006/12/27~ 2007/1/10	- 03 -	<ul style="list-style-type: none"> <li>● Change HW thermal shunt down circuit</li> </ul>				
		- 13 -	<ul style="list-style-type: none"> <li>● Change RNT1, RNT2, RNT3 trace connect</li> </ul>				
		- 15 -	<ul style="list-style-type: none"> <li>● Add C498 for EMI</li> </ul>				
		- 21 -	<ul style="list-style-type: none"> <li>● Change RB6, RT6, R23 pull-high from 100K to 10K</li> </ul>				
		- 25 -	<ul style="list-style-type: none"> <li>● Change R292, R293, R414, R415, R416 from 220R to 180R</li> <li>● Change LED6 from D0C-0400500-L05 to D0C-0403520-L05</li> <li>● Change LED7 from D0C-0401000-R06 to LED7: D0C-0403520-L05 to LED9: D0C-0403000-E07</li> <li>● Change LED8 from D0C-0403000-L05 to D0C-0403520-L05</li> </ul>				
		- 32 -	<ul style="list-style-type: none"> <li>● Change PR185 from 10K to 11.5K to improve DIMM power</li> </ul>				
		- 34 -	<ul style="list-style-type: none"> <li>● SWAP PQ24, PQ25, PQ26, PQ27, PR168, PC158 with PQ28, PQ29, PQ30, PQ31, PR177, PC170</li> </ul>				
		- 37 -	<ul style="list-style-type: none"> <li>● Change footprint H5, H7, H9, H15, H19 from mask to non-mask for SMT DFM request</li> <li>● Change H10 footprint for SMT DFM request</li> <li>● Change H17 from Top to Bottom</li> <li>● Add C1213 for EMI request</li> </ul>				

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