

**CoolMOS™ Power Transistor**
**Features**

- New revolutionary high voltage technology
- Extreme dv/dt rated
- High peak current capability
- Qualified according to JEDEC<sup>1)</sup> for target applications
- Pb-free lead plating; RoHS compliant
- Ultra low gate charge
- Ultra low effective capacitances
- Fully isolated package (2500 VAC; 1 minute)

**CoolMOS™ 800V designed for:**

- Industrial application with high DC bulk voltage
- Switching Application ( i.e. active clamp forward )

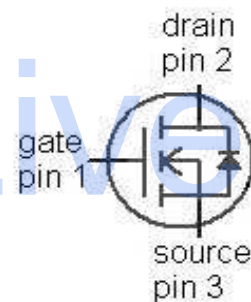
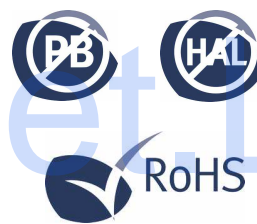
**Product Summary**

$V_{DS}$	800	V
$R_{DS(on)max}$ @ $T_j = 25^\circ\text{C}$	0.45	$\Omega$
$Q_{g,typ}$	64	nC

PG-TO220-3 (fully isolated)



Type	Package	Marking
SPA11N80C3	PG-TO220-3	11N80C3


**Maximum ratings, at  $T_j=25^\circ\text{C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current <sup>2)</sup>	$I_D$	$T_C=25^\circ\text{C}$	11	A
		$T_C=100^\circ\text{C}$	7.1	
Pulsed drain current <sup>3)</sup>	$I_{D,pulse}$	$T_C=25^\circ\text{C}$	33	
Avalanche energy, single pulse	$E_{AS}$	$I_D=2.2\text{ A}, V_{DD}=50\text{ V}$	470	mJ
Avalanche energy, repetitive $t_{AR}$ <sup>3),4)</sup>	$E_{AR}$	$I_D=11\text{ A}, V_{DD}=50\text{ V}$	0.2	
Avalanche current, repetitive $t_{AR}$ <sup>3),4)</sup>	$I_{AR}$		11	A
MOSFET dv/dt ruggedness	dv/dt	$V_{DS}=0\dots640\text{ V}$	50	V/ns
Gate source voltage	$V_{GS}$	static	$\pm 20$	V
		AC ( $f>1\text{ Hz}$ )	$\pm 30$	
Power dissipation	$P_{tot}$	$T_C=25^\circ\text{C}$	34	W
Operating and storage temperature	$T_j, T_{stg}$		-55 ... 150	$^\circ\text{C}$
Mounting torque		M2.5 screws	50	Ncm

**Maximum ratings**, at  $T_j=25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous diode forward current	$I_S$	$T_C=25\text{ °C}$	11	A
Diode pulse current <sup>3)</sup>	$I_{S,pulse}$		33	
Reverse diode $dv/dt$ <sup>5)</sup>	$dv/dt$		4	V/ns

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Thermal characteristics**

Thermal resistance, junction - case	$R_{thJC}$		-	-	3.7	K/W
Thermal resistance, junction - ambient	$R_{thJA}$	leaded	-	-	80	
Soldering temperature, wave soldering only allowed at leads	$T_{sold}$	1.6 mm (0.063 in.) from case for 10s	-	-	260	°C

**Electrical characteristics**, at  $T_j=25\text{ °C}$ , unless otherwise specified

**Static characteristics**

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}$ , $I_D=250\text{ }\mu\text{A}$	800	-	-	V
Avalanche breakdown voltage	$V_{(BR)DS}$	$V_{GS}=0\text{ V}$ , $I_D=11\text{ A}$	-	870	-	
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$ , $I_D=0.68\text{ mA}$	2.1	3	3.9	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=800\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$	-	-	20	$\mu\text{A}$
		$V_{DS}=800\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=150\text{ °C}$	-	100	-	
Gate-source leakage current	$I_{GSS}$	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{ V}$ , $I_D=7.1\text{ A}$ , $T_j=25\text{ °C}$	-	0.39	0.45	$\Omega$
		$V_{GS}=10\text{ V}$ , $I_D=7.1\text{ A}$ , $T_j=150\text{ °C}$	-	1.05	-	
Gate resistance	$R_G$	$f=1\text{ MHz}$ , open drain	-	1.2	-	$\Omega$

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics**

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=100\text{ V},$	-	1600	-	pF
Output capacitance	$C_{oss}$	$f=1\text{ MHz}$	-	65	-	
Effective output capacitance, energy related <sup>6)</sup>	$C_{o(er)}$	$V_{GS}=0\text{ V}, V_{DS}=0\text{ V}$ to 480 V	-	50	-	
Effective output capacitance, time related <sup>7)</sup>	$C_{o(tr)}$		-	140	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=400\text{ V},$ $V_{GS}=0/10\text{ V}, I_D=11\text{ A},$ $R_G=7.5\text{ }\Omega, T_j = 25^\circ\text{C}$	-	25	-	ns
Rise time	$t_r$		-	15	-	
Turn-off delay time	$t_{d(off)}$		-	72	-	
Fall time	$t_f$		-	10	-	

**Gate Charge Characteristics**

Gate to source charge	$Q_{gs}$	$V_{DD}=640\text{ V}, I_D=11\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	8	-	nC
Gate to drain charge	$Q_{gd}$		-	30	-	
Gate charge total	$Q_g$		-	64	85	
Gate plateau voltage	$V_{plateau}$		-	5.5	-	V

**Reverse Diode**

Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=I_S=11\text{ A},$ $T_j=25^\circ\text{C}$	-	1	1.2	V
Reverse recovery time	$t_{rr}$	$V_R=400\text{ V},$ $I_F=I_S=11\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	550	-	ns
Reverse recovery charge	$Q_{rr}$		-	10	-	$\mu\text{C}$
Peak reverse recovery current	$I_{rrm}$		-	33	-	A

<sup>1)</sup> J-STD20 and JESD22

<sup>2)</sup> Limited only by maximum temperature

<sup>3)</sup> Pulse width  $t_p$  limited by  $T_{j,max}$ 
<sup>4)</sup> Repetitive avalanche causes additional power losses that can be calculated as  $P_{AV}=E_{AR} \cdot f$ .

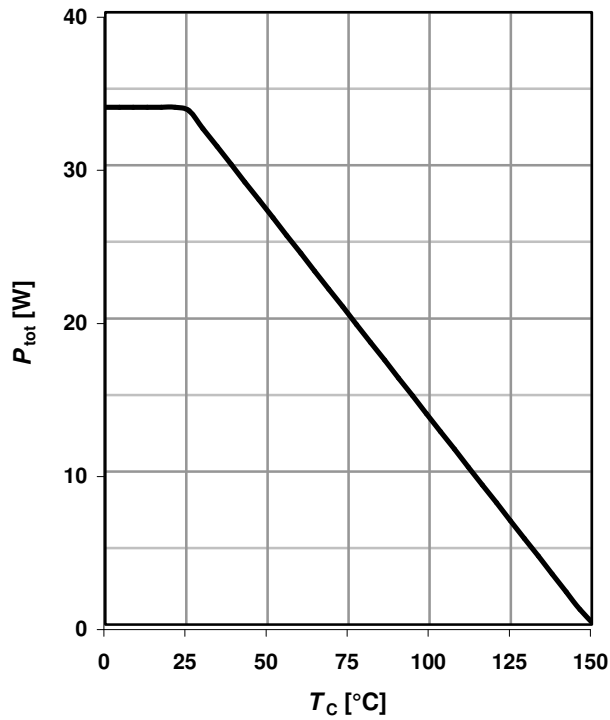
<sup>5)</sup>  $I_{SD}=I_D, di/dt=400\text{ A}/\mu\text{s}, V_{DClink} = 400\text{ V}, V_{peak}<V_{(BR)DSS}, T_j<T_{j,max}$ , identical low side and high side switch

<sup>6)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

<sup>7)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

**1 Power dissipation**

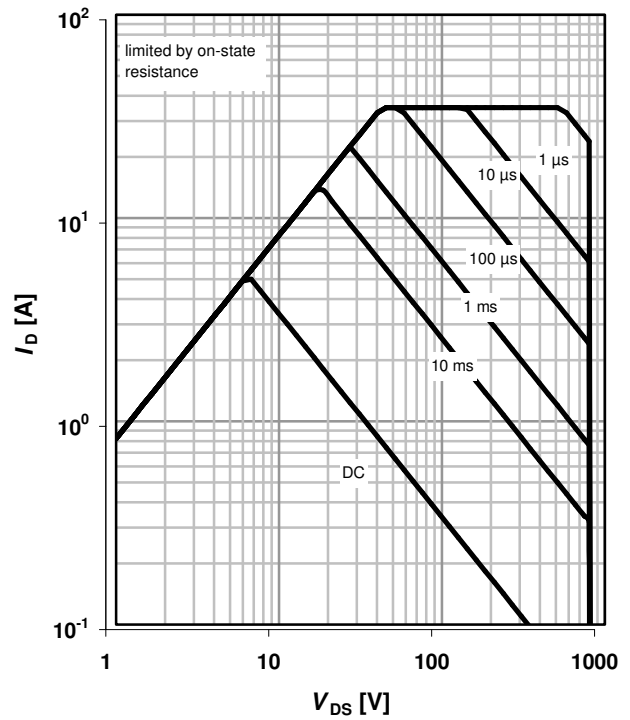
$P_{tot}=f(T_C)$



**2 Safe operating area**

$I_D=f(V_{DS}); T_C=25\text{ °C}; D=0$

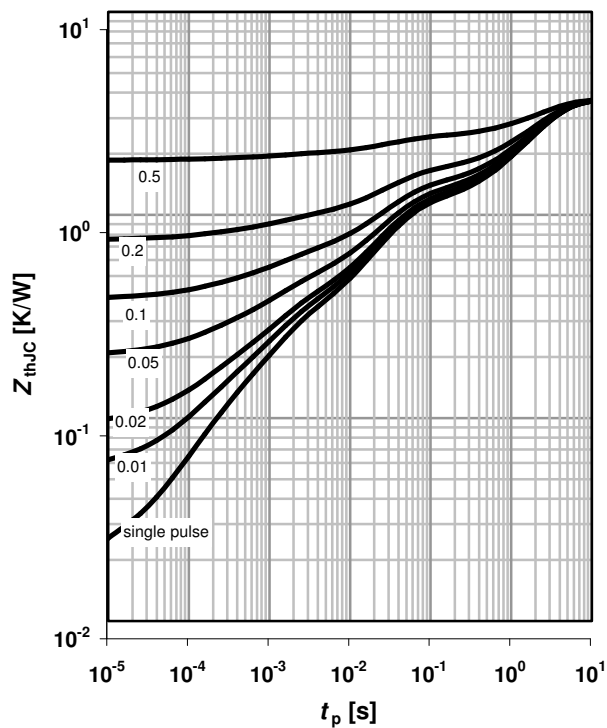
parameter:  $t_p$



**3 Max. transient thermal impedance**

$Z_{thJC}=f(t_p)$

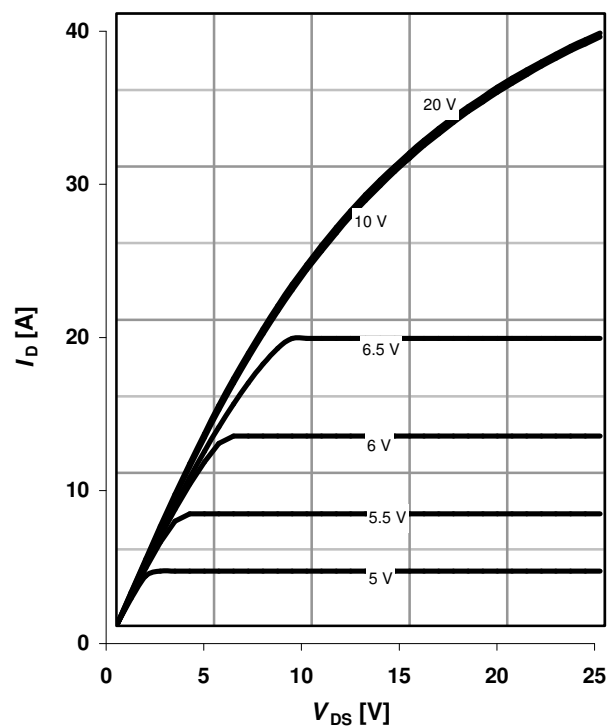
parameter:  $D=t_p/T$



**4 Typ. output characteristics**

$I_D=f(V_{DS}); T_j=25\text{ °C}; t_p=10\text{ μs}$

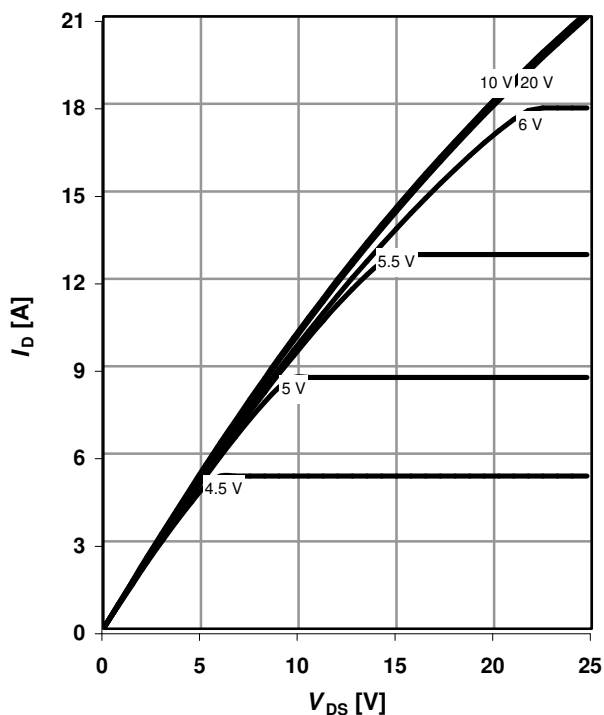
parameter:  $V_{GS}$



**5 Typ. output characteristics**

$I_D=f(V_{DS}); T_j=150\text{ °C}; t_p=10\text{ }\mu\text{s}$

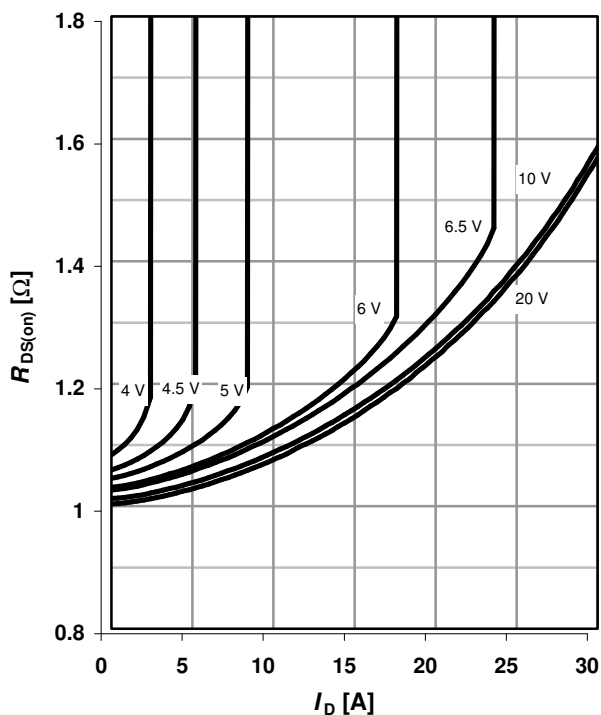
parameter:  $V_{GS}$



**6 Typ. drain-source on-state resistance**

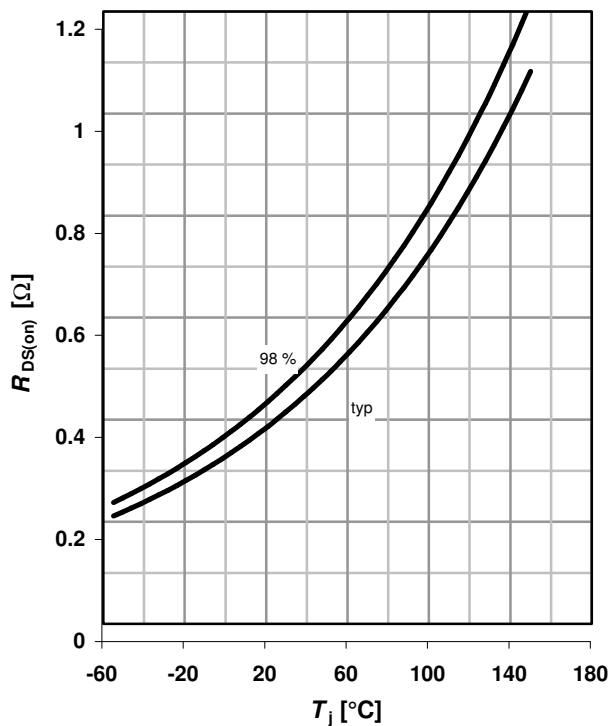
$R_{DS(on)}=f(I_D); T_j=150\text{ °C}$

parameter:  $V_{GS}$



**7 Drain-source on-state resistance**

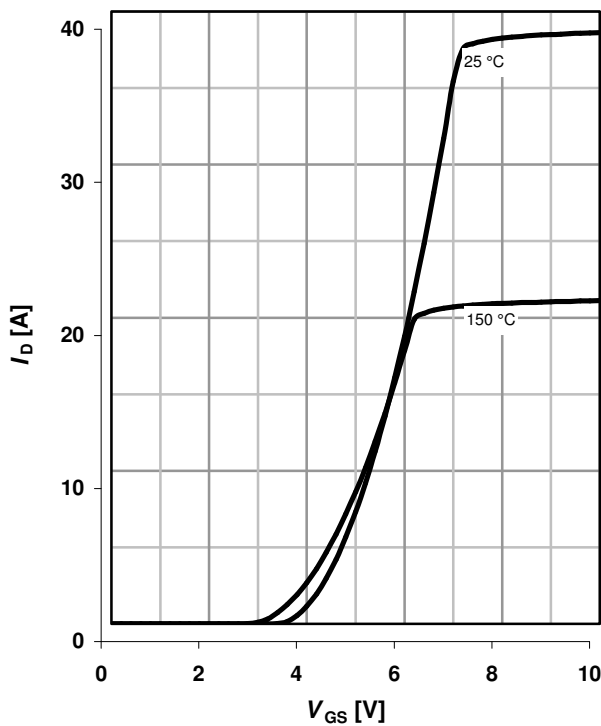
$R_{DS(on)}=f(T_j); I_D=7.1\text{ A}; V_{GS}=10\text{ V}$



**8 Typ. transfer characteristics**

$I_D=f(V_{GS}); |V_{DS}|>2|I_D|R_{DS(on)max}; t_p=10\text{ }\mu\text{s}$

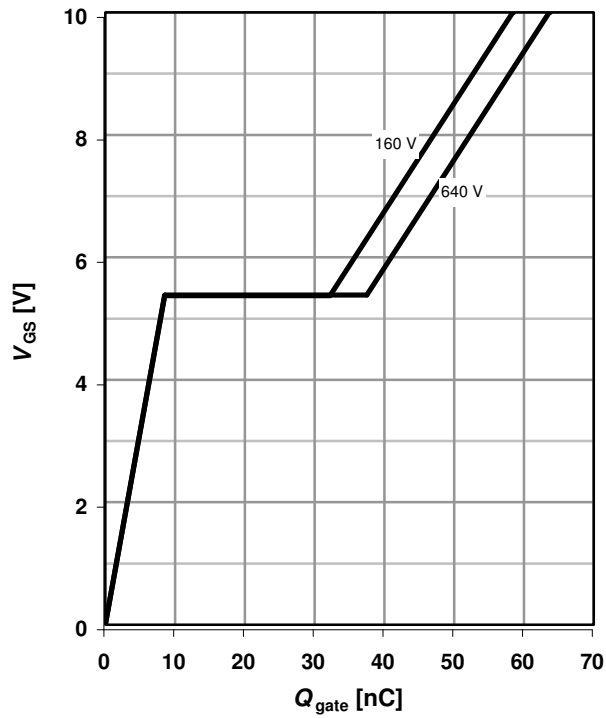
parameter:  $T_j$



**9 Typ. gate charge**

$V_{GS}=f(Q_{gate}); I_D=11\text{ A pulsed}$

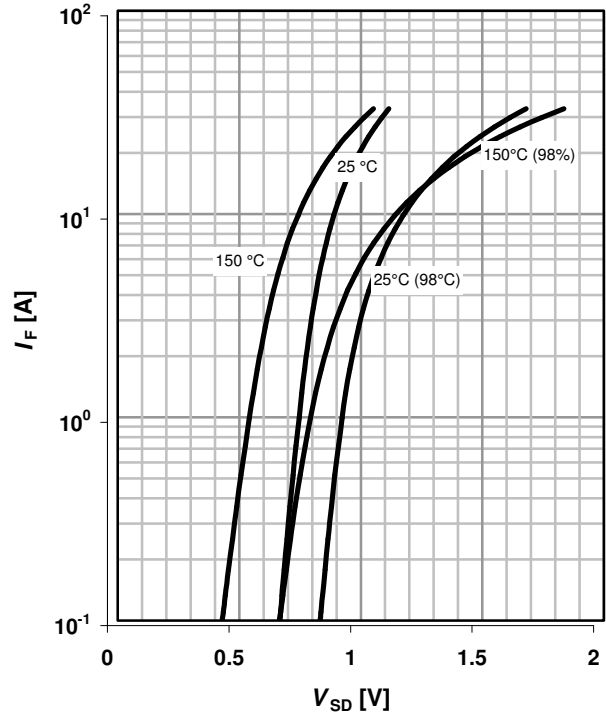
parameter:  $V_{DD}$



**10 Forward characteristics of reverse diode**

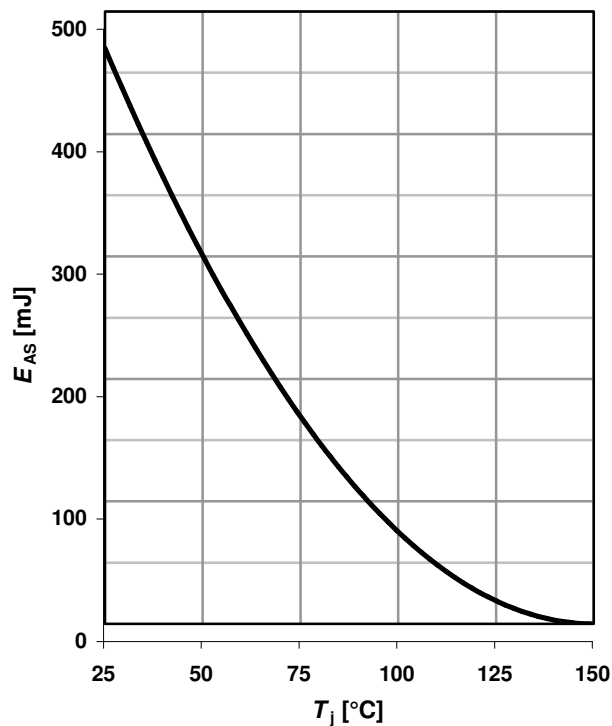
$I_F=f(V_{SD}); t_p=10\ \mu s$

parameter:  $T_j$



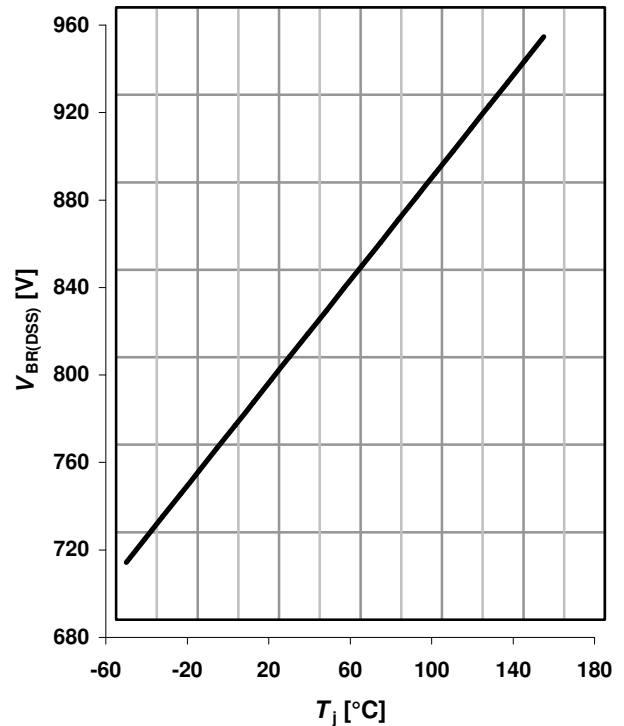
**11 Avalanche energy**

$E_{AS}=f(T_j); I_D=2.2\text{ A}; V_{DD}=50\text{ V}$



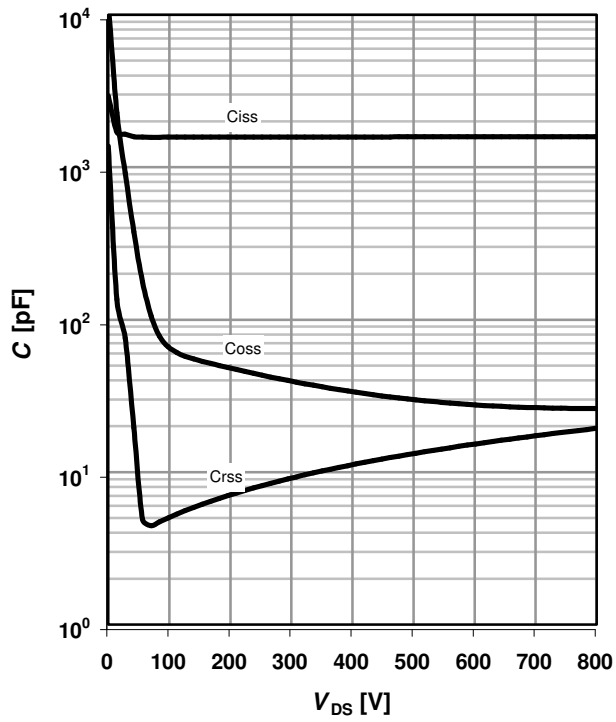
**12 Drain-source breakdown voltage**

$V_{BR(DSS)}=f(T_j); I_D=0.25\text{ mA}$



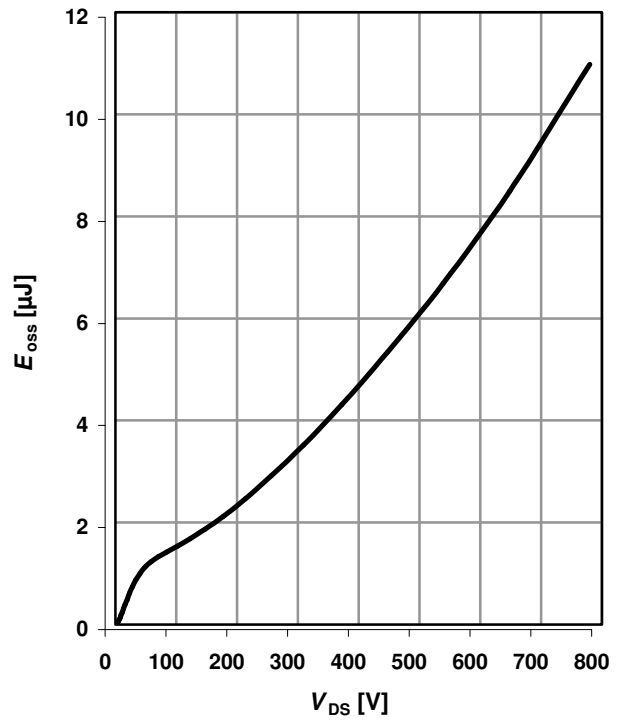
**13 Typ. capacitances**

$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$

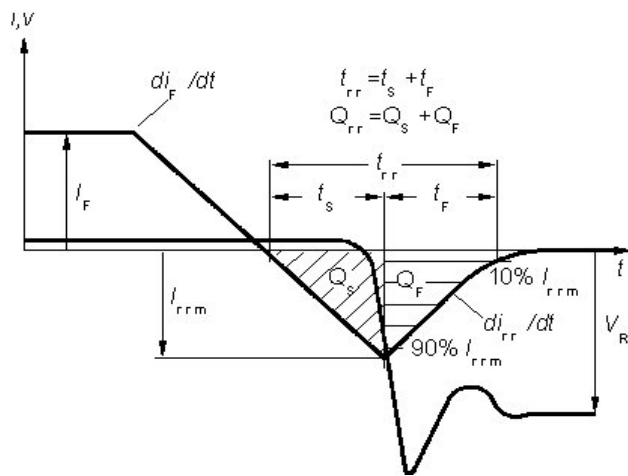


**14 Typ. Coss stored energy**

$E_{oss}=f(V_{DS})$

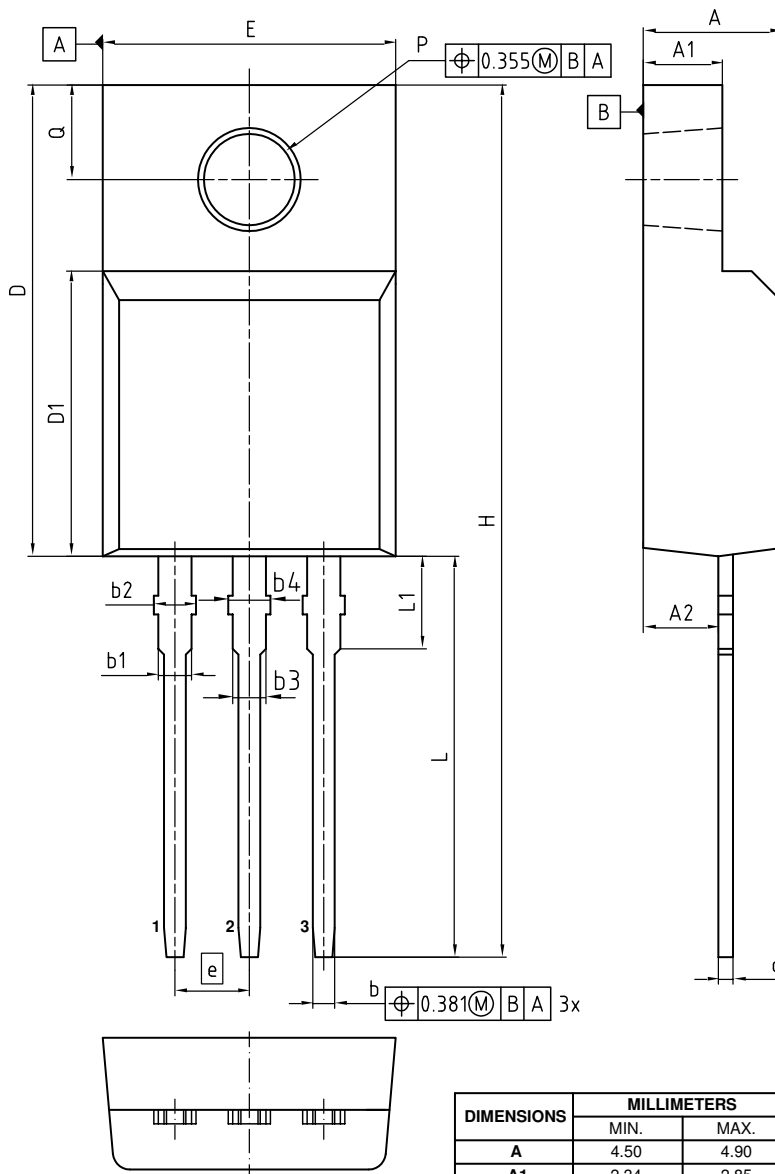


Definition of diode switching characteristics





Outline PG-TO220 FullPAK



NOTES:  
 ALL DIMENSIONS REFER TO JEDEC STANDARD TO-281  
 AND DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS  
 OR GATE BURRS  
 GATE BURRS ARE LESS THAN 0.5 mm

DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.50	4.90
A1	2.34	2.85
A2	2.42	2.86
b	0.65	0.90
b1	0.95	1.38
b2	0.95	1.51
b3	0.65	1.38
b4	0.65	1.51
c	0.40	0.63
D	15.67	16.15
D1	8.97	9.83
E	10.00	10.65
e	2.54	
H	28.70	29.75
L	12.78	13.75
L1	2.83	3.45
øP	3.00	3.30
Q	3.15	3.50

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### Revision History

SPA11N80C3

**Revision: 2018-02-27, Rev. 2.93**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.92	2014-02-21	Ptot change according to diagramme 1 "power dissipation"
2.93	2018-02-27	Outline PG-TO-220 FullPAK update

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