National Semiconductor

ADVANCE INFORMATION
July 1989

NS16C451
Universal Asynchronous Receiver/Transmitter with Parallel Interface†

General Description

The NS16C451 integrates a CMOS version of the NS16450 UART with a bidirectional parallel interface into a single IC. The serial port is fully compatible with all existing software written for the INS8250A, INS82C50A, NS16450, and NS16C450. The parallel port is fully compatible with all existing software written for the IBM® PC, XT, AT, PS/2 and Centronics parallel ports.

The serial port includes one programmable baud rate generator capable of dividing the clock input by divisor of 1 to ($2^{16} - 1$), and producing a 16 × clock for driving the internal logic of both the receiver and transmitter sections. The serial port has MODEM-control capability and a processor interrupt system which supports 4 types of interrupts.

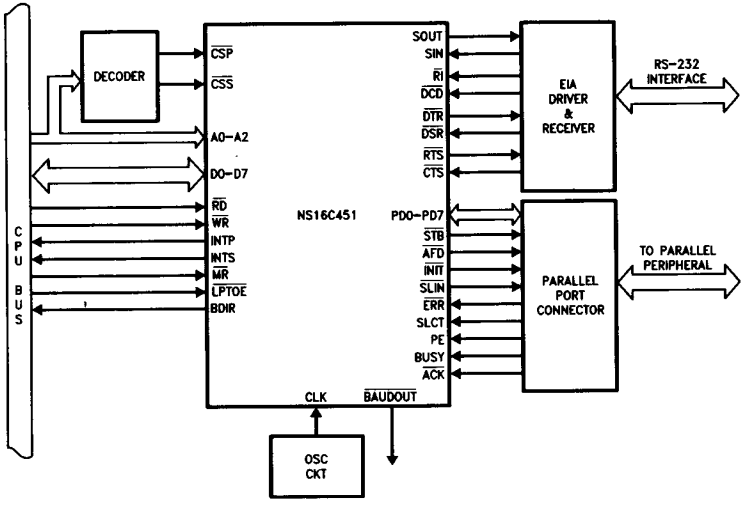
The parallel port has three registers—data, status, and control registers and is bidirectional. All of the signals required by PC and Centronics printers to transfer data and monitor printer status are provided.

Features

- Serial port capable of running existing software written for INS8250A and NS16450 series of products used in the IBM PC, XT, AT and PS/2
- Parallel port capable of running existing software written for the standard parallel port on the IBM PC, XT, AT and Centronics printers
- National's 1.25μ CMOS technology provides faster AC timing
- Maximum operating frequency 24 MHz
- Separate interrupt request lines for the parallel and serial ports
- Separate Chip Select signals for the parallel and serial ports
- Bus Direction control output helps avoid bus conflict when using an external data bus latch
- Adds or deletes standard asynchronous communication bits (start, parity, and stop) to or from the serial data
- Independently controlled transmit, receive, line status, and data set interrupts
- Programmable baud generator divides any input clock by 1 to ($2^{16} - 1$) and generate the 16 × clock
- MODEM control functions (CTS, RTS, DSR, DTR, RI and DCD)
- Fully programmable serial-interface characteristics:
  — 5, 6, 7, or 8 bit characters
  — Even, odd, or no parity generation and detection
  — 1, 1½, or 2 stop bit generation
- High current drive capability for the parallel port

†**Note:** This part is patented.

Basic Configuration



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1.0 Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to V_{SS}	−0.5V to +7.0V
Power Dissipation	1W

Note: *Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC electrical characteristics.*

2.0 DC Electrical Characteristics

T_A = 0°C to +70°C, V_{DD} = +5V ±10%, V_{SS} = 0V, unless otherwise specified

Symbol	Parameter	Conditions	Min	Max	Units
V_{IL}	Input Low Voltage		−0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}	V
V_{OL}	Output Low Voltage	I_{OL} = 12 mA on D0–D7 I_{OL} = 24 mA on PD0–PD7 I_{OL} = 20 mA on $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$ and $\overline{SLIN}$ (Note 1) I_{OL} = 2.0 mA on All Other Outputs		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA on D0–D7 I_{OH} = −15 mA on PD0–PD7 I_{OH} = −1 mA on $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$ and $\overline{SLIN}$ I_{OH} = −0.2 mA on All Other Outputs	2.4		V
I_{CC}	Power Supply Current	V_{DD} = 5.5V, No Loads on the Outputs; $\overline{CSS}$, $\overline{CSP}$, $\overline{RD}$, $\overline{WR}$, SIN, $\overline{DSR}$, $\overline{DCD}$, $\overline{CTS}$, $\overline{RI}$ = 2V; All Other Inputs = 0.8V; CLK = 24 MHz; DIVISOR = EFFF		20	mA
I_{IL}	Input Leakage	V_{DD} = 5.5V, V_{SS} = 0V All Other Pins Floating		±10	μA
I_{OZ}	TRI-STATE® Leakage	V_{DD} = 5.5V, V_{SS} = 0V, V_{OUT} = 0V, 5.5V 1) Chip Deselected 2) Chip and Write Mode Selected		±20	μA
V_{IL} ($\overline{MR}$)	$\overline{MR}$ Schmitt V_{IL}			0.8	V
V_{IH} ($\overline{MR}$)	$\overline{MR}$ Schmitt V_{IH}		2.0		V

Note 1: $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$, and $\overline{SLIN}$ are open collector output pins that require pull-up resistor (4.7k) to V_{CC}. This will generate a maximum of 2.0 mA of internal I_{OL}. In addition to this internal current, each pin will sink at least 20 mA, while maintaining the V_{OL} specification of 0.4V Max.

Capacitance T_A = 25°C, V_{DD} = V_{SS} = 0V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{IN}	Input Capacitance	f_C = 1 MHz Unmeasured Pins Returned to V_{SS}		5	7	pF
C_{OUT}	Output Capacitance			6	8	pF
$C_{I/O}$	Input/Output Capacitance			10	12	pF

3.0 AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{DD} = +5V \pm 10\%$

Symbol	Parameter	Conditions	Min	Max	Units
3.1 CPU INTERFACE					
t_{AR}	$\overline{RD}$ Delay from Address		15		ns
t_{AW}	$\overline{WR}$ Delay from Address		15		ns
t_{CH}	Duration of Clock High Pulse	External Clock (24 MHz Max)	17		ns
t_{CL}	Duration of Clock Low Pulse	External Clock (24 MHz Max)	17		ns
t_{DH}	Data Hold Time		5		ns
t_{DS}	Data Setup Time		15		ns
t_{HZ}	$\overline{RD}$ to Floating Data Delay	(Note 1)	10	20	ns
t_{RA}	Address Hold Time from $\overline{RD}$		0		ns
t_{RBH}	$\overline{RD}$ Strobe to BDIR High			25	ns
t_{RBL}	$\overline{RD}$ Strobe to BDIR Low			20	ns
t_{RC}	Read Cycle Update		29		ns
t_{RD}	$\overline{RD}$ Strobe Width		40		ns
t_{RVD}	Delay from $\overline{RD}$ to Data			25	ns
t_{RW}	Reset Pulse Width		500		ns
t_{WA}	Address Hold Time from $\overline{WR}$		0		ns
t_{WC}	Write Cycle Update		29		ns
t_{WR}	$\overline{WR}$ Strobe Width		40		ns
RC	Read Cycle = $t_{AR} + t_{RD} + t_{RC}$		84		ns
WC	Write Cycle = $t_{AW} + t_{WR} + t_{WC}$		84		ns
3.2 SERIAL INTERFACE BAUD GENERATOR					
N	Baud Divisor		1	$2^{16} - 1$	
t_{BHD}	Baud Output Positive Edge Delay	CLK = 24 MHz ÷ 2, 100 pF Load		45	ns
t_{BLD}	Baud Output Negative Edge Delay	CLK = 24 MHz ÷ 2, 100 pF Load		45	ns

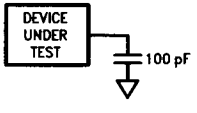
Note 1: Charge and discharge time is determined by V_{OL}, V_{OH} and the external loading.

Note 2: All AC timings can be met with current loads that don't exceed 3.2 mA or $-80\ \mu A$ at 100 pF capacitive loading.

Note 3: For capacitive loads that exceed 100 pF the following typical derating factors should be used:

$100\ pF < C_L \leq 150\ pF$, $t = (0.1\ ns/pF)(C_L - 100\ pF)$ typical
$150\ pF < C_L \leq 200\ pF$, $t = (0.08\ ns/pF)(C_L - 100\ pF)$ and
$t = (0.5\ ns/mA)(I_{SINK}\ mA)$ or
$t = -(0.5\ ns/mA)(I_{SOURCE\ mA})$
I_{SOURCE} is always negative, $I_{SINK} \leq 4.8\ mA$, $I_{SOURCE} \leq -120\ \mu A$, $C_L \leq 250\ pF$

AC Testing Load Circuit



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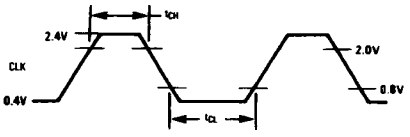
3.0 AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{DD} = +5V \pm 10\%$ (Continued)

Symbol	Parameter	Conditions	Min	Max	Units
TRANSMITTER					
t_{HR}	Delay from $\overline{WR}$ (WR THR) to Reset Interrupt			40	ns
t_{IR}	Delay from $\overline{RD}$ (RD IIR) to Reset Interrupt (THRE)			40	ns
t_{IRS}	Delay from Initial INTR Reset to Transmit Start		8	24	BAUDOUT Cycles
t_{SI}	Delay from Initial Write to Interrupt		16	24	BAUDOUT Cycles
t_{STI}	Delay from Start to Interrupt (THRE)			8	BAUDOUT Cycles
MODEM CONTROL					
t_{MDO}	Delay from $\overline{WR}$ (WR MCR) to Output			40	ns
t_{RIM}	Delay to Reset Interrupt from $\overline{RD}$ (RD MSR)			78	ns
t_{SIM}	Delay to Set Interrupt from MODEM Input			40	ns
RECEIVER					
t_{RAI}	Delay from Active Edge of $\overline{RD}$ to Reset Interrupt			78	ns
t_{RINT}	Delay from Inactive Edge of $\overline{RD}$ (RD LSR) to Reset Interrupt			40	ns
t_{SCD}	Delay from R_{CLK} to Sample Time			33	ns
t_{SINT}	Delay from Stop to Set Interrupt			2	BAUDOUT Cycles
3.3 PARALLEL INTERFACE					
t_{PDH}	Port Data Hold		500		ns
t_{PDS}	Port Data Setup		500		ns
t_{PI}	Port Interrupt		33		ns
t_{PS}	Port Setup		10		ns
t_{RBH}	Read to BDIR High			25	ns
t_{RBL}	Read to BDIR Low			20	ns
t_{SW}	Strobe Width		500		ns
t_{WO}	Write to Output		33		ns

4.0 Timing Waveforms All timings are referenced to valid 0 and valid 1

External Clock Input (24 MHz Max)



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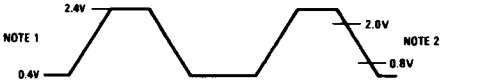
AC Test Points



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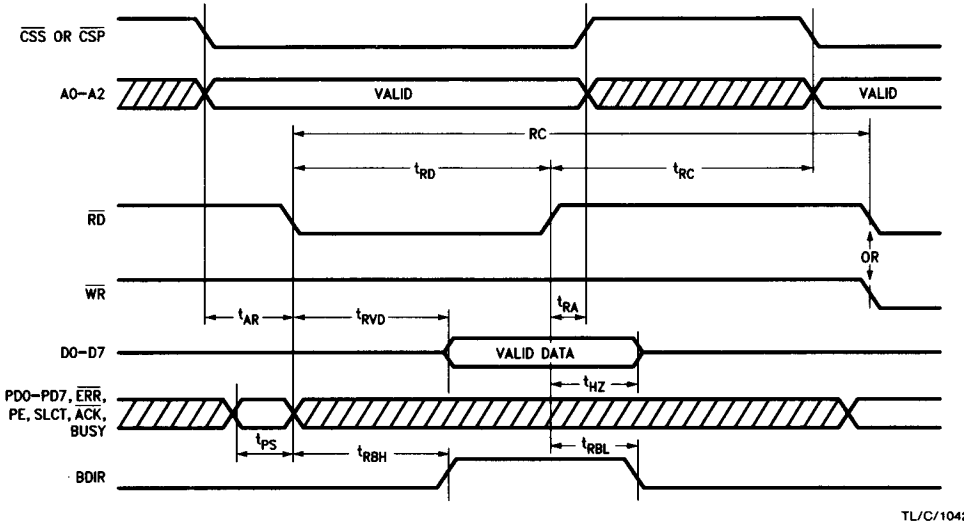
Note 1: The 2.4V and 0.4V levels are the voltages that the inputs are driven to during AC testing.
Note 2: The 2.0V and 0.8V levels are the voltages at which the timing tests are made.

4.1 CPU INTERFACE

Read Cycle



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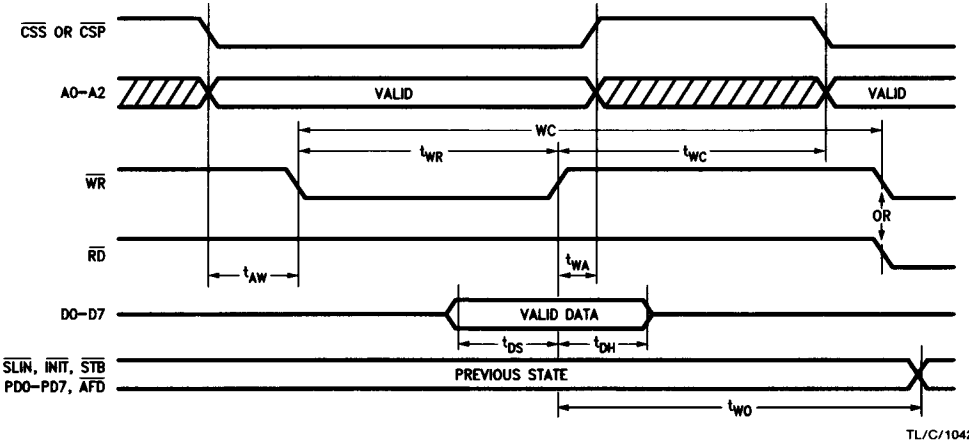
Write Cycle



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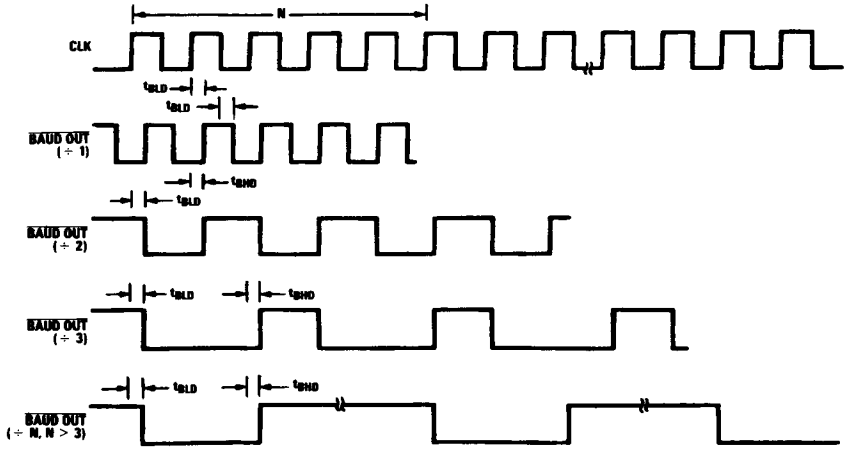
4.0 Timing Waveforms All timings are referenced to valid 0 and valid 1 (Continued)

4.2 SERIAL INTERFACE

$\overline{\text{BAUDOUT}}$ Timing



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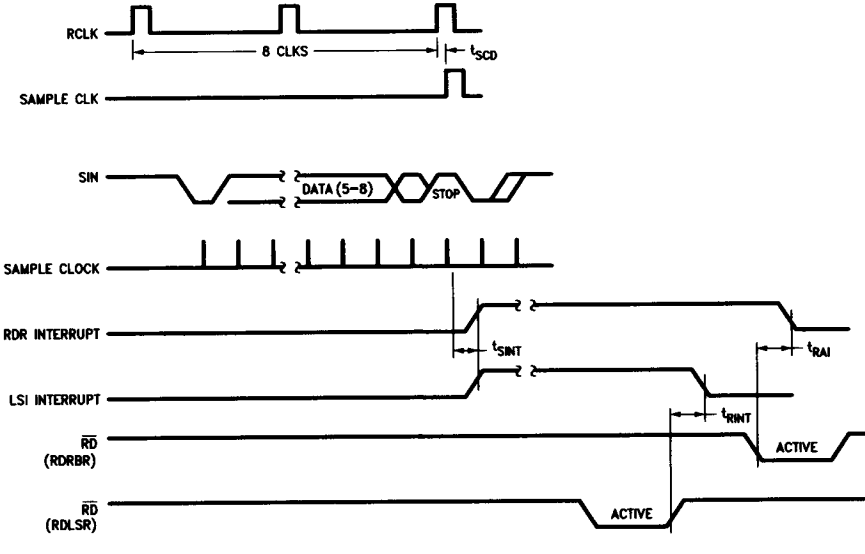
Receiver Timing



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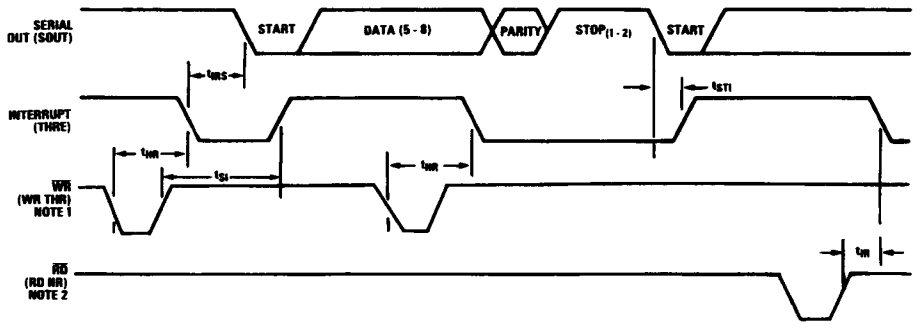
4.0 Timing Waveforms All timings are referenced to valid 0 and valid 1 (Continued)

Transmitter Timing



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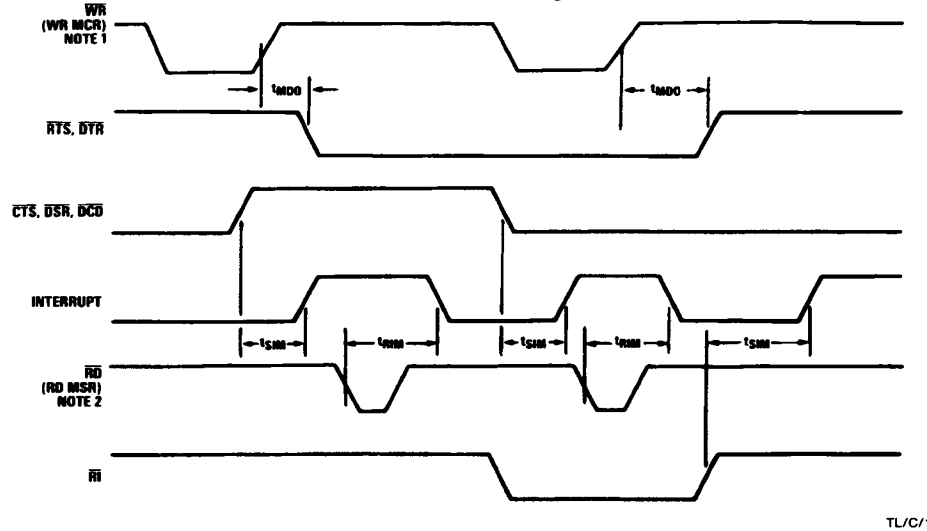
MODEM Control Timing



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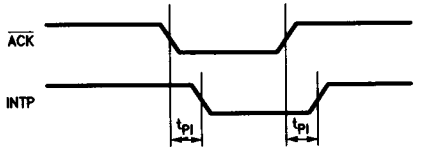
Note 1: See Write Cycle timing.

Note 2: See Read Cycle timing.

4.0 Timing Waveforms All timings are referenced to valid 0 and valid 1 (Continued)

4.3 PARALLEL INTERFACE

Interrupt Timing



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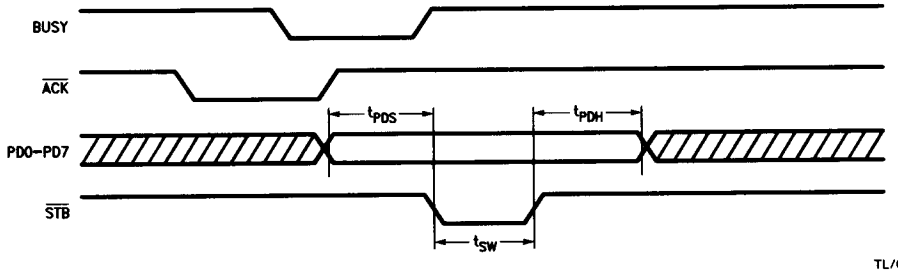
Typical Peripheral Data Exchange



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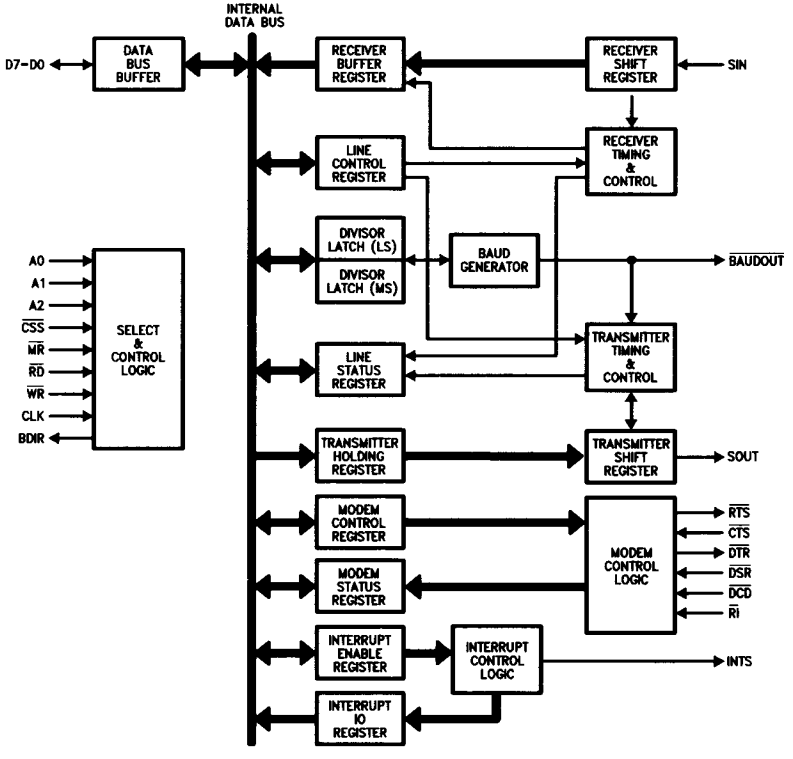
5.0 Block Diagram

5.1 BLOCK DIAGRAM OF THE SERIAL PORT



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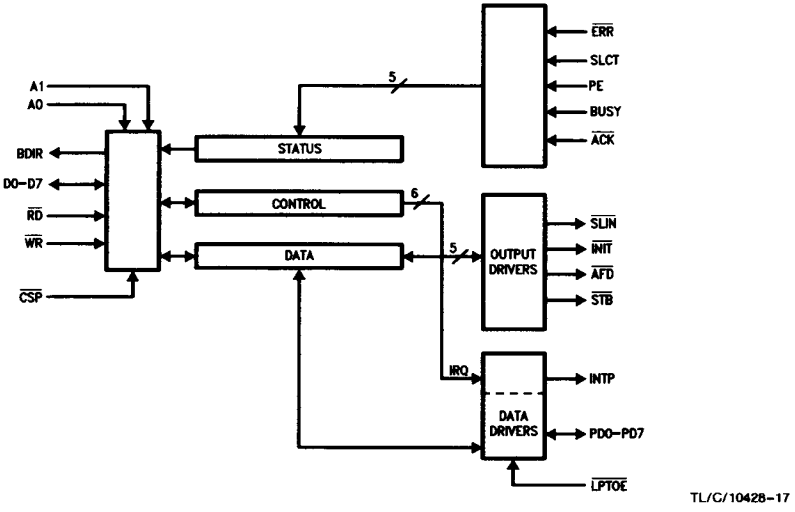
5.2 BLOCK DIAGRAM OF THE PARALLEL PORT



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6.0 Pin Descriptions

The following describes the function of all pins. In the following descriptions, a low represents a logic 0 (0V) and a high represents a logic 1 (+2.4V).

A0, A1, A2 (Register Select), Pins 35–33: Address signals connected to these 3 inputs select a register for the CPU to read from or write to during data transfer. Tables I and VI show the registers and their addresses. Note that the state of the Divisor Latch Access Bit (DLAB), which is the most significant bit of the Line Control Register, affects the selection of certain serial port registers. The DLAB must be set high by the system software to access the Baud Generator Divisor Latches.

$\overline{\text{ACK}}$ (Acknowledge), Pin 68: This input is set low by the printer to indicate that it has received data. A positive transition on this pin will generate an interrupt.

$\overline{\text{AFD}}$ (Automatic Feed XT), Pin 56: When this output is low the printer should automatically line feed after each line printed. This is an open collector output pin and it requires an external pull-up resistor (4.7 kΩ is recommended).

$\overline{\text{BAUDOUT}}$ (Baud Out), Pin 10: This is the 16 × clock signal from the transmitter section of the UART. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches.

BDIR (Bus Direction Control), Pin 44: When either serial port or parallel port is read, this pin goes high. This output pin can be used to control the bus transceiver (74LS245) when it is required to interface with a CPU.

BUSY (Printer Busy), Pin 66: This input is set high by the printer when it is not ready to accept another character.

CLK (Clock Input), Pin 4: This is the external clock input to the serial port.

$\overline{\text{CSP}}$ (Parallel Port Chip Select), Pin 38: Chip select signal for parallel port.

$\overline{\text{CSS}}$ (Serial Port Chip Select), Pin 32: Chip select signal for serial port.

$\overline{\text{CTS}}$ (Clear to Send), Pin 28: When low, this input indicates that the MODEM or data set is ready to exchange data. The $\overline{\text{CTS}}$ is a MODEM status input whose condition the CPU can test by reading bit 4 (CTS) of the MODEM Status Register. Bit 4 is the complement of the CTS signal. Bit 0 (DCTS) of the MODEM Status Register indicates whether the $\overline{\text{CTS}}$ input has changed state since the previous reading of the MODEM Status Register. $\overline{\text{CTS}}$ has no effect on the Transmitter.

Note: Whenever the CTS bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

D0–D7 (Data Bus), Pins 14–21: This bus contains eight TRI-STATE input/output lines. The bus provides bidirectional communications between the NS16C451 and the CPU. Data, control words, and status information are transferred via the D0–D7 Data Bus. These lines are normally in the high-impedance state except during read operation.

$\overline{\text{DCD}}$ (Data Carrier Detect), Pin 29: When low, this input indicates that the data carrier has been detected by the MODEM or data set. The $\overline{\text{DCD}}$ signal is a MODEM status input whose condition the CPU can test by reading bit 7 (DCD) of the MODEM Status Register. Bit 7 is the complement of the $\overline{\text{DCD}}$ signal. Bit 3 (DDCD) of the MODEM Status Register indicates whether the $\overline{\text{DCD}}$ input has changed state since the previous reading of the MODEM Status Register. $\overline{\text{DCD}}$ has no effect on the receiver.

Note: Whenever the DCD bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status interrupt is enabled.

TABLE I. Serial Port Register Addresses

DLAB	A2	A1	A0	Address	Register	Read/Write
0	0	0	0	0	THR/RBR	THR-Write RBR-Read
0	0	0	1	1	IER	Read/Write
X	0	1	0	2	IIR	Read
X	0	1	1	3	LCR	Read/Write
X	1	0	0	4	MCR	Read/Write
X	1	0	1	5	LSR	Read
X	1	1	0	6	MSR	Read
X	1	1	1	7	SCR	Read/Write
1	0	0	0	0	DLL	Read/Write
1	0	0	1	1	DLM	Read/Write

6.0 Pin Descriptions (Continued)

$\overline{DSR}$ (Data Set Ready), Pin 31: When low, this input indicates that the MODEM or data set is ready to establish the communications link with the UART. The $\overline{DSR}$ signal is a MODEM status input whose condition the CPU can test by reading bit 5 (DSR) of the MODEM Status Register. Bit 5 is the complement of the $\overline{DSR}$ signal. Bit 1 (DDSR) of the MODEM Status Register indicates whether the $\overline{DSR}$ input has changed state since the previous reading of the MODEM Status Register.

Note: Whenever the DSR bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

$\overline{DTR}$ (Data Terminal Ready), Pin 25: When low, this output indicates to the MODEM or data set that the UART is ready to establish a communications link. The $\overline{DTR}$ output signal can be set to an active low by programming bit 0 (DTR) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.

$\overline{ERR}$ (Error), Pin 63: This input is set low by the printer when it has detected an error.

$\overline{INIT}$ (Initialize), Pin 57: This output initializes the printer when it is low. This is an open collector output pin and it requires an external pull-up resistor (4.7 kΩ is recommended).

INTP (Parallel Port Interrupt), Pin 59: This is an active high, TRI-STATE output signal generated by the positive transition of $\overline{ACK}$. It is enabled/disabled through bit 4 in the Control Register. Upon System Reset, it is in TRI-STATE. When the interrupt is disabled by writing 0 to Bit 4 in the control register, INTP is also in TRI-STATE.

INTS (Serial Port Interrupt), Pin 45: This is an active high, TRI-STATE output signal. It can be enabled/disabled through Bit 3 in the MCR. It goes high when one of the following conditions happens: Receiver Error Indication, Received Data Available, Transmitter Holding Register empty, and MODEM status. The interrupt is cleared upon appropriate service (read register) or system Reset.

$\overline{LPTOE}$ (Parallel Port Output Enable), Pin 1: When low, data written to Data Register in the parallel port is output through PD0–PD7. When high, PD0–PD7 are in high-impedance state functioning as inputs, data can then be read through these lines into CPU. This pin is usually tied low for printer operation.

$\overline{MR}$ (Master Reset), Pin 39: When this input is low, it clears all the registers (except the parallel port data and status registers, the serial port receiver buffer, Transmitter Holding Register and Divisor Latches). The states of various output signals are affected by an active $\overline{MR}$ input (Reference Tables II and VII).

PD0–PD7 (Port Data), Pins 53–46: These bidirectional pins transfer data to and from the peripheral data bus. PD0–PD7 are held in high-impedance state when $\overline{LPTOE}$ is in high state. These pins have high current drive capability. (See DC Electrical Characteristics.)

PE (Paper End), Pin 67: This input is set high by the printer when it is out of paper.

$\overline{RD}$ (Read), Pin 37: When this input is low while the chip is selected, the CPU can read status information or data from the selected serial or parallel port register.

$\overline{RI}$ (Ring Indicator), Pin 30: When low, this input indicates that a telephone ringing signal has been received by the MODEM or data set. The $\overline{RI}$ signal is a MODEM status input whose condition the CPU can test by reading bit 6 (RI) of the MODEM Status Register. Bit 6 is the complement of the $\overline{RI}$ signal. Bit 2 (TERI) of the MODEM Status Register indicates whether the $\overline{RI}$ input signal has changed from a low to a high state since the previous reading of the MODEM Status Register.

Note: Whenever the RI bit of the MODEM Status Register changes from a high to a low state, an interrupt is generated if the MODEM Status interrupt is enabled.

$\overline{RTS}$ (Request to Send), Pin 24: When low, this output indicates to the MODEM or data set the UART is ready to exchange data. The $\overline{RTS}$ output signal can be set to an active low by programming bit 1 (RTS) of the MODEM Control Register. A Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.

SIN (Serial Input), Pin 41: This input receives serial data from the communications link (peripheral device, MODEM, or data set). In Loop mode operation, data input on this pin is disabled.

SLCT (Select), Pin 65: This input is set high by the printer when it is selected.

$\overline{SLIN}$ (Select Input), Pin 58: This output selects the printer when it is low. This is an open collector output pin and it requires an external pull-up resistor (4.7 kΩ is recommended).

SOUT (Serial Output), Pin 26: This output sends composite serial data from the transmitter to the communications link (peripheral, MODEM or data set). The SOUT signal is set to the Marking (logic 1) state upon a Reset operation, or when transmitter is empty or in loop mode operation.

$\overline{STB}$ (Data Strobe), Pin 55: This output indicates to the peripheral that the data at the parallel port is valid. An active low latches the data currently on the parallel port. This is an open collector output pin and it requires an external pull-up resistor (4.7 kΩ is recommended).

V_{DD} (Power), Pin 3, 23, 40, 64: +5V Supply.

V_{SS} (Ground), Pin 2, 5–9, 13, 22, 27, 42, 43, 54, 61, 62: 0V reference. All pins must be tied to ground for proper operation.

$\overline{WR}$ (Write), Pin 36: When this input is low while the chip is selected, the CPU can write control information or data to the selected serial or parallel port register.

6.0 Pin Descriptions (Continued)

TABLE II. UART Reset Functions

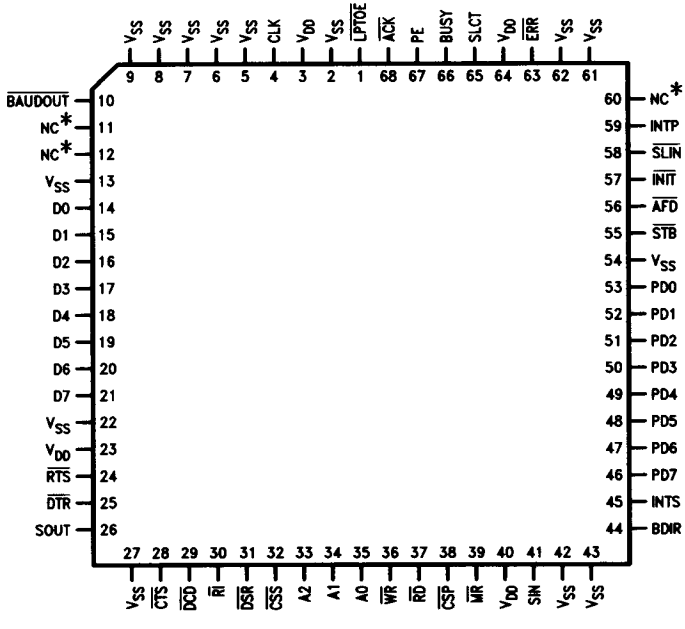
Register/Signal	Reset Control	Reset State
Interrupt Enable Register	$\overline{MR}$	**0000** 0000 (Note 1)
Interrupt Identification Register	$\overline{MR}$	**0000 0**001
Line Control Register	$\overline{MR}$	0000 0000
MODEM Control Register	$\overline{MR}$	**000**0 0000
Line Status Register	$\overline{MR}$	**0**110 0000
MODEM Status Register	$\overline{MR}$	XXXX 0000 (Note 2)
SOUT Pin	$\overline{MR}$	High
INTS Pin (RCVR Errs)	Read LSR/$\overline{MR}$	Low
INTS Pin (RCVR Data Ready)	Read RBR/$\overline{MR}$	Low
INTS Pin (THRE)	Read IIR/Write THR/$\overline{MR}$	Low
INTS Pin (Modem Status Changes)	Read MSR/$\overline{MR}$	Low
$\overline{RTS}$ Pin	$\overline{MR}$	High
$\overline{DTR}$ Pin	$\overline{MR}$	High

Note 1: Boldface bits are permanently low.

Note 2: Bits 7–4 are driven by the input signals.

7.0 Connection Diagram

NS16C451



TL/C/10428–18

Top View

*Not connecting these NC pins will maintain socket-compatibility with NS16C551.

8.0 Serial Port Registers

The system programmer may access any of the UART registers summarized in Table III via the CPU. These registers control UART operations including transmission and reception of data. Each register bit in Table III has its name shown.

8.1 LINE CONTROL REGISTER

The system programmer specifies the format of the asnychronous data communications exchange and sets the Divisor Latch Access bit via the Line Control Register (LCR). The programmer can also read the contents of the Line Control Register. The read capability simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. Table III shows the contents of the LCR. Details on each bit follow:

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Character Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits transmitted and received in each serial character. If bit 2 is a logic 0, one Stop bit is generated or checked in the transmitted data. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one and a half Stop bits are generated. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two Stop bits are generated. The Receiver checks the first Stop-bit only, regardless of the number of Stop bits selected.

TABLE III. Summary of Registers

	Register Address										
	0 DLAB = 0	0 DLAB = 0	1 DLAB = 0	2	3	4	5	6	7	0 DLAB = 1	1 DLAB = 1
Bit No.	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register (Read Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Register	Divisor Latch (LS)	Divisor Latch (MS)
	RBR	THR	IER	IIR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Bit 0 (Note 1)	Data Bit 0	Received Data Available	"0" if Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Transmitter Holding Register Empty	Interrupt ID Bit (0)	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Receiver Line Status	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1 Bit	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	MODEM Status	0	Parity Enable (PEN)	INTS Enable	Framing Error (FE)	Delta Data Carrier Detect (DDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

Note 1: Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

8.0 Serial Port Registers (Continued)

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is logic 1, an even number of logic 1s is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bits 3, 4, and 5 are logic 1 the Parity bit is transmitted and checked as a logic 0. If bits 3 and 5 are 1 and bit 4 is a logic 0 then the Parity bit is transmitted and checked as a logic 1. If bit 5 is a logic 0 Stick Parity is disabled.

Bit 6: This bit is the Break Control bit. It causes a break condition to be transmitted by the UART. When it is set to a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state. The break is disabled by clearing bit 6 to a logic 0. The Break Control bit acts only on SOUT and has no effect on the transmitter logic.

Note: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is used, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all 0s, pad character,in response to THRE.
2. Set break after the next THRE.
3. Wait for the transmitter to be idle, (TEMT = 1), and clear break when normal transmission has to be restored.

   During the break, the Transmitter can be used as a character timer to accurately establish the break duration.

Bit 7: Ths bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

8.2 PROGRAMMABLE BAUD GENERATOR

The UART contains a programmable Baud Generator that is capable of taking any clock input from DC to 24 MHz and dividing it by any divisor from 1 to $2^{16} - 1$. The output frequency of the Baud Generator is 16 × the Baud [divisor # = (frequency input) ÷ (baud rate × 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to ensure proper operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded.

Table IV provides decimal divisors to use with crystal frequencies of 1.8432 MHz, 2.4576 MHz, 3.072 MHz and 18.432 MHz respectively for common baud rates. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen. Using a divisor of 0 is **not** recommended.

TABLE IV. Divisors, Baud Rate, and Clock Frequencies

Frequency	1.8432 MHz Clock		2.4576 MHz Clock		3.072 MHz Clock		18.432 MHz Clock	
Divisor Baud Rate	Decimal Divisor for 16 × Clock	Percent Error	Decimal Divisor for 16 × Clock	Percent Error	Decimal Divisor for 16 × Clock	Percent Error	Decimal Divisor for 16 × Clock	Percent Error
50	2304	—	3072	—	3840	—	23040	—
75	1536	—	2048	—	2560	—	15360	—
110	1047	0.026	1396	0.026	1745	0.026	10473	—
134.5	857	0.058	1142	0.0007	1428	0.034	8565	—
150	768	—	1024	—	1280	—	7680	—
300	384	—	512	—	640	—	3840	—
600	192	—	256	—	320	—	1920	—
1200	96	—	128	—	160	—	920	—
1800	64	—	85	0.392	107	0.312	640	—
2000	58	0.69	77	0.260	96	—	576	—
2400	48	—	64	—	80	—	480	—
3600	32	—	43	0.775	53	0.628	320	—
4800	24	—	32	—	40	—	240	—
7200	16	—	21	1.587	27	1.23	160	—
9600	12	—	16	—	20	—	120	—
19200	6	—	8	—	10	-	60	—
38400	3	—	4	—	5	—	30	—
56000	2	2.86	—	—	—	—	21	2.04
128000	—	—	—	—	—	—	9	—

Note: For baud rates of 250k, 300k, 375k, 500k, and 1.5M using a 24 MHz clock causes minimal error.

8.0 Serial Port Registers (Continued)

8.3 LINE STATUS REGISTER

This 8-bit register provides status information to the CPU concerning the data transfer. Table III shows the contents of the Line Status Register. Details on each bit follow:

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 is reset to a logic 0 by reading the data in the Receiver Buffer Register.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is set to a logic 1 upon detection of an overrun condition and reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is a logic 0 (Spacing level). The FE indicator is reset whenever the CPU reads the contents of the Line Status Register. The UART will try to resynchronize after a framing error. To do this it assumes that the framing error was due to the next start bit, so it samples this "start" bit twice and then takes in the "data".

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits). The BI indicator is reset whenever the CPU reads the contents of the Line Status Register. Restarting after a break is received, requires the SIN pin to be logical 1 for at least ½ bit time.

Note: Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 whenever the CPU loads the Transmitter Holding Register.

Bit 6: This bit is the Transmitter Empty (TEMT) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. It is reset to a logic 0 whenever either the THR or TSR contains a data character.

Bit 7: This bit is permanently set to logic 0.

Note: The Line Status Register is intended for read operations only. Writing to this register is not recommended as this operation is only used for factory testing.

8.4 INTERRUPT IDENTIFICATION REGISTER

In order to provide minimum software overhead during data character transfers, the UART prioritizes interrupts into four levels and records these in the Interrupt Identification Register. The four levels of interrupt conditions in order of priority are Receiver Line Status; Received Data Ready; Transmitter Holding Register Empty; and MODEM Status.

When the CPU accesses the IIR, the UART freezes all interrupts and indicates the highest priority pending interrupt to the CPU. While this CPU access is occurring, the UART records new interrupts, but does not change its current indication until the access is complete. Table III shows the contents of the IIR. Details on each bit follow:

Bit 0: This bit can be used in an interrupt environment to indicate whether an interrupt condition is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table V.

Bits 3 through 7: These five bits of the IIR are always logic 0.

8.5 INTERRUPT ENABLE REGISTER

This register enables the four types of UART interrupts. Each interrupt can individually activate the interrupt (INTS) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register (IER). Similarly, setting bits of this register to a logic 1, enables the selected interrupt(s). Disabling an interrupt prevents it from being indicated as active in the IIR and from activating the INTS output signal. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. Table III shows the contents of the IER. Details on each bit follow.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

8.6 MODEM CONTROL REGISTER

This register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register (MCR) are indicated in Table III and are described below. Table III shows the contents of the MCR. Details on each bit follow.

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.

Note: The $\overline{DTR}$ output of the UART may be applied to an EIA inverting line driver (such as the MS1488) to obtain the proper polarity input at the succeeding MODEM or data set. In local loopback mode, this bit controls bit 5 of the MODEM Status Register.

8.0 Serial Port Registers (Continued)

TABLE V. Interrupt Control Functions

Interrupt Identification Register				Interrupt Set and Reset Functions		
Bit 2	**Bit 1**	**Bit 0**	**Priority Level**	**Interrupt Type**	**Interrupt Source**	**Interrupt Reset Control**
0	0	1	—	None	None	—
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0. In local loopback mode, this bit controls bit 4 of the MODEM Status Register.

Bit 2: This bit is the OUT1 bit. It does not have an output pin associated with it. It can be written to and read by the CPU. In local loopback mode, this bit controls bit 6 of the Modem Status Register.

Bit 3: This bit enables the interrupt when set. No external pin is associated with this bit. In local loopback mode, this bit controls bit 7 of the MODEM Status Register.

Bit 4: This bit provides a local loopback feature for diagnostic testing of the UART. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control inputs ($\overline{DSR}$, $\overline{CTS}$, $\overline{RI}$ and $\overline{DCD}$) are disconnected; and the DTR, RTS, OUT1, INTS ENABLE bits in MCR are internally connected to DSR, CTS, RI and DCD in MSR respectively. The MODEM Control output pins are forced to their inactive state (high). In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit-and-received-data paths of the serial port.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Status Interrupts are also operational, but the interrupts' sources are the lower four bits of MCR instead of the four MODEM control inputs. Writing a 1 to any of them will cause an interrupt. The interrupts are still controlled by the Interrupt Enable Register.

Bits 5 through 7: These bits are permanently set to logic 0.

8.7 MODEM STATUS REGISTER

This register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

Table III shows the contents of the MSR. Details on each bit follow.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from a low to a high state.

Bit 3: This bit is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the $\overline{DCD}$ input to the chip has changed state.

Note: Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send ($\overline{CTS}$) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.

Bit 5: This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to DTR in the MCR.

Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 1 in the MCR.

Bit 7: This bit is the complement of the Data Carrier Detect ($\overline{DCD}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to INTS ENABLE in the MCR.

8.8 SCRATCHPAD REGISTER

This 8-bit Read/Write Register does not control the UART in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

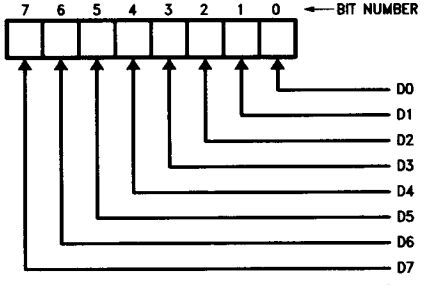
9.0 Parallel Port Registers

This parallel interface is designed to provide all of the signals and registers needed to communicate through a standard parallel printer port as found in the IBM PC, XT, AT, PS/2, and Centronics. The address decoding of the registers utilizing A0 and A1 is shown in Table VI. Table VII shows the Reset states of Parallel port registers and pin signals. All bits in the registers are located in the same positions and have the same functions as the registers of the systems listed above. These registers are shown in Sections 9.1, 9.2 and 9.3.

TABLE VI. Parallel Interface Register Addresses

$\overline{CSP}$	A1	A0	Address	Register	Read/Write
0	0	0	0	Data	Read/Write
0	0	1	1	Status	Read
0	1	0	2	Control	Read/Write
0	1	1	3	TRI-STATE	—

9.1 DATA REGISTER (DTR)



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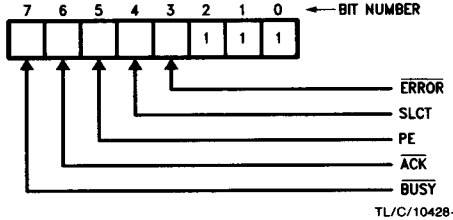
This is a bidirectional data port that transfers 8-bit data in the direction determined by the logic state of $\overline{LPTOE}$ pin and the $\overline{RD}$ and $\overline{WR}$ strobes.

9.2. STATUS REGISTER (STR)



TL/C/10428–20

This register provides status for the signals listed below. It is a read only register. Writing to it is an invalid operation that has no effect.

Bits 0, 1, 2: These bits are always 1.

Bit 3: This bit represents the current state of the printer error signal ($\overline{ERROR}$). The printer sets this bit low when there is a printer error. This bit follows the state of the $\overline{ERR}$ pin.

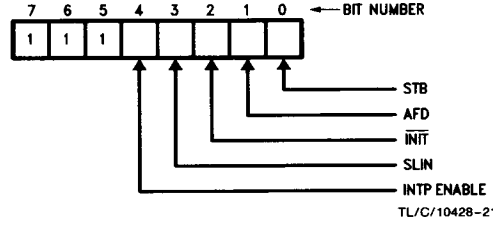
Bit 4: This bit represents the current state of the printer select signal (SLCT). The printer sets this bit high when it is selected. This bit follows the state of the SLCT pin.

Bit 5: This bit represents the current state of the printer paper end signal (PE). The printer sets this bit high when it detects the end of the paper. This bit follows the state of the PE pin.

Bit 6: This bit represents the current state of the printer acknowledge signal ($\overline{ACK}$). The printer sets this signal to low after it has received a character and is ready to receive another one. This bit follows the state of the $\overline{ACK}$ pin.

Bit 7: This bit represents the current state of the printer busy signal (BUSY). The printer sets this bit low when it is busy and cannot accept another character. This bit is the inverse of the (BUSY) pin.

9.3 CONTROL REGISTER (CTR)



TL/C/10428–21

This register provides all output signals to control the printer. This is a read and write register.

Bit 0: This bit directly controls the data strobe signal to the printer via the $\overline{STB}$ pin. This bit is the inverse of the $\overline{STB}$ pin.

Bit 1: This bit directly controls the automatic feed XT signal to the printer via the $\overline{AFD}$ pin. Setting this bit high causes the printer to automatically feed after each line is printed. This bit is the inverse of the $\overline{AFD}$ pin.

Bit 2: This bit directly controls the signal to initialize the printer via the $\overline{INIT}$ pin. Setting this bit to low initializes the printer. This bit follows the $\overline{INIT}$ pin.

Bit 3: This bit directly controls the select in signal to the printer via the $\overline{SLIN}$ pin. Setting this bit high selects the printer. This bit is the inverse of the $\overline{SLIN}$ pin.

Bit 4: This bit enables the parallel port interrupt. When this bit is set high, the INTP signal follows the $\overline{ACK}$ signal transitions.

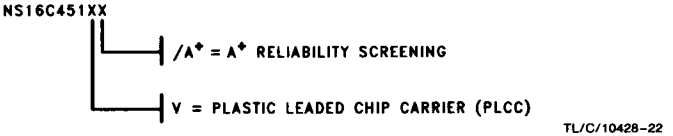
Bits 5, 6, 7: These bits are always 1.

TABLE VII. Parallel Port Reset Functions

Register/ Signal	Reset Control	Reset State
Status Register	$\overline{MR}$	xxxxx111 (Note 1)
Control Register	$\overline{MR}$	11100000
$\overline{SLIN}$ Pin	$\overline{MR}$	High
$\overline{INIT}$ Pin	$\overline{MR}$	High
$\overline{AFD}$ Pin	$\overline{MR}$	High
$\overline{STB}$ Pin	$\overline{MR}$	High
INTP Pin	$\overline{MR}$	TRI-STATE
BDIR Pin	$\overline{MR}$	Low

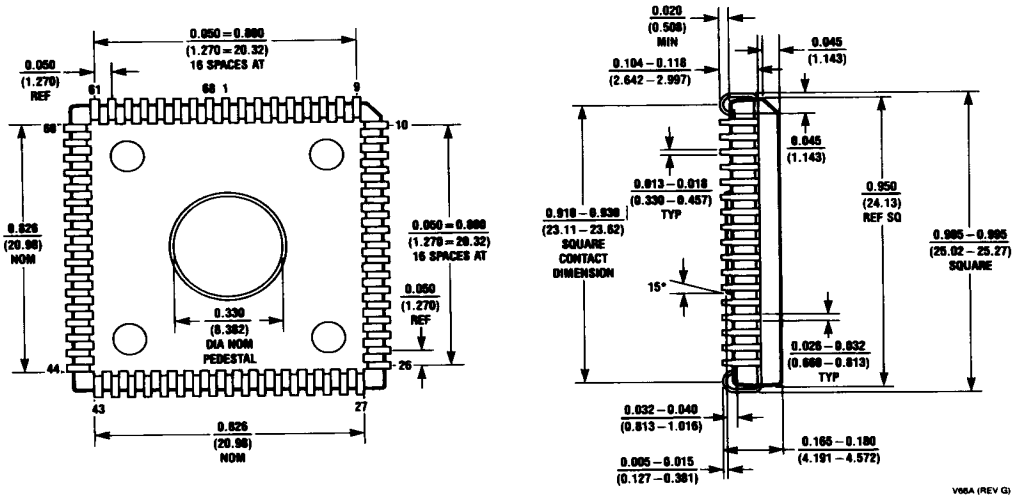
Note 1: Bits 7–3 are driven by the input signals.

10.0 Ordering Information



TL/C/10428–22

11.0 Physical Dimensions inches (millimeters)



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Order Number NS16C451V
NS Package Number V68A

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